TEXAS INSTRUMENTS

AM26LS31, AM26LS31C, AM26LS31I, AM26LS31M

SLLS114L – JANUARY 1979 – REVISED OCTOBER 2018

AM26LS31x Quadruple Differential Line Driver

1 Features

- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B and ITU
- Operates From a Single 5-V Supply
- TTL-Compatible
- Complementary Outputs
- High Output Impedance in Power-Off Conditions
- Complementary Output-Enable Inputs
- Available MIL-PRF-38535-Qualified Options (M): All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Motor Encoders
- Field Transmitters: Pressure Sensors and Temperature Sensors
- Military and Avionics Imaging
- Temperature Sensors or Controllers Using Modbus

3 Description

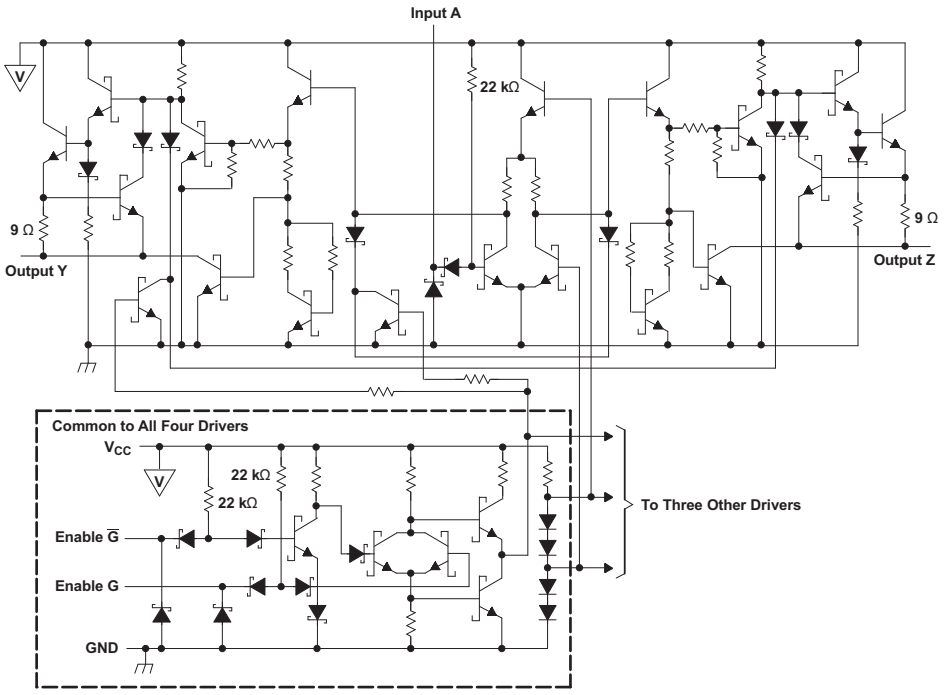
The AM26LS31 family of devices is a quadruple complementary-output line driver designed to meet the requirements of ANSI TIA/EIA-422-B and ITU (formerly CCITT) Recommendation V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they are in the high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable (G, $\overline{G}$) input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AM26LS31MFK	LCCC (20)	8.89 mm × 8.89 mm
AM26LS31MJ	CDIP (16)	19.60 mm × 6.92 mm
AM26LS31MW	CFP (16)	10.30 mm × 6.73 mm
AM26LS31CD	SOIC (16)	9.90 mm × 3.91 mm
AM26LS31CDB	SSOP (16)	6.20 mm × 5.30 mm
AM26LS31CN	PDIP (16)	19.30 mm × 6.35 mm
AM26LS31xNS	SO (16)	10.30 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic (Each Driver)



All resistor values are nominal.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (July 2016) to Revision L — **Page**

- Changed VCC pin number From: 8 To: 16 in the *Pin Functions* table ... 3
- Changed GND pin number From: 16 To: 8 in the *Pin Functions* table ... 3

Changes from Revision J (January 2014) to Revision K — **Page**

- Added *Applications* section, the *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Split up *Switching Characteristics* table into two tables specified for each part ... 5

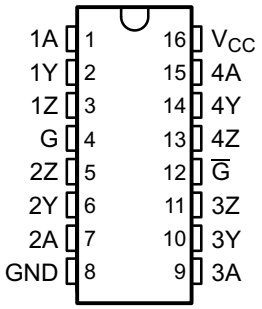
Changes from Revision I (February 2006) to Revision J — **Page**

- Updated document to new TI data sheet format - no specification changes. ... 1
- Deleted *Ordering Information* table. ... 1
- Updated Features. ... 1
- Added Device and Documentation Support section. ... 14

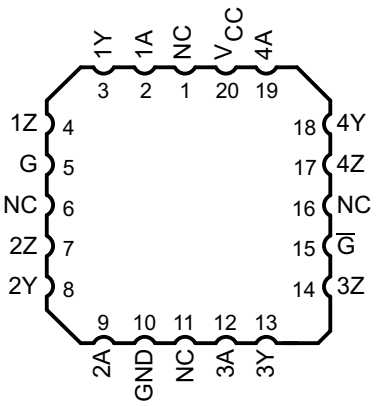
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5 Pin Configuration and Functions

D, DB, N , NS, J, or W Package
SOIC, SSOP, PDIP, SO, CDIP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, PDIP, SO, CDIP, or CFP	LCCC		
1A	1	2	I	Logic Data Input to RS422 Driver number 1
1Y	2	3	O	RS-422 Data Line (Driver 1)
1Z	3	4	O	RS-422 Data Line (Driver 1)
G	4	5	I	Driver Enable (active high)
$\overline{G}$	12	15	I	Driver Enable (active Low)
2A	7	9	I	Logic Data Input to RS422 Driver number 2
2Y	6	8	O	RS-422 Data Line (Driver 2)
2Z	5	7	O	RS-422 Data Line (Driver 2)
3A	9	12	I	Logic Data Input to RS422 Driver number 3
3Y	10	13	O	RS-422 Data Line (Driver 3)
3Z	11	14	O	RS-422 Data Line (Driver 3)
4A	15	19	I	Logic Data Input to RS422 Driver number 4
4Y	14	18	O	RS-422 Data Line (Driver 4)
4Z	13	17	O	RS-422 Data Line (Driver 4)
VCC	16	20	–	Power Input. Connect to 5-V Power Source.
GND	8	10	–	Device Ground Pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			7	V
V_I	Input voltage			7	V
	Output off-state voltage			5.5	V
	Lead temperature 1,6 mm (1/16 in) from case for 10 s			260	°C
	Lead temperature 1,6 mm (1/16 in) from case for 60 s	J package		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential output voltage V_{OD}, are with respect to network GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	AM26LS31C	4.75	5	5.25	V
		AM26LS31M	4.5	5	5.5	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	AM26LS31C	0		70	°C
		AM26LS31I	–40		85	
		AM26LS31M	–55		125	

6.4 Thermal Information

THERMAL METRIC(1)		AM26LS31x				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	73	82	67	64	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.1	–	–	32.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.7	–	–	36.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	–	–	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.4	–	–	36.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –20 mA		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA				0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MIN,	V_O = 0.5 V			–20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				–0.36	mA
I_{OS}	Short-circuit output current(3)	V_{CC} = MAX		–30		–150	mA
I_{CC}	Supply current	V_{CC} = MAX, all outputs disabled			32	80	mA

(1) For C-suffix devices, V_{CC} min = 4.75 V and V_{CC} max = 5.25 V. For M-suffix devices, V_{CC} min = 4.5 V and V_{CC} max = 5.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

6.6 Switching Characteristics – AM26LS31

T_A = 25°C, V_{CC} = 5 V (see Figure 11)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30 pF, S1 and S2 open			14	20	ns
t_{PHL}	Propagation delay time, high- to low-level output				14	20	
t_{PZH}	Output enable time to high level	C_L = 30 pF	R_L = 75 Ω		25	40	ns
t_{PZL}	Output enable time to low level		R_L = 180 Ω		37	45	
t_{PHZ}	Output disable time from high level	C_L = 10 pF, S1 and S2 closed			21	30	ns
t_{PLZ}	Output disable time from low level				23	35	
t_{SKEW}	Output-to-output skew	C_L = 30 pF, S1 and S2 open			1	6	ns

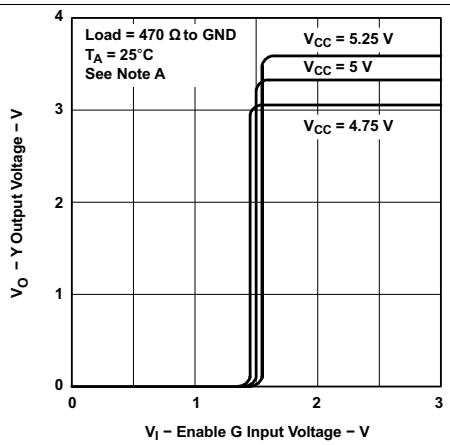
6.7 Switching Characteristics – AM26LS31M

T_A = 25°C, V_{CC} = 5 V (see Figure 11)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30 pF, S1 and S2 open			30	ns
t_{PHL}	Propagation delay time, high- to low-level output				30	
t_{PZH}	Output enable time to high level	C_L = 30 pF	R_L = 75 Ω		60	ns
t_{PZL}	Output enable time to low level		R_L = 180 Ω		68	
t_{PHZ}	Output disable time from high level	C_L = 10 pF, S1 and S2 closed			45	ns
t_{PLZ}	Output disable time from low level				53	
t_{SKEW}	Output-to-output skew	C_L = 30 pF, S1 and S2 open			9	ns

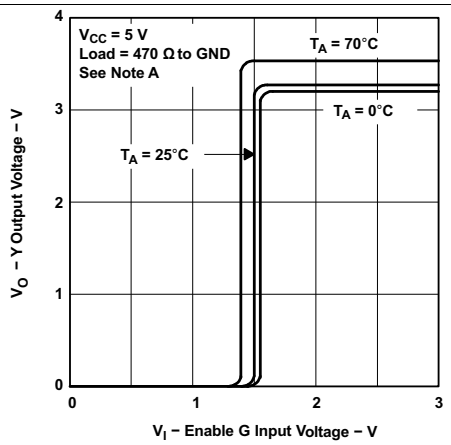
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6.8 Typical Characteristics



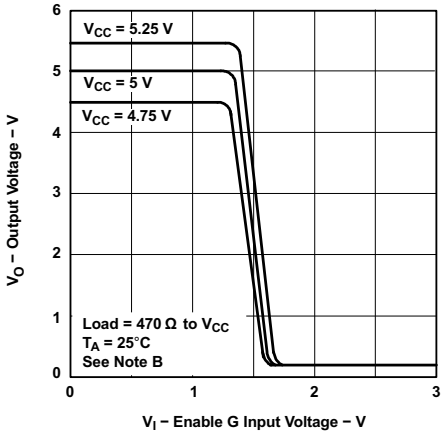
A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 1. Output Voltage vs Enable G Input Voltage



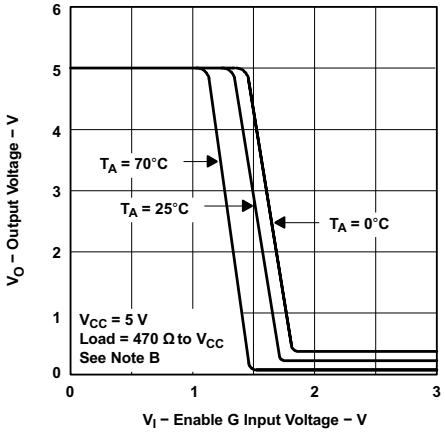
A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 2. Output Voltage vs Enable G Input Voltage



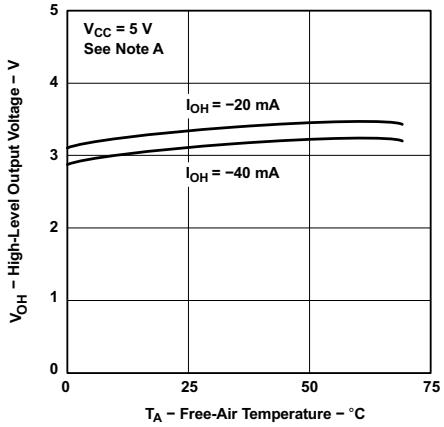
B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 3. Output Voltage vs Enable G Input Voltage



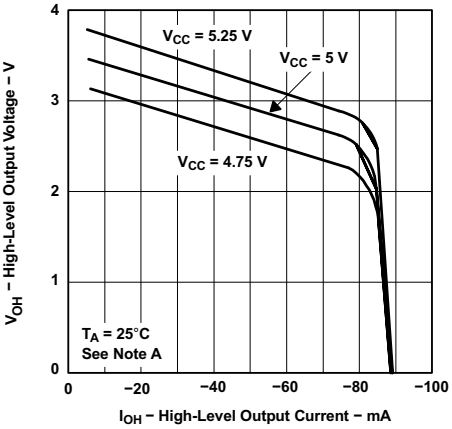
B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 4. Output Voltage vs Enable G Input Voltage



A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 5. High-Level Output Voltage vs Free-Air Temperature

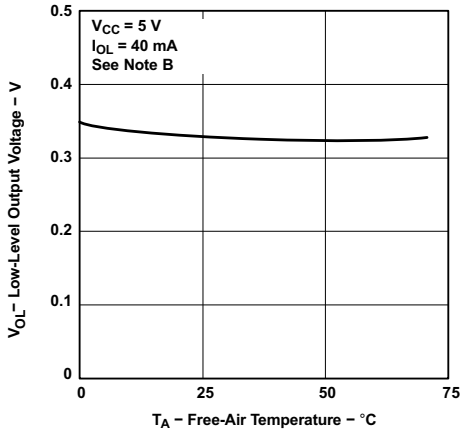


A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 6. High-Level Output Voltage vs High-Level Output Current

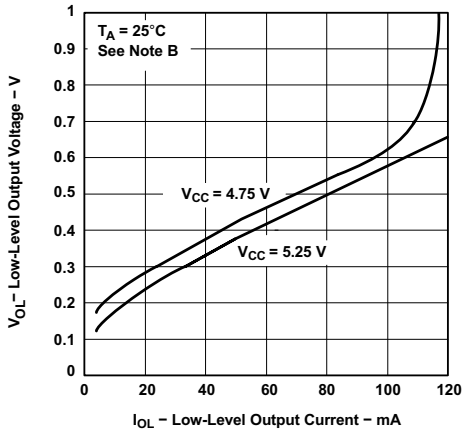
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Typical Characteristics (continued)



B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 7. Low-Level Output Voltage vs Free-Air Temperature



B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 8. Low-Level Output Voltage vs Low-Level Output Current

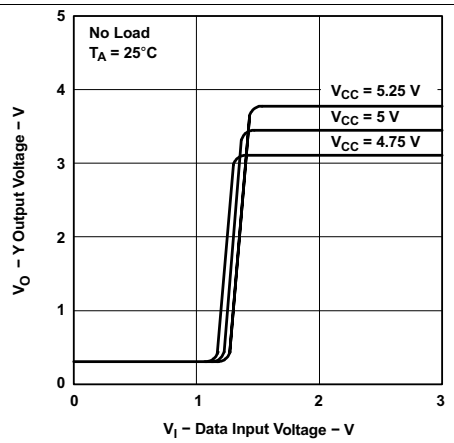


Figure 9. Y Output Voltage vs Data Input Voltage

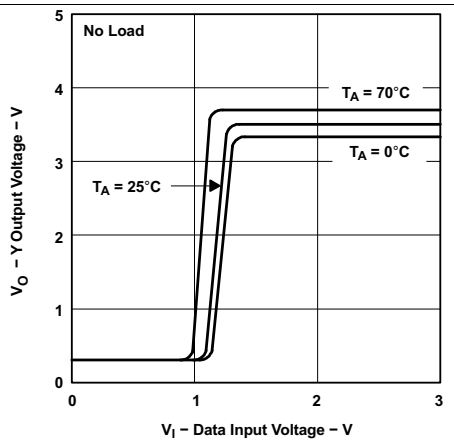
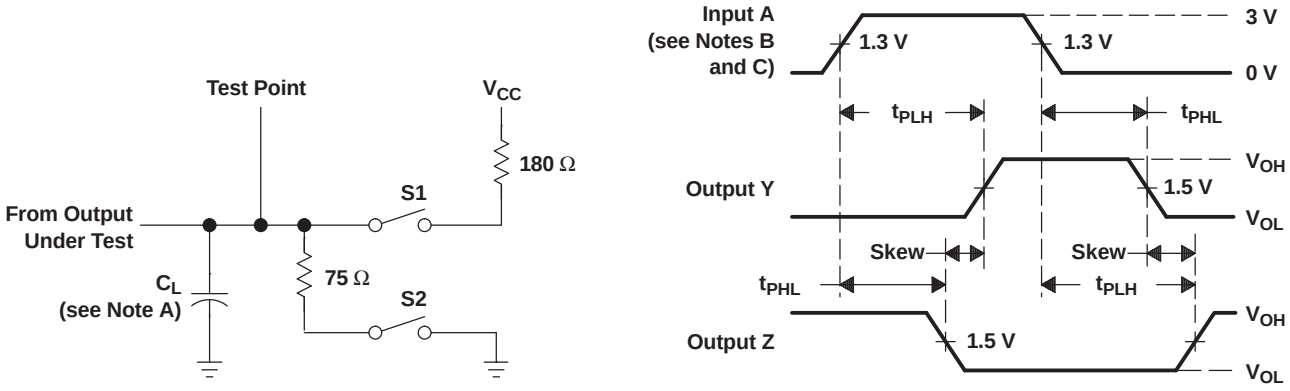


Figure 10. Y Output Voltage vs Data Input Voltage

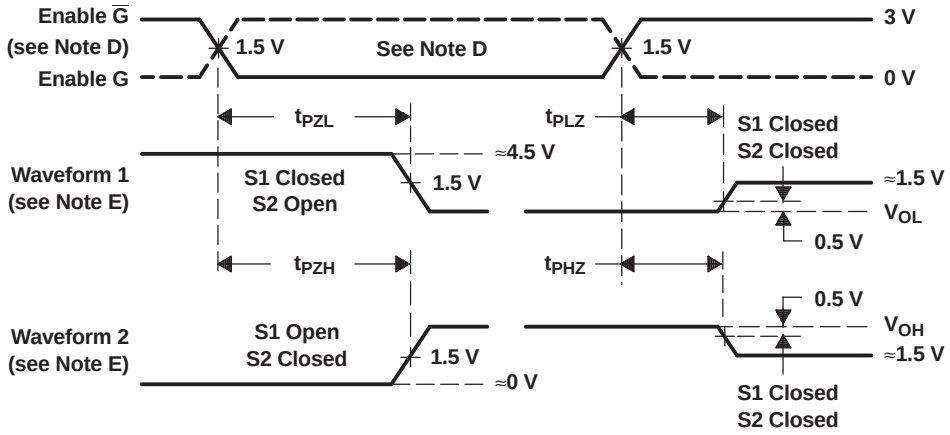
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7 Parameter Measurement Information



PROPAGATION DELAY TIMES AND SKEW

TEST CIRCUIT



ENABLE AND DISABLE TIME WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, t_f ≤ 6 ns.
C. When measuring propagation delay times and skew, switches S1 and S2 are open.
D. Each enable is tested separately.
E. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

Figure 11. Test Circuit and Voltage Waveforms

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8 Detailed Description

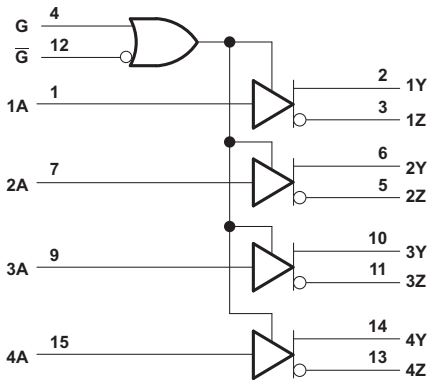
8.1 Overview

The AM26LS31x differential bus transmitter is a monolithic integrated circuit designed for unidirectional data communication on transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The AM26LS31x has a four 3-state differential line drivers that operate from a single 5-V power supply. The driver also integrates active-high and active-low enables for precise device control.

The driver is designed to handle loads of a minimum of ±30 mA of sink or source current. The driver features positive- and negative-current limiting for protection from line fault conditions.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Complementary Output-Enable Inputs

The AM26LS31x can be configured using the G and $\overline{G}$ logic inputs to control transmitter outputs. Setting either G to a logic HIGH or $\overline{G}$ to an logic LOW enables the transmitter outputs. If G is set to logic LOW and $\overline{G}$ is set to logic HIGH, the transmitter outputs are disabled. See Table 1 for a complete truth table.

8.3.2 High Output Impedance in Power-Off Conditions

When the AM26LS31x transmitter outputs are disabled using G and $\overline{G}$, the outputs are set to a high impedance state.

8.3.3 Complementary Outputs

The AM26LS31x is the driver half of a pair of devices, with the AM26LS32 being the complementary receiver. TI recommends using these devices together for optimal performance, but any RS-422 compliant receive must ensure proper RS-422 communication and logic level translation.

8.4 Device Functional Modes

Table 1 lists the functional modes of the AM26LS31.

Table 1. Function Table(1) (Each Driver)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level,
X = irrelevant,
Z = high impedance (off)

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and, indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LS31 and AM26LS32C, respectively, were tested at room temperature with a 5-V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable; the second plot shows input waveforms to the receiver at the far end of the cable.

9.2 Typical Application

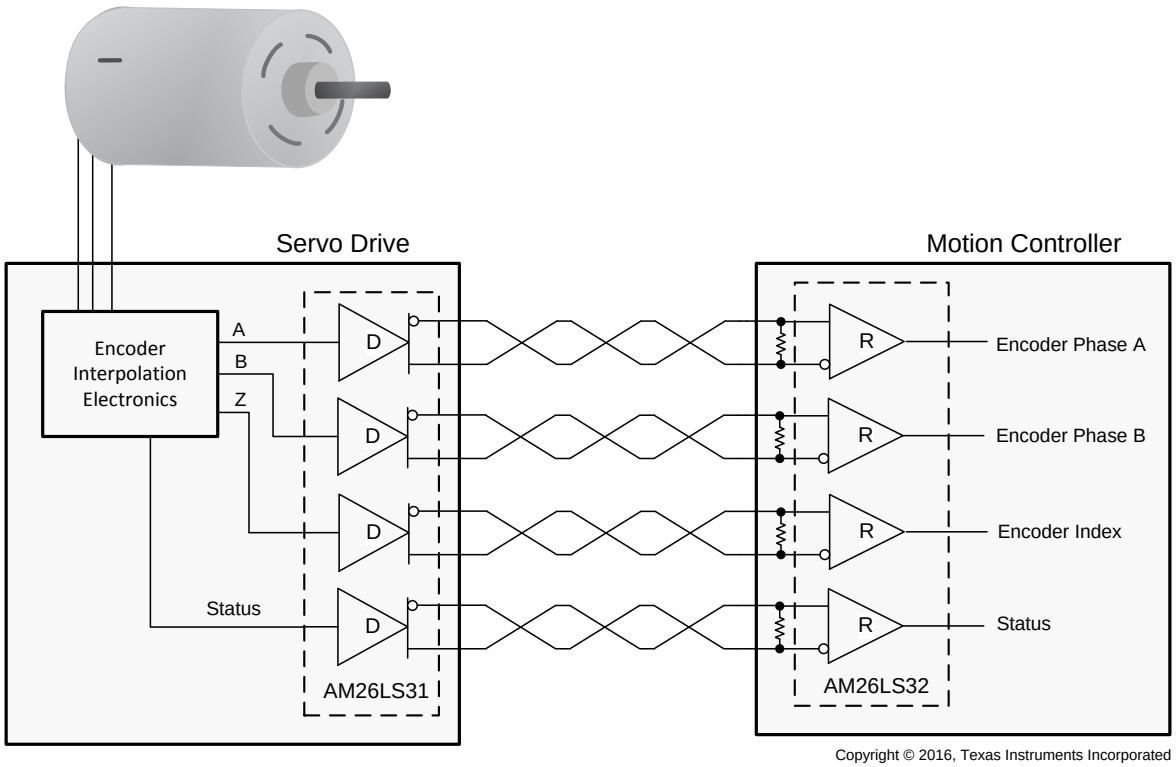


Figure 12. Encoder Application

Typical Application (continued)

9.2.1 Design Requirements

This example requires the following:

- 5-V power source
- RS-485 bus operating at 10 Mbps or less
- Connector that ensures the correct polarity for port pins

9.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line.

If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state (see *Failsafe in RS-485 data buses*).

9.2.3 Application Curve

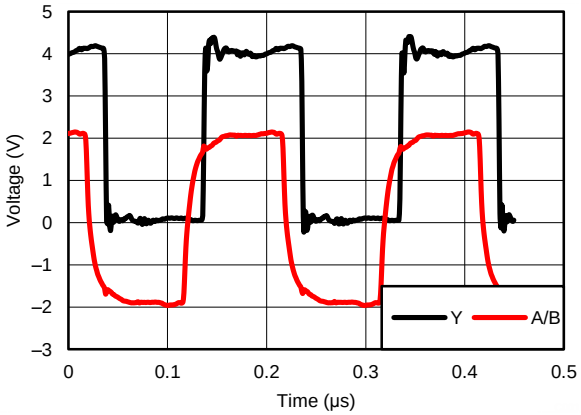


Figure 13. Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)

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10 Power Supply Recommendations

Place a 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can often propagate into analog circuitry through the power supply of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

11.2 Layout Example

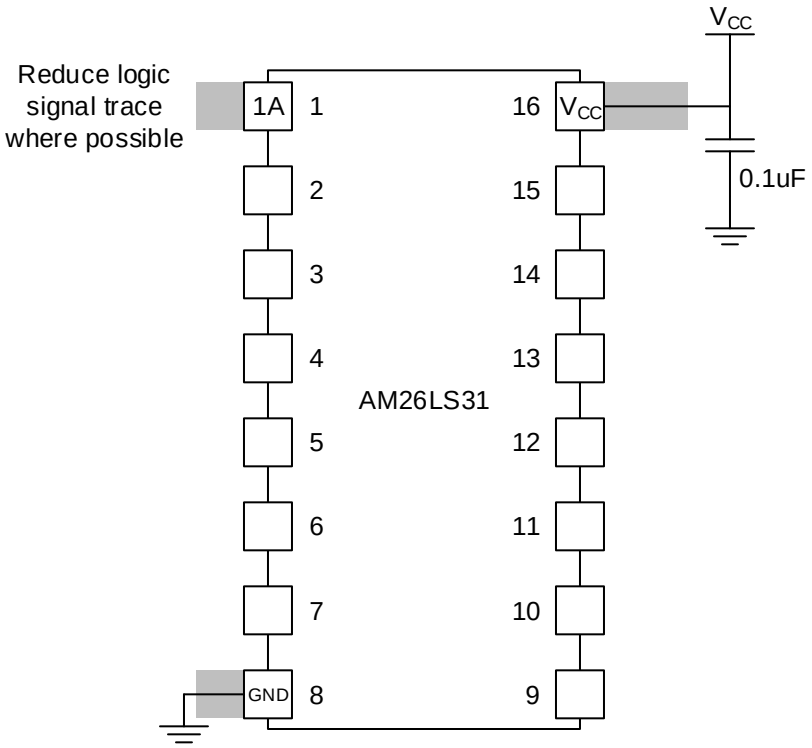


Figure 14. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Failsafe in RS-485 data buses (SLYT080)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
AM26LS31	Click here	Click here	Click here	Click here	Click here
AM26LS31C	Click here	Click here	Click here	Click here	Click here
AM26LS31I	Click here	Click here	Click here	Click here	Click here
AM26LS31M	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7802301M2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802301M2A AM26LS31 MFKB	Samples
5962-7802301MEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802301MEA AM26LS31MJB	Samples
5962-7802301MFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802301MFA AM26LS31MWB	Samples
5962-7802301Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type		5962-7802301Q2A AM26LS31M	Samples
AM26LS31CD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LS31C	Samples
AM26LS31CDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SA31C	Samples
AM26LS31CDE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LS31C	Samples
AM26LS31CDG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LS31C	Samples
AM26LS31CDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LS31C	Samples
AM26LS31CDRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LS31C	Samples
AM26LS31CDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LS31C	Samples
AM26LS31CN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	AM26LS31CN	Samples
AM26LS31CNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS31	Samples
AM26LS31INSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LS31	Samples
AM26LS31MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802301M2A AM26LS31 MFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LS31MJB	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802301ME A AM26LS31MJB	Samples
AM26LS31MWB	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802301MF A AM26LS31MWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM26LS31, AM26LS31M :

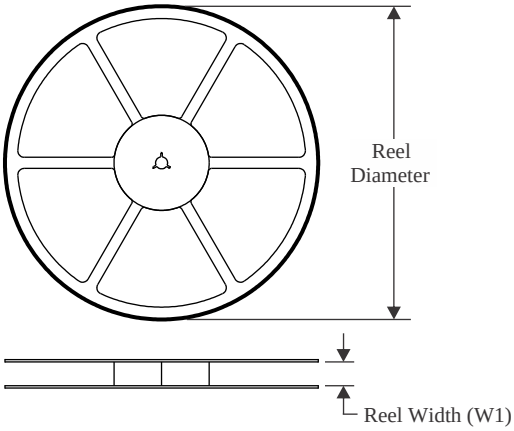
- Catalog : AM26LS31
- Military : AM26LS31M

NOTE: Qualified Version Definitions:

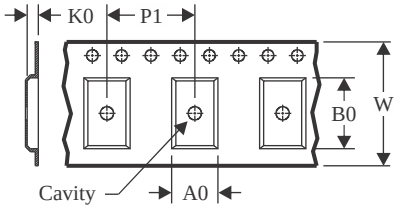
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

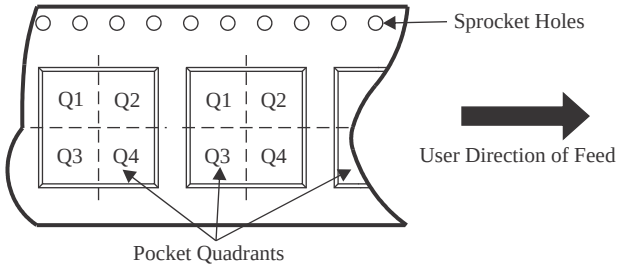


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

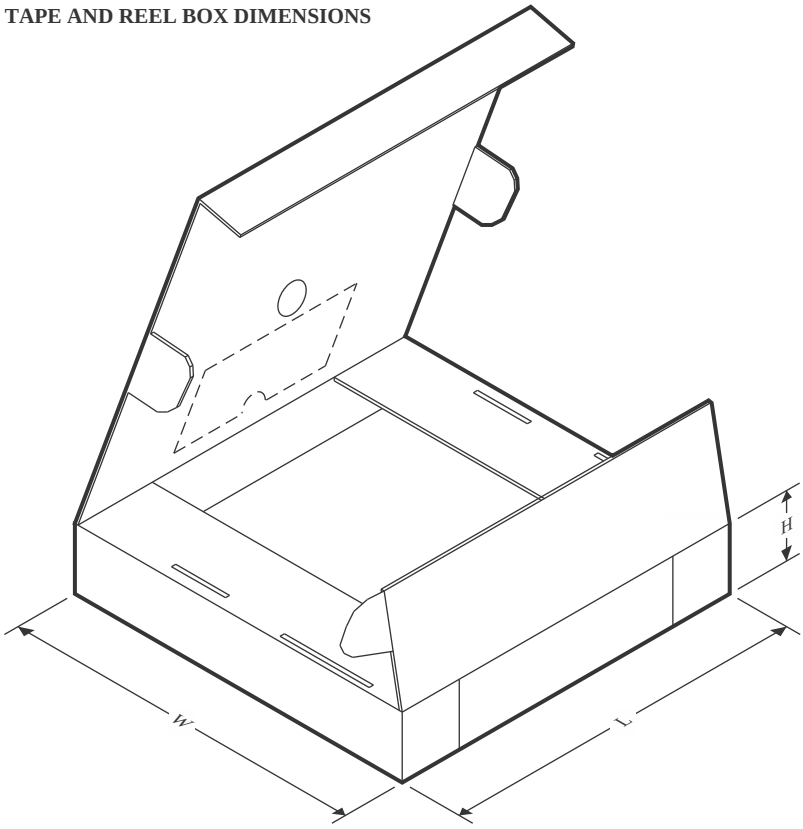
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LS31CDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
AM26LS31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS31CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS31CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS31CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LS31INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

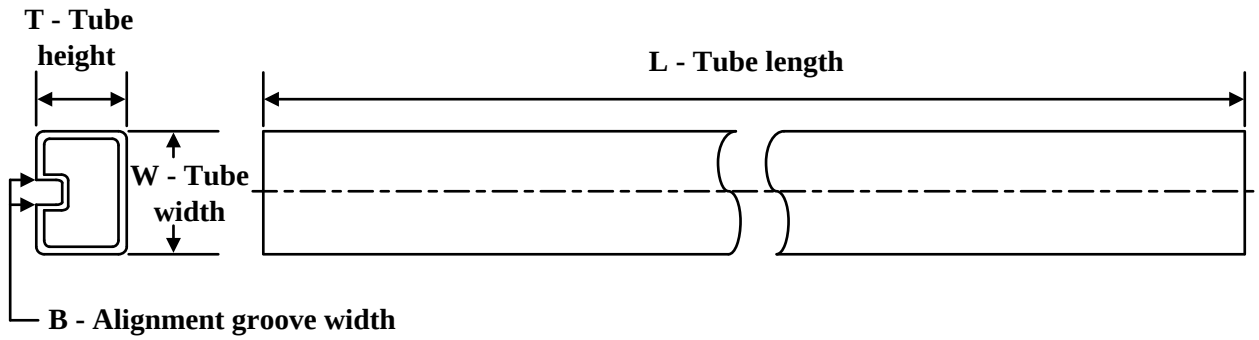
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

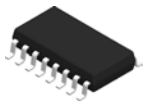
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LS31CDBR	SSOP	DB	16	2000	356.0	356.0	35.0
AM26LS31CDR	SOIC	D	16	2500	356.0	356.0	35.0
AM26LS31CDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LS31CDRG4	SOIC	D	16	2500	340.5	336.1	32.0
AM26LS31CDRG4	SOIC	D	16	2500	356.0	356.0	35.0
AM26LS31CNSR	SO	NS	16	2000	367.0	367.0	38.0
AM26LS31INSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-7802301M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-7802301MFA	W	CFP	16	1	506.98	26.16	6220	NA
5962-7802301Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
AM26LS31CD	D	SOIC	16	40	506.6	8	3940	4.32
AM26LS31CD	D	SOIC	16	40	507	8	3940	4.32
AM26LS31CDE4	D	SOIC	16	40	506.6	8	3940	4.32
AM26LS31CDE4	D	SOIC	16	40	507	8	3940	4.32
AM26LS31CDG4	D	SOIC	16	40	507	8	3940	4.32
AM26LS31CDG4	D	SOIC	16	40	506.6	8	3940	4.32
AM26LS31CN	N	PDIP	16	25	506	13.97	11230	4.32
AM26LS31MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
AM26LS31MWB	W	CFP	16	1	506.98	26.16	6220	NA

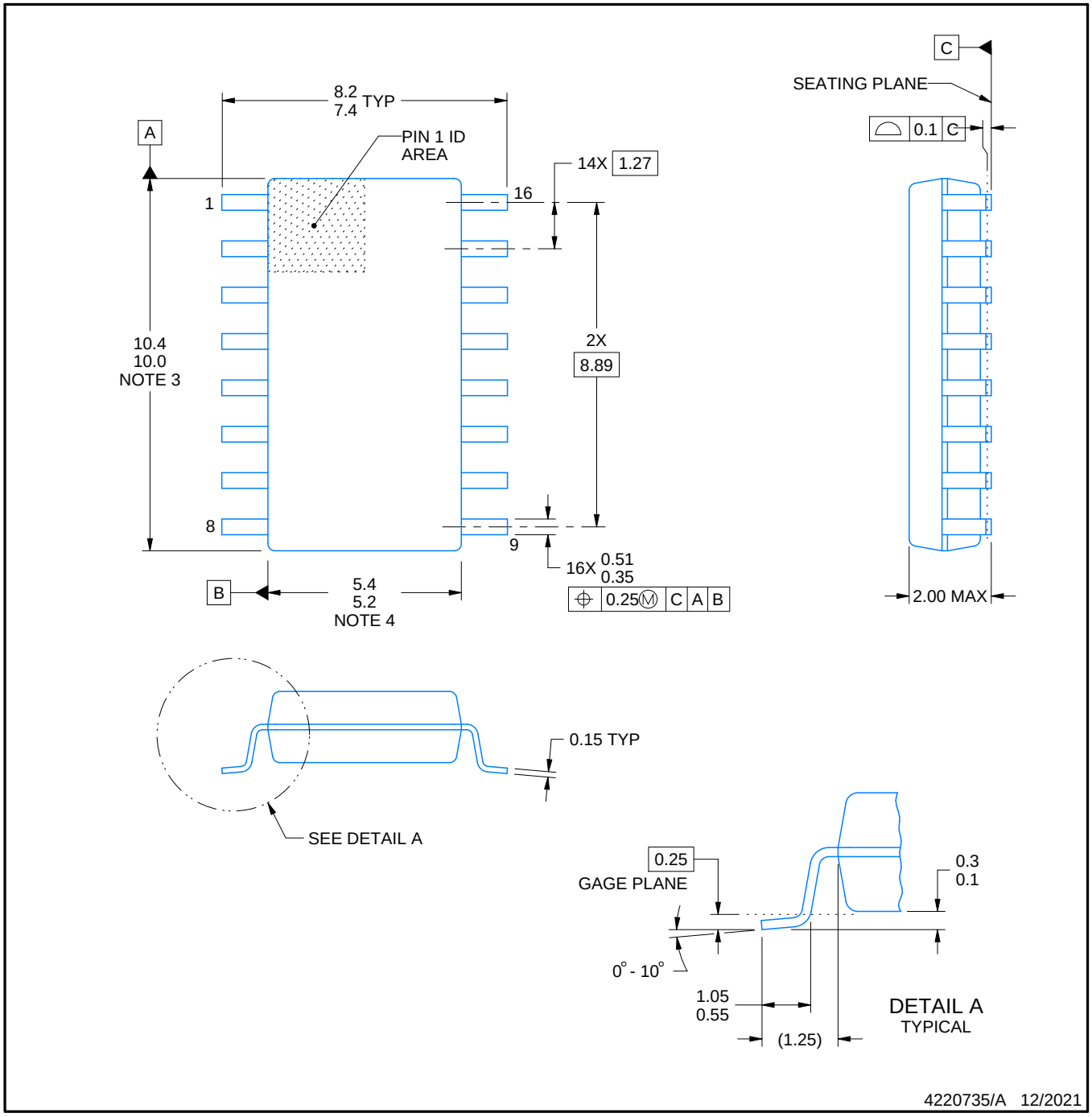


PACKAGE OUTLINE

NS0016A

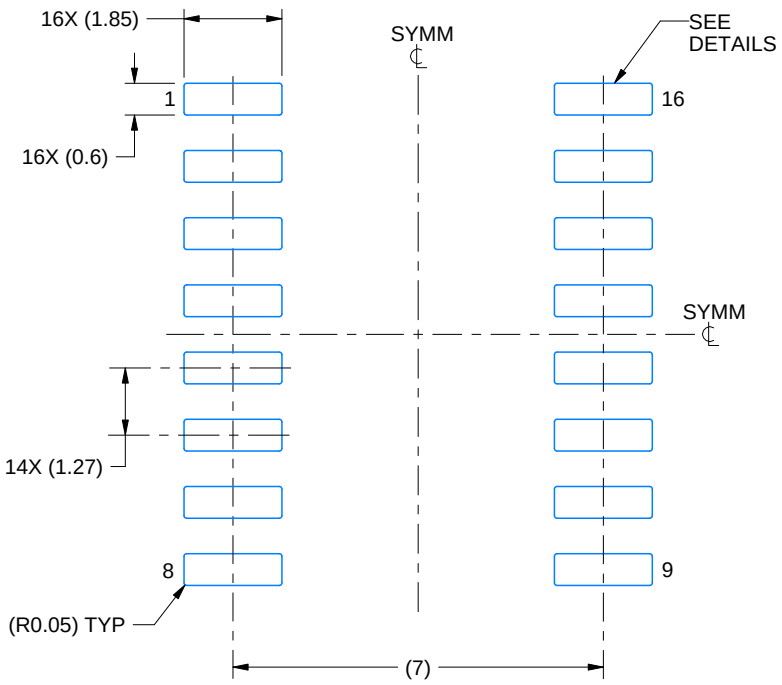
SOP - 2.00 mm max height

SOP

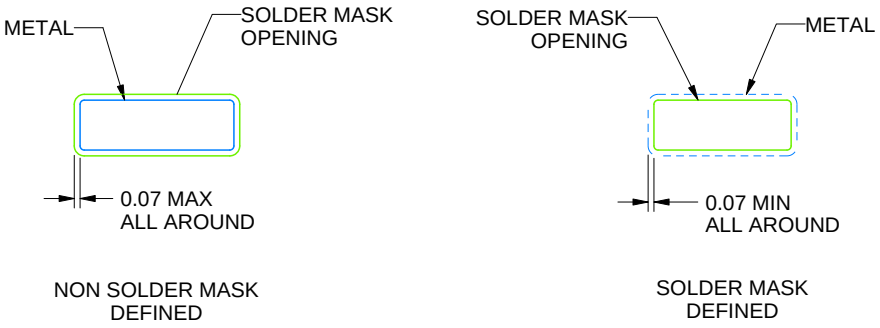


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

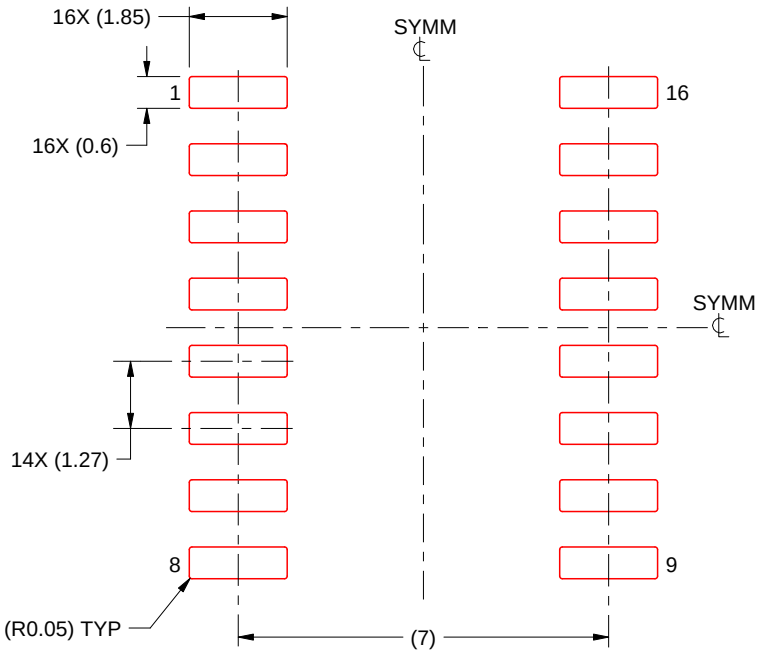
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

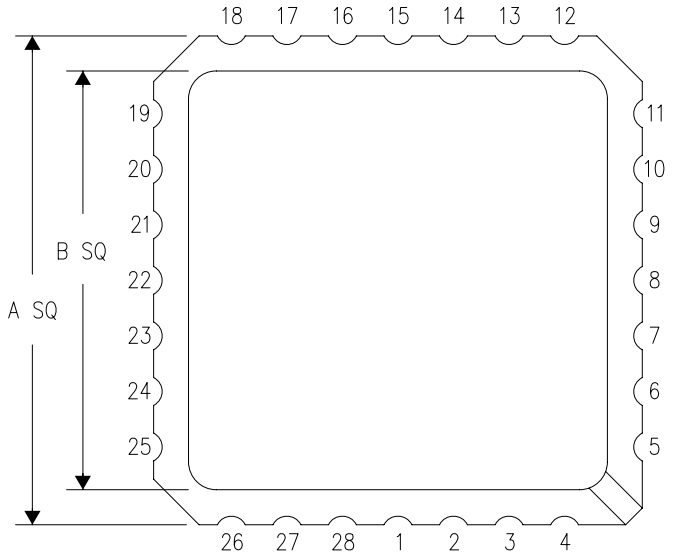
4220735/A 12/2021

NOTES: (continued)

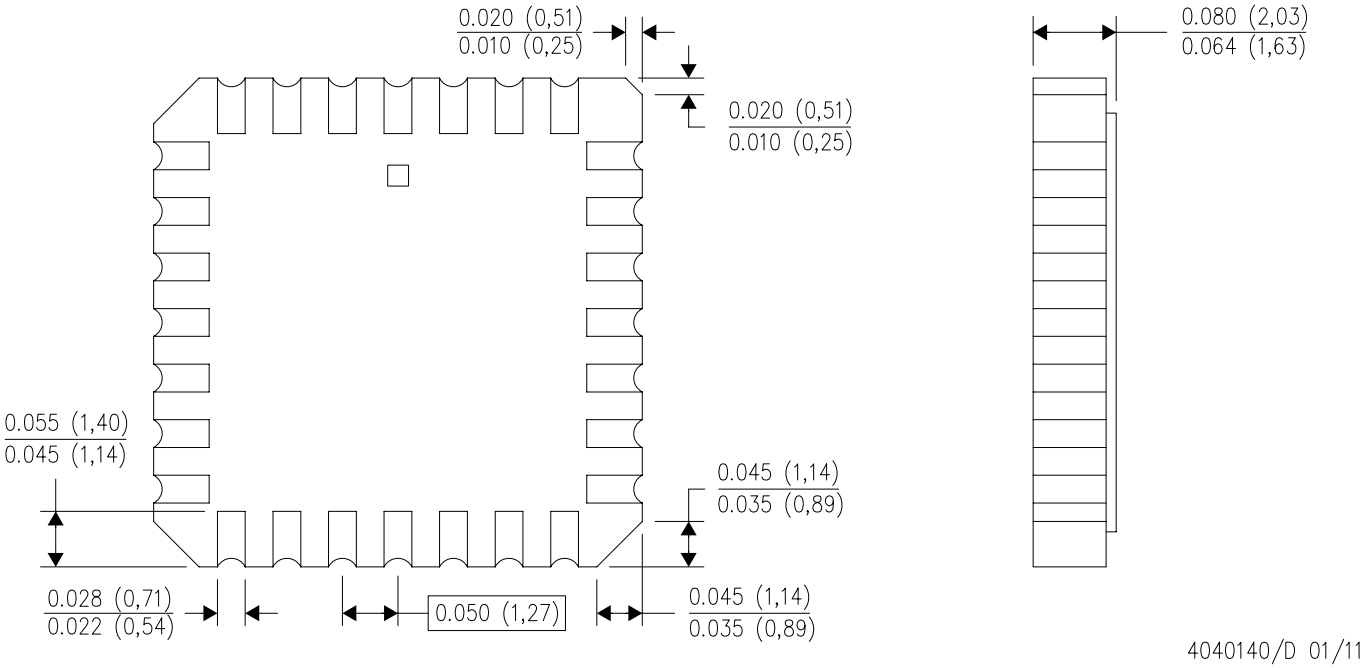
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



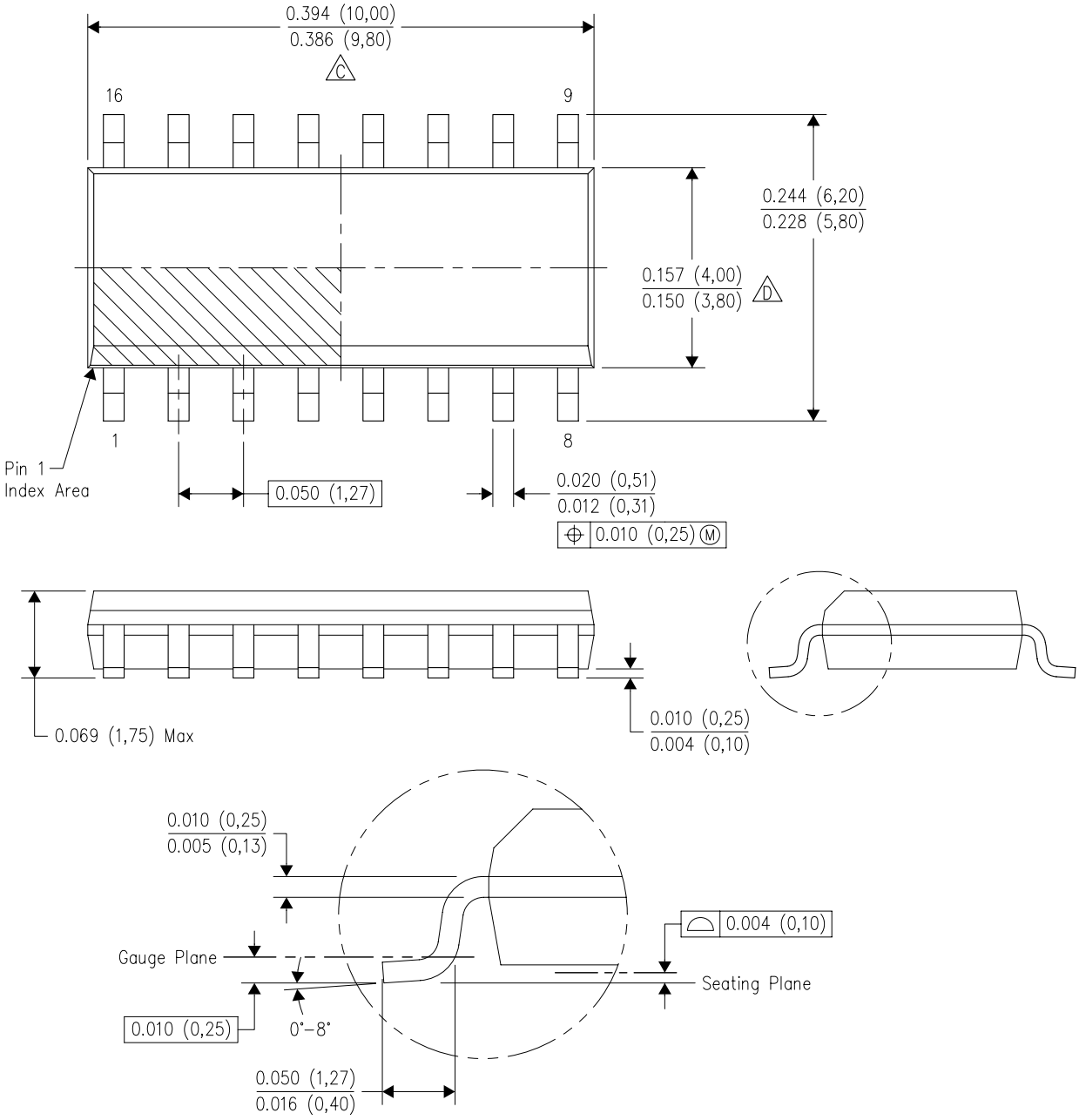
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

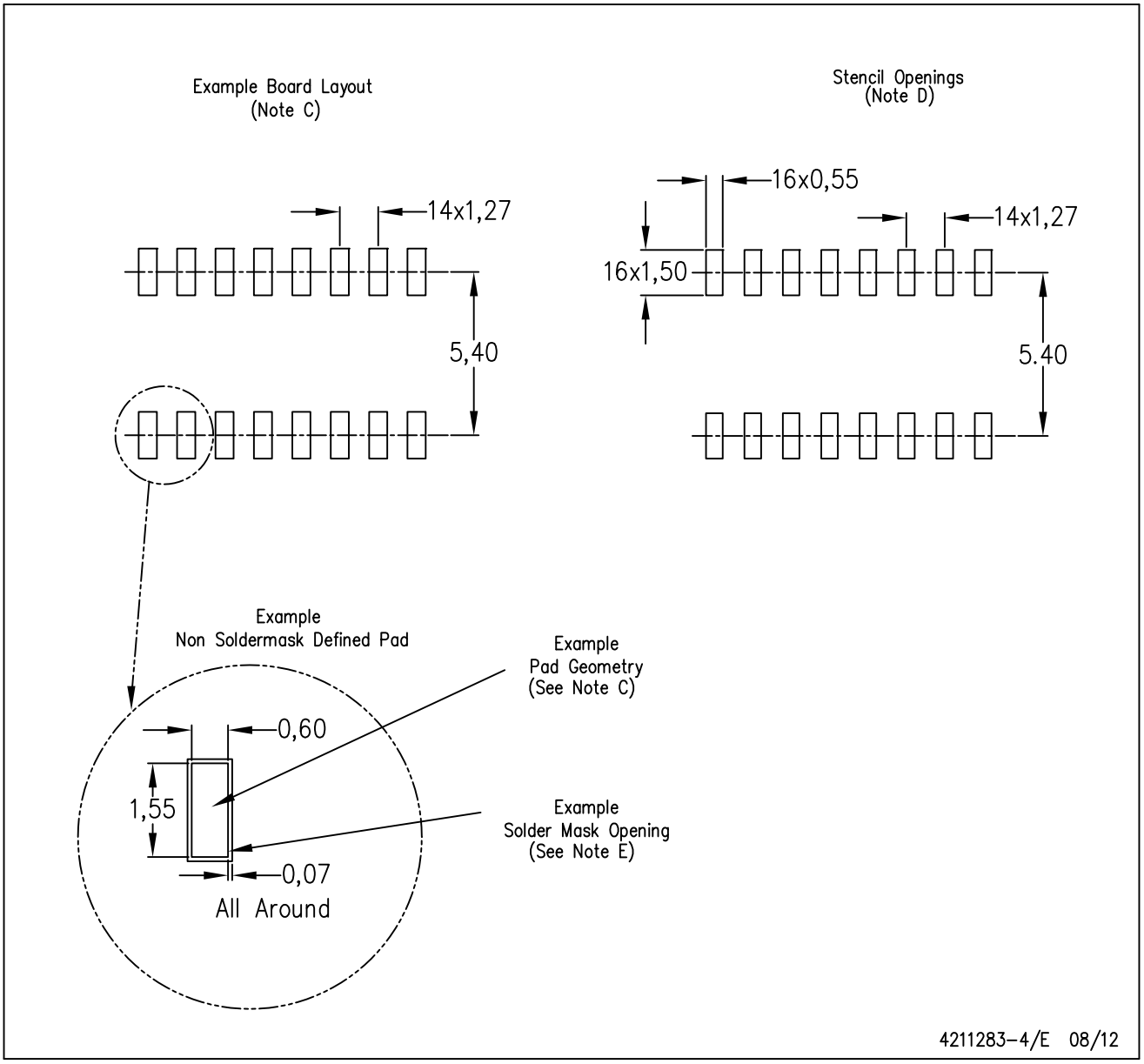
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



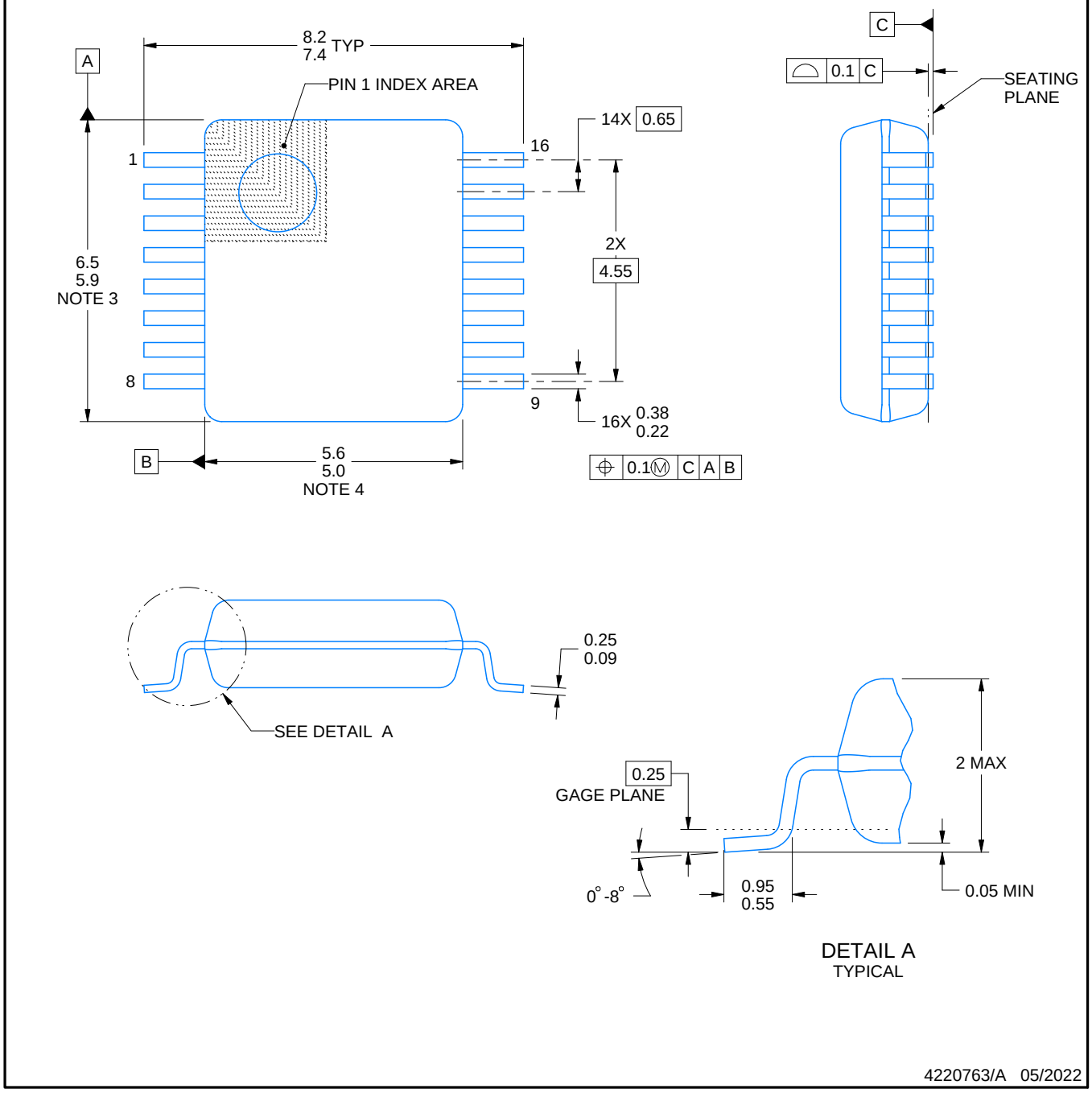
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0016A

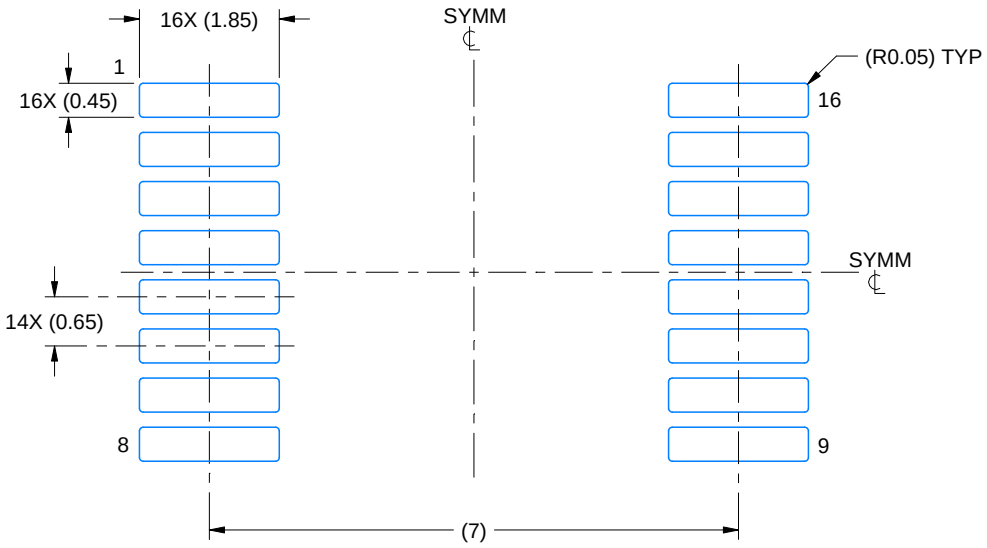
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

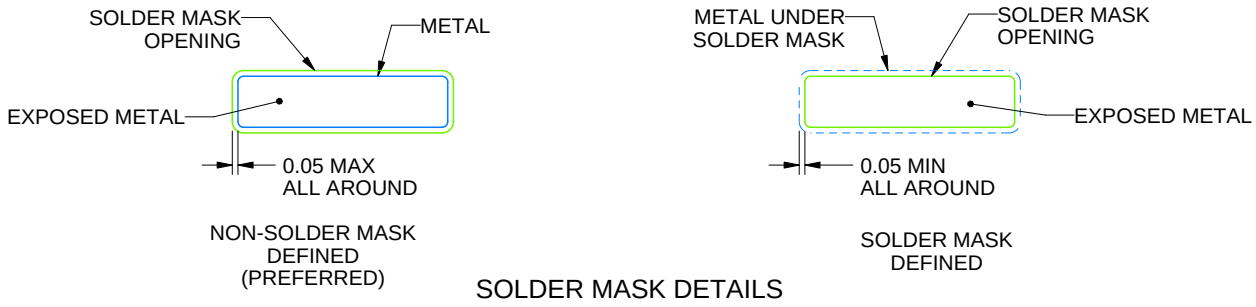


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

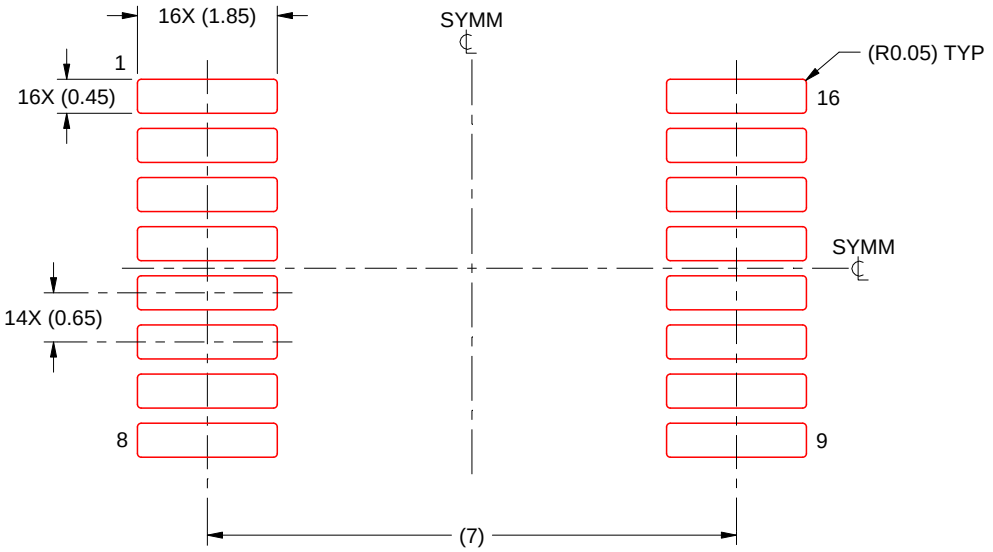


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

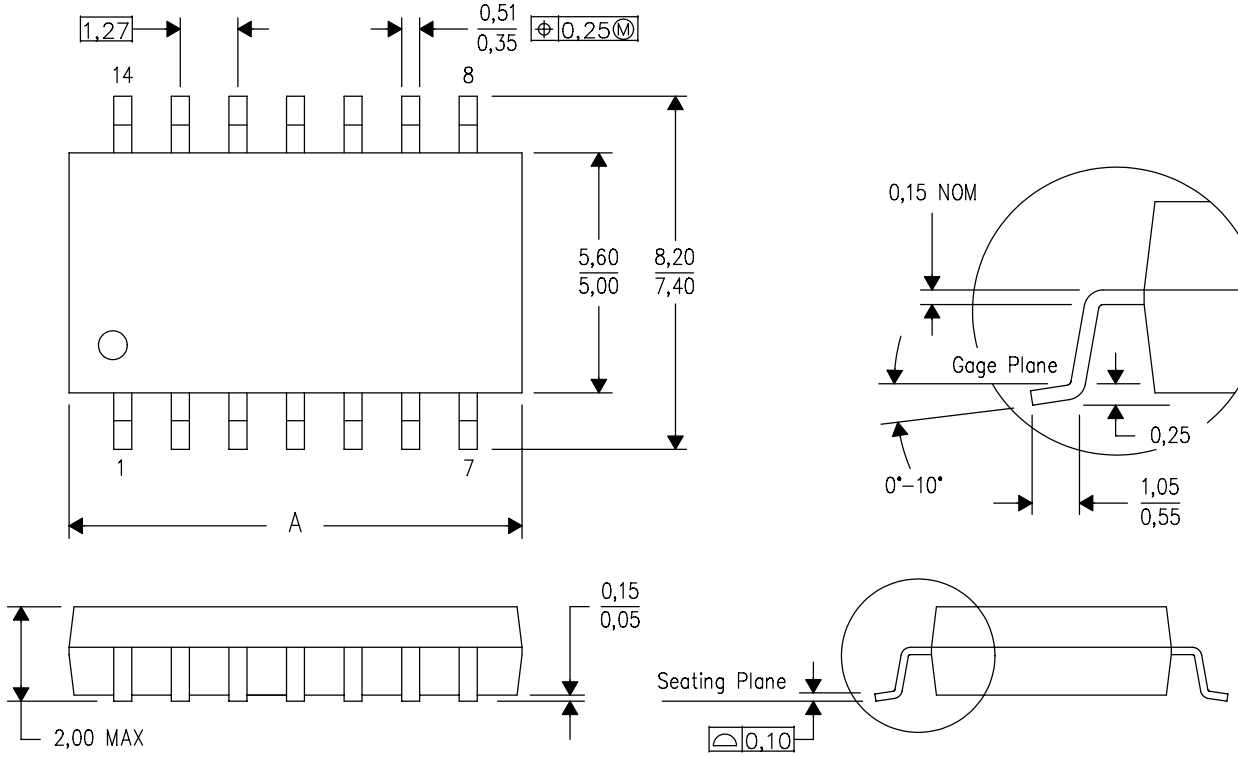
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

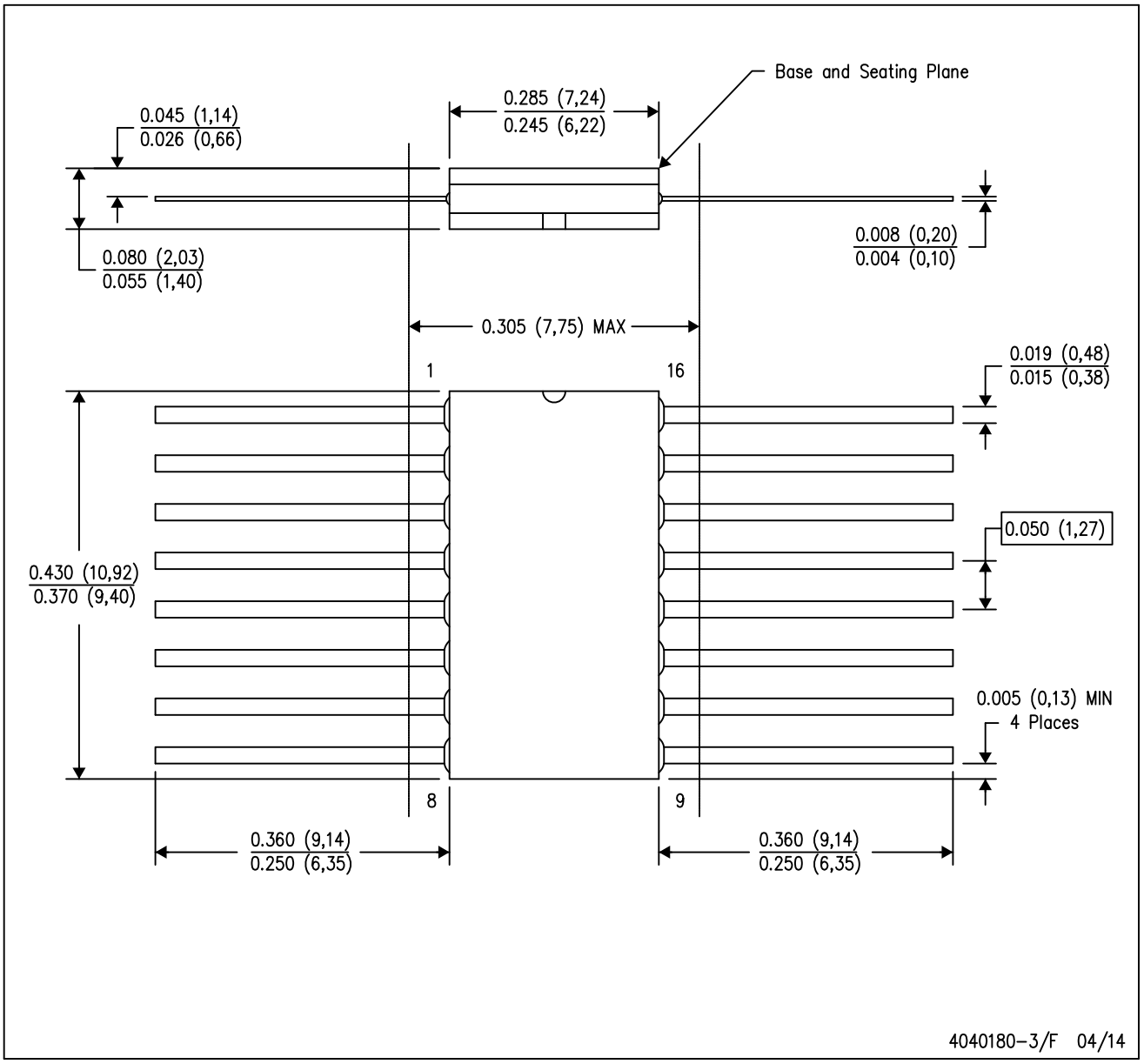


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

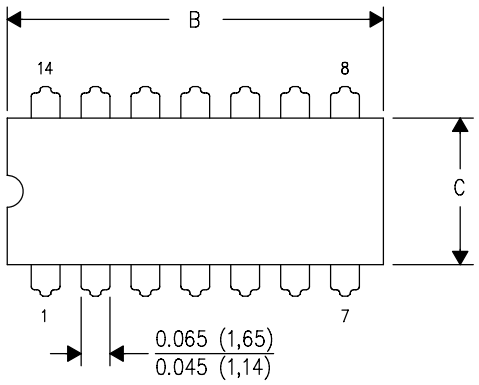


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

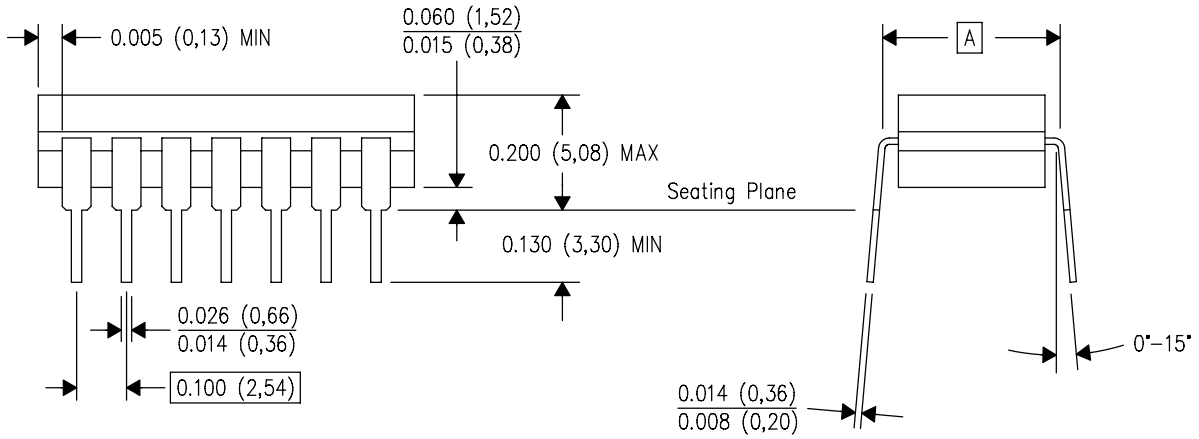
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



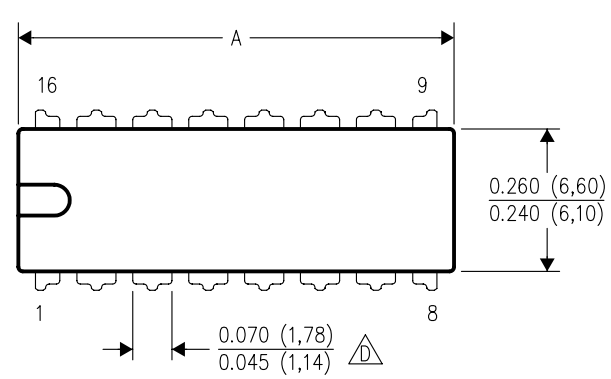
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

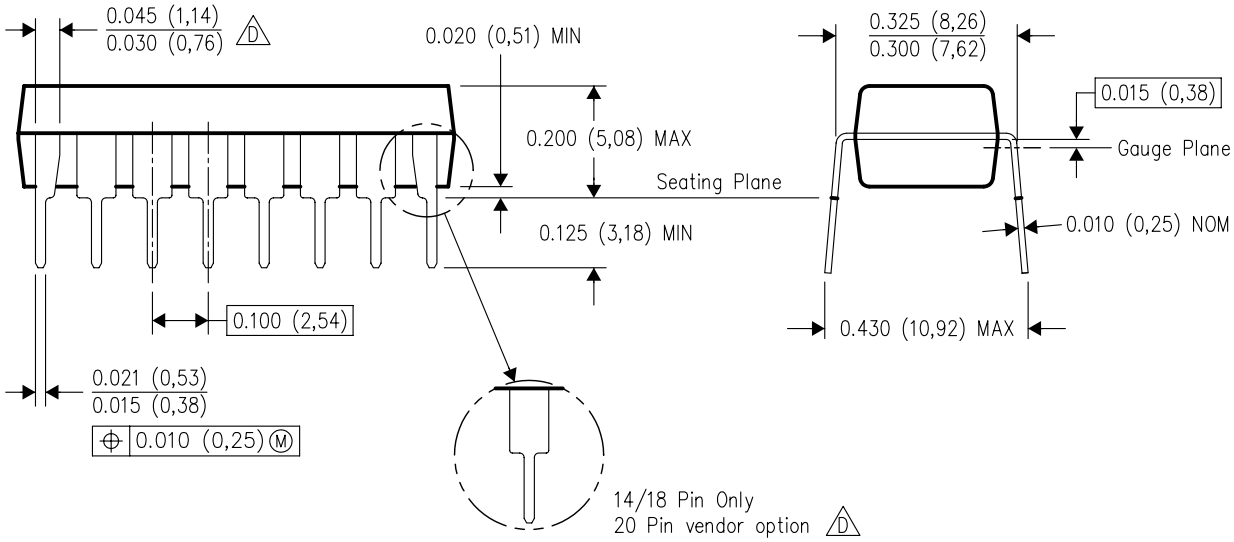
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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