TEXAS INSTRUMENTS

UC1846, UC1847, UC2846
UC2847, UC3846, UC3847

SLUS352C – JANUARY 1997 – REVISED DECEMBER 2015

UCx846/7 Current Mode PWM Controller

1 Features

- Automatic Feedforward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-Pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double-Pulse Suppression
- 500-mA (Peak) Totem-pole Outputs
- ±1% Band Gap Reference
- Undervoltage Lockout
- Soft-Start Capability
- Shutdown Terminal
- 500-kHz Operation

2 Applications

- Telecommunication Power Converters
- Industrial Power Converters

3 Description

The UC1846/7 family of control devices provides all of the necessary features to implement fixed-frequency, current-mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel *power modules* while maintaining equal current sharing.

Protection circuitry includes built-in undervoltage lockout and programmable current limit, in addition to soft-start capability. A shutdown function is also available, which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully-latched operation, double-pulse suppression, deadline adjust capability, and a ±1% trimmed band gap reference.

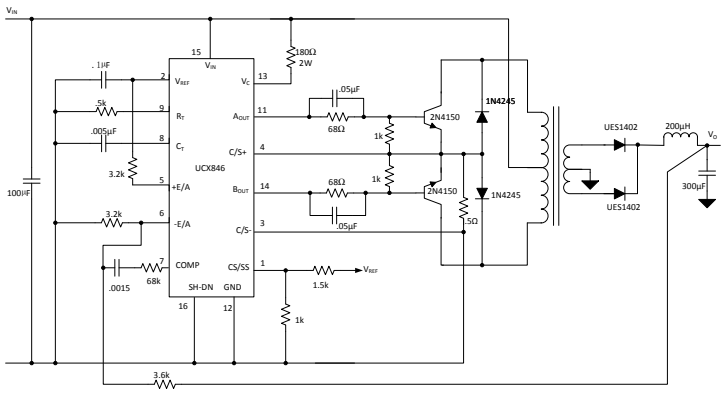
The UC1846 features low outputs in the OFF state, while the UCx847 features high outputs in the OFF state.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC1846	LCCC (20)	8.89 mm × 8.89 mm
	CDIP (16)	6.92 mm × 19.56 mm
UC2846, UC3846	PLCC (20)	8.96 mm × 8.96 mm
	SOIC (16)	7.5 mm × 10.3 mm
	PDIP (16)	6.35 mm × 19.3 mm
UC2847, UC3847	SOIC (16)	7.5 mm × 10.3 mm
	PDIP (16)	6.35 mm × 19.3 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2010) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed soldering temperature ... 4

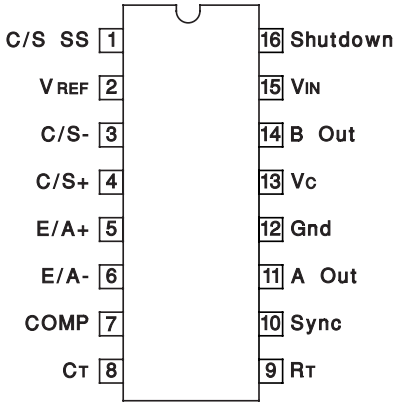
Changes from Revision A (February 2002) to Revision B — **Page**

- Updated Block Diagram. ... 1

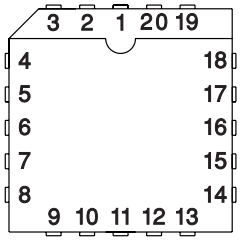
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5 Pin Configuration and Functions

J or N, DW Packages
16-Pin CDIP or PDIP, SOIC
Top View



FN or FK Packages
20-Pin PLCC or LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
DIL, SOIC NO.	PLCC, LCC NO.	NAME		
1	2	C/S SS	I	Current limit/soft-start programming
2	3	V_{REF}	O	5.1-V reference voltage output
3	4	C/S –	I	Current sense comparator inverting input
4	5	C/S +	I	Current sense comparator non-inverting input
5	7	E/A +	I	Error amplifier inverting input
6	8	E/A –	I	Error amplifier inverting input
7	9	COMP	I/O	Error amplifier output and input to the PWM comparator
8	10	C_T	I	Oscillator frequency programming capacitor pin
9	12	C_R	I	Oscillator frequency programming resistor pin
10	13	Sync	I/O	Synchronization out from master controller or input of slave controller
11	14	A Out	O	PWM drive signal output A, Pin11 and P14 are complementary
12	15	GND	G	All signals are referenced to this node
13	17	V_C	I	Bias supply input for output stage
14	18	B Out	O	PWM drive signal output B, Pin11 and P14 are complementary
15	19	V_{IN}	I	Bias supply input
16	20	Shutdown	I	External shutdown signal input
—	1, 6, 11, 16	N/C		

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage (Pin 15)		40	V
Collector Supply Voltage (Pin 13)		40	V
Output Current, Source or Sink (Pins 11, 14)		500	mA
Analog Inputs (Pins 3, 4, 5, 6, 16)	–0.3	$+V_{IN}$	V
Reference Output Current (Pin 2)		–30	mA
Sync Output Current (Pin 10)		–5	mA
Error Amplifier Output Current (Pin 7)		–5	mA
Soft Start Sink Current (Pin 1)		50	mA
Oscillator Charging Current (Pin 9)		5	mA
Power Dissipation at T_A = 25°C		1000	mW
Power Dissipation at T_C = 25°C		2000	mW
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VREF terminal external capacitance	1		2.2	µF

6.4 Thermal Information

THERMAL METRIC(1)		UCx846/7		UNIT
		N or DW (PDIP or SOIC)	J or DW (CDIP or SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	73.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.5	34.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	38.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.0	7.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.7	37.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

T_A=–55°C to +125°C for UC1846/7; –40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15 V, R_T=10k, C_T=4.7 nF, T_A=T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	UC1846/7 UC2846/7			UC3846/7			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE								
Output Voltage	T_J = 25°C, I_O = 1 mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 V to 40 V		5	20		5	20	mV
Load Regulation	I_L = 1 mA to 10 mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (1)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (1)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10 Hz ≤ f ≤10 kHz, T_J = 25°C(1)		100			100		µV
Long Term Stability	T_J = 125°C, 1000 Hrs(1)		5			5		mV
Short Circuit Output Current	V_{REF} = 0 V	–10	–45		–10	–45		mA
OSCILLATOR								
Initial Accuracy	T_J = 25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN} =8 V to 40 V		–1%	2%		–1%	2%	
Temperature Stability	Over Operating Range (1)		–1%			–1%		
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8 = 0 V	3.9			3.9			V
Sync Input Low Level	Pin 8 = 0 V			2.5			2.5	V
Sync Input Current	Sync Voltage = 3.9 V, Pin 8 = 0 V		1.3	1.5		1.3	1.5	mA
ERROR AMPLIFIER								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			–0.6	–1		–0.6	–2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN} = 8 V to 40 V	0		V_{IN} - 2 V	0		V_{IN} - 2 V	V
Open Loop Voltage Gain	ΔV_O = 1.2 to 3 V, V_{CM} = 2 V	80	105		80	105		dB
Unity Gain Bandwidth	T_J = 25°C(1)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM} = 0 V to 38 V, V_{IN} = 40 V	75	100		75	100		dB
PSRR	V_{IN} = 8 V to 40 V	80	105		80	105		dB
Output Sink Current	V_{ID} = –15 mV to -5 V, V_{PIN7} = 1.2 V	2	6		2	6		mA
Output Source Current	V_{ID} = 15 mV to -5 V, V_{PIN7} = 2.5 V	–0.4	–0.5		–0.4	–0.5		mA
High Level Output Voltage	R_L = (Pin 7) 15 kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	R_L = (Pin 7) 15 kΩ		0.7	1		0.7	1	V
CURRENT SENSE AMPLIFIER								
Amplifier Gain	$V_{PIN\ 3}$ = 0 V, Pin 1 Open(2), (3)	2.5	2.75	3.0	2.5	2.75	3.0	V

(1) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.
(2) Parameter measured at trip point of latch with VPIN 5 = VREF, VPIN 6 = 0 V.
(3) Amplifier gain defined as: G = ΔV_{PIN7} / ΔV_{PIN4}; V_{PIN4} = 0 to 1.0 V

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Electrical Characteristics (continued)

T_A=–55°C to +125°C for UC1846/7; –40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15 V, R_T=10k, C_T=4.7 nF, T_A=T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	UC1846/7 UC2846/7			UC3846/7			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (2); R_L (Pin 7) = 15 kW	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN\ 1}$ = 0.5 V, Pin 7 Open(2)		5	25		5	25	mV
CMRR	V_{CM} = 1 V to 12 V	60	83		60	83		dB
PSRR	V_{IN} = 8 V to 40 V	60	84		60	84		dB
Input Bias Current	$V_{PIN\ 1}$ = 0.5 V, Pin 7 Open(2)		–2.5	–10		–2.5	–10	µA
Input Offset Current	$V_{PIN\ 1}$ = 0.5 V, Pin 7 Open(2)		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_J = 25°C (1)		200	500		200	500	ns
CURRENT LIMIT ADJUST								
Current Limit Offset	$V_{PIN\ 3}$ = 0 V, $V_{PIN\ 4}$ = 0 V, Pin 7 Open (2)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0 V		–10	–30		–10	–30	µA
SHUTDOWN TERMINAL								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current (I_{PIN1})		(4)3.0	1.5		3.0	1.5		mA
Maximum Latching Current (I_{PIN1})			(5)1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_J = 25°C (1)		300	600		300	600	ns
OUTPUT								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C = 40 V (6)			200			200	µA
Output Low Level	I_{SINK} = 20 mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 100 mA		0.4	2.1		0.4	2.1	
Output High Level	I_{SOURCE} = 20 mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100 mA	12	13.5		12	13.5		
Rise Time	C_L (1) = 1 nF, T_J = 25°C		50	300		50	300	ns
Fall Time	C_L (1) = 1 nF, T_J = 25°C		50	300		50	300	ns
UNDERVOLTAGE LOCKOUT								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
TOTAL STANDBY CURRENT								
Supply Current			17	21		17	21	mA

(4) Current into Pin 1 ensured to latch circuit in shutdown state.
(5) Current into Pin 1 ensured not to latch circuit in shutdown state.
(6) Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.

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6.6 Typical Characteristics

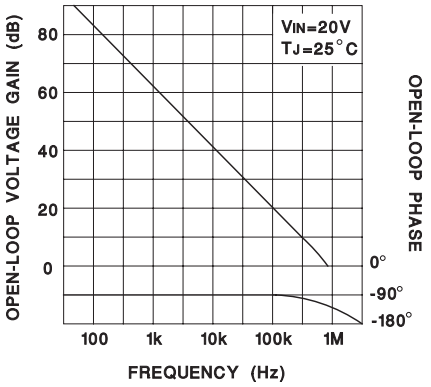


Figure 1. Error Amplifier Gain and Phase vs Frequency

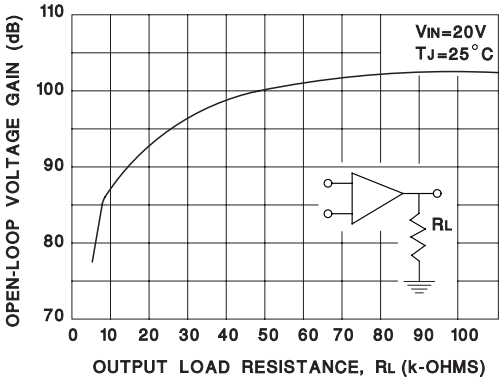


Figure 2. Error amplifier Open-Logic DC Gain vs Load Resistance

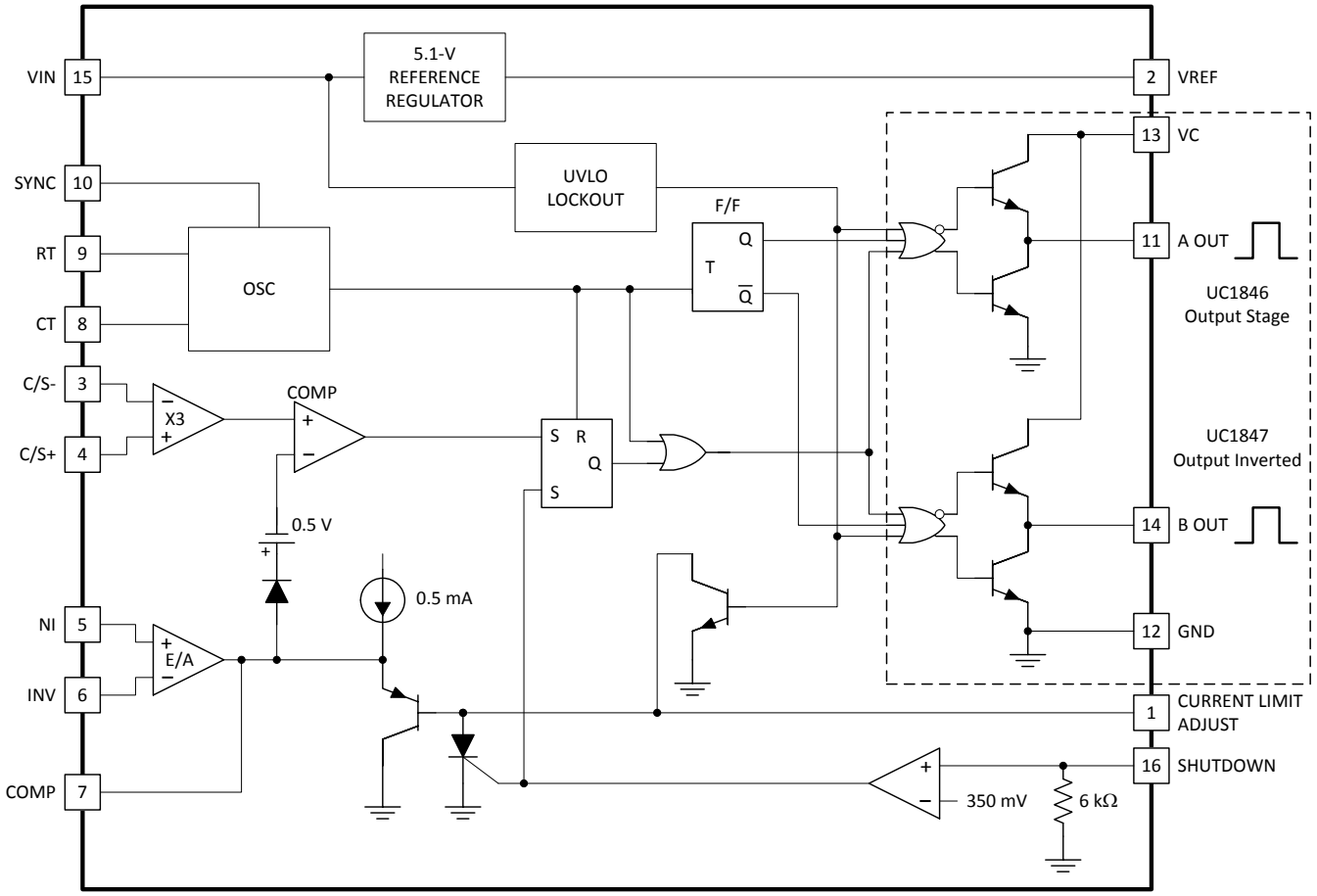
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7 Detailed Description

7.1 Overview

The UCx846/7 family of control devices provides the necessary features to implement off-line or DC-to-DC fixed-frequency, current-mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amplifier input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high-peak current. The output stage, suitable for driving either N-Channel MOSFETs or bipolar transistor switches, is low in the off state.

7.2 Functional Block Diagram



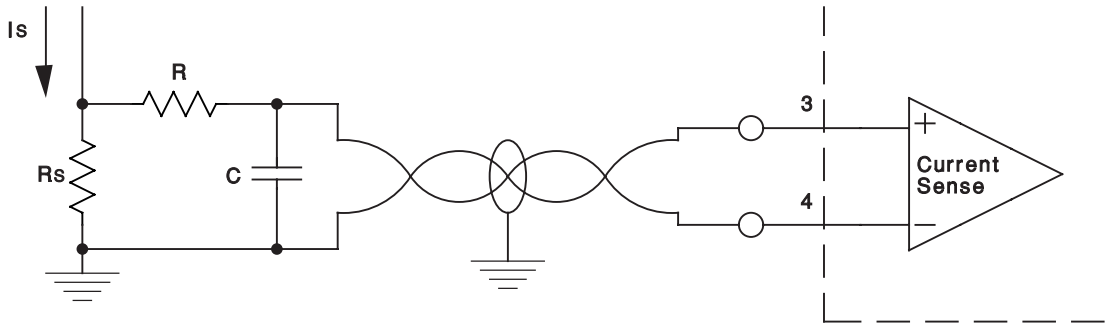
7.3 Feature Description

7.3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to *Functional Block Diagram*, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5 V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2 V at the current sense inputs.

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Feature Description (continued)



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

Figure 3. Current Sense Amplifier Connection

7.3.2 Oscillator

By implementing the oscillator using all NPN transistors, the UCx846/7 achieves excellent temperature stability and waveform clarity at frequencies in excess of 1 MHz.

Referring to Figure 4, an external resistor R_T is used to generate a constant current into a capacitor C_T to produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{OSC} = \frac{2.2}{R_T C_T} \quad (1)$$

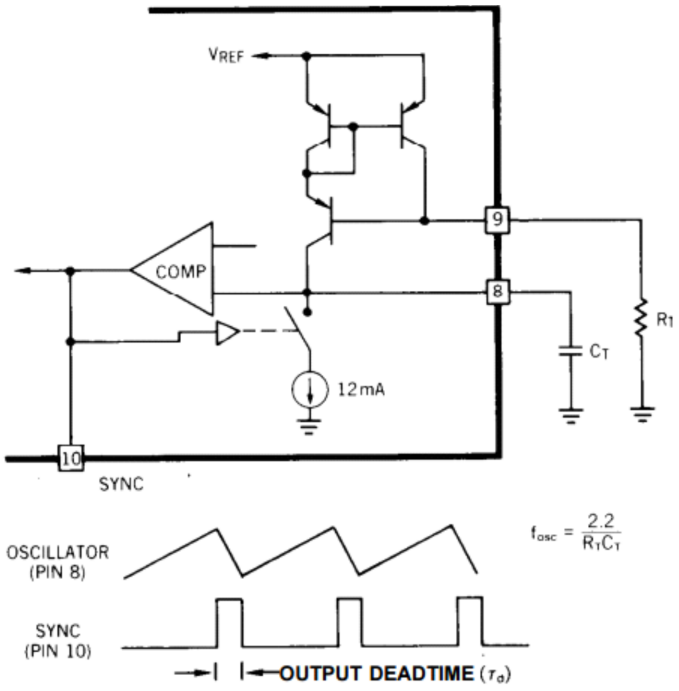


Figure 4. Oscillator Circuit

7.4 Device Functional Modes

7.4.1 Current Limit

One of the most attractive features of a current-mode converter is the ability to limit peak-switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value.

7.4.2 Shutdown

The shutdown circuit was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350-mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350 mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCx846/7 family of control devices provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters. Protection circuitry includes undervoltage lockout and programmable current limit in addition to soft-start capability. A shutdown function is also available which initiates either a complete shutdown with automatic restart or latch the supply off.

8.2 Typical Application

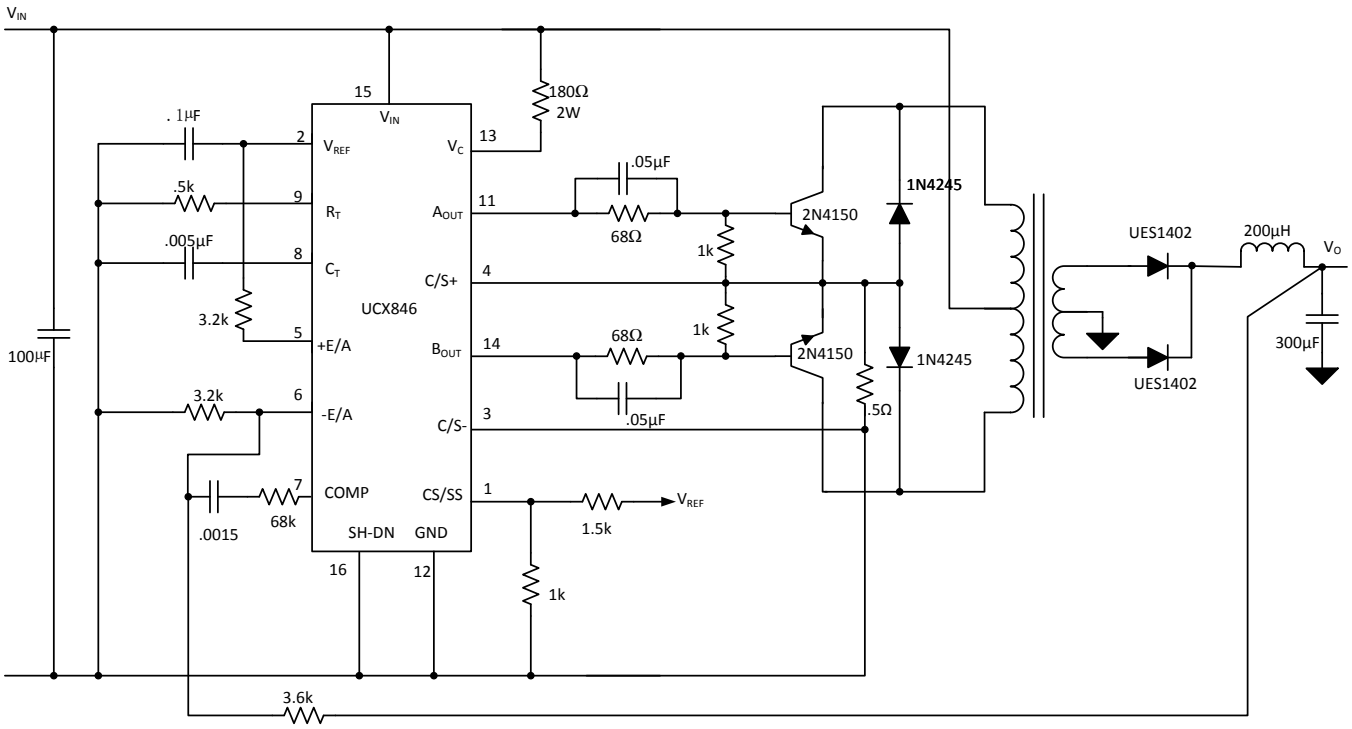


Figure 5. Typical Application Diagram

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

DESIGN PARAMETER	TARGET VALUE
Typical efficiency	85%
Switching frequency	880 kHz
Pulse by pulse current limit threshold	1 A

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8.2.2 Detailed Design Procedure

This section details the design procedure based on the design requirements.

8.2.2.1 Design Switching Frequency

Output deadtime is determined by the external capacitor, C_T, according to the formula:

$$Td(\mu s) = 145\,C_T(\mu F)\left[\frac{ID}{ID - \frac{3.6}{RT(k\Omega)}}\right] \quad (2)$$

where

- ID = Oscillator discharge current at 25°C; typically is 7.5.

For large values of R_T: τd (μs) ≈145CT (μF).

Oscillator frequency is approximated by the formula:

$$fT(kHz) \approx \frac{2.2}{\left(R_T(k\Omega) \times C_T(\mu F)\right)} \quad (3)$$

8.2.2.2 Error Amplifier Output Configuration

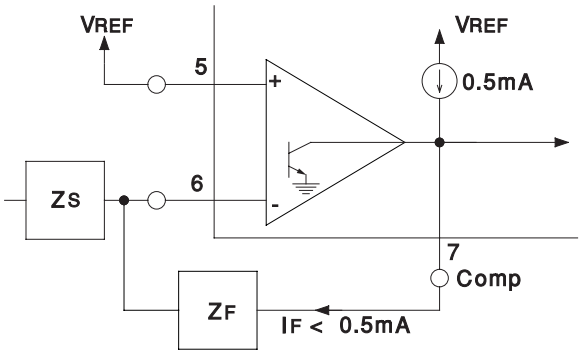
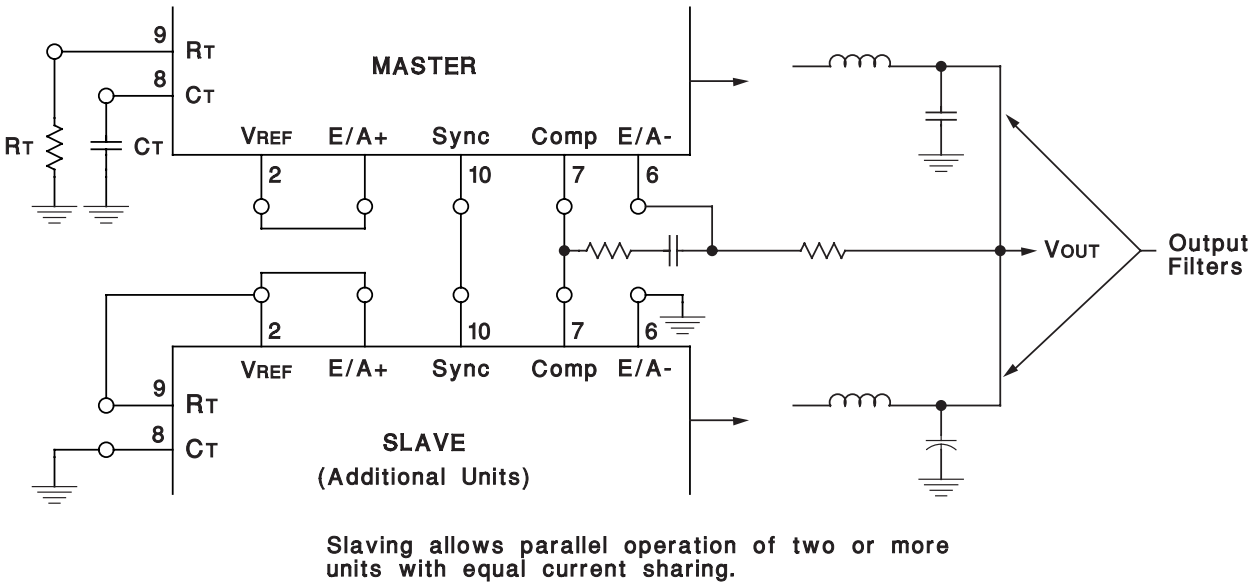


Figure 6. Error Amplifier Output Configuration

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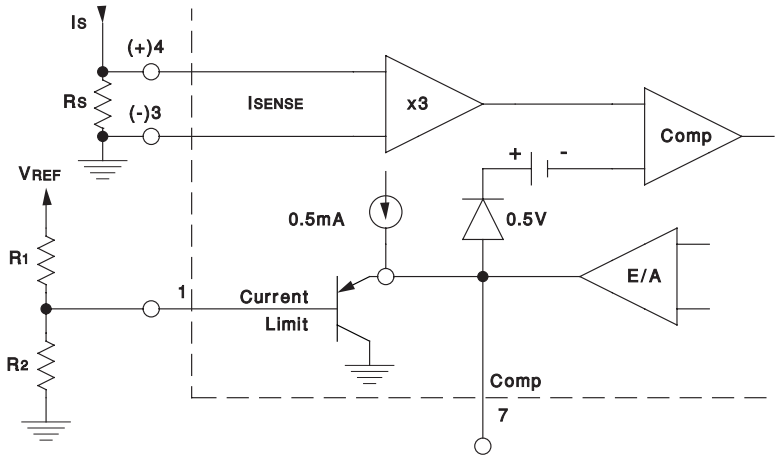
8.2.2.3 Parallel Operation Configuration



Slaving allows parallel operation of two or more units with equal current sharing.

Figure 7. Parallel Operation

8.2.2.4 Design Pulse by Pulse Current Limit Threshold



Peak Current (Is) is determined by the formula: $IS = \frac{\frac{R2\,VREF}{R1 + R2} - 0.5}{3RS}$

Figure 8. Pulse by Pulse Current Limiting

8.2.2.5 Soft-Start and Shutdown, Restart Function Design

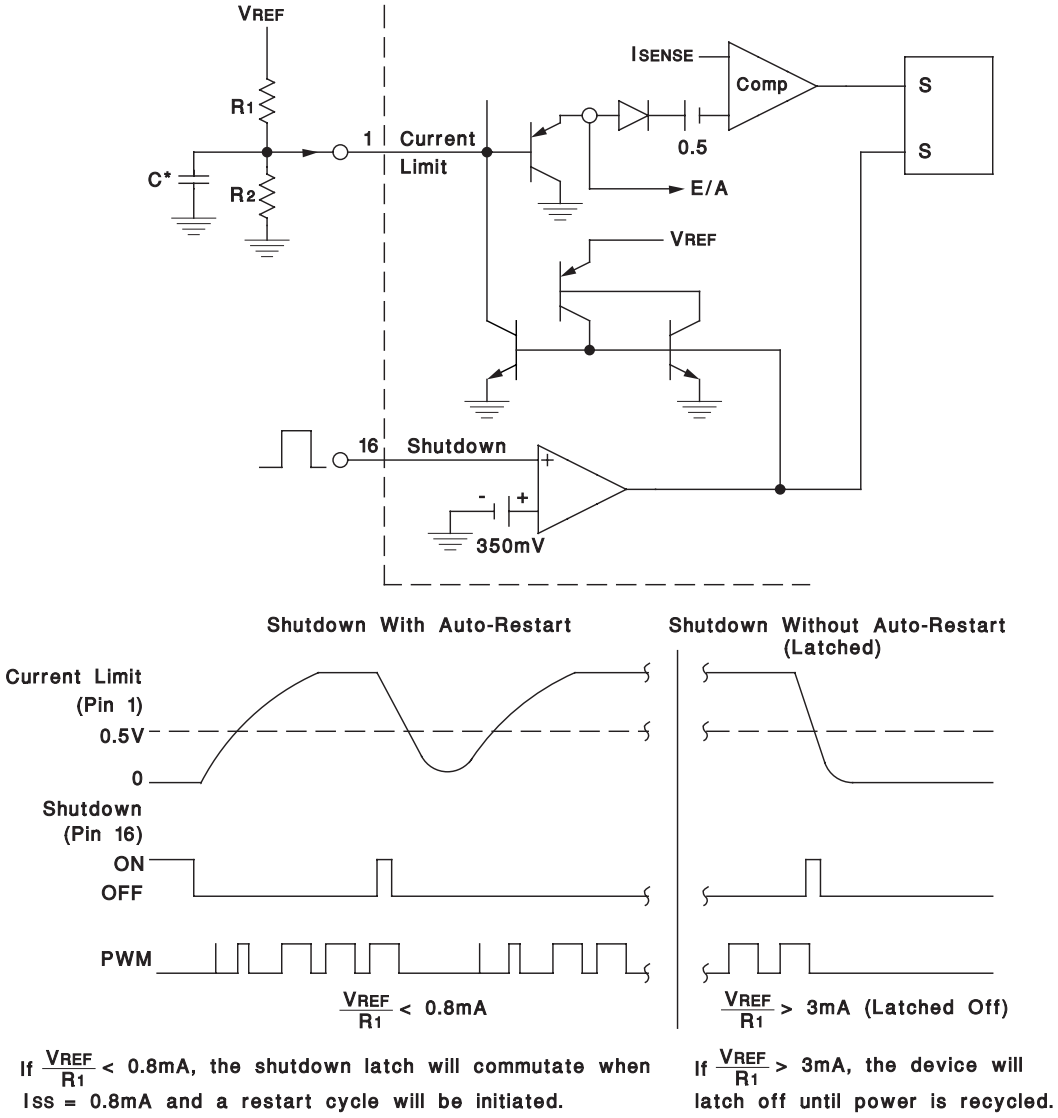
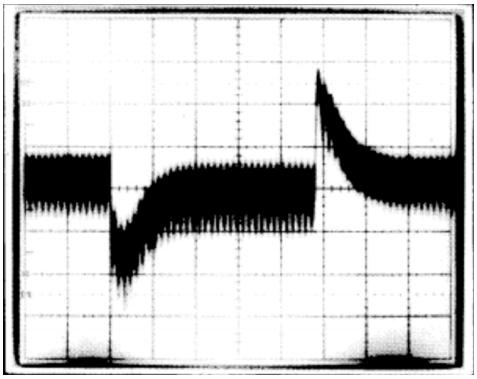


Figure 9. Soft-Start and Shutdown, Restart Functions

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8.2.3 Application Curves



t = 0.2 ms/div output response = 20 mV/div

Figure 10. Responsive to a Step Load Change of 1 A

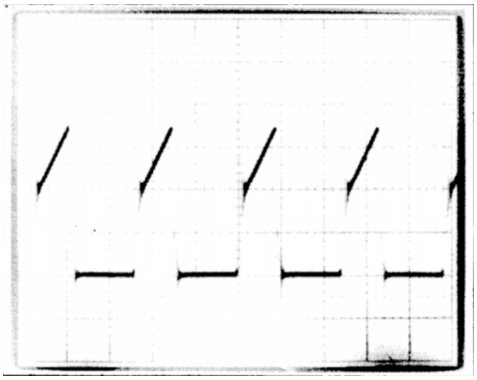


Figure 11. Switch Current Showing Flux Balance in UCX846/7

9 Power Supply Recommendations

The VIN power terminal for the device requires the placement of low esr noise-decoupling capacitance as directly as possible from the VIN terminal to the GND terminal. Ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better.

The VC power terminal for the device requires the placement of resistance as directly as possible from the VC terminal to the VIN terminal.

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10 Layout

10.1 Layout Guidelines

- Place a low ESR and ESL decoupling capacitor C_{REF} in the 1-µF to 2.2-µF range, preferably ceramic, from VREF pin to GND.
- The EA+ is a non-inverting input, the EA– is an inverting input and the COMP is the output of the error amplifier. Place resistor and capacitor series network between EA+ pin and COMP pin, and reduce the trace of resistor and capacitor series network as much as possible.
- Place a low ESR and ESL capacitor C_T, preferably ceramic, from CT pin to GND, and place C_T close to UCx846/7 as much as possible.
- Place a resistor R_T from RT pin to GND, and place R_T close to UCx846/7 as much as possible.

10.2 Layout Example

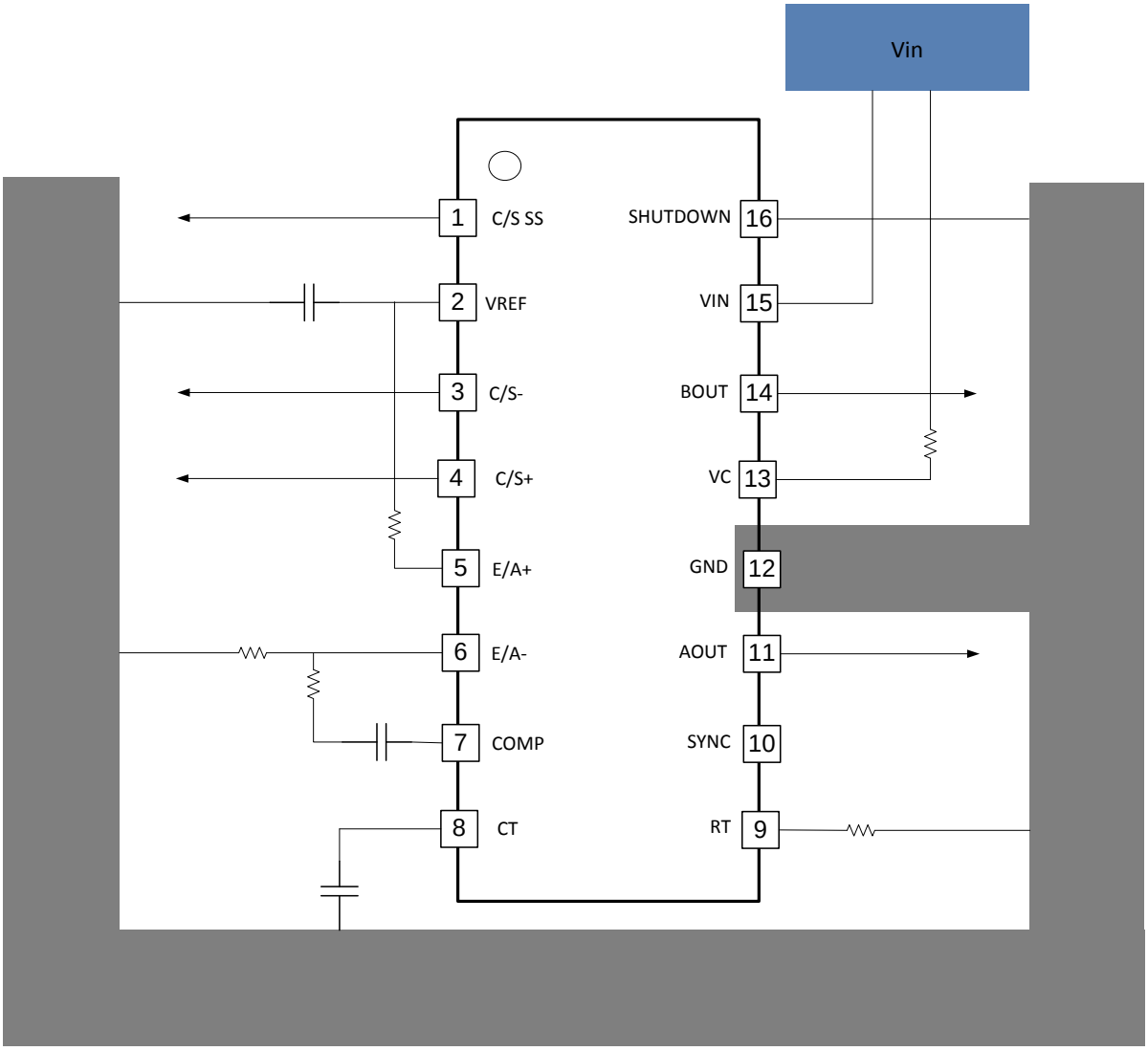


Figure 12. UCx84x Layout Example

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1846	Click here	Click here	Click here	Click here	Click here
UC1847	Click here	Click here	Click here	Click here	Click here
UC2846	Click here	Click here	Click here	Click here	Click here
UC2847	Click here	Click here	Click here	Click here	Click here
UC3846	Click here	Click here	Click here	Click here	Click here
UC3847	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86806012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-86806012A UC1846L/ 883B	Samples
5962-8680601EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8680601EA UC1846J/883B	Samples
UC1846J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1846J	Samples
UC1846J883B	ACTIVE	CDIP	J	16	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8680601EA UC1846J/883B	Samples
UC1846L883B	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-86806012A UC1846L/ 883B	Samples
UC2846DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2846DW	Samples
UC2846DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2846DW	Samples
UC2846DWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2846DW	Samples
UC2846J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-40 to 85	UC2846J	Samples
UC2846N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UC2846N	Samples
UC2846NG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UC2846N	Samples
UC3846DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3846DW	Samples
UC3846DWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3846DW	Samples
UC3846DWTRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3846DW	Samples
UC3846N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3846N	Samples
UC3846NG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3846N	Samples
UC3847DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3847DW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC1846, UC2846, UC2846M, UC3846 :

- Catalog : UC3846, UC2846
- Enhanced Product : UC1846-EP, UC1846-EP
- Military : UC2846M, UC1846

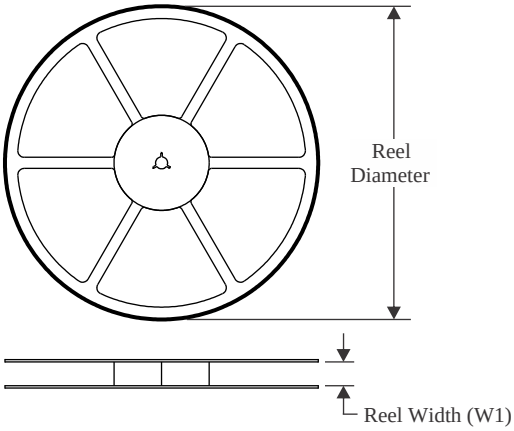
- Space : UC1846-SP, UC1846-SP

NOTE: Qualified Version Definitions:

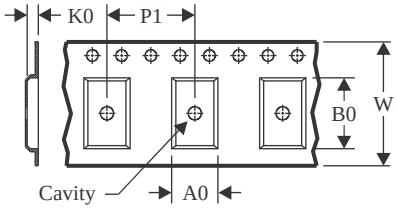
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

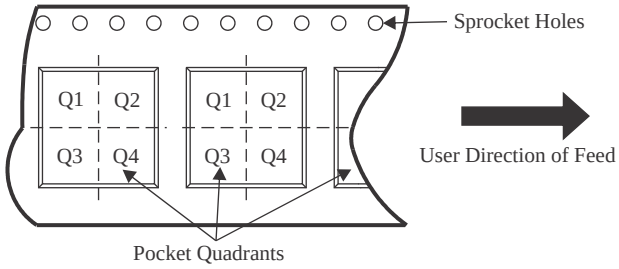


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

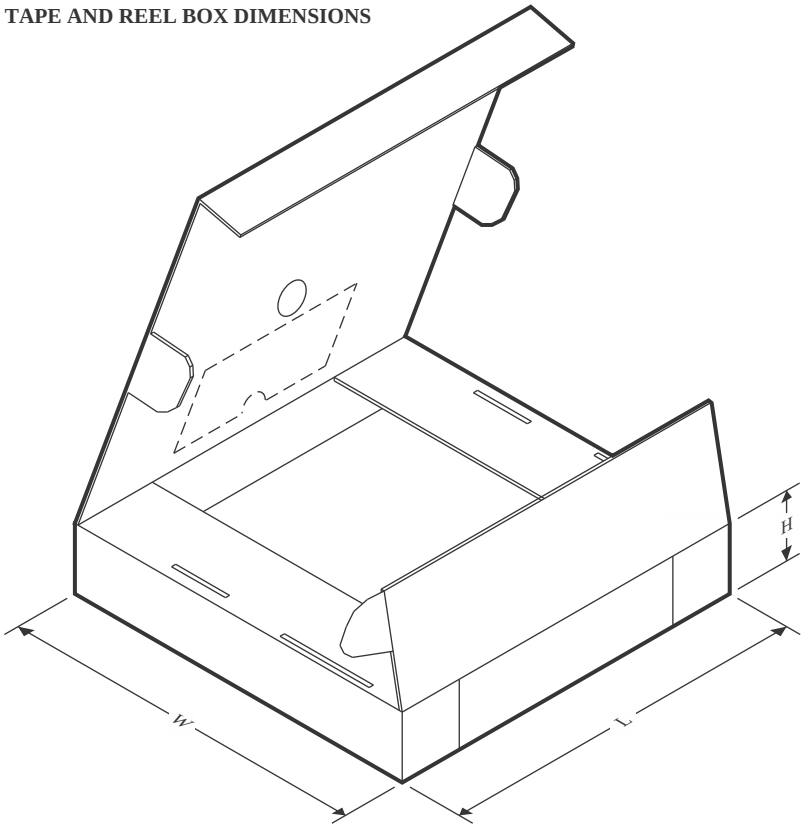
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2846DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3846DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

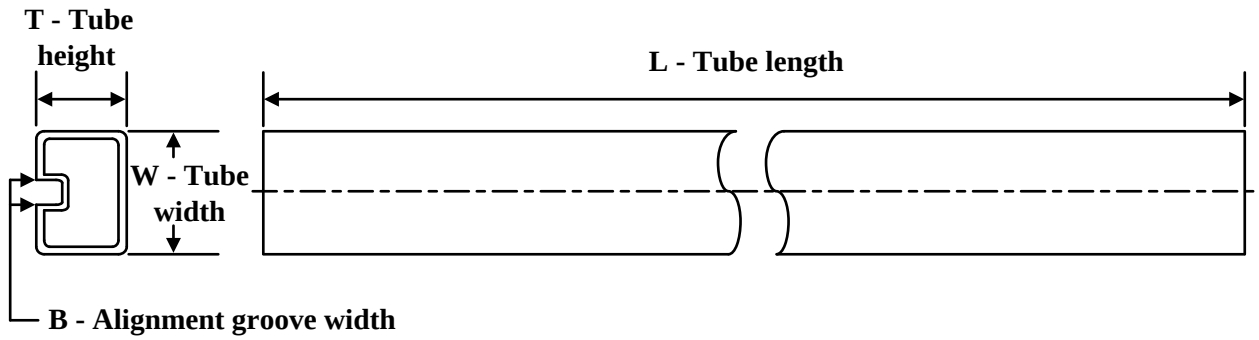
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2846DWTR	SOIC	DW	16	2000	356.0	356.0	35.0
UC3846DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-86806012A	FK	LCCC	20	1	506.98	12.06	2030	NA
UC1846L883B	FK	LCCC	20	1	506.98	12.06	2030	NA
UC2846DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2846DWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC2846N	N	PDIP	16	25	506	13.97	11230	4.32
UC2846NG4	N	PDIP	16	25	506	13.97	11230	4.32
UC3846DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3846N	N	PDIP	16	25	506	13.97	11230	4.32
UC3846NG4	N	PDIP	16	25	506	13.97	11230	4.32
UC3847DW	DW	SOIC	16	40	507	12.83	5080	6.6

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