# ISO²-CMOS MT8870D/MT8870D-1
## Integrated DTMF Receiver

ISSUE 3 May1995

### Features
- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

### Applications
- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

**Ordering Information**

| | |
|---|---|
| MT8870DE/DE-1 | 18 Pin Plastic DIP |
| MT8870DC/DC-1 | 18 Pin Ceramic DIP |
| MT8870DS/DS-1 | 18 Pin SOIC |
| MT8870DN/DN-1 | 20 Pin SSOP |
| MT8870DT/DT-1 | 20 Pin TSSOP |

**-40 °C to +85 °C**

### Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

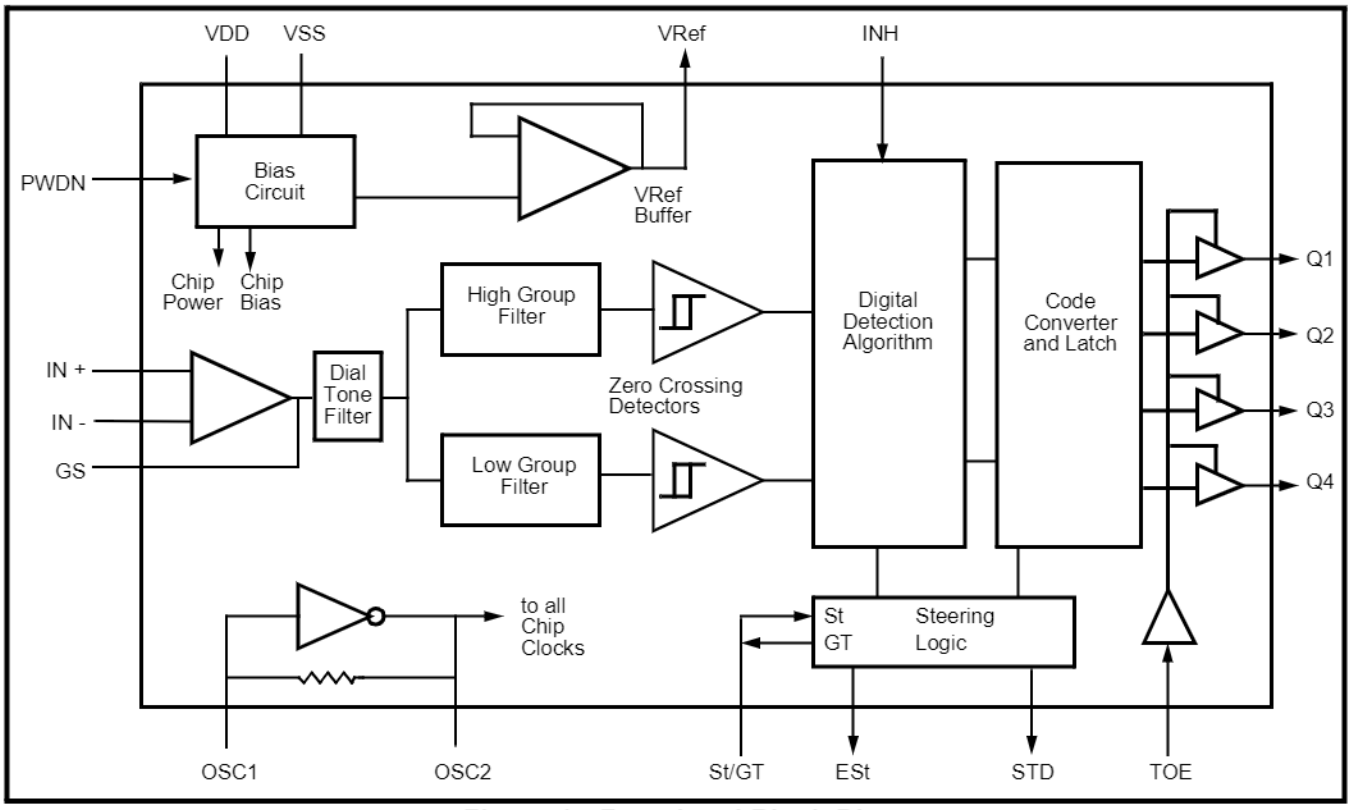



**Figure 1 - Functional Block Diagram**

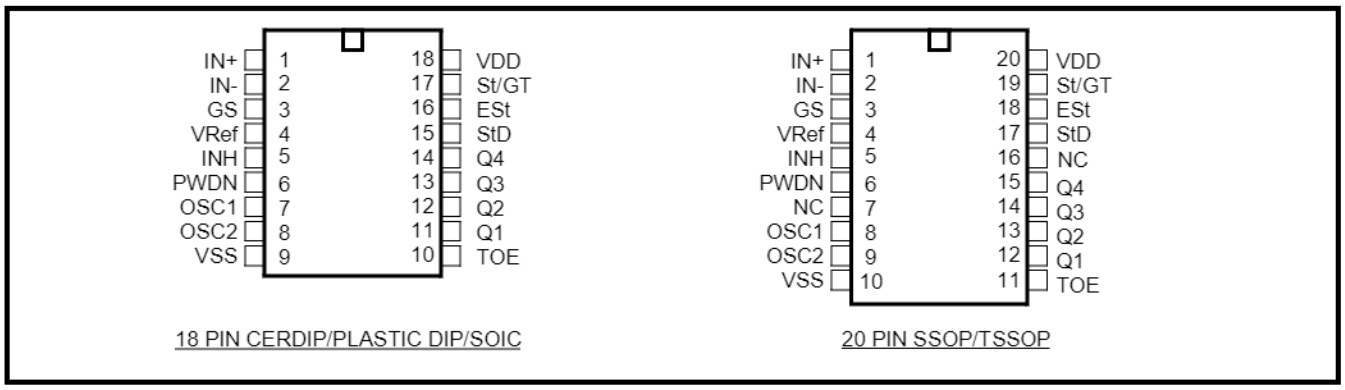



**Figure 2 - Pin Connections**

## Pin Description

| Pin # | | Name | Description |
|---|---|---|---|
| 18 | 20 | | |
| 1 | 1 | IN+ | **Non-Inverting Op-Amp (Input)**. |
| 2 | 2 | IN- | **Inverting Op-Amp (Input)**. |
| 3 | 3 | GS | **Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor. |
| 4 | 4 | $V_{Ref}$ | **Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10). |
| 5 | 5 | INH | **Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down. |
| 6 | 6 | PWDN | **Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down. |
| 7 | 8 | OSC1 | **Clock (Input)**. |
| 8 | 9 | OSC2 | **Clock (Output)**. A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit. |
| 9 | 10 | $V_{SS}$ | **Ground (Input)**. 0V typical. |
| 10 | 11 | TOE | **Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally. |
| 11-14 | 12-15 | Q1-Q4 | **Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance. |
| 15 | 17 | StD | **Delayed Steering (Output).**Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below $V_{TSt}$. |
| 16 | 18 | ESt | **Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low. |
| 17 | 19 | St/GT | **Steering Input/Guard time (Output) Bidirectional.** A voltage greater than $V_{TSt}$ detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than $V_{TSt}$ frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St. |
| 18 | 20 | $V_{DD}$ | **Positive power supply (Input)**. +5V typical. |
| | 7, 16 | NC | No Connection. |

## Functional Description

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

### Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

### Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while

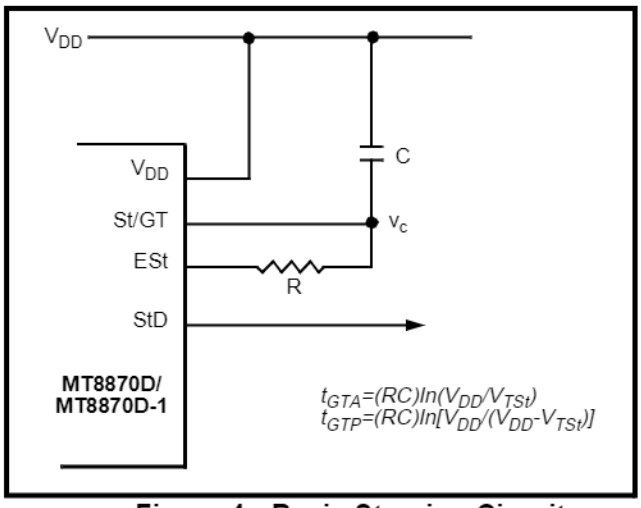



**Figure 4 - Basic Steering Circuit**

providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

### Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes $v_c$ (see Figure 4) to rise as the capacitor discharges. Provided signal

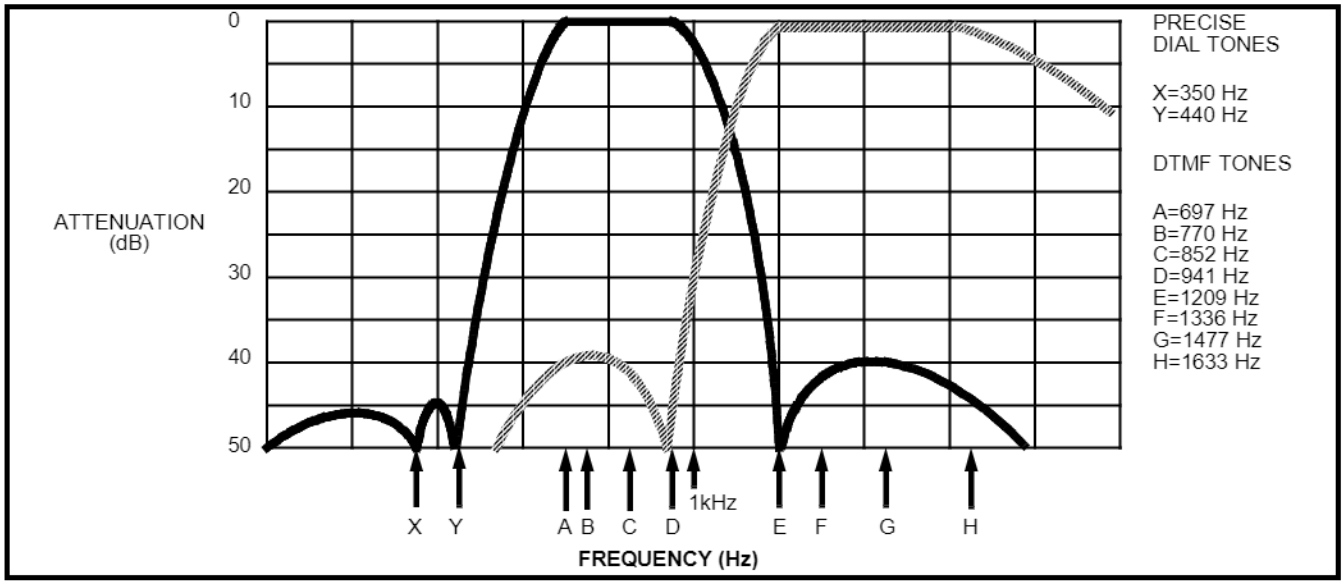



**Figure 3 - Filter Response**

condition is maintained (ESt remains high) for the validation period ($t_{GTP}$), $v_c$ reaches the threshold ($V_{TSt}$) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives $v_c$ to $V_{DD}$. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

### Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 4 is applicable. Component values are chosen according to the formula:

$$t_{REC}=t_{DP}+t_{GTP}$$
$$t_{ID}=t_{DA}+t_{GTA}$$

The value of $t_{DP}$ is a device parameter (see Figure 11) and $t_{REC}$ is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer.

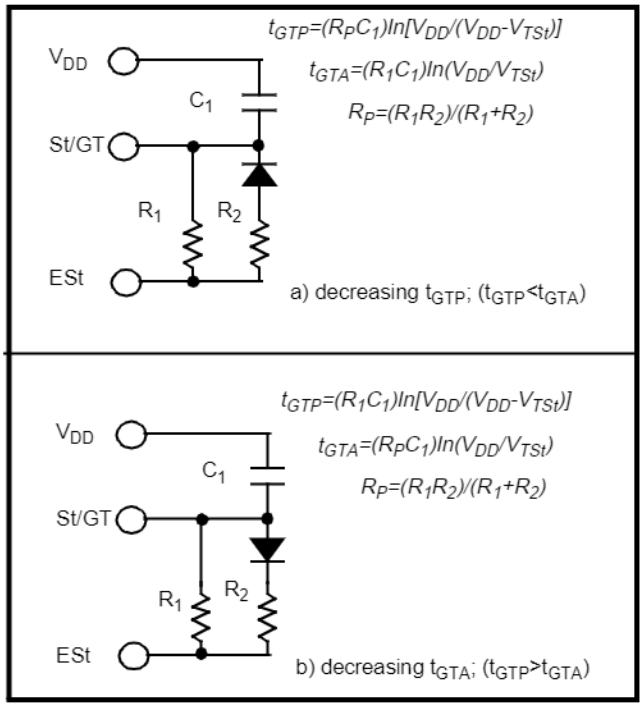



**Figure 5 - Guard Time Adjustment**

| Digit | TOE | INH | ESt | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ |
|---|---|---|---|---|---|---|---|
| ANY | L | X | H | Z | Z | Z | Z |
| 1 | H | X | H | 0 | 0 | 0 | 1 |
| 2 | H | X | H | 0 | 0 | 1 | 0 |
| 3 | H | X | H | 0 | 0 | 1 | 1 |
| 4 | H | X | H | 0 | 1 | 0 | 0 |
| 5 | H | X | H | 0 | 1 | 0 | 1 |
| 6 | H | X | H | 0 | 1 | 1 | 0 |
| 7 | H | X | H | 0 | 1 | 1 | 1 |
| 8 | H | X | H | 1 | 0 | 0 | 0 |
| 9 | H | X | H | 1 | 0 | 0 | 1 |
| 0 | H | X | H | 1 | 0 | 1 | 0 |
| * | H | X | H | 1 | 0 | 1 | 1 |
| # | H | X | H | 1 | 1 | 0 | 0 |
| A | H | L | H | 1 | 1 | 0 | 1 |
| B | H | L | H | 1 | 1 | 1 | 0 |
| C | H | L | H | 1 | 1 | 1 | 1 |
| D | H | L | H | 0 | 0 | 0 | 0 |
| A | H | H | L | undetected, the output code will remain the same as the previous detected code | | | |
| B | H | H | L | | | | |
| C | H | H | L | | | | |
| D | H | H | L | | | | |

**Table 1. Functional Decode Table**

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

Different steering arrangements may be used to select independently the guard times for tone present ($t_{GTP}$) and tone absent ($t_{GTA}$). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing $t_{REC}$ improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short $t_{REC}$ with a long $t_{DO}$ would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

### Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

### Differential Input Configuration

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a bias source ($V_{Ref}$) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and $V_{Ref}$ biasing the input at $^1/_2V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor $R_5$.

### Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several MT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

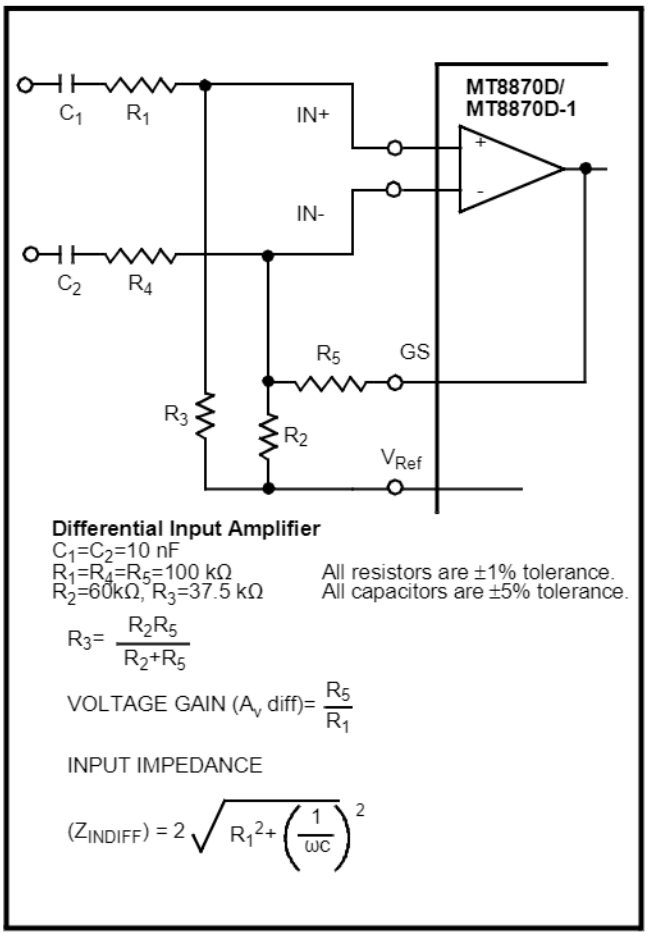



**Figure 6 - Differential Input Configuration**

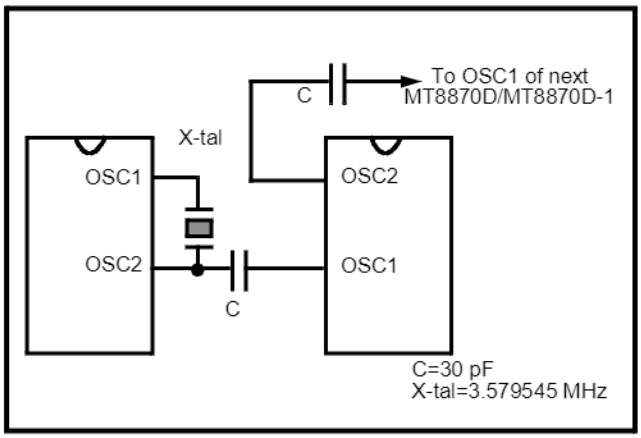



**Figure 7 - Oscillator Connection**

| Parameter | Unit | Resonator |
|---|---|---|
| R1 | Ohms | 10.752 |
| L1 | mH | .432 |
| C1 | pF | 4.984 |
| C0 | pF | 37.915 |
| Qm | - | 896.37 |
| Δf | % | ±0.2% |

**Table 2. Recommended Resonator Specifications**

Note: Qm=quality factor of RLC model, i.e., 1/2Π*f*R1C1.

## Applications

### RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 9 illustrates the use of MT8870D-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of $R_1$ and $R_2$ to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870D-1. As shown in the diagram, the component values of $R_3$ and $C_2$ are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 8.

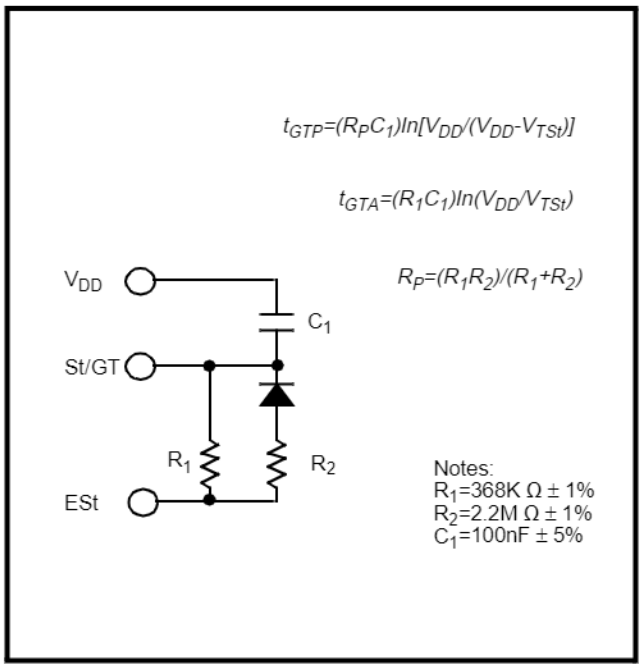



**Figure 8 - Non-Symmetric Guard Time Circuit**

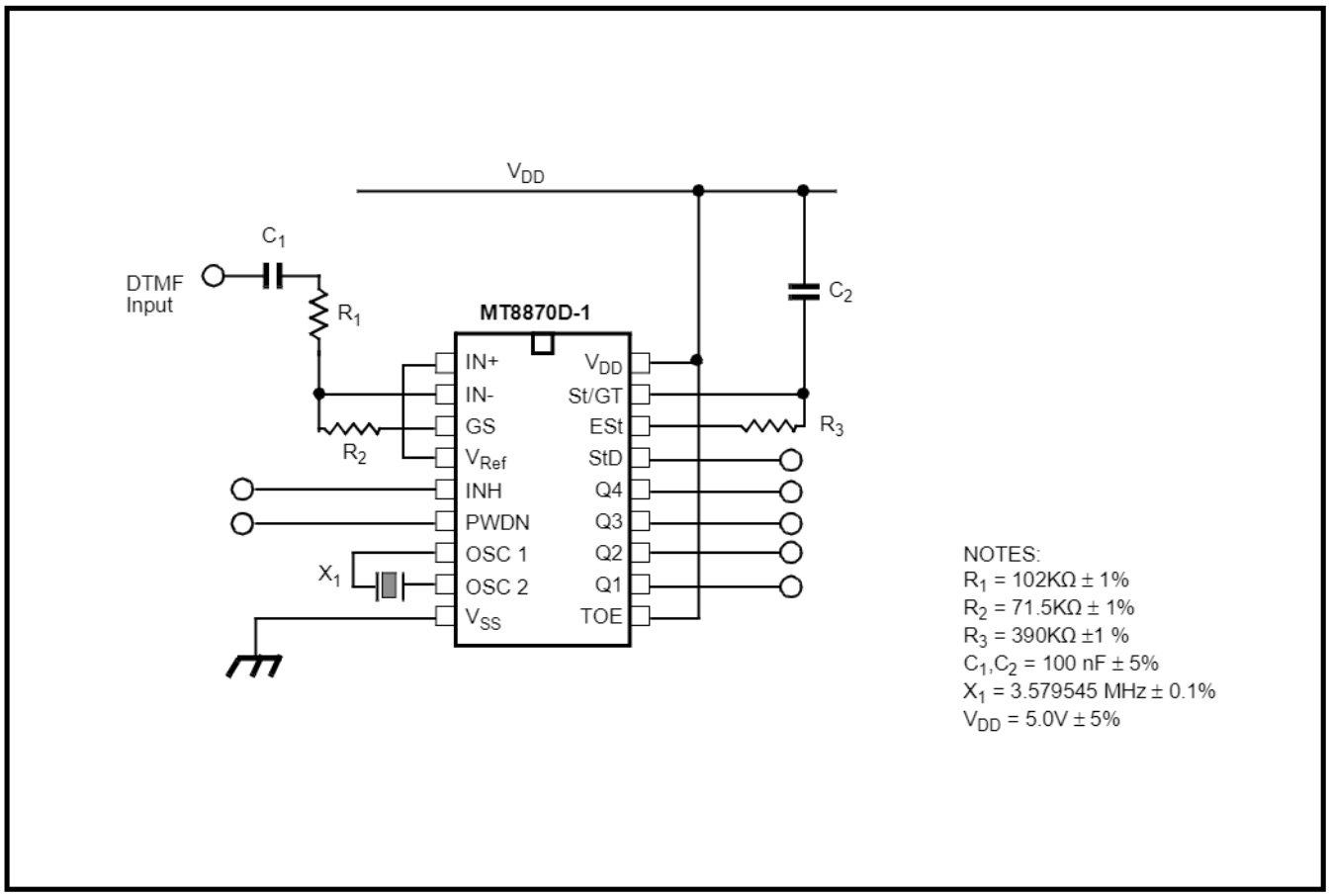



**Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec**

## Absolute Maximum Ratings†

| | Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| 1 | DC Power Supply Voltage | $V_{DD}$ | | 7 | V |
| 2 | Voltage on any pin | $V_I$ | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| 3 | Current at any pin (other than supply) | $I_I$ | | 10 | mA |
| 4 | Storage temperature | $T_{STG}$ | -65 | +150 | °C |
| 5 | Package power dissipation | $P_D$ | | 500 | mW |

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C. All leads soldered to board.

## Recommended Operating Conditions - Voltages are with respect to ground ($V_{SS}$) unless otherwise stated.

| | Parameter | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | DC Power Supply Voltage | $V_{DD}$ | 4.75 | 5.0 | 5.25 | V | |
| 2 | Operating Temperature | $T_O$ | -40 | | +85 | °C | |
| 3 | Crystal/Clock Frequency | fc | | 3.579545 | | MHz | |
| 4 | Crystal/Clock Freq.Tolerance | Δfc | | ±0.1 | | % | |

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

## DC Electrical Characteristics - $V_{DD}$=5.0V± 5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C, unless otherwise stated.

| | | Characteristics | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| 1 | SUPPLY | Standby supply current | $I_{DDQ}$ | | 10 | 25 | μA | PWDN=$V_{DD}$ |
| 2 | | Operating supply current | $I_{DD}$ | | 3.0 | 9.0 | mA | |
| 3 | | Power consumption | $P_O$ | | 15 | | mW | fc=3.579545 MHz |
| 4 | INPUTS | High level input | $V_{IH}$ | 3.5 | | | V | $V_{DD}$=5.0V |
| 5 | | Low level input voltage | $V_{IL}$ | | | 1.5 | V | $V_{DD}$=5.0V |
| 6 | | Input leakage current | $I_{IH}/I_{IL}$ | | 0.1 | | μA | $V_{IN}$=$V_{SS}$ or $V_{DD}$ |
| 7 | | Pull up (source) current | $I_{SO}$ | | 7.5 | 20 | μA | TOE (pin 10)=0, $V_{DD}$=5.0V |
| 8 | | Pull down (sink) current | $I_{SI}$ | | 15 | 45 | μA | INH=5.0V, PWDN=5.0V, $V_{DD}$=5.0V |
| 9 | | Input impedance (IN+, IN-) | $R_{IN}$ | | 10 | | MΩ | @ 1 kHz |
| 10 | | Steering threshold voltage | $V_{TSt}$ | 2.2 | 2.4 | 2.5 | V | $V_{DD}$ = 5.0V |
| 11 | OUTPUTS | Low level output voltage | $V_{OL}$ | | | $V_{SS}$+0.03 | V | No load |
| 12 | | High level output voltage | $V_{OH}$ | $V_{DD}$-0.03 | | | V | No load |
| 13 | | Output low (sink) current | $I_{OL}$ | 1.0 | 2.5 | | mA | $V_{OUT}$=0.4 V |
| 14 | | Output high (source) current | $I_{OH}$ | 0.4 | 0.8 | | mA | $V_{OUT}$=4.6 V |
| 15 | | $V_{Ref}$ output voltage | $V_{Ref}$ | 2.3 | 2.5 | 2.7 | V | No load, $V_{DD}$ = 5.0V |
| 16 | | $V_{Ref}$ output resistance | $R_{OR}$ | | 1 | | kΩ | |

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

## Operating Characteristics - $V_{DD}$=5.0V±5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C ,unless otherwise stated.

**Gain Setting Amplifier**

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Input leakage current | $I_{IN}$ | | | 100 | nA | $V_{SS} \le V_{IN} \le V_{DD}$ |
| 2 | Input resistance | $R_{IN}$ | 10 | | | MΩ | |
| 3 | Input offset voltage | $V_{OS}$ | | | 25 | mV | |
| 4 | Power supply rejection | PSRR | 50 | | | dB | 1 kHz |
| 5 | Common mode rejection | CMRR | 40 | | | dB | 0.75 V ≤ $V_{IN}$ ≤ 4.25 V biased at $V_{Ref}$ =2.5 V |
| 6 | DC open loop voltage gain | $A_{VOL}$ | 32 | | | dB | |
| 7 | Unity gain bandwidth | $f_C$ | 0.30 | | | MHz | |
| 8 | Output voltage swing | $V_O$ | 4.0 | | | $V_{pp}$ | Load ≥ 100 kΩ to $V_{SS}$ @ GS |
| 9 | Maximum capacitive load (GS) | $C_L$ | | | 100 | pF | |
| 10 | Resistive load (GS) | $R_L$ | | | 50 | kΩ | |
| 11 | Common mode range | $V_{CM}$ | 2.5 | | | $V_{pp}$ | No Load |

## MT8870D AC Electrical Characteristics - $V_{DD}$=5.0V ±5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C , using Test Circuit shown in Figure 10.

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Notes* |
|---|---|---|---|---|---|---|---|
| 1 | Valid input signal levels (each tone of composite signal) | | -29 | | +1 | dBm | 1,2,3,5,6,9 |
| | | | 27.5 | | 869 | $mV_{RMS}$ | 1,2,3,5,6,9 |
| 2 | Negative twist accept | | | | 8 | dB | 2,3,6,9,12 |
| 3 | Positive twist accept | | | | 8 | dB | 2,3,6,9,12 |
| 4 | Frequency deviation accept | | ±1.5% ± 2 Hz | | | | 2,3,5,9 |
| 5 | Frequency deviation reject | | ±3.5% | | | | 2,3,5,9 |
| 6 | Third tone tolerance | | | -16 | | dB | 2,3,4,5,9,10 |
| 7 | Noise tolerance | | | -12 | | dB | 2,3,4,5,7,9,10 |
| 8 | Dial tone tolerance | | | +22 | | dB | 2,3,4,5,8,9,11 |

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES**

1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz ) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

## MT8870D-1 AC Electrical Characteristics

- $V_{DD}$=5.0V±5%, $V_{SS}$=0V, -40°C ≤ $T_O$ ≤ +85°C , using Test Circuit shown in Figure 10.

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Notes* |
|---|---|---|---|---|---|---|---|
| 1 | Valid input signal levels (each tone of composite signal) | | -31 | | +1 | dBm | Tested at $V_{DD}$=5.0V 1,2,3,5,6,9 |
| | | | 21.8 | | 869 | $mV_{RMS}$ | |
| 2 | Input Signal Level Reject | | -37 | | | dBm | Tested at $V_{DD}$=5.0V 1,2,3,5,6,9 |
| | | | 10.9 | | | $mV_{RMS}$ | |
| 3 | Negative twist accept | | | | 8 | dB | 2,3,6,9,13 |
| 4 | Positive twist accept | | | | 8 | dB | 2,3,6,9,13 |
| 5 | Frequency deviation accept | | ±1.5%± 2 Hz | | | | 2,3,5,9 |
| 6 | Frequency deviation reject | | ±3.5% | | | | 2,3,5,9 |
| 7 | Third zone tolerance | | | -18.5 | | dB | 2,3,4,5,9,12 |
| 8 | Noise tolerance | | | -12 | | dB | 2,3,4,5,7,9,10 |
| 9 | Dial tone tolerance | | | +22 | | dB | 2,3,4,5,8,9,11 |

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES**

1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz ) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
13. Guaranteed by design and characterization.

## AC Electrical Characteristics - $V_{DD}$=5.0V±5%, $V_{SS}$=0V, -40°C ≤ To ≤ +85°C , using Test Circuit shown in Figure 10.

| | | Characteristics | Sym | Min | Typ‡ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 1 | TIMING | Tone present detect time | $t_{DP}$ | 5 | 11 | 14 | ms | Note 1 |
| 2 | | Tone absent detect time | $t_{DA}$ | 0.5 | 4 | 8.5 | ms | Note 1 |
| 3 | | Tone duration accept | $t_{REC}$ | | | 40 | ms | Note 2 |
| 4 | | Tone duration reject | $t_{\overline{REC}}$ | 20 | | | ms | Note 2 |
| 5 | | Interdigit pause accept | $t_{ID}$ | | | 40 | ms | Note 2 |
| 6 | | Interdigit pause reject | $t_{DO}$ | 20 | | | ms | Note 2 |
| 7 | OUTPUTS | Propagation delay (St to Q) | $t_{PQ}$ | | 8 | 11 | µs | TOE=$V_{DD}$ |
| 8 | | Propagation delay (St to StD) | $t_{PStD}$ | | 12 | 16 | µs | TOE=$V_{DD}$ |
| 9 | | Output data set up (Q to StD) | $t_{QStD}$ | | 3.4 | | µs | TOE=$V_{DD}$ |
| 10 | | Propagation delay (TOE to Q ENABLE) | $t_{PTE}$ | | 50 | | ns | load of 10 kΩ, 50 pF |
| 11 | | Propagation delay (TOE to Q DISABLE) | $t_{PTD}$ | | 300 | | ns | load of 10 kΩ, 50 pF |
| 12 | PDWN | Power-up time | $t_{PU}$ | | 30 | | ms | Note 3 |
| 13 | | Power-down time | $t_{PD}$ | | 20 | | ms | |
| 14 | CLOCK | Crystal/clock frequency | $f_C$ | 3.5759 | 3.5795 | 3.5831 | MHz | |
| 15 | | Clock input rise time | $t_{LHCL}$ | | | 110 | ns | Ext. clock |
| 16 | | Clock input fall time | $t_{HLCL}$ | | | 110 | ns | Ext. clock |
| 17 | | Clock input duty cycle | $DC_{CL}$ | 40 | 50 | 60 | % | Ext. clock |
| 18 | | Capacitive load (OSC2) | $C_{LO}$ | | | 30 | pF | |

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES:**
1. Used for guard-time calculation purposes only.
2. These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
3. With valid tone present at input, $t_{PU}$ equals time from PDWN going low until ESt going high.

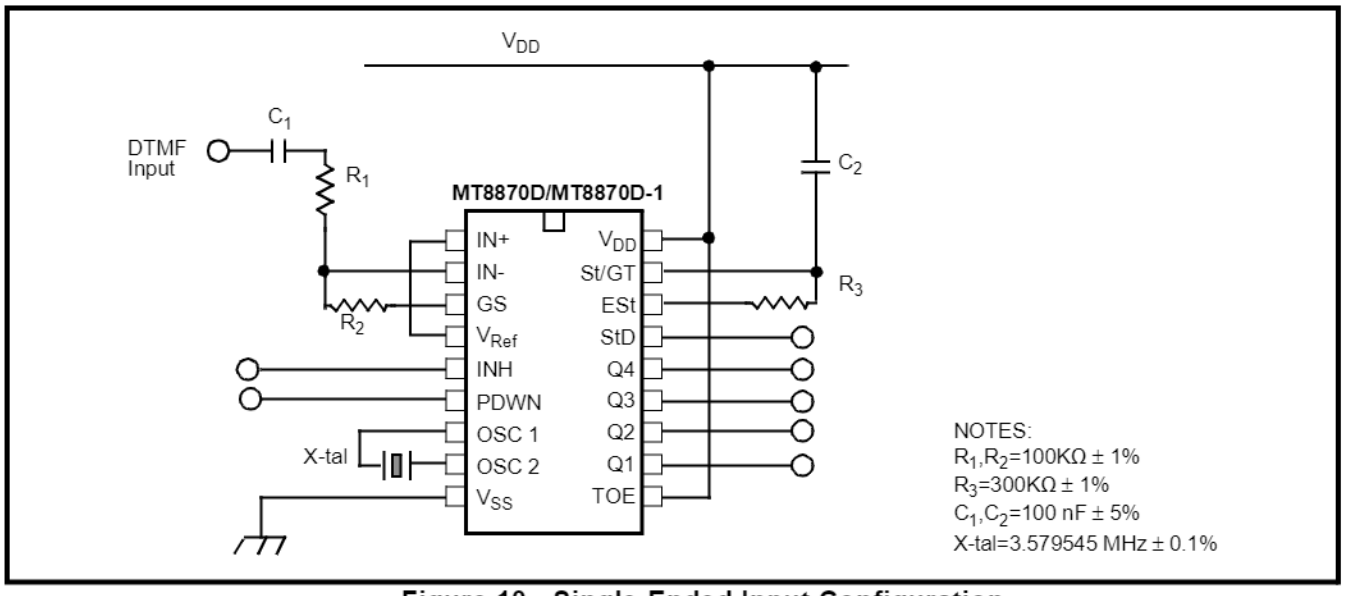
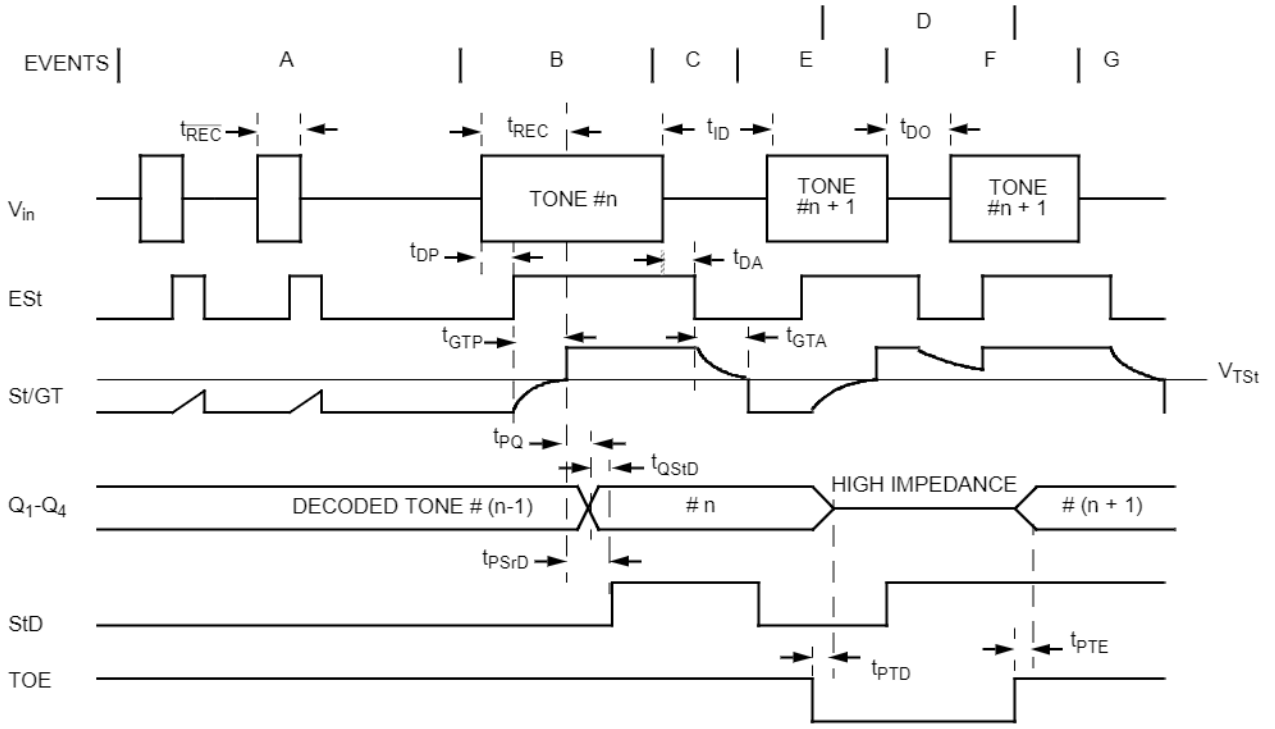



**Figure 10 - Single-Ended Input Configuration**




**EXPLANATION OF EVENTS**

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMIAN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

**EXPLANATION OF SYMBOLS**

$V_{in}$ DTMF COMPOSITE INPUT SIGNAL.

ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.

St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.

$Q_1$-$Q_4$ 4-BIT DECODED TONE OUTPUT.

StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.

TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS $Q_1$-$Q_4$ TO ITS HIGH IMPEDANCE STATE.

$t_{\overline{REC}}$ MAXIMUM DTMF SIGNAL DURATION NOT DETECED AS VALID

$t_{REC}$ MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION

$t_{ID}$ MAXIMUM TIME BETWEEN VALID DTMF SIGNALS.

$t_{DO}$ MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.

$t_{DP}$ TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.

$t_{DA}$ TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.

$t_{GTP}$ GUARD TIME, TONE PRESENT.

$t_{GTA}$ GUARD TIME, TONE ABSENT.

**Figure 11 - Timing Diagram**

**NOTES:**