FSD210, FSD200

Green Mode Fairchild Power Switch (FPS™)

Features

- Single Chip 700V Sense FET Power Switch
- Precision Fixed Operating Frequency (134kHz)
- Advanced Burst-Mode operation Consumes under 0.1W at 265Vac and no load (FSD210 only)
- Internal Start-up Switch and Soft Start
- Under Voltage Lock Out (UVLO) with Hysteresis
- Pulse by Pulse Current Limit
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Frequency Modulation for EMI
- FSD200 does not require an auxiliary bias winding

Applications

- Charger & Adaptor for Mobile Phone, PDA & MP3
- Auxiliary Power for White Goods, PC, C-TV & Monitor

Description

The FSD200 and FSD210 are integrated Pulse Width Modulators (PWM) and Sense FETs specially designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. Both devices are monolithic high voltage power switching regulators which combine an LDMOS Sense FET with a voltage mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), optimized gate turn-on/turn-off driver, thermal shut down protection (TSD), temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSD200 and FSD210 reduce total component count, design size, weight and at the same time increase efficiency, productivity, and system reliability. The FSD200 eliminates the need for an auxiliary bias winding at a small cost of increased supply power. Both devices are a basic platform well suited for cost effective designs of flyback converters.

OUTPUT POWER TABLE				
PRODUCT	230VAC ±15%(3)		85-265VAC	
	Adapter(1)	Open Frame(2)	Adapter(1)	Open Frame(2)
FSD210	5W	7W	4W	5W
FSD200	5W	7W	4W	5W
FSD210M	5W	7W	4W	5W
FSD200M	5W	7W	4W	5W

Table 1. Notes: 1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient. 2. Maximum practical continuous power in an open frame design at 50°C ambient. 3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

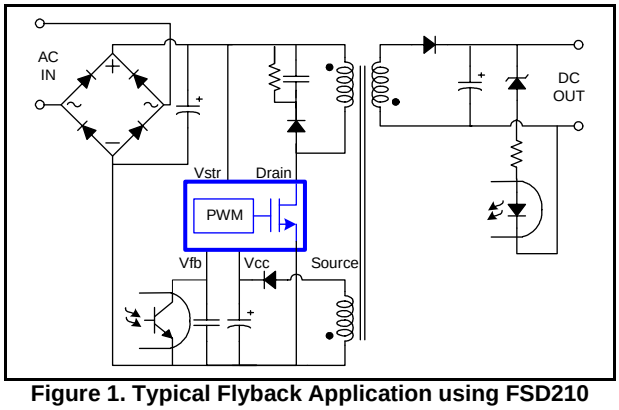


Figure 1. Typical Flyback Application using FSD210

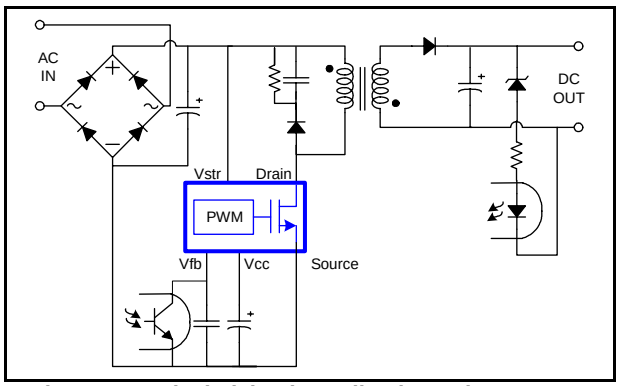


Figure 2. Typical Flyback Application using FSD200

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Internal Block Diagram

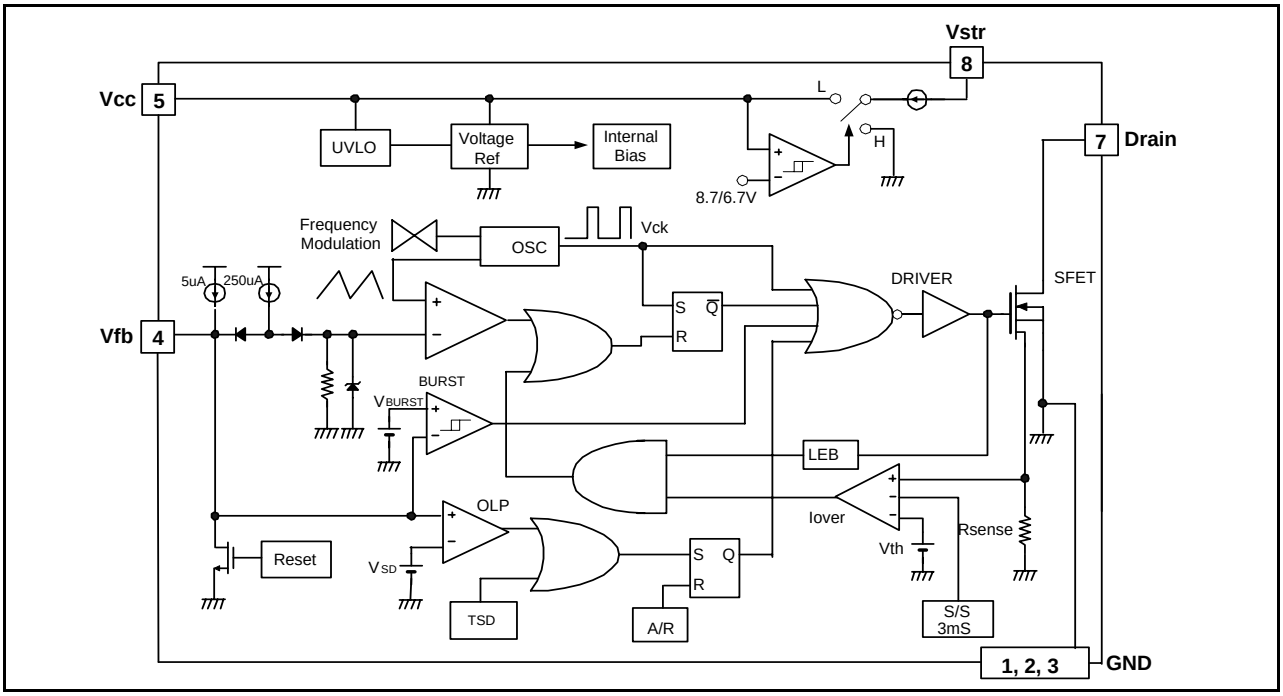


Figure 3. Functional Block Diagram of FSD210

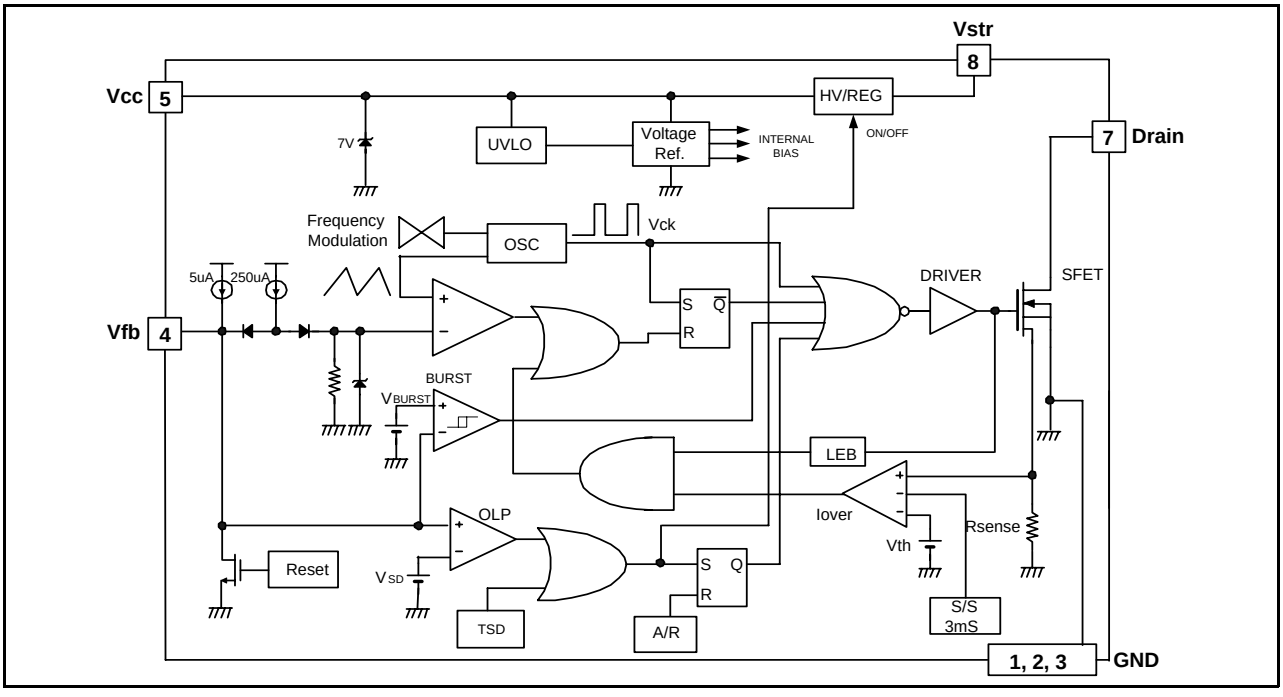


Figure 4. Functional Block Diagram of FSD200 showing internal high voltage regulator

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1, 2, 3	GND	Sense FET source terminal on primary side and internal control ground.
4	Vfb	The feedback voltage pin is the inverting input to the PWM comparator with nominal input levels between 0.5Vand 2.5V. It has a 0.25mA current source connected internally while a capacitor and opto coupler are typically connected externally. A feedback voltage of 4V triggers overload protection (OLP). There is a time delay while charging between 3V and 4V using an internal 5uA current source, which prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
5	Vcc	**FSD210** Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 8 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (8.7V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding. **FSD200** This pin is connected to a storage capacitor. A high voltage regulator connected between pin 8 (Vstr) and this pin, provides the supply voltage to the FSD200 at startup and when switching during normal operation. The FSD200 eliminates the need for auxiliary bias winding and associated external components.
7	Drain	The Drain pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 700V. Minimizing the length of the trace connecting this pin to the transformer will decrease leakage inductance.
8	Vstr	The startup pin connects directly to the rectified AC line voltage source for both the FSD200 and FSD210. For the FSD210, at start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once this reaches 8.7V, the internal current source is disabled. For the FSD200, an internal high voltage regulator provides a constant supply voltage.

Pin Configuration

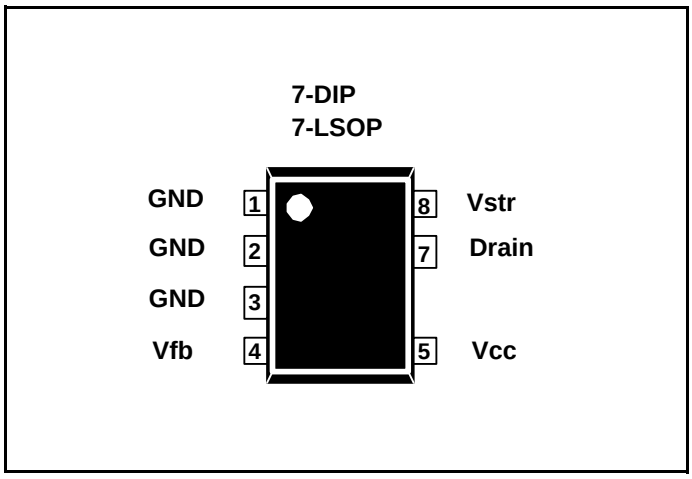


Figure 5. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage (FSD200)	$V_{CC,MAX}$	10	V
Maximum Supply Voltage (FSD210)	$V_{CC,MAX}$	20	V
Input Voltage Range	V_{FB}	–0.3 to V_{STOP}	V
Operating Junction Temperature.	T_J	+150	°C
Operating Ambient Temperature	T_A	–25 to +85	°C
Storage Temperature Range	T_{STG}	–55 to +150	°C

Thermal Impedance

Parameter	Symbol	Value	Unit
7DIP			
Junction-to-Ambient Thermal	θ_{JA}(1)	74.07(3)	°C/W
	θ_{JA}(1)	60.44(4)	°C/W
Junction-to-Case Thermal	θ_{JC}(2)	22.00	°C/W
7LSOP			
Junction-to-Ambient Thermal	θ_{JA}(1)	-	°C/W
	θ_{JA}(1)	-	°C/W
Junction-to-Case Thermal	θ_{JC}(2)	-	°C/W

Note:

1. Free standing without heat sink.
2. Measured on the GND pin close to plastic interface.
3. Soldered to 100mm^2 copper clad.
4. Soldered to 300mm^2 copper clad.

Electrical Characteristics

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{CC} = 0V, I_D = 100μA	700	-	-	V
Startup Voltage (Vstr) Breakdown	BV_{STR}		700	-	-	V
Off-State Current	I_{DSS}	V_{DS} = 560V	-	-	100	μA
On-State Resistance	$R_{DS(ON)}$	Tj = 25°C, I_D = 25mA	-	28	32	Ω
		Tj = 100°C, I_D = 25mA	-	42	48	Ω
Rise Time	T_R	V_{DS} = 325V, I_D = 50mA	-	100	-	ns
Fall Time	T_F	V_{DS} = 325V, I_D = 25mA	-	50	-	ns
CONTROL SECTION						
Output Frequency	F_{OSC}	Tj = 25°C	126	134	142	kHz
Output Frequency Modulation	F_{MOD}	Tj = 25°C	-	±4	-	kHz
Feedback Source Current	I_{FB}	Vfb = 0V	0.22	0.25	0.28	mA
Maximum Duty Cycle	D_{MAX}	Vfb = 3.5V	60	65	70	%
Minimum Duty Cycle	D_{MIN}	Vfb = 0V	0	0	0	%
UVLO Threshold Voltage (FSD200)	V_{START}		6.3	7	7.7	V
	V_{STOP}	After turn on	5.3	6	6.7	V
UVLO Threshold Voltage (FSD210)	V_{START}		8.0	8.7	9.4	V
	V_{STOP}	After turn on	6.0	6.7	7.4	V
Supply Shunt Regulator (FSD200)	V_{CCREG}	-	-	7	-	V
Internal Soft Start Time	$T_{S/S}$		-	3	-	ms
BURST MODE SECTION						
Burst Mode Voltage	V_{BURH}	Tj = 25°C	0.58	0.64	0.7	V
	V_{BURL}		0.5	0.58	0.64	V
	Hysteresis		-	60	-	mV
PROTECTION SECTION						
Drain to Source Peak Current Limit	I_{OVER}		0.275	0.320	0.365	A
Current Limit Delay(1)	T_{CLD}	Tj = 25°C	-	220	-	ns
Thermal Shutdown Temperature (Tj)(1)	T_{SD}		125	145	160	°C
Shutdown Feedback Voltage	V_{SD}	-	3.5	4.0	4.5	V
Feedback Shutdown Delay Current	I_{DELAY}	Vfb = 4.0V	3	5	7	μA
Leading Edge Blanking Time(2)	T_{LEB}		200	-	-	ns
TOTAL DEVICE SECTION						
Operating Supply Current (FSD200)	I_{OP}	Vcc = 7V	-	600	-	μA
Operating Supply Current (FSD210)	I_{OP}	Vcc = 11V	-	700	-	μA
Start Up Current (FSD200)	I_{START}	Vcc = 0V	-	1	1.2	mA
Start Up Current (FSD210)	I_{START}	Vcc = 0V	-	700	900	μA
Vstr Supply Voltage		Vcc = 0V	20	-	-	V

Note:

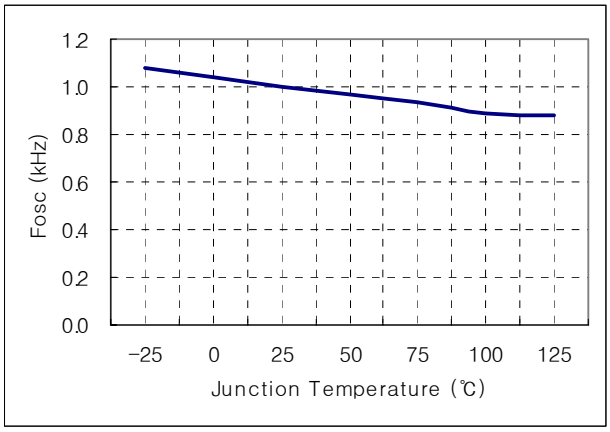
1. These parameters, although guaranteed, are not 100% tested in production
2. This parameter is derived from characterization

Comparison Between FSDH565 and FSD210

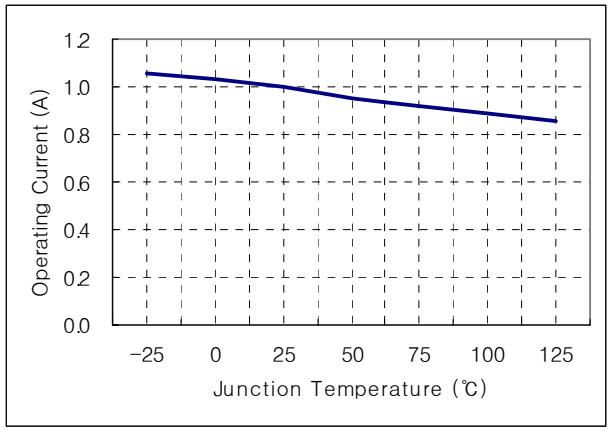
Function	FSDH0565	FSD210	FSD210 Advantages
Soft-Start	not applicable	3mS	• Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Switching Frequency	100kHz	134kHz	• Smaller transformer
Frequency Modulation	not applicable	±4kHz	• Reduced conducted EMI
Burst Mode Operation	not applicable	Yes-built into controller	• Improve light load efficiency • Reduces no-load consumption • Transformer audible noise reduction
Drain Creepage at Package	1.02mm	3.56mm DIP 3.56mm LSOP	• Greater immunity to acting as a result of build-up of dust, debris and other contaminants

Typical Performance Characteristics

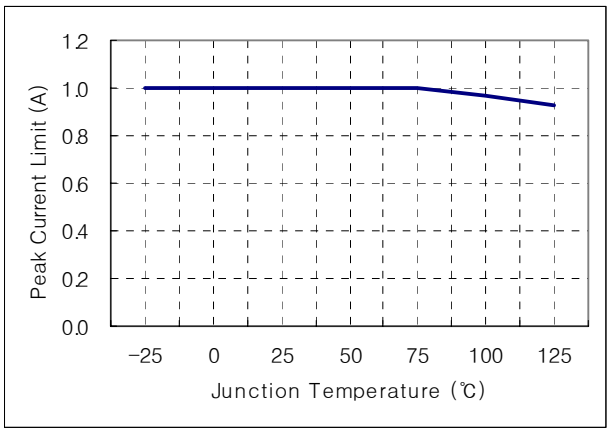
(These characteristic graphs are normalized at Ta=25℃)



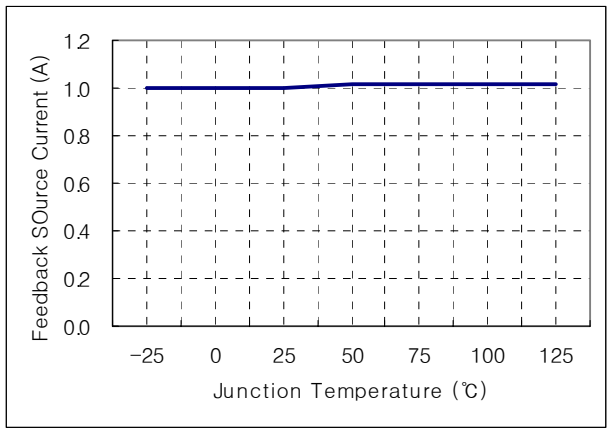
Frequency vs. Temp



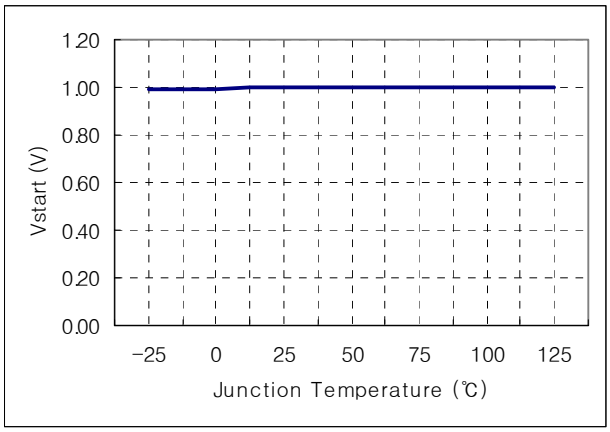
Operating Current vs. Temp



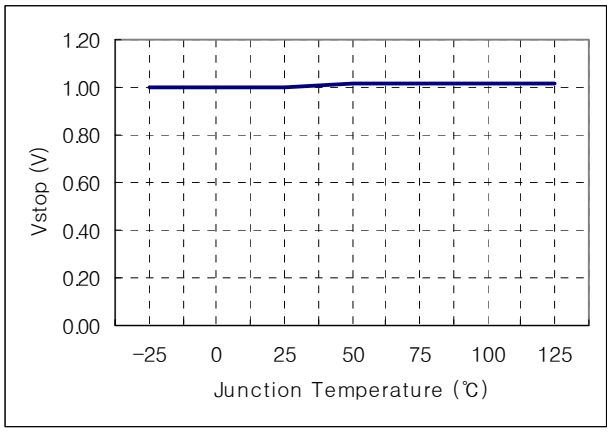
Peak Current Limit vs. Temp



Feedback Source Current vs. Temp



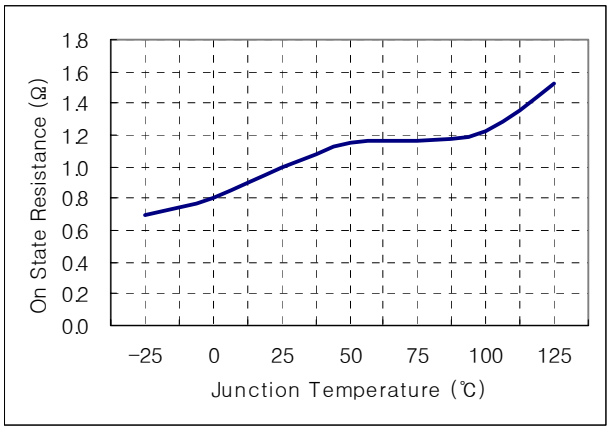
Vstart Voltage vs. Temp



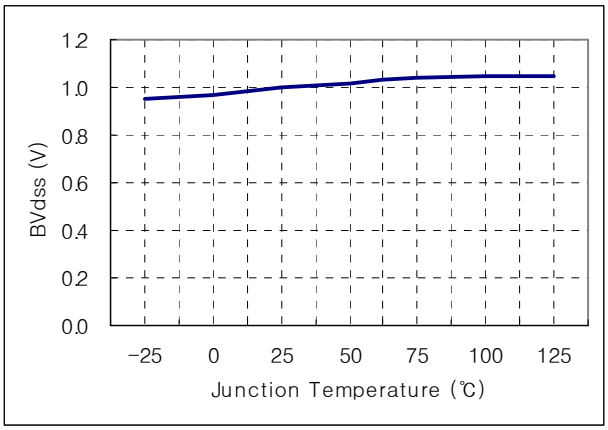
Vstop Voltage vs. Temp

Typical Performance Characteristics (Continued)

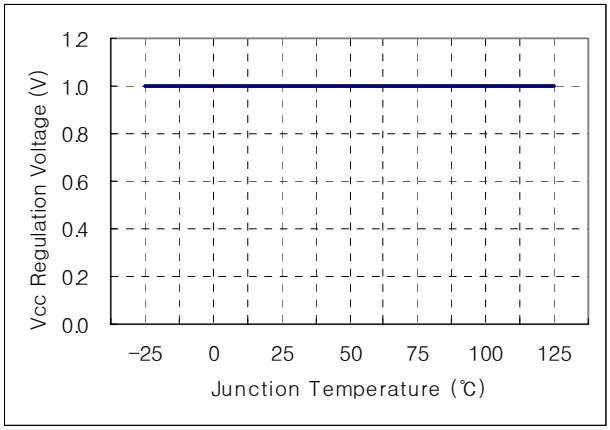
(These characteristic graphs are normalized at Ta=25℃)



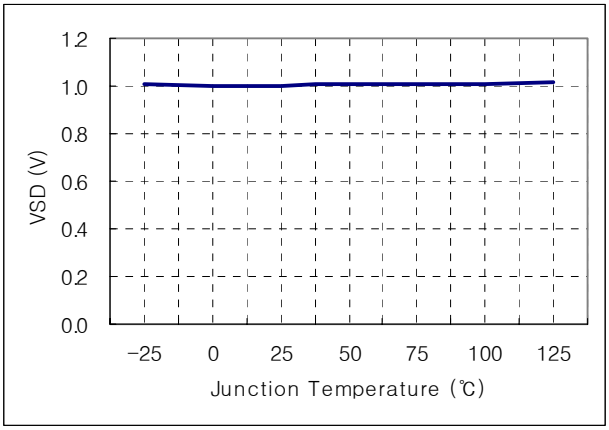
On State Resistance vs. Temp



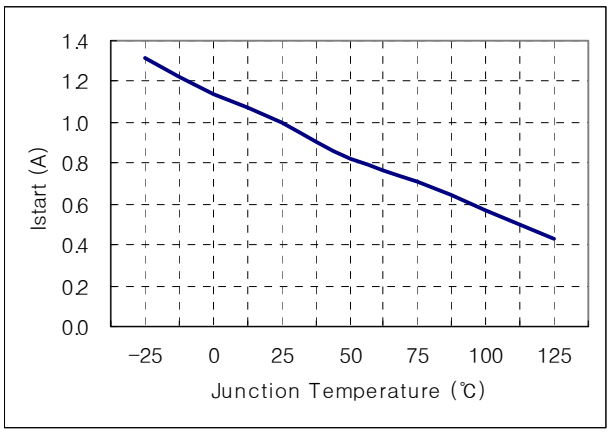
Breakdown Voltage vs. Temp



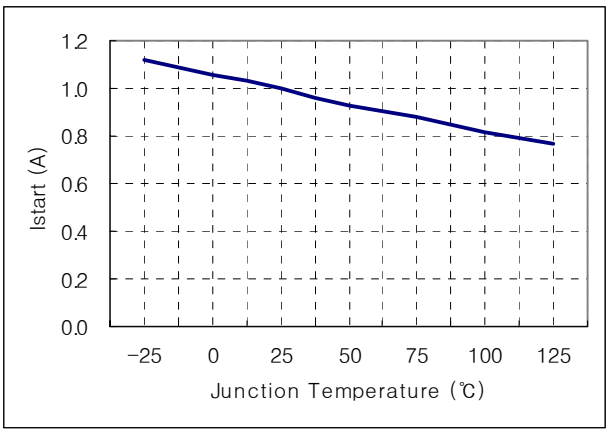
Vcc Regulation Voltage vs. Temp (for FSD200)



Shutdown Feedback Voltage vs. Temp



Start Up Current vs. Temp (for FSD210)



Start Up Current vs. Temp (for FSD200)

Functional Description

1. Startup : At startup, the internal high voltage current source supplies the internal bias and charges the external Vcc capacitor as shown in figure 7. In the case of the FSD210, when Vcc reaches 8.7V the device starts switching and the internal high voltage current source is disabled (see figure 1). The device continues to switch provided that Vcc does not drop below 6.7V. For FSD210, after startup, the bias is supplied from the auxiliary transformer winding. In the case of FSD200, Vcc is continuously supplied from the external high voltage source and Vcc is regulated to 7V by an internal high voltage regulator (HVReg), thus eliminating the need for an auxiliary winding (see figure 2).

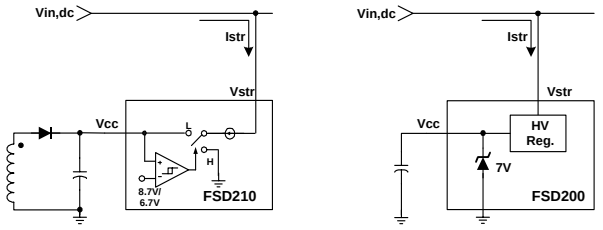


Figure 6. Internal startup circuit

Calculating the Vcc capacitor is an important step to designing in the FSD200/210. At initial start-up in both the FSD200/210, the stand-by maximum current is 100uA, supplying current to UVLO and Vref Block. The charging current (i) of the Vcc capacitor is equal to Istr - 100uA. After Vcc reaches the UVLO start voltage only the bias winding supplies Vcc current to device. When the bias winding voltage is not sufficient, the Vcc level decreases to the UVLO stop voltage. At this time Vcc oscillates. In order to prevent this ripple it is recommended that the Vcc capacitor be sized between 10uF and 47uF.

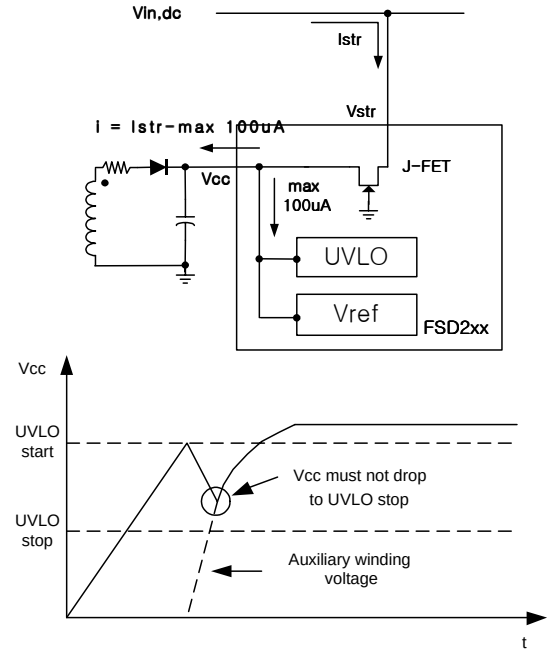


Figure 7. Charging the Vcc capacitor through Vstr

2. Feedback Control : The FSD200/210 are both voltage mode devices as shown in Figure 8. Usually, a H11A817 optocoupler and KA431 voltage reference (or a FOD2741 integrated optocoupler and voltage reference) are used to implement the isolated secondary feedback network. The feedback voltage is compared with an internally generated sawtooth waveform, directly controlling the duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the optocoupler LED current increases pulling down the feedback voltage and reducing the duty cycle. This event will occur when either the input voltage increases or the output load decreases.

3. Leading edge blanking (LEB) : At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by the primary side capacitance and secondary side rectifier diode reverse recovery. Exceeding the pulse-by-pulse current limit could cause premature termination of the switching pulse (see Protection Section). To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the over current comparator for a short time (TLEB) after the Sense FET is turned on.

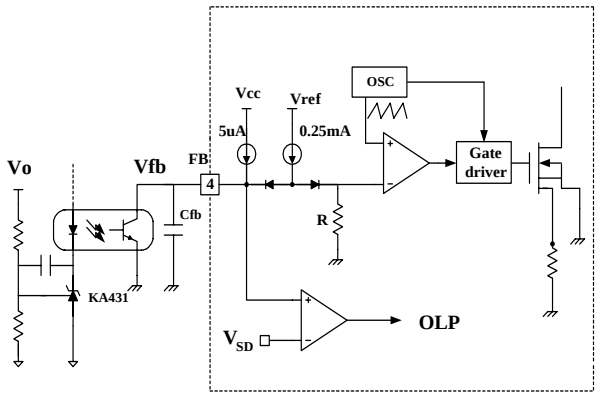


Figure 8. PWM and feedback circuit

4. Protection Circuit : The FSD200/210 has 2 self protection functions: over load protection (OLP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC with no external components, system

reliability is improved without a cost increase. If either of these thresholds are triggered, the FPS starts an auto-restart cycle. Once the fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage (6.7V:FSD210, 6V:FSD200), the protection is reset and the internal high voltage current source charges the Vcc capacitor. When Vcc reaches the UVLO start voltage (8.7V:FSD210,7V:FSD200), the device attempts to resume normal operation. If the fault condition is no longer present start up will be successful. If it is still present the cycle is repeated (see figure 10).

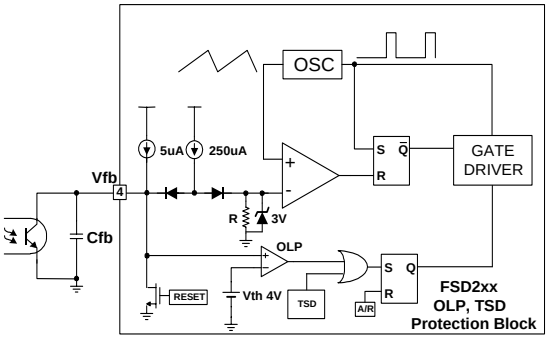


Figure 9. Protection block

4.1 Over Load Protection (OLP) : Over load protection occurs when the load current exceeds a pre-set level due to an abnormal situation. If this occurs, the protection circuit should be triggered to protect the SMPS. It is possible that a short term load transient can occur under normal operation. In order to avoid false shutdowns, the over load protection circuit is designed to trigger after a delay. Therefore the device can differentiate between transient over loads and true fault conditions. The maximum input power is limited using the pulse-by-pulse current limit feature. If the load tries to

draw more than this, the output voltage will drop below its set value. This reduces the optocoupler LED current which in turn reduces the photo-transistor current (see figure 9). Therefore, the 250uA current source will charge the feedback pin capacitor, Cfb, and the feedback voltage, Vfb, will increase. The input to the feedback comparator is clamped at 3V. Once Vfb reaches 3V, the device switches at maximum power, the 250uA current source is blocked and the 5uA source continues to charge Cfb. Once Vfb reaches 4V, switching stops.and overload protection is triggered. The resultant shutdown delay time is set by the time required to charge Cfb from 3Vto 4Vwith 5uA as shown in Fig. 10.

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

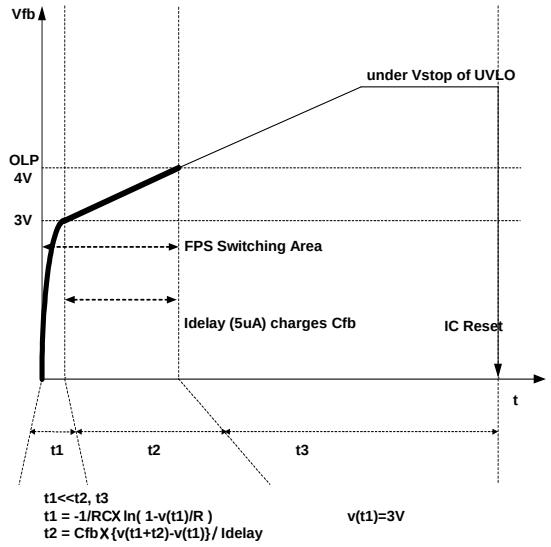
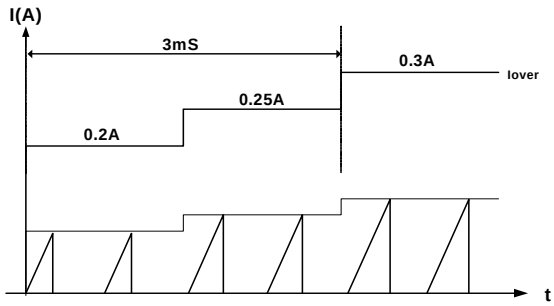


Figure 10. Over load protection delay

5. Soft Start : FSD200/210 has an internal soft start circuit that gradually increases current through the Sense FET as shown in figure 11. The soft start time is 3msec in FSD200/210.



FSD200/210

Figure 11. Internal Soft Start

6. Burst operation : In order to minimize the power dissipation in standby mode, the FSD200/210 implements burst mode functionality (see figure 12). As the load decreases, the feedback voltage decreases. As shown in figure 13, the device automatically enters burst mode when the feedback voltage drops below V_{BURL}(0.58V). At this point switching stops and the output voltages start to drop at a rate dependant on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}(0.64V) switching starts again. The feedback voltage falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in

standby mode.

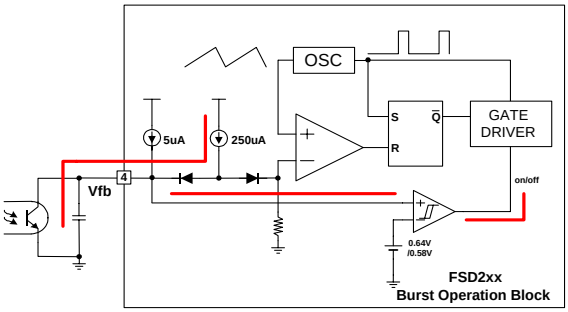


Figure 12. Circuit for burst operation

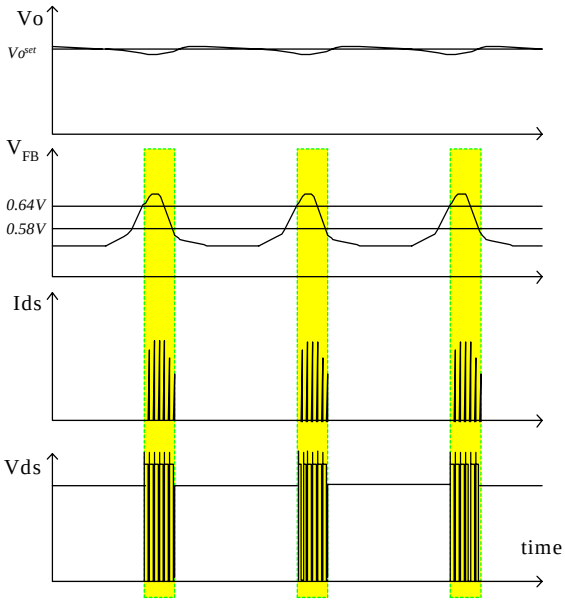


Figure 13. Burst mode operation

7. Frequency Modulation : EMI reduction can be accomplished by modulating the switching frequency of a SMPS. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range. The amount of EMI reduction is directly related to the level of modulation (Fmod) and the rate of modulation. As can be seen in Figure 14, the frequency changes from 130kHz to 138kHz in 4mS for the FSD200/FSD210. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

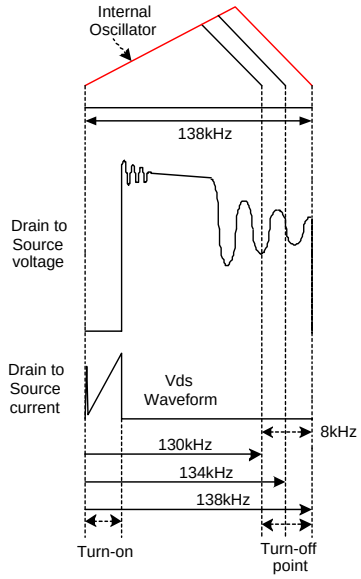


Figure 14. Frequency Modulation Waveforms

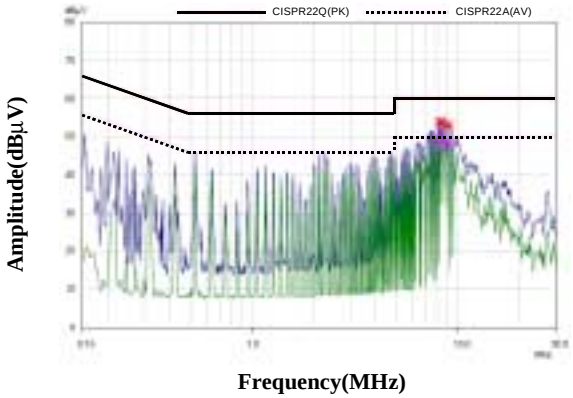


Figure 15. FSDH0165 Full Range EMI scan(100kHz, no Frequency Modulation) with charger set

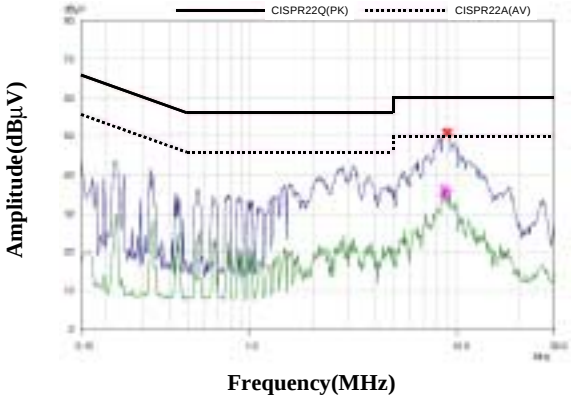


Figure 16. FSD210 Full Range EMI scan(134kHz, with Frequency Modulation) with charger set

Typical application circuit

Application	Output power	Input voltage	Output voltage (Max current)
Cellular Phone Charger	3.38W	Universal input (85-265Vac)	5.2V (650mA)

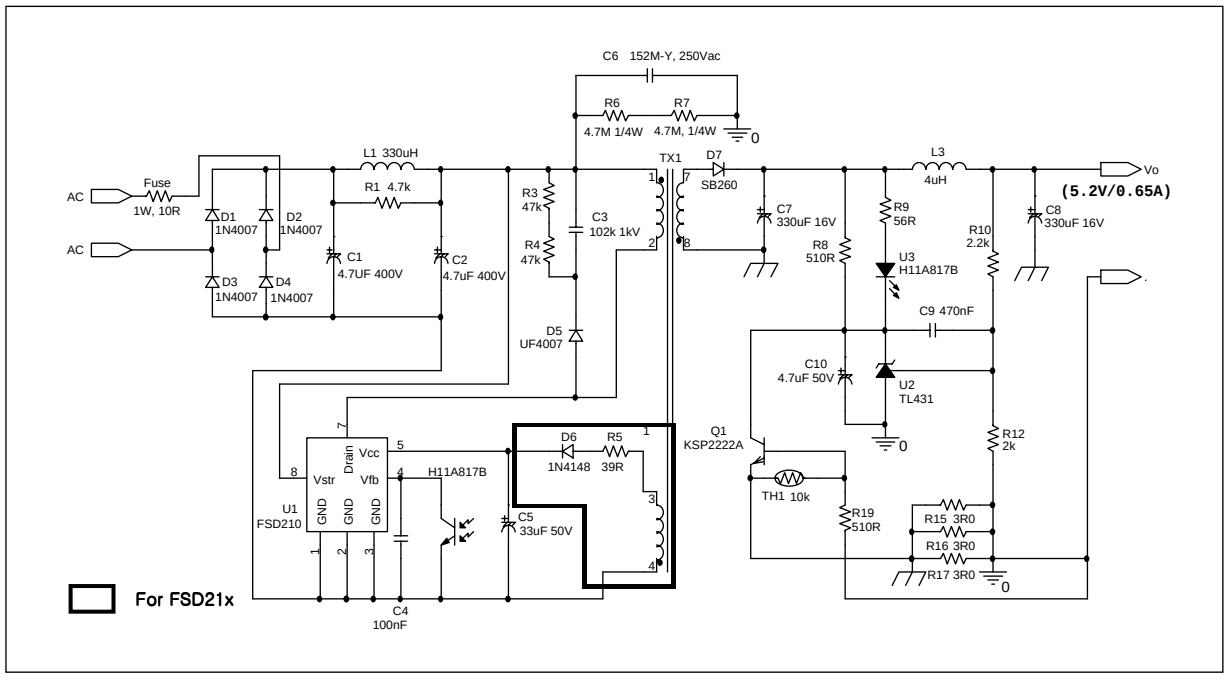
Features

- High efficiency (>67% at Universal Input)
- Low zero load power consumption (<100mW at 240Vac) with FSD210
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (3ms)
- Frequency Modulation for low EMI

Key Design Notes

- The constant voltage (CV) mode control is implemented with resistors, R8, R9, R10 and R11, shunt regulator, U2, feedback capacitor, C9 and opto-coupler, U3.
- The constant current (CC) mode control is designed with resistors, R8, R9, R15, R16, R17 and R19, NPN transistor, Q1 and NTC, TH1. When the voltage across current sensing resistors, R15,R16 and R17 is 0.7V, the NPN transistor turns on and the current through the opto coupler LED increases. This reduces the feedback voltage and duty ratio. Therefore, the output voltage decreases and the output current is regulated.
- The NTC(negative thermal coefficient) is used to compensate the temperature characteristics of the transistor Q1.

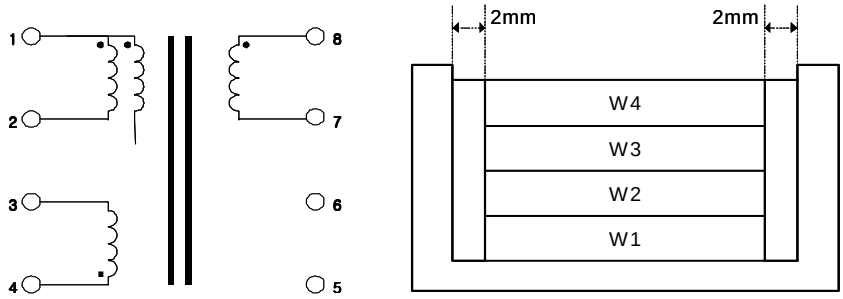
1. Schematic



2. Demo Circuit Part List

Reference	Part #	Quantity	Description	Requirement/Comment
D1,D2,D3,D4	1N4007	4	1A/1000V Junction Rectifier	DO41 Type
D5	UF4007	1	1A/1000V Ultra Fast Diode	DO41 Type
D6	1N4148	1	10mA/100V Junction Diode	D0-213 Type
D7	SB260	1	2A/60V Schottky Diode	D0-41 Type
Q1	KSP2222A	1	Ic=600mA, Vce=30V	TO-92 Type
U1	FSD210 (FSD200)	1	0.5A/700V	Iover=0.3A, Fairchildsemi
U2	KA431AZ	1	Vref=2.495V(Typ.)	TO-92 Type, LM431
U3	H11A817A	1	CTR 80~160%	-

3. Transformer Schematic Diagram



CORE : EE1616
BOBBIN : EE1616(H)

4. Winding Specification

No.	Pin (S → F)	Wire	Turns	Winding Method
W1	1 → 2	0.16Φ X 1	99 Ts	SOLENOID WINDING
INSULATION : POLYESTER TAPE t=0.025mm / 10mm, 2Ts				
W2	4 → 3	0.16Φ X 1	18 Ts	CENTER SOLENOID WINDING
INSULATION : POLYESTER TAPE t=0.025mm / 10mm, 2Ts				
W3	1 → open	0.16Φ X 1	50 Ts	SOLENOID WINDING
INSULATION : POLYESTER TAPE t=0.025mm / 10mm, 3Ts				
W4	8 → 7	0.40Φ X 1	9 Ts	SOLENOID WINDING
INSULATION : POLYESTER TAPE t=0.025mm / 10mm, 3Ts				

5. Electrical Characteristics

ITEM	TERMINAL	SPECIFICATION	REMARKS
INDUCTANCE	1 – 2	1.6mH	1kHz, 1V
LEAKAGE L	1 – 2	50uH	3,4,7,8 short 100kHz, 1V

Typical application circuit

Application	Output power	Input voltage	Output voltage (Max current)
Non Isolation Buck	1.2W	Universal dc input (100 ~ 375Vac)	12V (100mA)

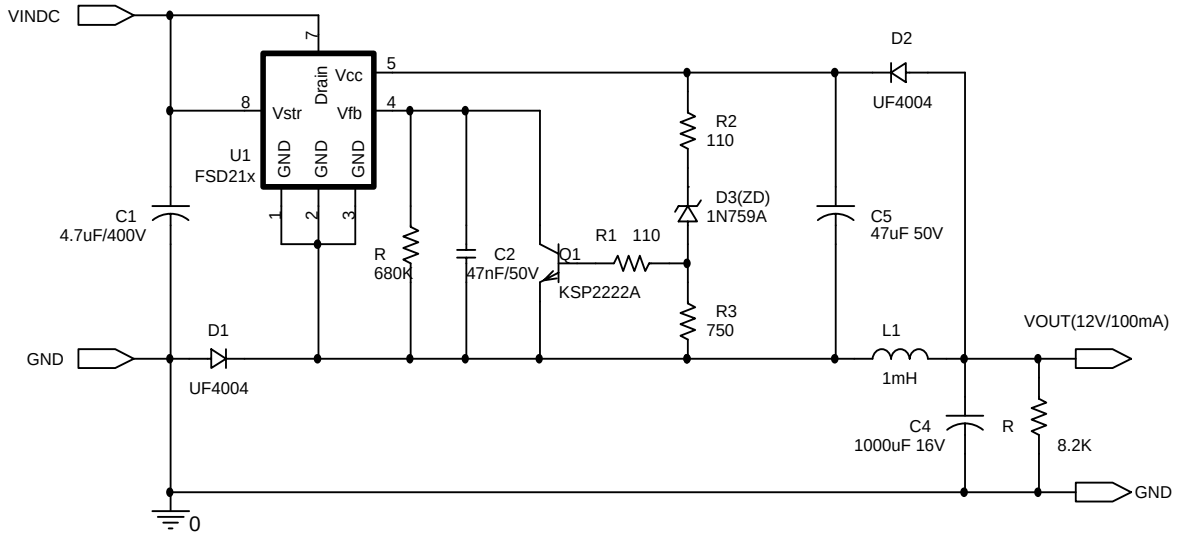
Features

- Non isolation buck converter
- Low component count
- Enhanced system reliability through various protection functions

Key Design Notes

- The output voltage(12V) is regulated with resistors, R1, R2 and R3, zener diode, D3, the transistor, Q1 and the capacitor, C2. While the FSD210 is off diodes, D1 and D2, are on. At this time the output voltage, 12V, can be sensed by the feedback components above. This output is also used with bias voltage for the FSD210.
- R, 680K, is to prevent the OLP(over load protection) at startup.
- R, 8.2K, is a dummy resistor to regulate output voltage in light load.

1. Schematic



2. Demo Circuit Part List

Reference	Part #	Quantity	Description	Requirement/Comment
D1,D2,	UF4007	2	1A/1000V Ultra Fast Diode	DO41 Type
Q1	KSP2222A	1	Ic=200mA, Vcc=40V	TO-92 Type
ZD1	1N759A	1	12VZD/0.5W	DO-35 Type
U1	FSD210	1	0.5A/700V	Iover=0.3A

Layout Considerations (for Flyback Convertor)

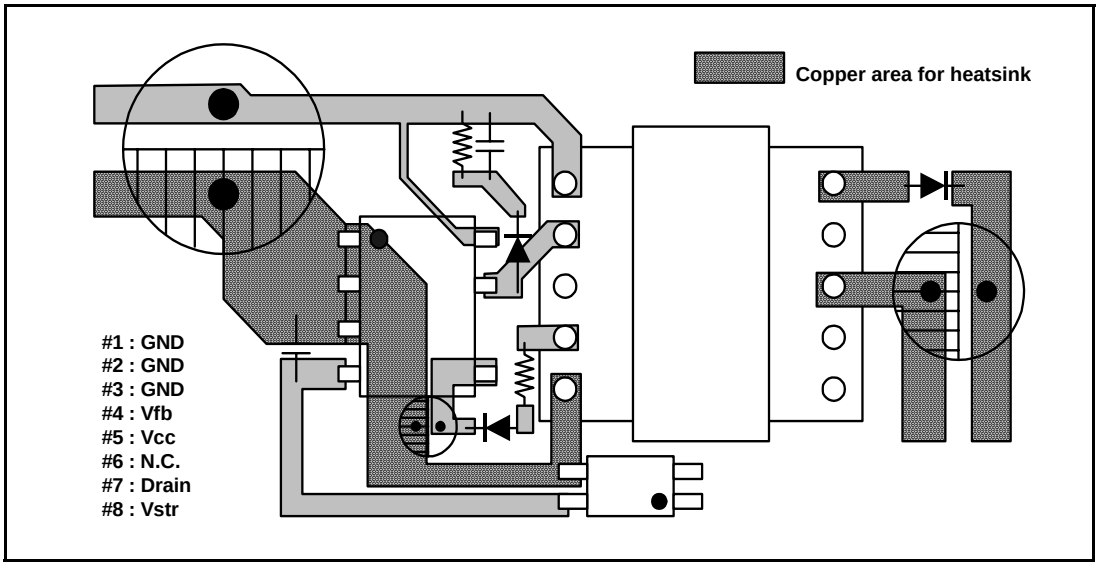
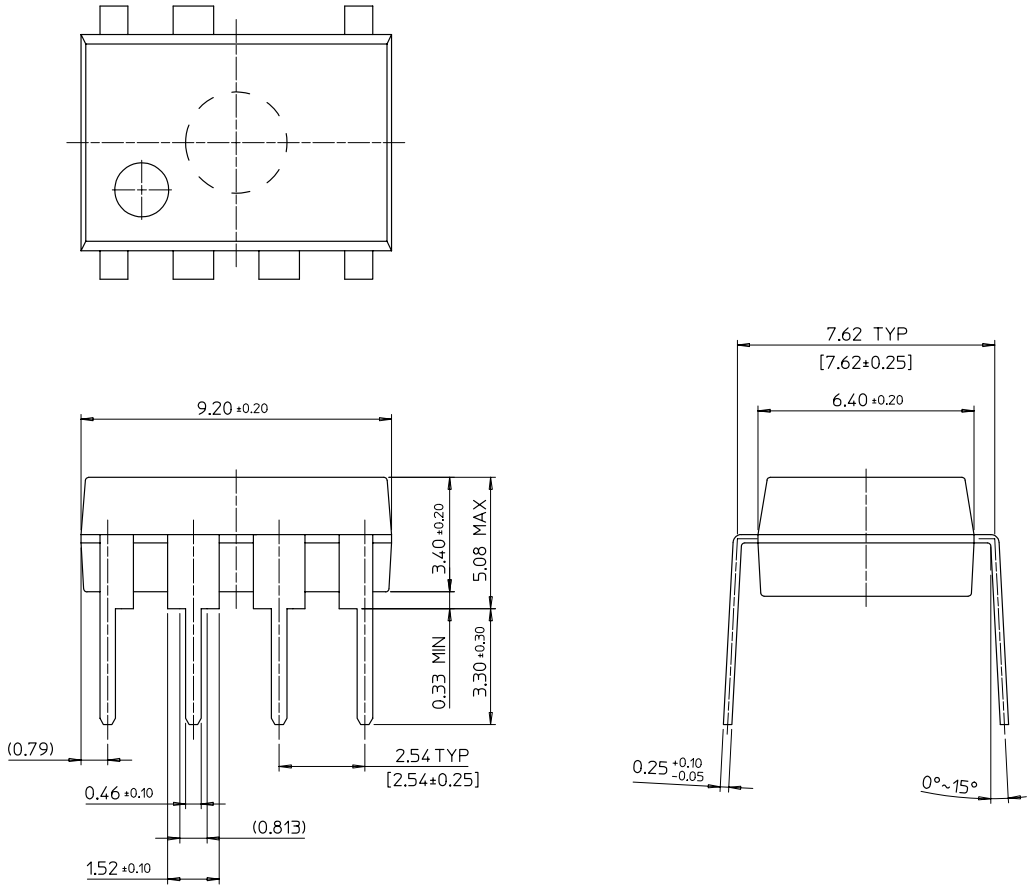


Figure 17. Layout Considerations for FSD2x0 using 7DIP

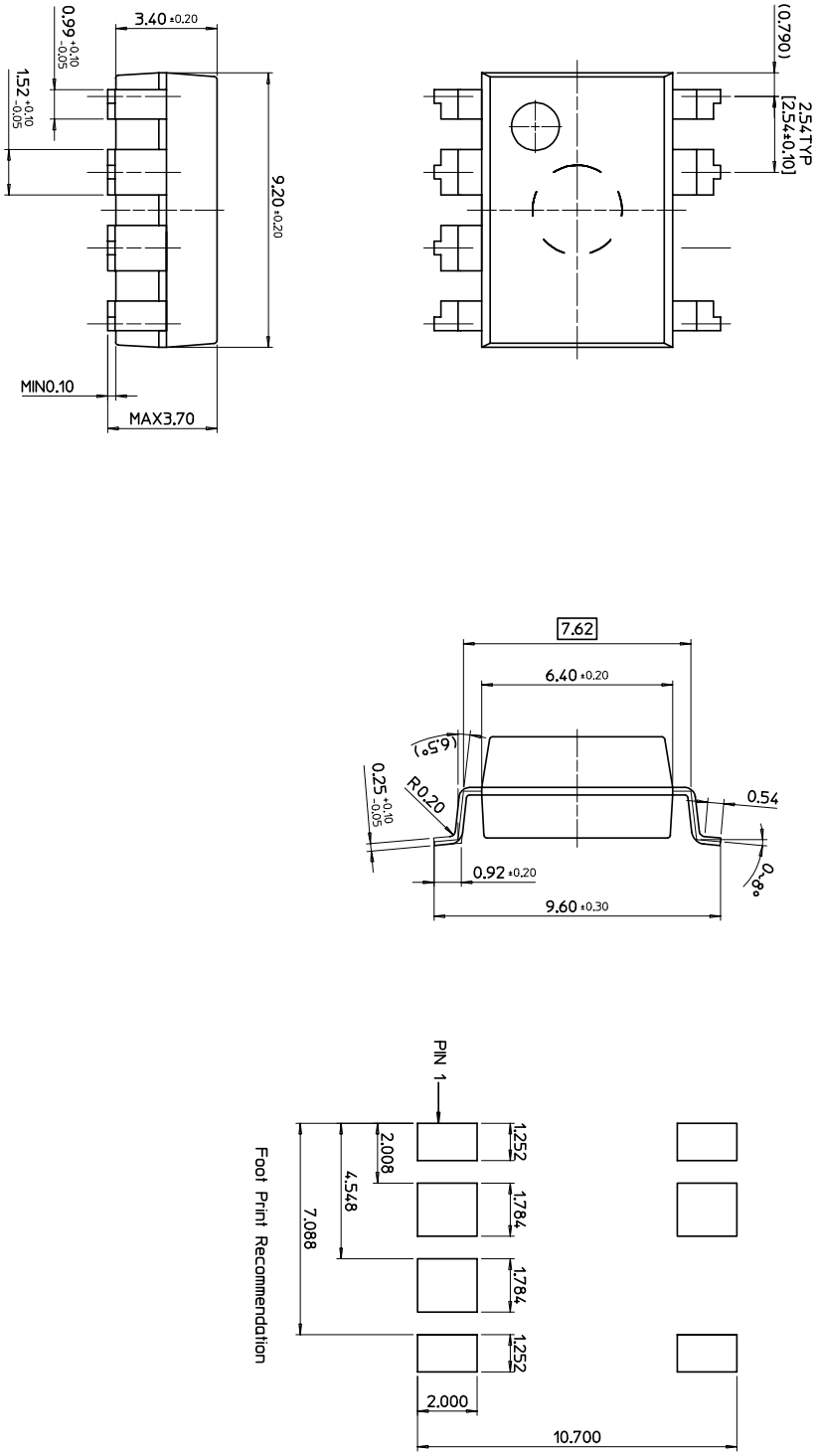
Package Dimensions

7-DIP



Package Dimensions (Continued)

7-LSOP



Ordering Information

Product Number	Package	Rating	Topr (°C)
FSD210	7DIP	700V, 0.5A	–25°C to +85°C
FSD200	7DIP	700V, 0.5A	–25°C to +85°C
FSD210M	7LSOP	700V, 0.5A	–25°C to +85°C
FSD200M	7LSOP	700V, 0.5A	–25°C to +85°C

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