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FAIRCHILD SEMICONDUCTOR®

November 2007

FSDM311A
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET
- Precision Fixed Operating Frequency: 67KHz
- Consumes Under 0.2W at 265V_{AC} & No Load with Advanced Burst-Mode Operation
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Over-Voltage Protection (OVP)
- Overload Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO) with Hysteresis
- Built-in Soft-Start
- Secondary-Side Regulation

Applications

- Charger & Adapter for Mobile Phone, PDA, & MP3
- Auxiliary Power for White Goods, PC, C-TV, & Monitors

8DIP



Description

The FSDM311A consists of an integrated Pulse Width Modulator (PWM) and SenseFET, and is specifically designed for high-performance, off-line, Switch-Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high-voltage power switching regulator that combines a VDMOS SenseFET with a voltage-mode PWM control block. The integrated PWM controller features include a fixed oscillator, Under-Voltage Lockout (UVLO) protection, Leading-Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature-compensated precision-current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDM311A device reduces total component count and design size and weight, while increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for the design of cost-effective flyback converters.

Related Resources

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)
AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)
AN-4138: Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch (FPS™)
AN-4140: Transformer Design Consideration for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)
AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications
AN-4147: Design Guidelines for RCD Snubber of Flyback
AN-4148: Audible Noise Reduction Techniques for FPS™ Applications

Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$
FSDM311A	8DIP	DM311A	650V	67KHz	14Ω

All packages are lead free per JEDEC: J-STD-020B standard.

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Typical Application & Output Power Table

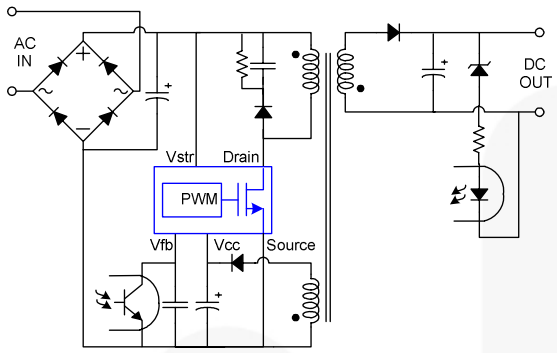


Figure 1. Typical Flyback Application

OUTPUT POWER TABLE		
Product	**Open Frame(1)**	
	230V$_{AC}$ ±15%(2)	**85~265V$_{AC}$**
FSDM311A	13W	8W

Notes:
1. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. 230V$_{AC}$ or 100/115V$_{AC}$ with doubler.

Internal Block Diagram

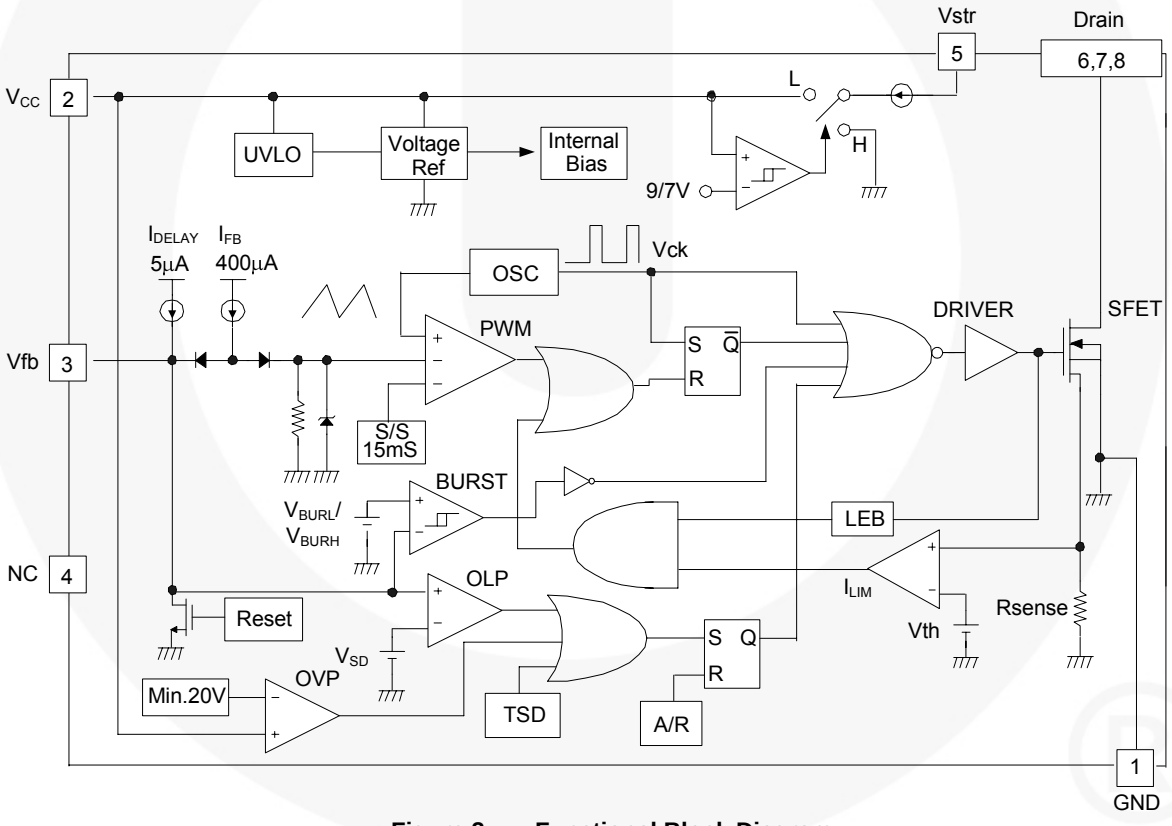


Figure 2. Functional Block Diagram

Pin Configuration

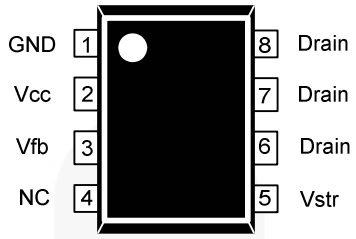


Figure 3. 8-Lead DIP Pin Assignments (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. SenseFET source terminal on primary side and internal control ground.
2	Vcc	**Positive supply voltage input**. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during start-up *(see the Internal Block Diagram in Figure 2)*. It is not until V_{CC} reaches the UVLO upper threshold (9V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	**Feedback**. Inverting input to the PWM comparator with its normal input level lies between 0.5V and 2.5V. It has a 0.4mA current source connected internally, while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 4.5V triggers overload protection (OLP). There is a time delay while charging external capacitor C_{FB} from 3V to 4.5V using an internal 5μA current source. This time delay prevents false triggering under transient conditions, but allows the protection mechanism to operate under true overload conditions.
4	NC	**No Connection**.
5	Vstr	**Start-up**. This pin connects directly to the rectified AC line voltage source. At start-up, the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the V_{CC} reaches 9V, the internal switch stops charging the capacitor.
6,7,8	Drain	**SenseFET Drain**. The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimize the length of the trace connecting these pins to the transformer to decrease leakage inductance.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C, unless otherwise specified.

Symbol	Parameter	Value	Unit
V_{DRAIN}	Drain Pin Voltage	650	V
V_{STR}	Vstr Pin Voltage	650	V
V_{DG}	Drain-Gate Voltage	650	V
V_{GS}	Gate-Source Voltage	±20	V
I_{DM}	Drain Current Pulsed(3)	1.5	A
I_D	Continuous Drain Current (T_C=25°C)	0.5	A
I_D	Continuous Drain Current (T_C=100°C)	0.32	A
E_{AS}	Single Pulsed Avalanche Energy(4)	10	mJ
V_{CC}	Supply Voltage	20	V
V_{FB}	Feedback Voltage Range	-0.3 to V_{STOP}	V
P_D	Total Power Dissipation	1.40	W
T_J	Operating Junction Temperature	Internally limited	°C
T_A	Operating Ambient Temperature	-25 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C

Notes:
3. Repetitive rating: Pulse width is limited by maximum junction temperature.
4. L = 24mH, starting T_J = 25°C

Thermal Impedance

T_A=25°C, unless otherwise specified.

Symbol	Parameter	Value	Unit
8DIP			
θ_{JA}	Junction-to-Ambient Thermal Impedance(5)	88.84	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance(6)	13.94	°C/W

Notes:
5. Free standing with no heatsink; without copper clad. (Measurement Condition – just before junction temperature T_J enters into OTP).
6. Measured on the DRAIN pin close to plastic interface.
7. All items are tested with the standards JESD 51-2 and 51-10 (DIP).

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Electrical Characteristics

T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SENSEFET SECTION						
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS}=650V, V_{GS}=0V			25	mA
		V_{DS}=520V, V_{GS}=0V, T_C=125°C			200	
$R_{DS(ON)}$	Drain-Source On-State Resistance[8]	V_{GS}=10V, I_D=0.5A		14	19	Ω
g_{fs}	Forward Trans-Conductance	V_{DS}=50V, I_D=0.5A	1.0	1.3		S
C_{ISS}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		162		pF
C_{OSS}	Output Capacitance			18		
C_{RSS}	Reverse Transfer Capacitance			3.8		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=325V, I_D=1.0A		9.5		ns
t_r	Rise Time			19		
$t_{d(off)}$	Turn-Off Delay Time			33		
t_f	Fall Time			42		
Q_g	Total Gate Charge	V_{GS}=10V, I_D=1.0A, V_{DS}=325V		7.0		nC
Q_{gs}	Gate-Source Charge			3.1		
Q_{gd}	Gate-Drain (Miller) Charge			0.4		
CONTROL SECTION						
f_{OSC}	Switching Frequency		61	67	73	KHz
Δf_{OSC}	Switching Frequency Variation[9]	-25°C ≤ T_A ≤ 85°C		±5	±10	%
D_{MAX}	Maximum Duty Cycle		60	67	74	%
V_{START}	UVLO Threshold Voltage	V_{FB}=GND	8	9	10	V
V_{STOP}		V_{FB}=GND	6	7	8	V
I_{FB}	Feedback Source Current	0V ≤ V_{FB} ≤ 3V	0.35	0.40	0.45	mA
$t_{S/S}$	Internal Soft-Start Time		10	15	20	ms
V_{REF}	Reference Voltage[10]		4.2	4.5	4.8	V
$\Delta V_{REF}/\Delta T$	Reference Voltage Variation with Temperature[9, 10]	-25°C ≤ T_A ≤ 85°C		0.3	0.6	mV/°C
BURST MODE SECTION						
V_{BURH}	Burst Mode Voltage	T_J=25°C	0.6	0.7	0.8	V
V_{BURL}			0.45	0.55	0.65	V
$V_{BUR(HYS)}$		Hysteresis		150		mV
PROTECTION SECTION						
I_{LIM}	Peak Current Limit	di/dt=90mA/μs	0.500	0.575	0.650	A
T_{SD}	Thermal Shutdown Temperature[10]		125	145		°C
V_{SD}	Shutdown Feedback Voltage		4.0	4.5	5.0	V
V_{OVP}	Over-Voltage Protection		20			V
I_{DELAY}	Shutdown Delay Current	3V ≤ V_{FB} ≤ V_{SD}	4	5	6	μA
TOTAL DEVICE SECTION						
I_{OP}	Operating Supply Current (control part only)	V_{CC} ≤ 16V		1.5	3.0	mA
I_{CH}	Start-up Charging Current	V_{CC}=0V, V_{STR}=50V	450	550	650	μA

Notes:

8. Pulse test: Pulse width ≤ 300μs, duty ≤ 2%.
9. These parameters, although guaranteed, are tested in EDS (wafer test) process.
10. These parameters, although guaranteed, are not 100% tested in production.

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Typical Performance Characteristics

Normalized at T_A = 25°C.

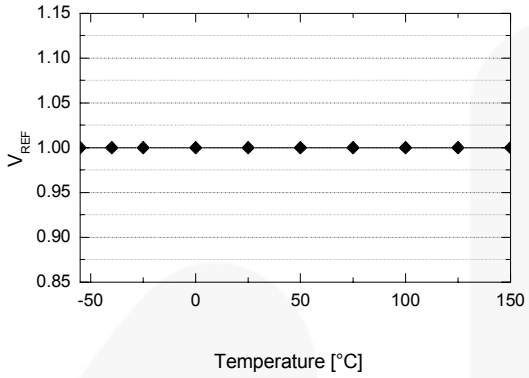


Figure 4. Reference Voltage (V_{REF}) vs. T_A

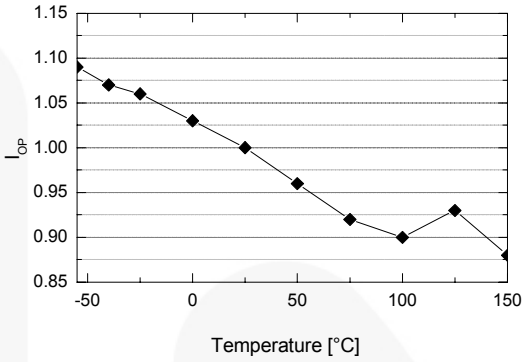


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

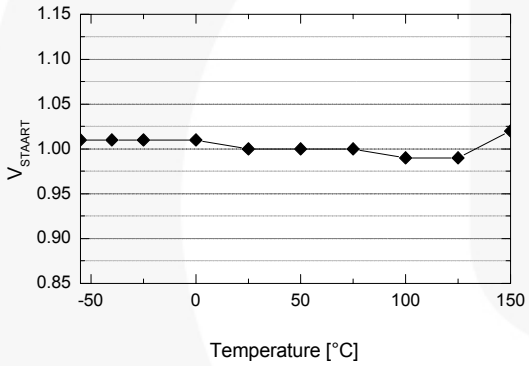


Figure 6. Start Threshold Voltage (V_{START}) vs. T_A

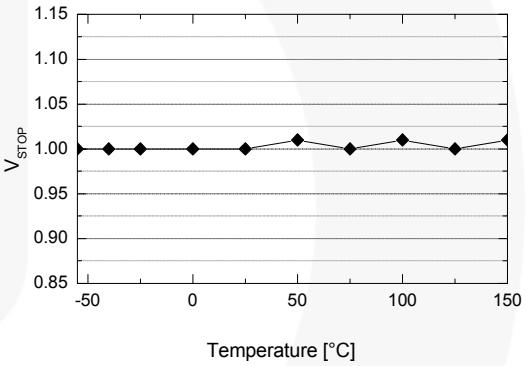


Figure 7. Stop Threshold Voltage (V_{STOP}) vs. T_A

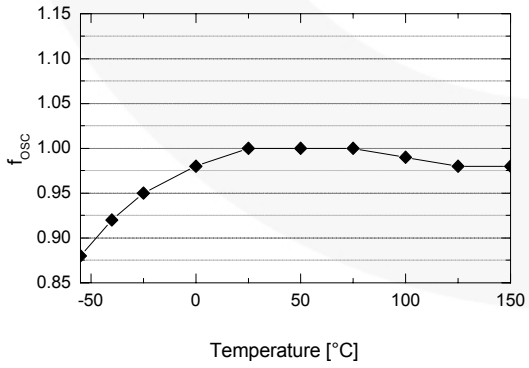


Figure 8. Operating Frequency (f_{OSC}) vs. T_A

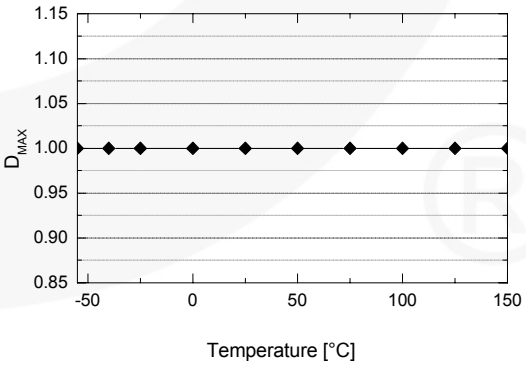


Figure 9. Maximum Duty Cycle (D_{MAX}) vs. T_A

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Typical Performance Characteristics (Continued)

Normalized at T_A = 25°C.

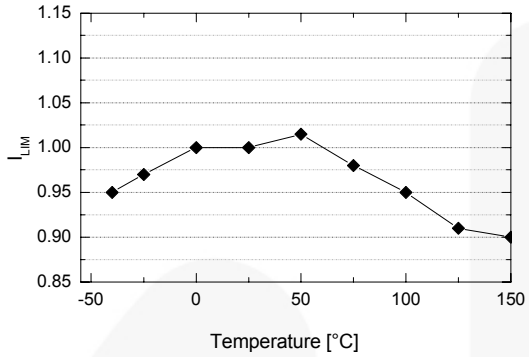


Figure 10. Peak Current Limit (I_{LIM}) vs. T_A

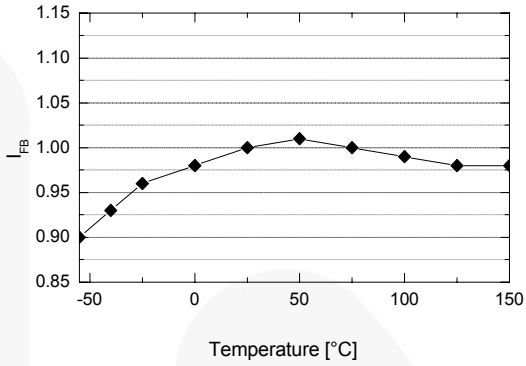


Figure 11. Feedback Source Current (I_{FB}) vs. T_A

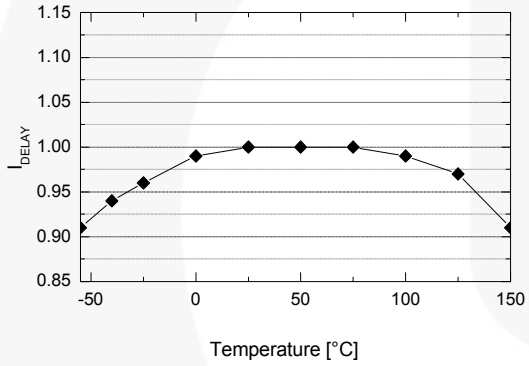


Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

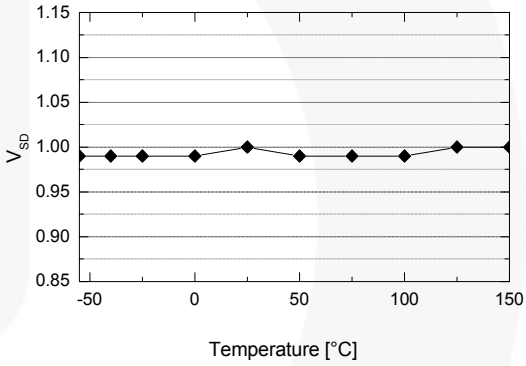


Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

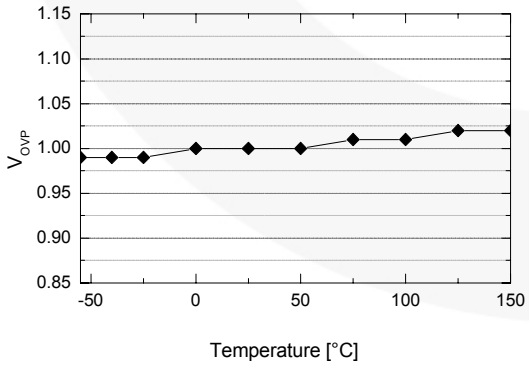


Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

Functional Description

1. Start-up: At start-up, the internal high-voltage current source supplies the internal bias and charges the external V_{CC} capacitor, as shown in Figure 15. When V_{CC} reaches 9V, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device is in normal operation provided V_{CC} does not drop below 7V. After start-up, the bias is supplied from the auxiliary transformer winding.

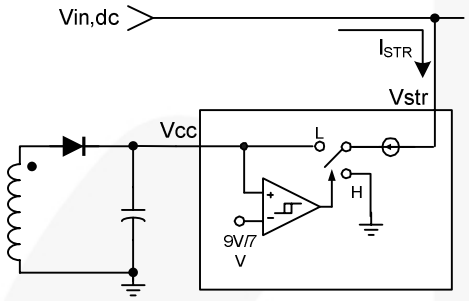


Figure 15. Internal Start-up Circuit

Calculating the V_{CC} capacitor is an important step in design with the FSDM311A. At initial start-up, the maximum value of start operating current I_{START} is about 100μA, which supplies current to UVLO and V_{REF} blocks. The charging current I_{Vcc} of the V_{CC} capacitor is equal to I_{STR} – 100μA. After V_{CC} reaches the UVLO start voltage, only the bias winding supplies V_{CC} current to the device. When the bias winding voltage is not sufficient, the V_{CC} level decreases to the UVLO stop voltage and the internal current source is activated again to charge the V_{CC} capacitor. To prevent this V_{CC} fluctuation (charging/discharging), the V_{CC} capacitor should be chosen for a value between 10μF and 47μF.

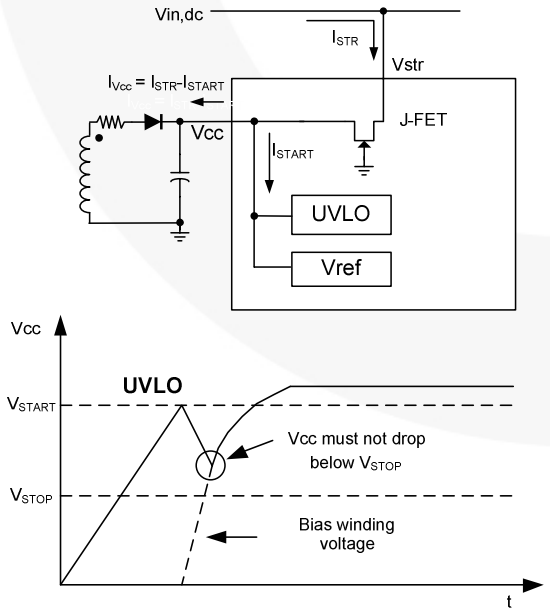


Figure 16. Charging V_{CC} Capacitor through V_{STR}

2. Feedback Control: The FSDM311A is the voltage-mode controlled device, as shown in Figure 17. Usually, an opto-coupler and shunt regulator, such as KA431, are used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform that directly controls the duty cycle. When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage V_{FB} is pulled down, and it reduces the duty cycle. This happens when the input voltage increases or the output load decreases.

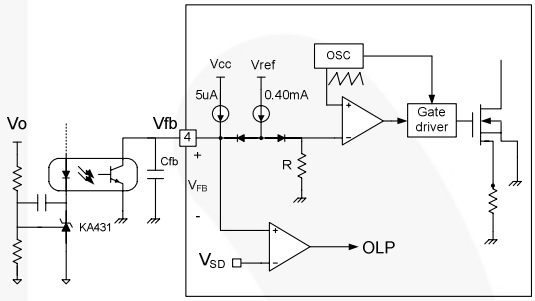


Figure 17. PWM and Feedback Circuit

3. Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high-current spike through the SenseFET. Excessive voltage across the R_{SENSE} resistor leads to incorrect pulse-by-pulse current limit protection. To avoid this, a leading-edge blanking (LEB) circuit disables pulse-by-pulse current limit protection block for a fixed time (t_{LEB}) after the SenseFET turns on.

4. Protection Circuit: The FSDM311A has several protective functions, such as overload protection (OLP), over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown (TSD). Because these protection circuits are fully integrated in the IC without external components, the reliability is improved without increasing costs. Once a fault condition occurs, switching is terminated and the SenseFET remains off, which causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage, V_{STOP} (7V), the protection is reset and the internal high-voltage current source charges the Vcc capacitor via the Vstr pin. When V_{CC} reaches the UVLO start voltage, V_{START} (9V), the device resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

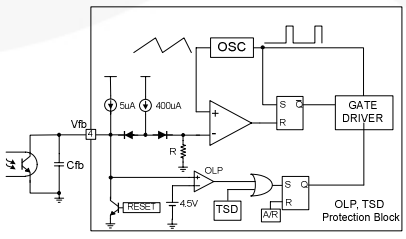
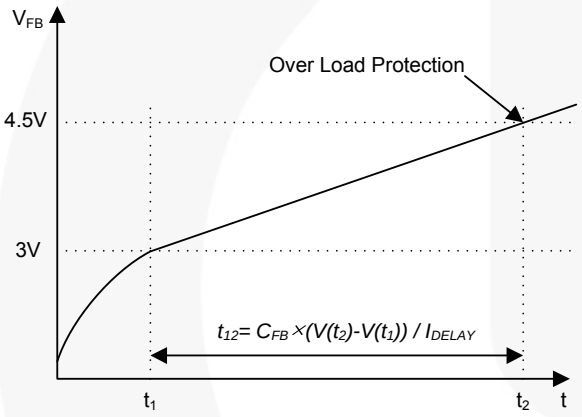


Figure 18. Protection Block

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4.1 Overload Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is operating normally, the overload protection (OLP) circuit can be activated during the load transition. To avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. If the output consumes more than the maximum power determined by I_{LIM}, the output voltage (V_O) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to charge C_{FB} slowly up to V_{CC}. In this condition, V_{FB} increases until it reaches 4.5V, when the switching operation is terminated, as shown in Figure 19. The shutdown delay time is the time required to charge C_{FB} from 3V to 4.5V with 5μA current source.



$$t_{12} = C_{FB}\frac{V(t_2)-V(t_1)}{I_{DELAY}}; \quad I_{DELAY} = 5\mu A, V(t_1) = 3V, V(t_2) = 4.5V$$

Figure 19. Overload Protection (OLP)

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC are integrated, making it easier for the control IC to detect the temperature of the SenseFET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

5. Soft-Start: The FPS has an internal soft-start circuit that slowly increases the feedback voltage with the SenseFET current right after it starts up. The typical soft-start time is 15ms, as shown in Figure 20, where progressive increment of the SenseFET current is allowed during the start-up phase. The soft-start circuit progressively increases current limits to establish proper working conditions for transformers, inductors, capacitors, and switching devices. It also helps to prevent transformer saturation and reduces the stress on the secondary diode.

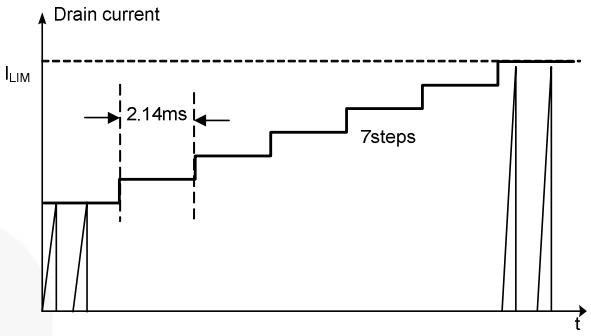


Figure 20. Internal Soft-Start

6. Burst Operation: To minimize the power dissipation in standby mode, the FSDM311A enters burst mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below V_{BURL} (0.55V). At this point, switching stops and the output voltages start to drop. This causes the feedback voltage to rise. Once is passes V_{BURH} (0.70V), switching starts again. The feedback voltage falls and the process repeats. Burst mode operation alternately enables and disables switching of the power MOSFET to reduce the switching loss in standby mode.

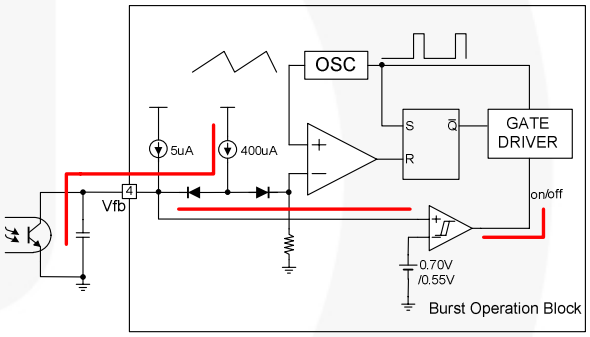


Figure 21. Burst Operation Block

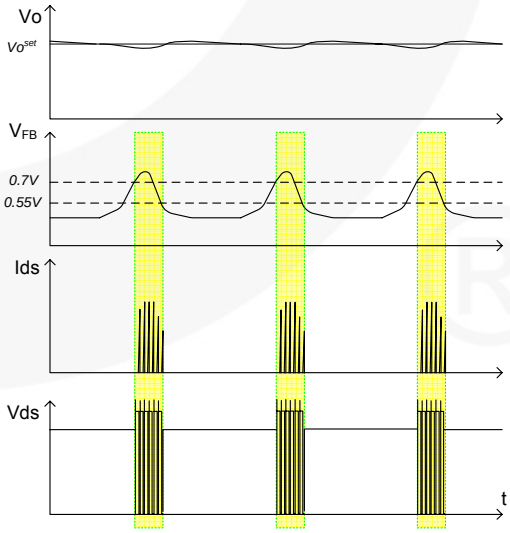


Figure 22. Burst Operation Function

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Application Information

Methods of Reducing Audible Noise

Switching-mode power converters have electronic and magnetic components that generate audible noise when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20kHz, they can make noise, depending on the load condition. Designers can employ several methods to reduce noise.

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil; and the chattering or magnetostriction of core, can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce transformer noise, but can crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink at a different rate.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise-reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. A snubber capacitor becomes one of the most significant sources of audible noise. It is possible to use a Zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency out of the 2~4kHz range another method of reducing perceptible noise. Generally, humans are more sensitive to noise in the range of 2~4kHz. When the fundamental frequency of noise is located in this range, it is perceived as louder, although the noise intensity level is identical *(refer to Figure 23, Equal Loudness Curves)*.

If burst-mode operation is suspected to be a source of noise, this method may be helpful. If the frequency of burst-mode operation lies between 2~4 kHz, adjusting the feedback loop can shift the frequency. To reduce the burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D), and feedback capacitor (C_B); and decrease a feedback gain resistor (R_F), as shown in Figure 24.

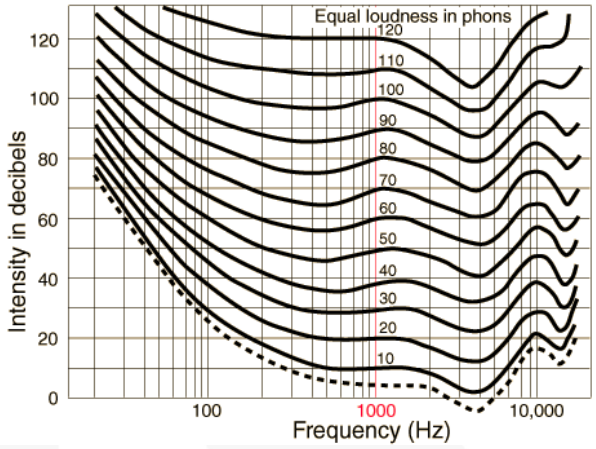


Figure 23. Equal Loudness Curves

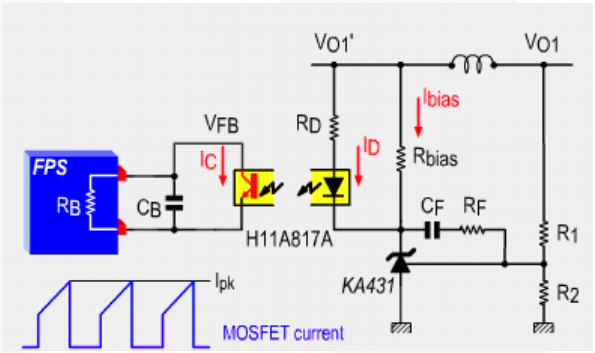
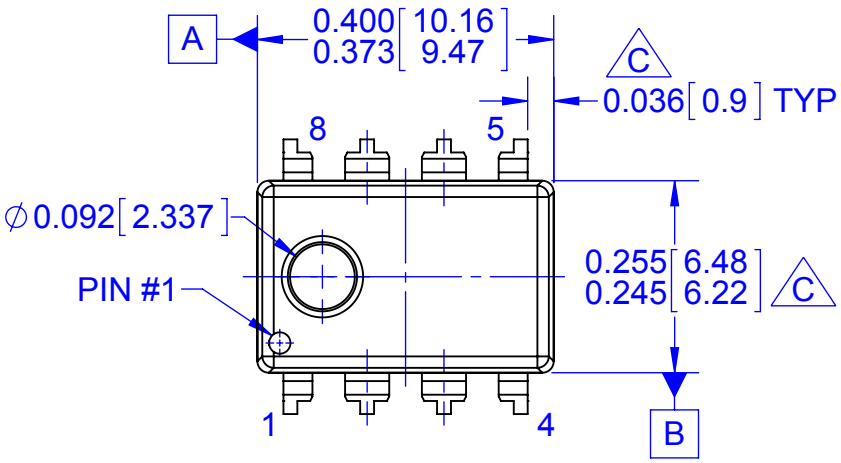


Figure 24. Typical Feedback Network of FPS™

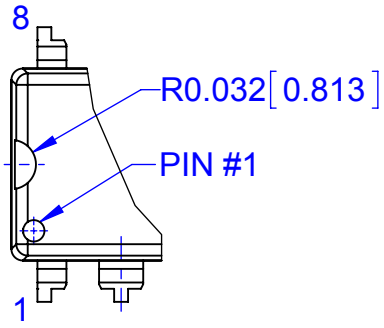
Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)
AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)
AN-4138: Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch (FPS™)
AN-4140: Transformer Design Consideration for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)
AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications
AN-4147: Design Guidelines for RCD Snubber of Flyback
AN-4148: Audible Noise Reduction Techniques for FPS™ Applications

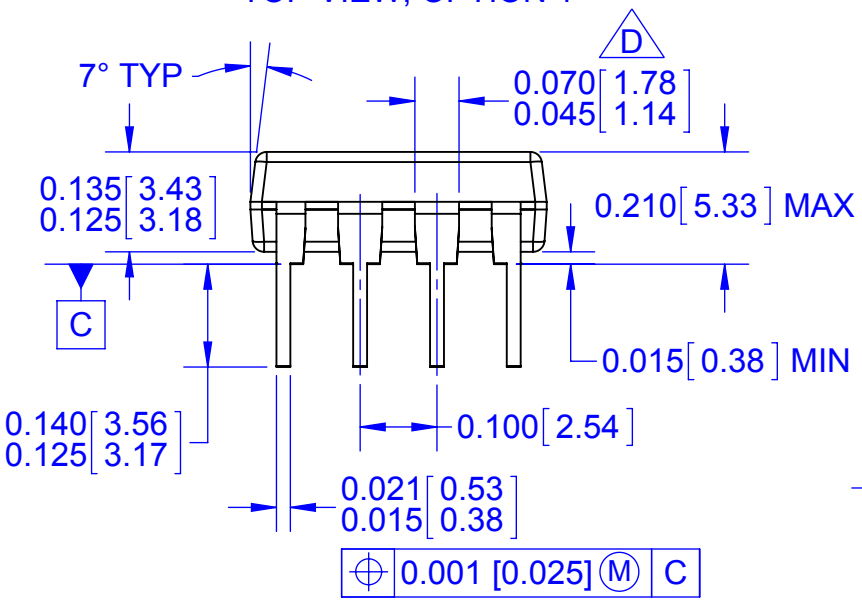
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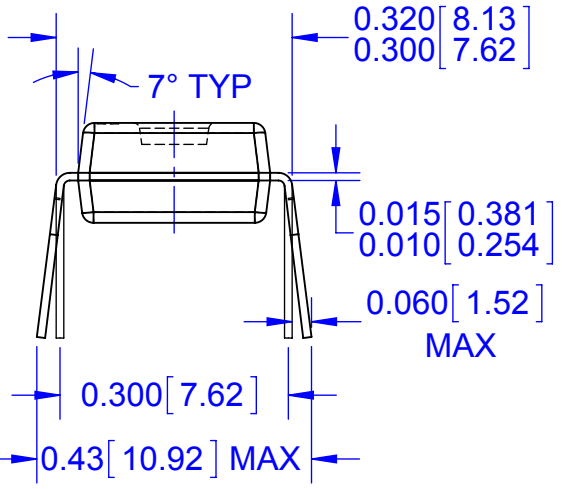
TOP VIEW, OPTION 1



TOP VIEW, OPTION 2



FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-001, VARIATION BA

B. CONTROLLING DIMENSIONS ARE IN INCHES.
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MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED
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