LM111, LM211, LM311 Differential Comparators

1 Features

- Fast Response Time: 165 ns
- Strobe Capability
- Maximum Input Bias Current: 300 nA
- Maximum Input Offset Current: 70 nA
- Can Operate From Single 5-V Supply
- Available in Q-Temp Automotive
  - High-Reliability Automotive Applications
  - Configuration Control and Print Support
  - Qualification to Automotive Standards
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Desktop PCs
- Body Control Modules
- White Goods
- Building Automation
- Oscillators
- Peak Detectors

3 Description

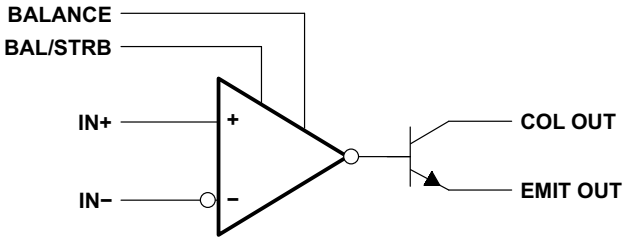
The LM111, LM211, and LM311 devices are single high-speed voltage comparators. These devices are designed to operate from a wide range of power-supply voltages, including ±15-V supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+} or V_{CC-}. Offset balancing and strobe capabilities are available, and the outputs can be wire-OR connected. If the strobe is low, the output is in the off state, regardless of the differential input.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE
LM111FK	LCCC (20)	8.89 mm × 8.89 mm
LM111JG	CDIP (8)	9.60 mm × 6.67 mm
LM311PS	SO (8)	6.20 mm × 5.30 mm
LM211D	SOIC (8)	4.90 mm × 3.91 mm
LM311D		
LM211P	PDIP (8)	9.81 mm × 6.35 mm
LM311P		
LM211PW	TSSOP (8)	3.00 mm × 4.40 mm
LM311PW		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (January 2017) to Revision K — **Page**

- Changed Human body model (HBM) from: ±1000 to: ±500 in *ESD Ratings* table ... 4

Changes from Revision I (June 2015) to Revision J — **Page**

- Changed the data sheet title From: LMx11 Quad Differential Comparators To: LM111, LM211, LM311 Differential Comparators ... 1
- Updated the *Applications* list ... 1
- Updated the *Thermal Information (8-Pin Packages)* table ... 5
- Changed text From: "over a −25°C to +85°C temperature range..." To: ""over a −40°C to +85°C temperature range..." in the *Overview* section ... 10
- Added text "The LM311 has a temperature range of −40°C to +125°C." to the *Overview* section ... 10

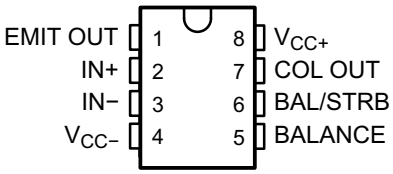
Changes from Revision H (August 2003) to Revision I — **Page**

- Updated *Features* with Military Disclaimer. ... 1
- Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. No specification changes. ... 1

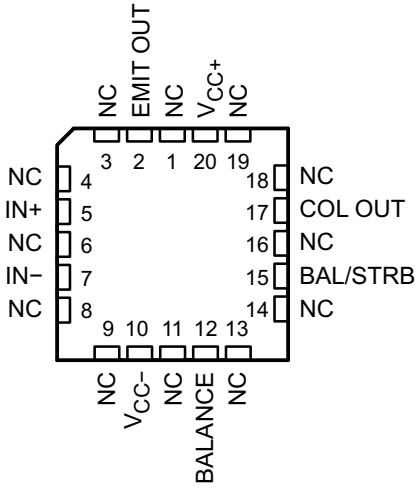
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5 Pin Configuration and Functions

LMx11 D, JG, P, PS, or PW Package
8-Pin SOIC, CDIP, PDIP, SO or TSSOP
Top View



LM111 FK Package
20-Pin LCCC(1)
Top View



(1) NC = No internal connection

Pin Functions

PIN					I/O(1)	DESCRIPTION
NAME	LM211, LM311	LM311	LM111	LM111		
	SOIC, PDIP, TSSOP	SO	CDIP	LCCC		
IN+	2	2	2	5	I	Noninverting comparator
IN–	3	3	3	7	I	Inverting input comparator
BALANCE	5	5	5	12	I	Balance
BAL/STRB	6	6	6	15	I	Strobe
COL OUT	7	7	7	17	O	Output collector comparator
EMIT OUT	1	1	1	2	O	Output emitter comparator
V_{CC}–	4	4	4	10	—	Negative supply
V_{CC}+	8	8	8	20	—	Positive supply
NC	—	—	—	1	—	No connect (No internal connection)
				3		
				4		
				6		
				8		
				9		
				11		
				13		
				14		
				16		
				18		
				19		

(1) I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage	V_{CC+}(2)		18	V
		V_{CC-}(2)		–18	
		$V_{CC+} - V_{CC-}$		36	
V_{ID}	Differential input voltage(3)			±30	V
V_I	Input voltage (either input)(2)(4)			±15	V
	Voltage from emitter output to V_{CC-}			30	V
	Voltage from collector output to V_{CC-}	LM111		50	V
		LM211		50	
		LM211Q		50	
		LM311		40	
	Duration of output short circuit to ground			10	s
T_J	Operating virtual-junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case, 10 s	JG package		300	°C
	Lead temperature 1,6 mm (1/16 inch) from case, 60 s	D, P, PS, or PW package		260	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 V, whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage		3.5	30	V
V_I	Input voltage ($\lvert V_{CC+} \rvert \le 15$ V)		V_{CC-} + 0.5	V_{CC+} – 1.5	V
T_A	Operating free-air temperature range	LM111	–55	125	°C
		LM211	–40	85	
		LM211Q	–40	125	
		LM311	0	70	

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6.4 Thermal Information (8-Pin Packages)

THERMAL METRIC[1]		LM211, LM311			LM311	LM111	UNIT
		D (SOIC)	P (PDIP)	PW (TSSOP)	PS (SO)	JG (CDIP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.3	57.5	162	121.8	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.7	47.3	44.6	81.6	14.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	34.6	93	66.5	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.4	24.9	2.6	31.4	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54	34.5	90.8	65.8	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information (20-Pin Package)

THERMAL METRIC[1]		LM111	UNIT
		FK (LCCC)	
		20 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.61	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	LM111, LM211, LM211Q			LM311			UNIT
					MIN	TYP (2)	MAX	MIN	TYP (2)	MAX	
V_{IO}	Input offset voltage	See (3)		25°C		0.7	3		2	7.5	mV
				Full range			4			10	
I_{IO}	Input offset current	See (3)		25°C		4	10		6	50	nA
				Full range			20			70	
I_{IB}	Input bias current	1 V ≤ V_O ≤ 14 V		25°C		75	100		100	250	nA
				Full range			150			300	
$I_{IL(S)}$	Low-level strobe current (4)	$V_{(strobe)}$ = 0.3 V, V_{ID} ≤ –10 mV		25°C		–3			–3		mA
V_{ICR}	Common-mode input-voltage range (3)	Lower range		Full range		–14.7	–14.5		–14.7	–14.5	V
		Upper range			13	13.8		13	13.8		
A_{VD}	Large-signal differential-voltage amplification	5 V ≤ V_O ≤ 35 V, R_L = 1 kΩ		25°C	40	200		40	200		V/mV
I_{OH}	High-level (collector) output leakage current	$I_{(strobe)}$ = –3 mA, V_{ID} = 5 mV	V_{OH} = 35 V	25°C		0.2	10				nA
				Full range			0.5				µA
		V_{ID} = 5 mV, V_{OH} = 35 V		25°C					0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	I_{OL} = 50 mA	V_{ID} = –5 mV	25°C		0.75	1.5				V
			V_{ID} = –10 mV	25°C					0.75	1.5	
		V_{CC+} = 4.5 V, V_{CC-} = 0 V, I_{OL} = 8 mA	V_{ID} = –6 mV	Full range		0.23	0.4				
			V_{ID} = –10 mV	Full range					0.23	0.4	
I_{CC+}	Supply current from V_{CC+} output low	V_{ID} = –10 mV,	No load	25°C		5.1	6		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-} output high	V_{ID} = 10 mV,	No load	25°C		–4.1	–5		–4.1	–5	mA

(1) Unless otherwise noted, all characteristics are measured with BALANCE and BAL/STRB open and EMIT OUT grounded. Full range for LM111 is –55°C to 125°C, for LM211 is –40°C to 85°C, for LM211Q is –40°C to 125°C, and for LM311 is 0°C to 70°C.
(2) All typical values are at T_A = 25°C.
(3) The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pullup resistor of 7.5 kΩ to V_{CC+}. These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.
(4) The strobe must not be shorted to ground; it must be current driven at –3 mA to –5 mA (see Figure 18 and Figure 31).

6.7 Switching Characteristics

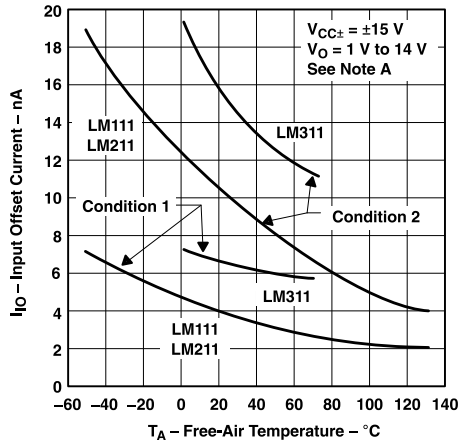
$V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LM111, LM211, LM211Q, LM311	UNIT
		TYP	
Response time, low-to-high-level outputSee (1)	R_C = 500 Ω to 5 V, C_L = 5 pF, see (2)	115	ns
Response time, high-to-low-level outputSee (1)		165	ns

(1) The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.
(2) The package thermal impedance is calculated in accordance with MIL-STD-883.

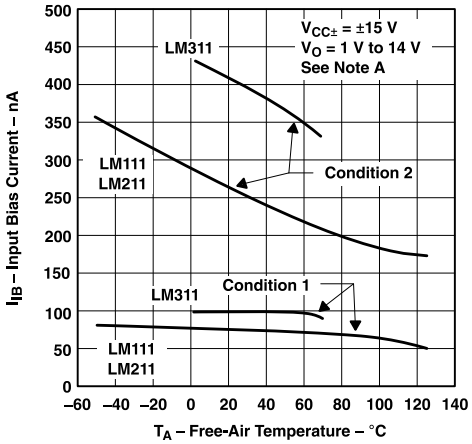
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6.8 Typical Characteristics



Condition 1 is with BALANCE and BAL/STRB open.
Condition 2 is with BALANCE and BAL/STRB connected to V_{CC+}.

Figure 1. Input Offset Current vs Free-Air Temperature



Condition 1 is with BALANCE and BAL/STRB open.
Condition 2 is with BALANCE and BAL/STRB connected to V_{CC+}.

Figure 2. Input Bias Current vs Free-Air Temperature

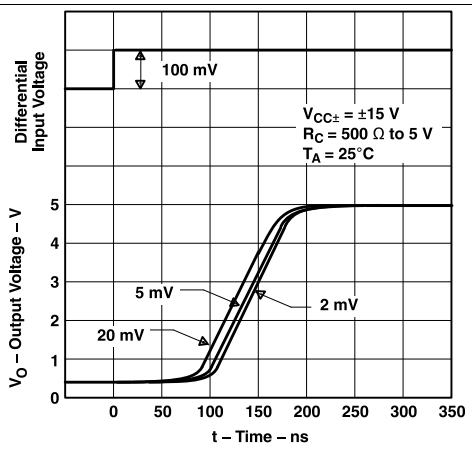


Figure 3. Output Response for Various Input Overdrives

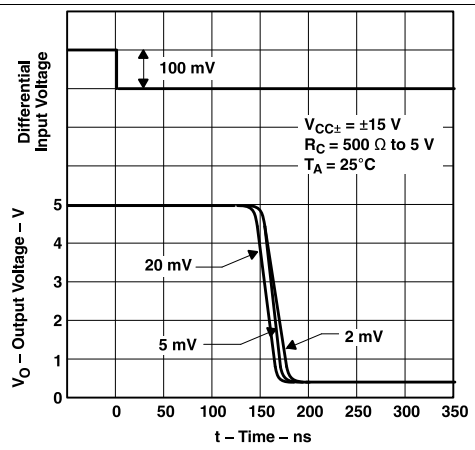


Figure 4. Output Response for Various Input Overdrives

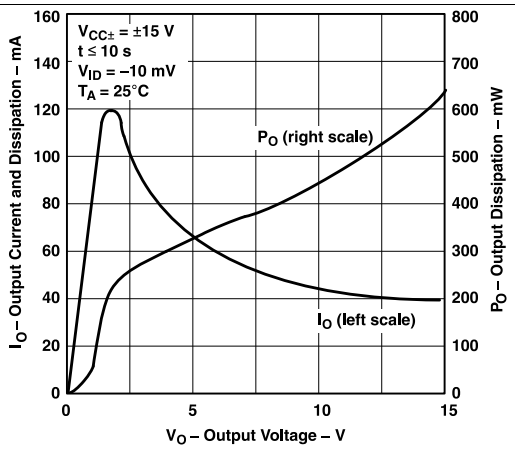


Figure 5. Output Current and Dissipation vs Output Voltage

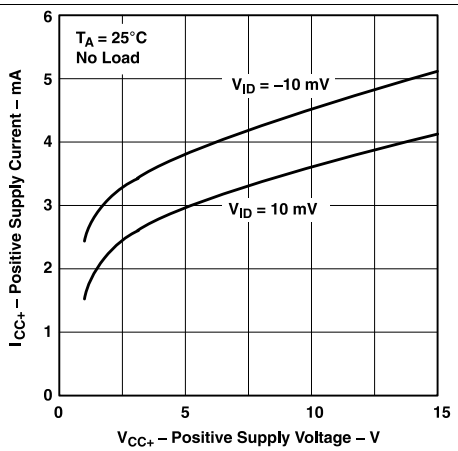


Figure 6. Positive Supply Current vs Positive Supply Voltage

Typical Characteristics (continued)

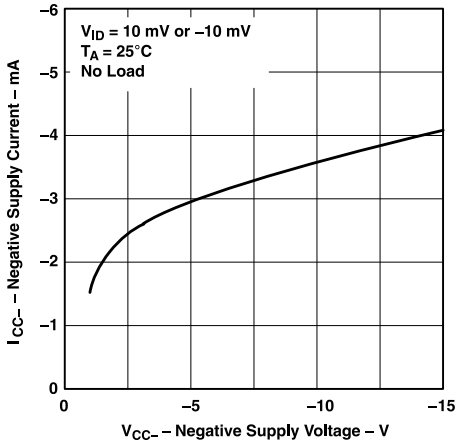


Figure 7. Negative Supply Current vs Negative Supply Voltage

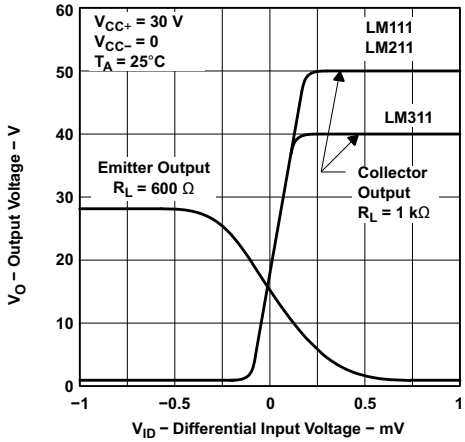
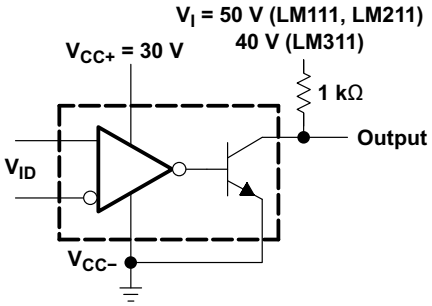


Figure 8. Voltage Transfer Characteristics and Test Circuits

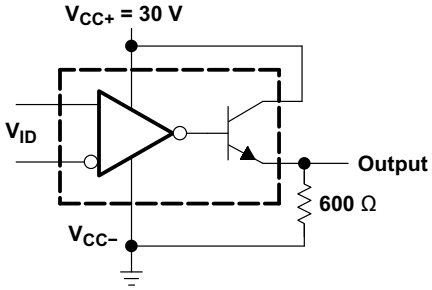
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7 Parameter Measurement Information



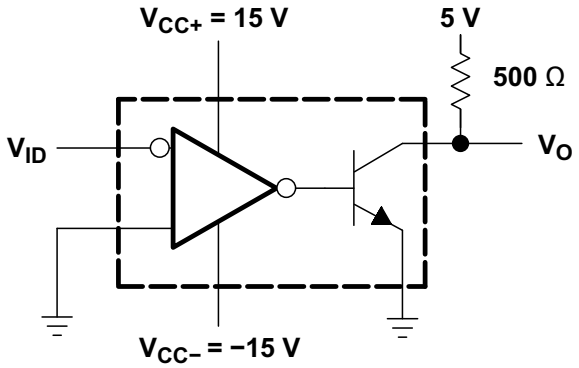
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Figure 9. Collector Output Transfer Characteristic Test Circuit



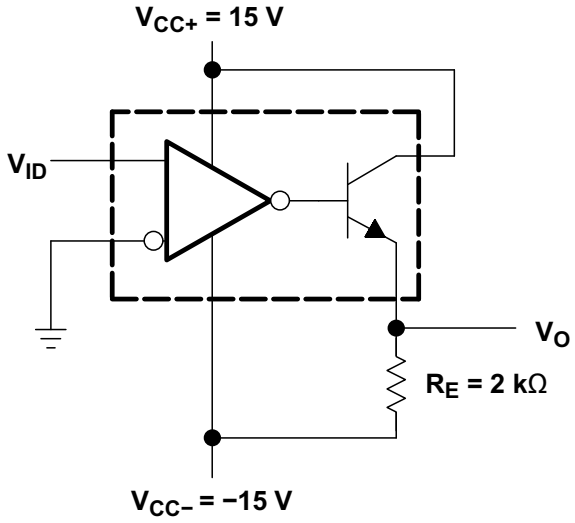
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Figure 10. Emitter Output Transfer Characteristic Test Circuit



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Figure 11. Test Circuit for Figure 3 and Figure 4



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Figure 12. Test Circuit for Figure 14 and Figure 15

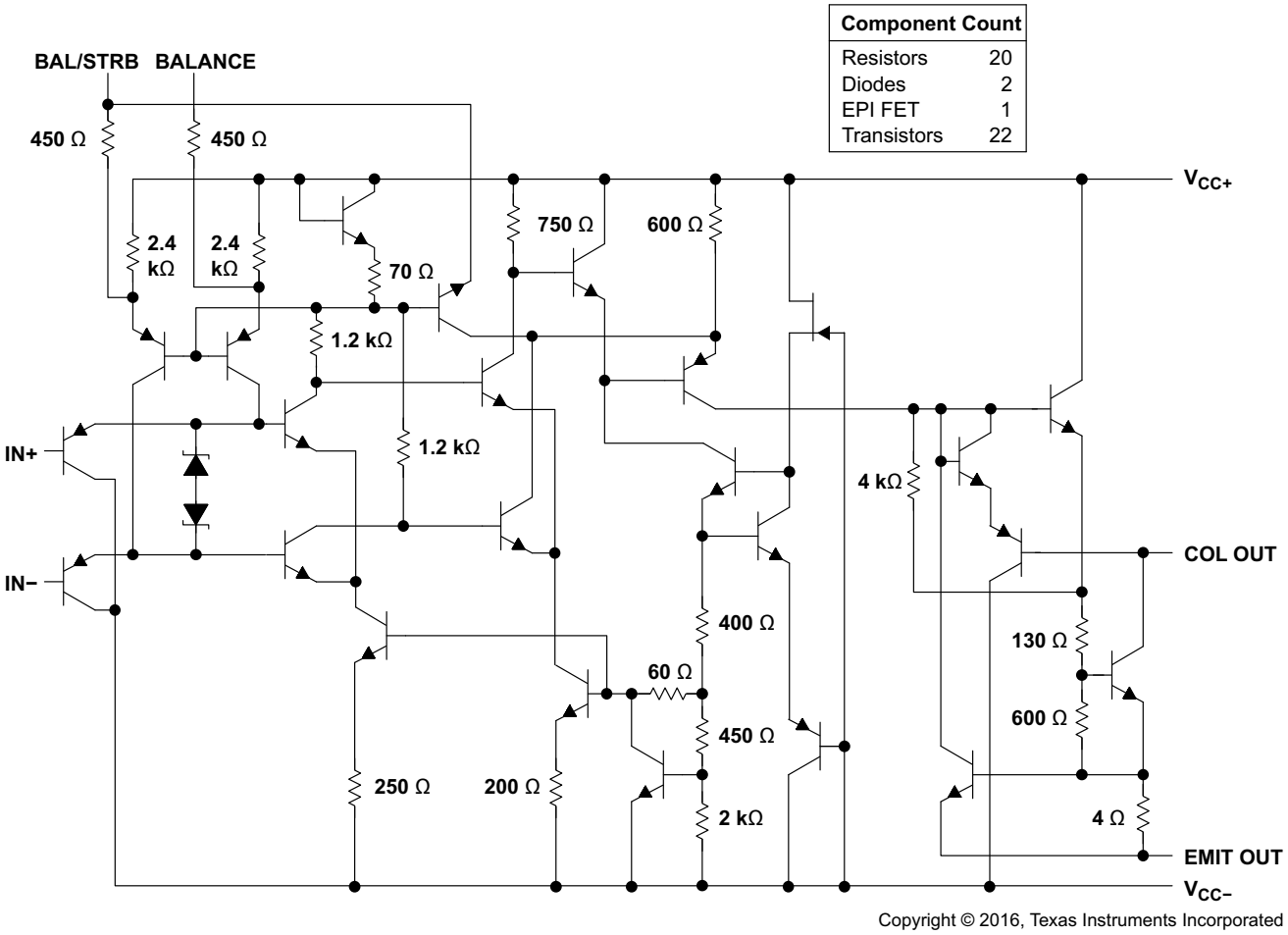
8 Detailed Description

8.1 Overview

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than legacy standard devices. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5-V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50 V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire ORed. The LM211 is identical to the LM111, except that its performance is specified over a −40°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C. The LM211Q has a temperature range of −40°C to +125°C.

8.2 Functional Block Diagram



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8.3 Feature Description

LMx11 consists of a PNP input stage to sense voltages near V_{CC-}. It also contains balance and strobe pins for external offset adjustment or trimming.

The input stage is followed by a very high gain stage for very fast response after a voltage difference on the input pins have been sensed.

This is then followed by the output stage that consists of an open collector NPN (pulldown or low-side) transistor. Unlike most open drain comparators, this NPN output stage has an isolated emitter from V_{CC-}, allowing this device to set the V_{OL} output value for collector output.

8.4 Device Functional Modes

8.4.1 Voltage Comparison

The LMx11 operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

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9 Application and Implementation

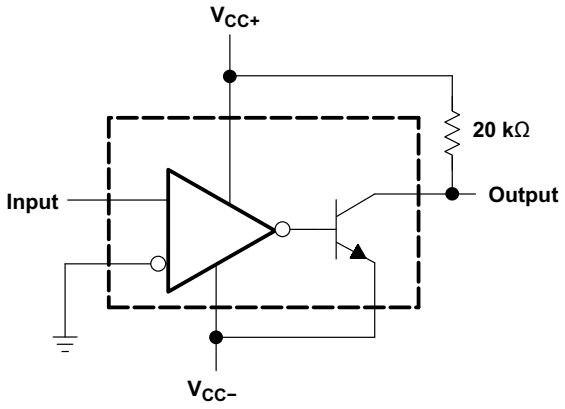
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

9.1 Application Information

A typical LMx11 application compares a single signal to a reference or two signals against each other. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMx11 optimal for level shifting to a higher or lower voltage.

9.2 Typical Application



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Figure 13. Zero-Crossing Detector

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	–15		13	V
V_{CC+}	Positive supply voltage			15	V
V_{CC-}	Negative supply voltage	–15			
I_{OUT}	Output current			20	mA

9.2.2 Detailed Design Procedure

When using LMx11 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

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9.2.2.1 Input Voltage Range

When choosing the input voltage range, consider the input common mode voltage range (V_{ICR}). Operation outside of this range can yield incorrect comparisons.

The following list describes the outcomes of some input voltage situations.

- When both IN– and IN+ are both within the common-mode range:
  - If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
  - If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
- When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
- When IN– and IN+ are both higher than common mode, the output is undefined

9.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 14 and Figure 15 show positive and negative response times with respect to overdrive voltage.

9.2.2.3 Output and Drive Current

Output current is determined by the pullup resistance and pullup voltage. The output current produces a output low voltage (V_{OL}) from the comparator, in which V_{OL} is proportional to the output current. Use Figure 5 to determine V_{OL} based on the output current.

The output current can also effect the transient response.

9.2.2.4 Response Time

The load capacitance (C_L), pullup resistance (R_{PULLUP}), and equivalent collector-emitter resistance (R_{CE}) levels determine the transient response. Equation 1 approximates the positive response time. Equation 2 approximates the negative response time. R_{CE} can be determine by taking the slope of Figure 5 in the linear region at the desired temperature, or by Equation 3.

$$\tau_P \cong R_{PULLUP} \times C_L \tag{1}$$

$$\tau_N \cong R_{CE} \times C_L \tag{2}$$

$$R_{CE} = \frac{V_{OL}}{I_{OUT}} \tag{3}$$

where

- V_{OL} is the low-level output voltage
- I_{OUT} is the output current

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9.2.3 Application Curves

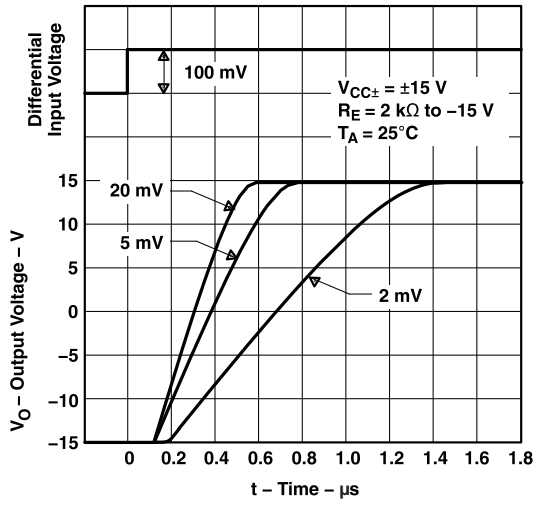


Figure 14. Output Response for Various Input Overdrives

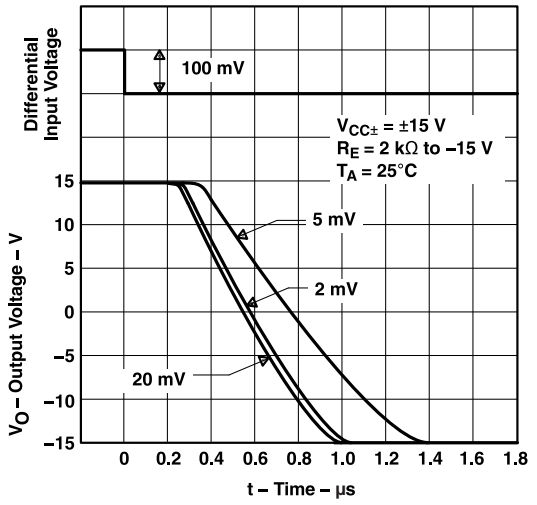
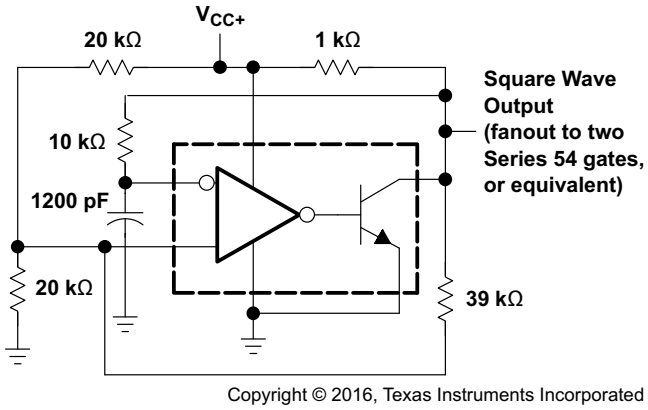


Figure 15. Output Response for Various Input Overdrives

9.3 System Examples

Figure 16 through Figure 33 show various applications for the LM111, LM211, and LM311 comparators.

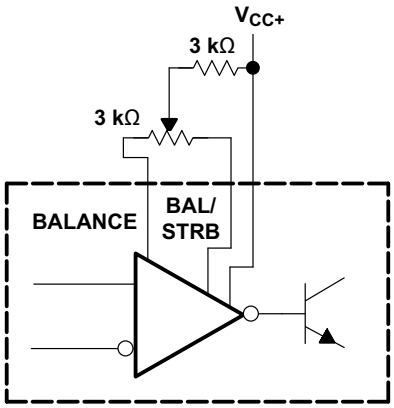


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Figure 16. 100-kHz Free-Running Multivibrator

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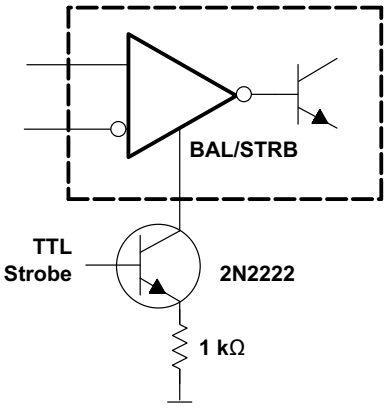
System Examples (continued)



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If offset balancing is not used, the BALANCE and BAL/STRB pins must be unconnected. It is also acceptable to short pins together.

Figure 17. Offset Balancing

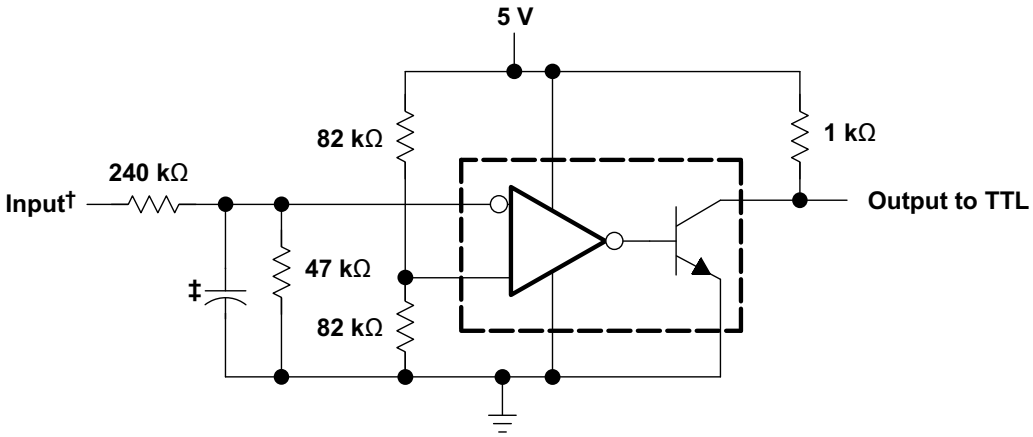


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Do not connect strobe pin directly to ground, because the output is turned off whenever current is pulled from the strobe pin.

Figure 18. Strobing

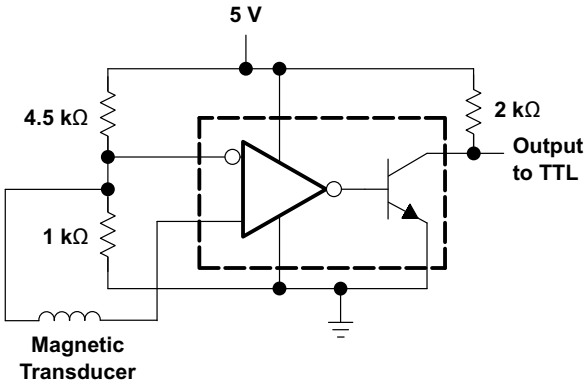
System Examples (continued)



† Resistor values shown are for a 0- to 30-V logic swing and a 15-V threshold.
‡ May be added to control speed and reduce susceptibility to noise spikes

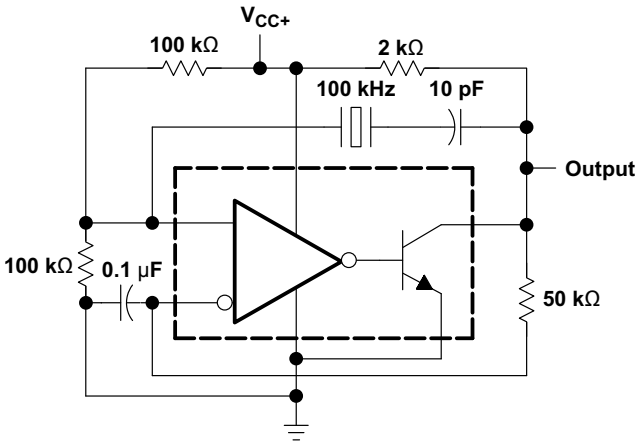
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Figure 19. TTL Interface With High-Level Logic



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Figure 20. Detector for Magnetic Transducer

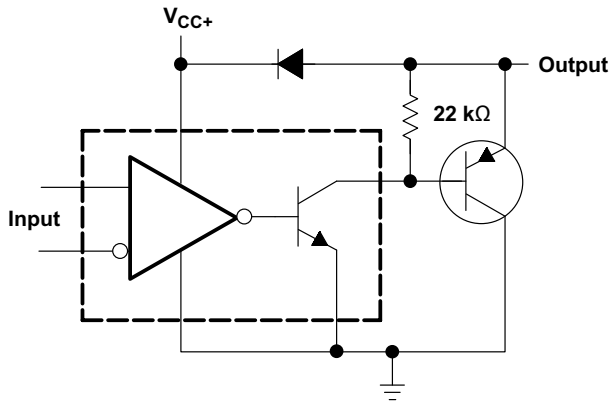


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Figure 21. 100-kHz Crystal Oscillator

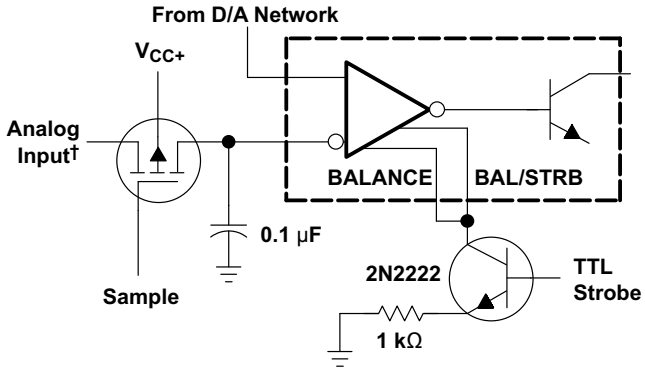
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System Examples (continued)



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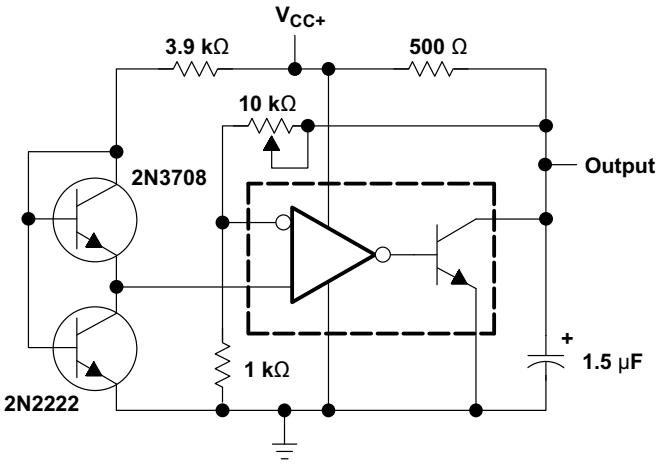
Figure 22. Comparator and Solenoid Driver



† Typical input current is 50 pA with inputs strobed off.

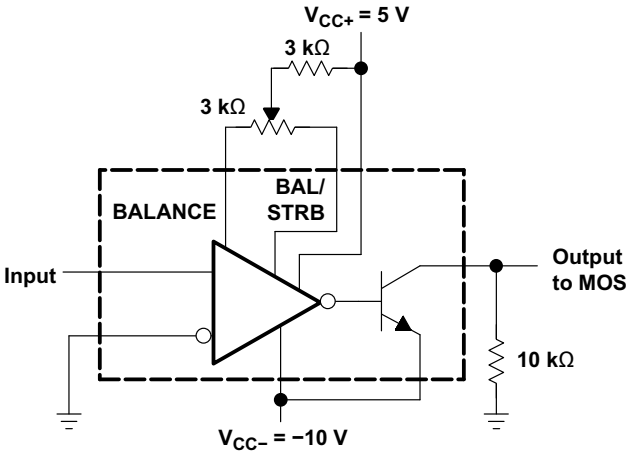
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Figure 23. Strobing Both Input and Output Stages Simultaneously



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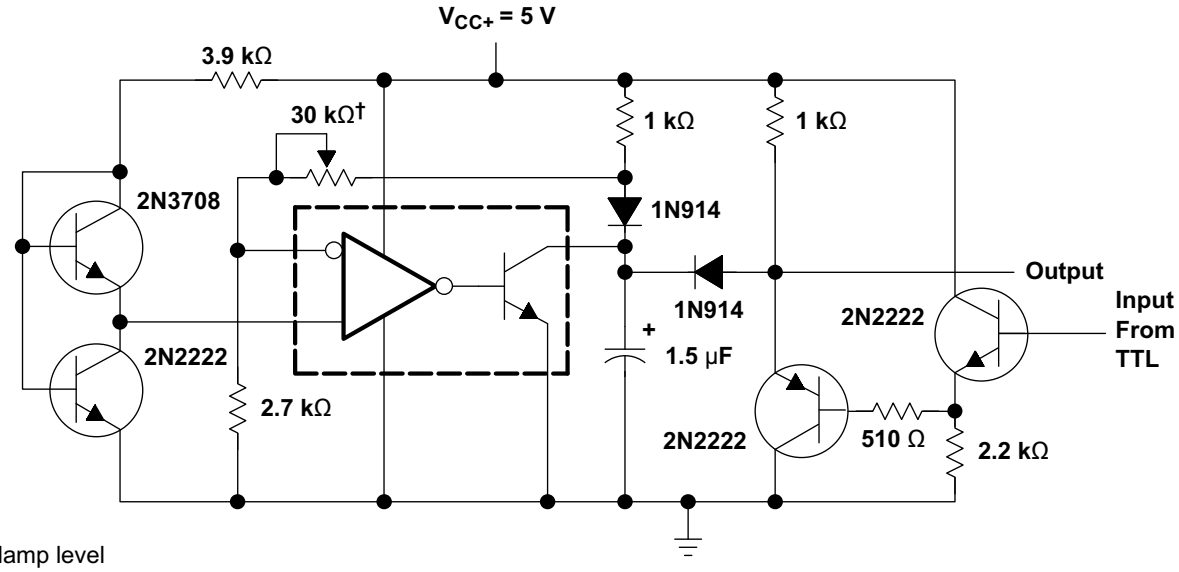
Figure 24. Low-Voltage Adjustable Reference Supply



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Figure 25. Zero-Crossing Detector Driving MOS Logic

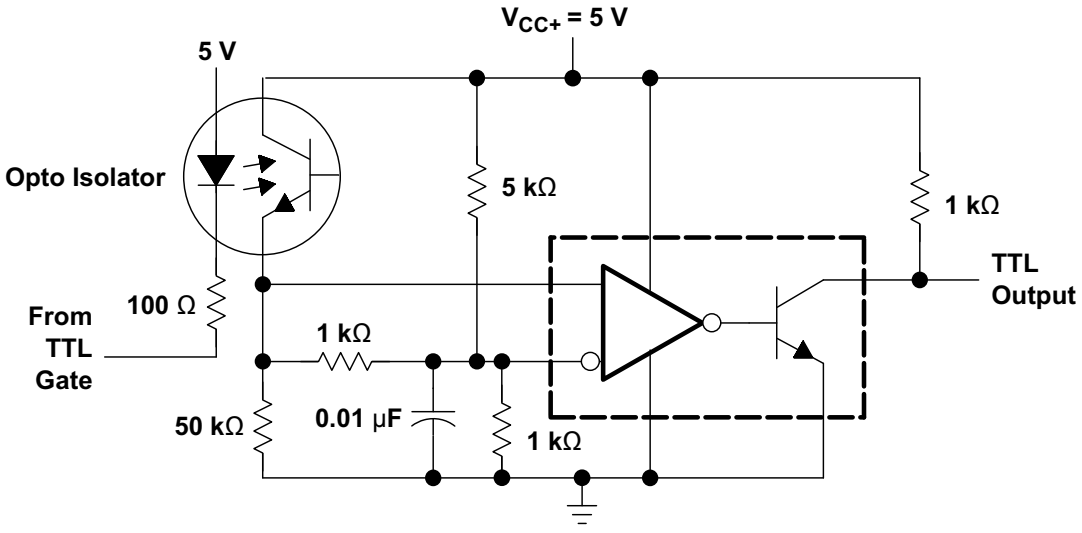
System Examples (continued)



† Adjust to set clamp level

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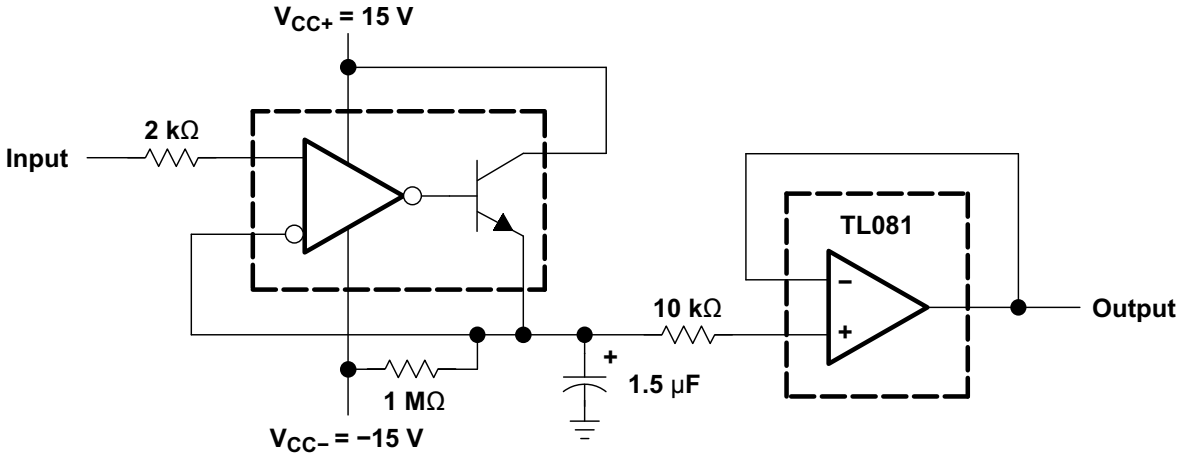
Figure 26. Precision Squarer



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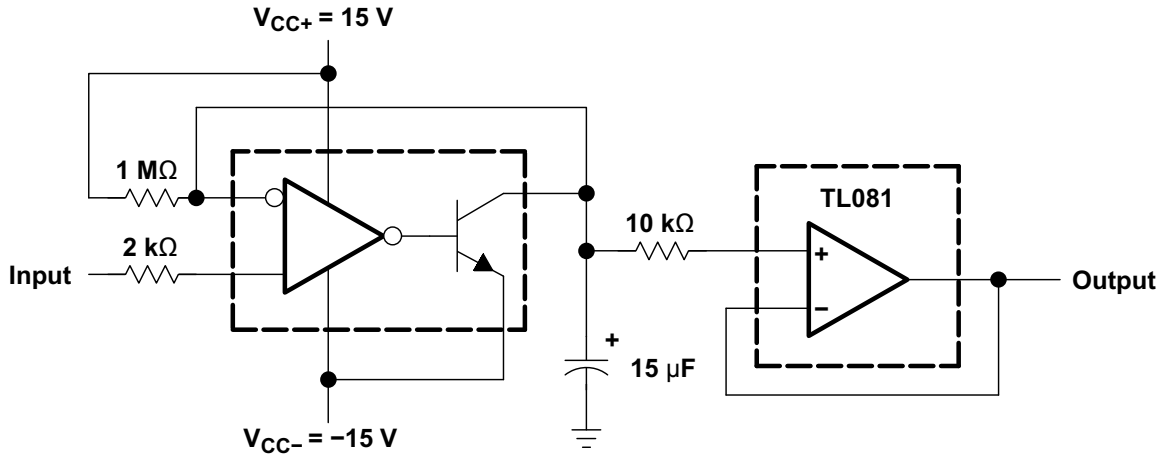
Figure 27. Digital Transmission Isolator

System Examples (continued)



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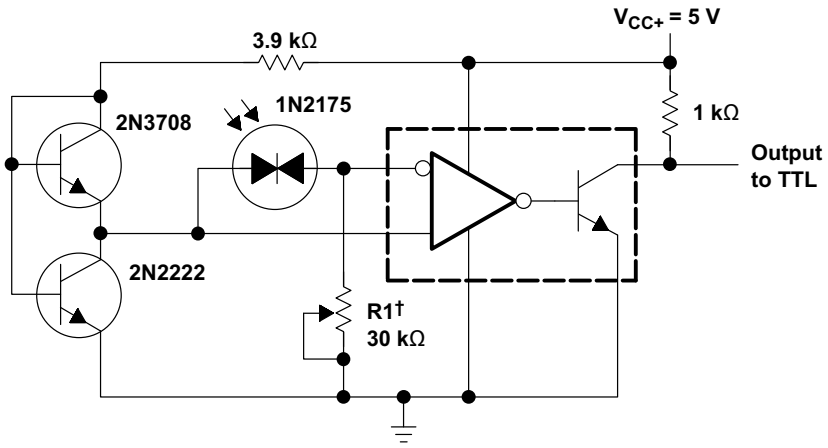
Figure 28. Positive-Peak Detector



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Figure 29. Negative-Peak Detector

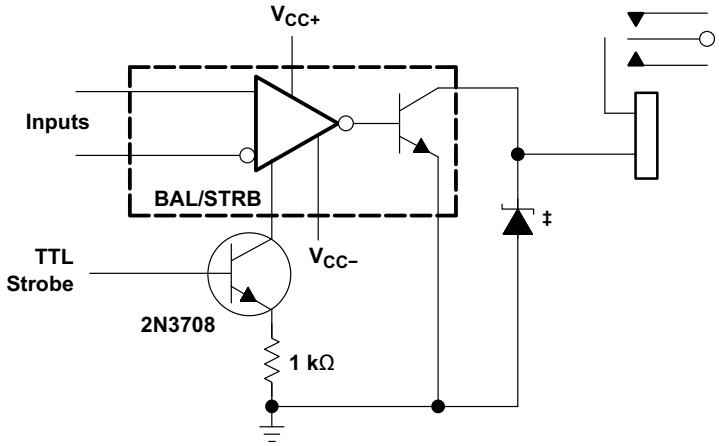
System Examples (continued)



† R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing dark current by an order of magnitude.

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Figure 30. Precision Photodiode Comparator

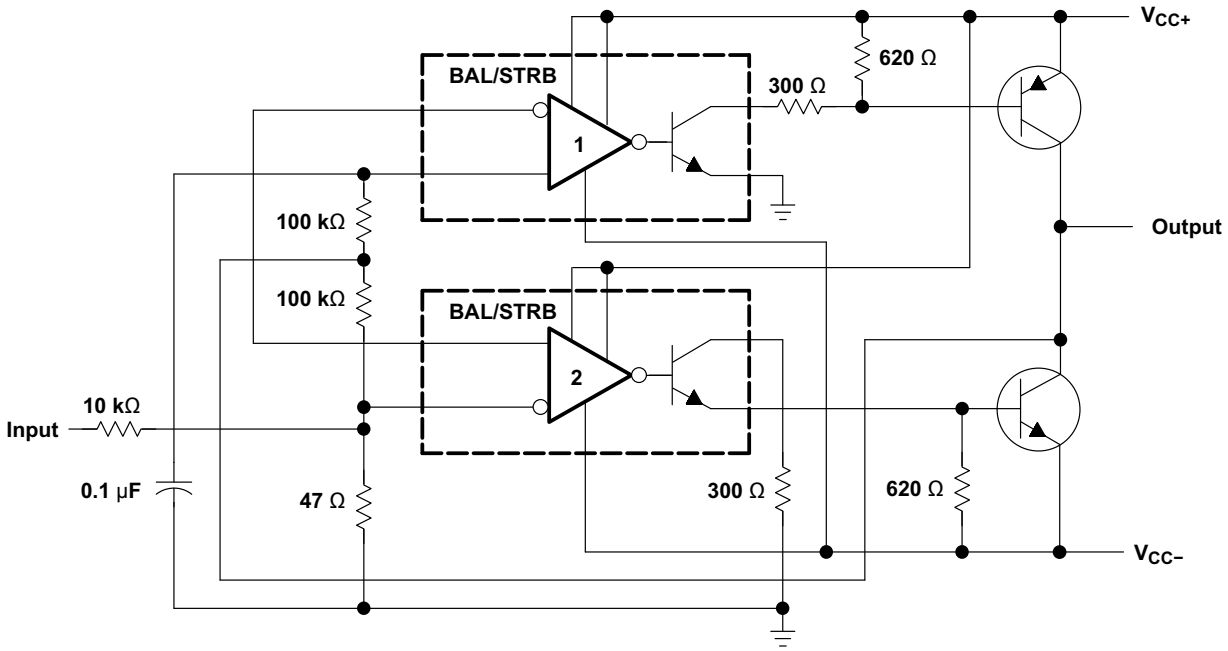


‡ Transient voltage and inductive kickback protection

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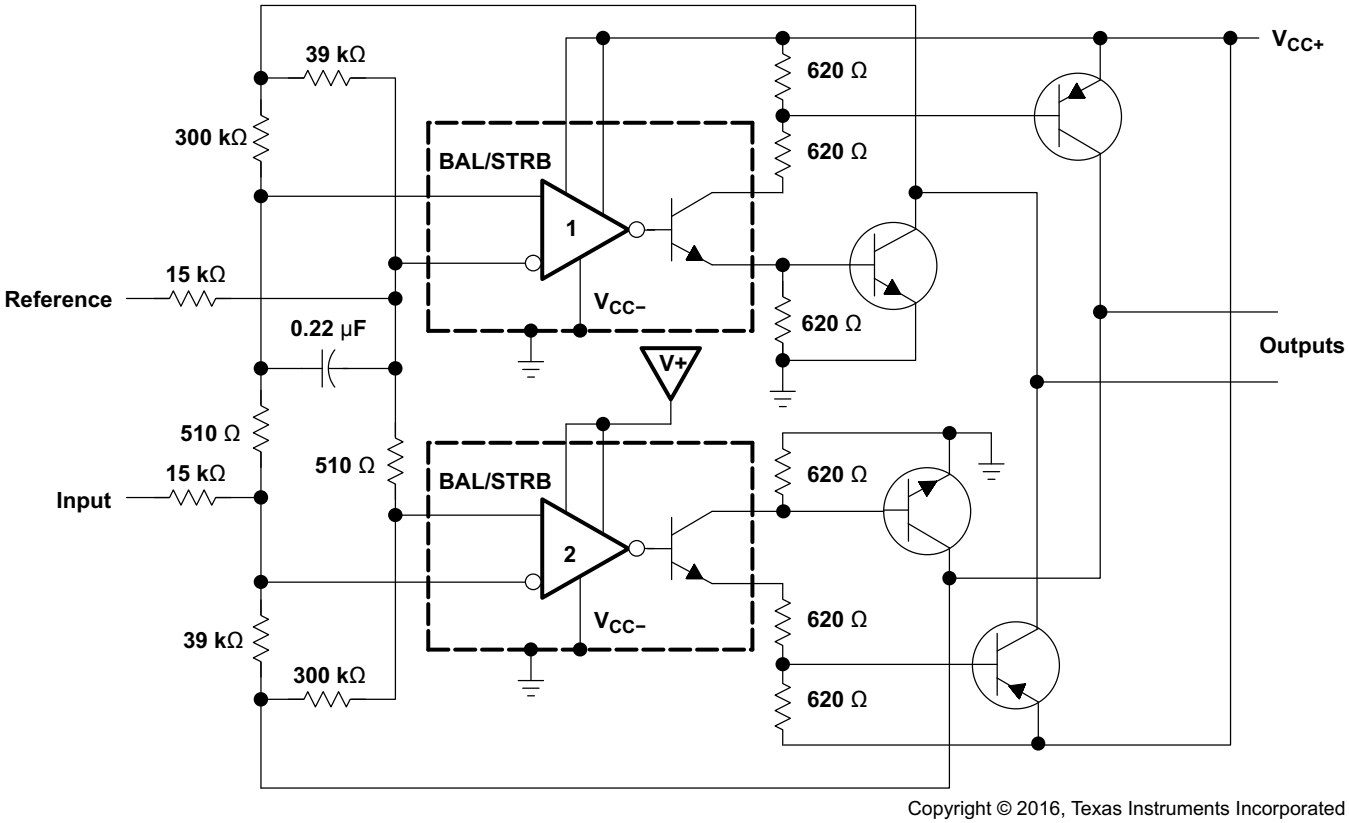
Figure 31. Relay Driver With Strobe

System Examples (continued)



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Figure 32. Switching Power Amplifier



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Figure 33. Switching Power Amplifiers

10 Power Supply Recommendations

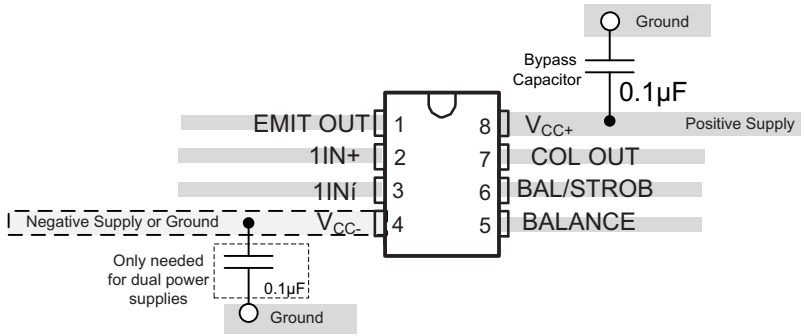
For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

11 Layout

11.1 Layout Guidelines

To create an accurate comparator application without hysteresis, maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. To achieve this accuracy, add a bypass capacitor between the supply voltage and ground. Place a bypass capacitor on the positive power supply and negative supply (if available).

11.2 Layout Example



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Figure 34. LMx11 Layout Example

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12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM111	Click here	Click here	Click here	Click here	Click here
LM211	Click here	Click here	Click here	Click here	Click here
LM311	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/10304BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10304BPA	Samples
LM111FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM111FKB	Samples
LM111JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM111JG	Samples
LM111JGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM111JGB	Samples
LM211D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM211	Samples
LM211P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	LM211P	Samples
LM211PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	LM211P	Samples
LM211PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L211	Samples
LM211PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L211	Samples
LM211PWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L211	Samples
LM211QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM211QDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM211QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM211QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	Samples
LM311D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM311DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	Samples
LM311P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM311P	Samples
LM311PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM311P	Samples
LM311PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
LM311PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	Samples
M38510/10304BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10304BPA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM211 :

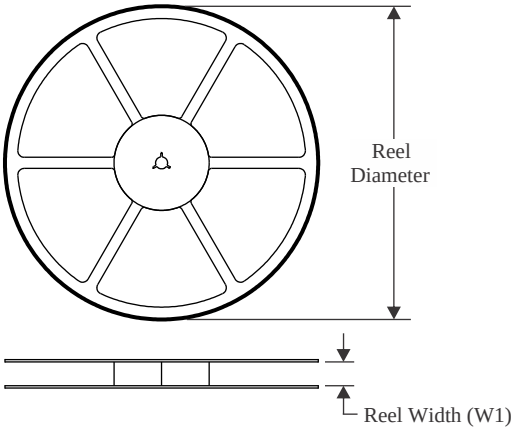
- Automotive : LM211-Q1
- Enhanced Product : LM211-EP

NOTE: Qualified Version Definitions:

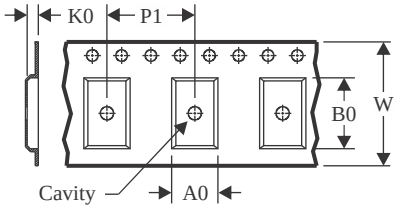
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

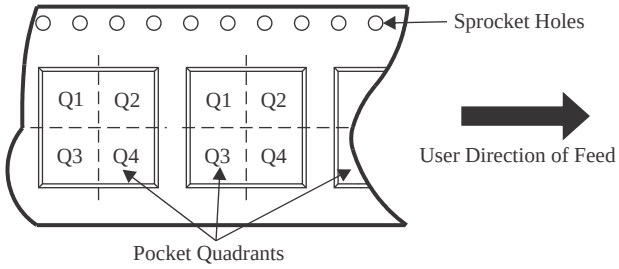


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

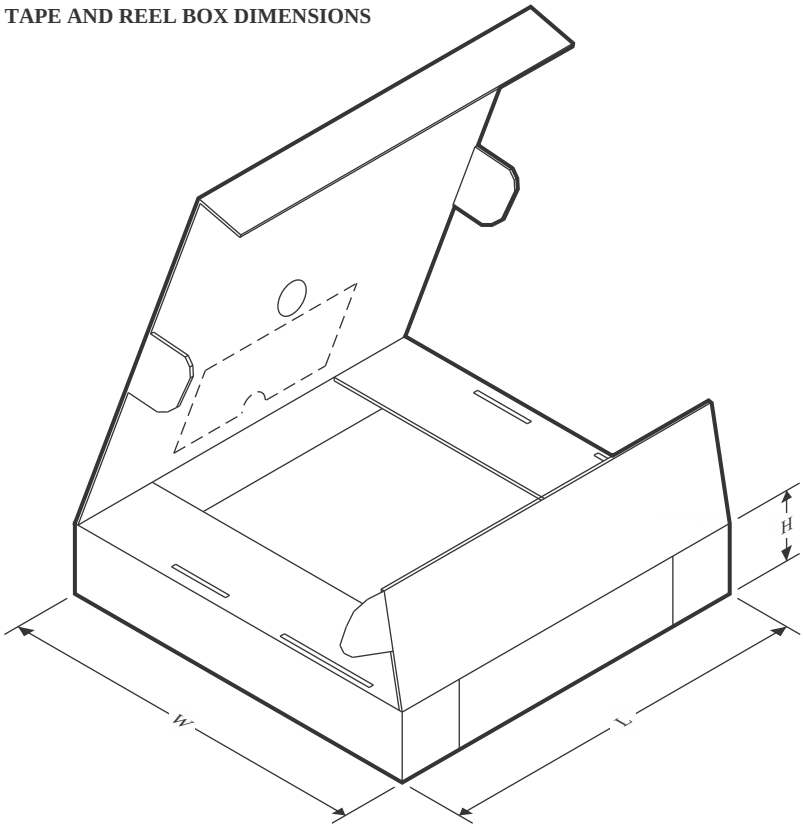
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM211DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM211PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM211QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM311DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM311PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM311PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

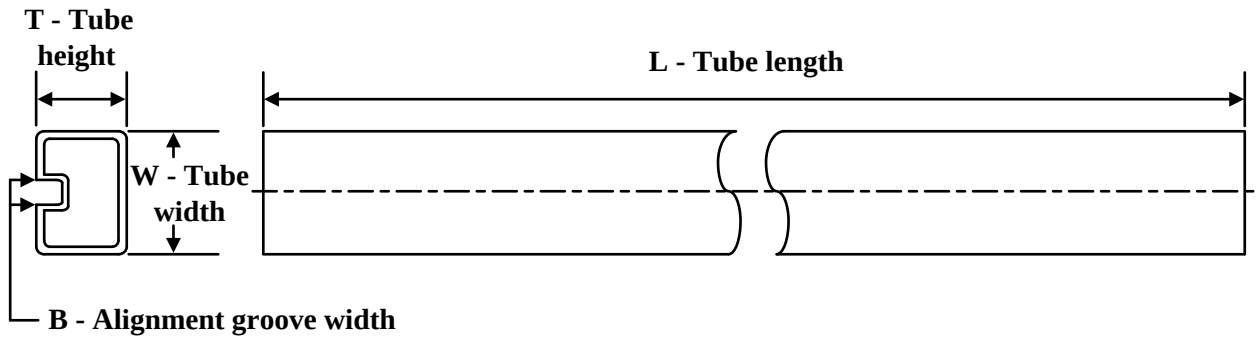
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM211DR	SOIC	D	8	2500	356.0	356.0	35.0
LM211DR	SOIC	D	8	2500	340.5	336.1	25.0
LM211DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM211DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM211PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM211QDR	SOIC	D	8	2500	340.5	336.1	25.0
LM311DR	SOIC	D	8	2500	356.0	356.0	35.0
LM311DR	SOIC	D	8	2500	340.5	336.1	25.0
LM311DR	SOIC	D	8	2500	364.0	364.0	27.0
LM311DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM311DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM311PSR	SO	PS	8	2000	356.0	356.0	35.0
LM311PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE

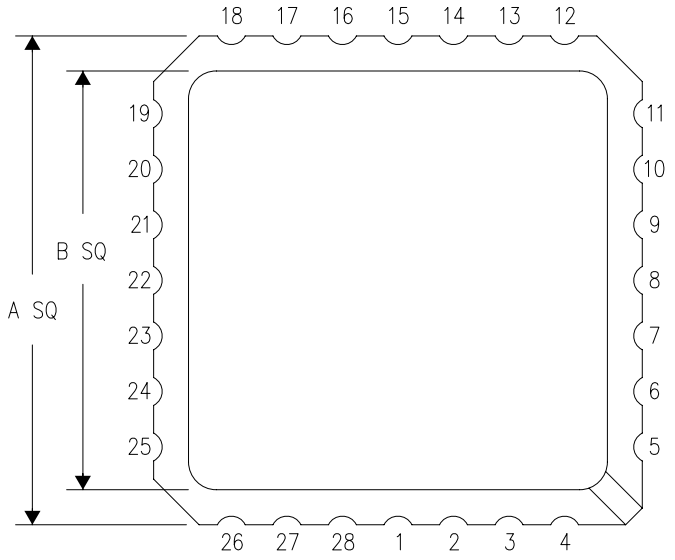


*All dimensions are nominal

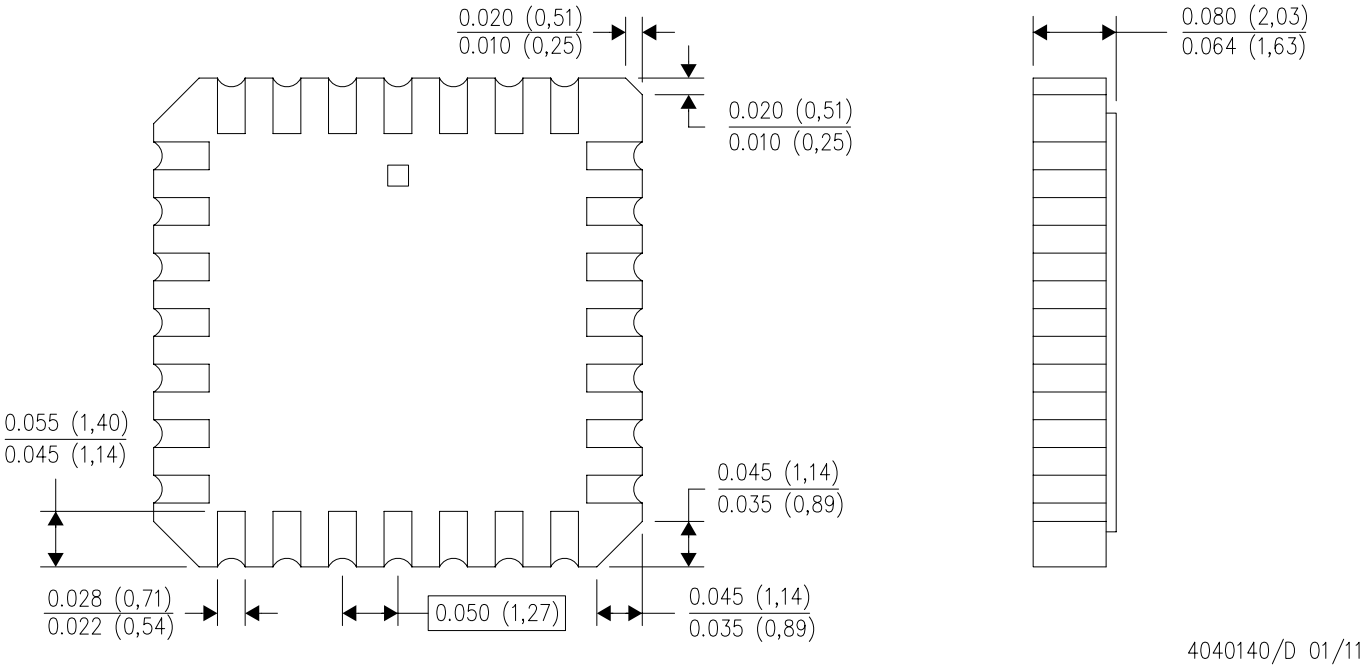
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM111FKB	FK	LCCC	20	1	506.98	12.06	2030	NA
LM211D	D	SOIC	8	75	506.6	8	3940	4.32
LM211D	D	SOIC	8	75	507	8	3940	4.32
LM211DE4	D	SOIC	8	75	507	8	3940	4.32
LM211DE4	D	SOIC	8	75	506.6	8	3940	4.32
LM211DG4	D	SOIC	8	75	507	8	3940	4.32
LM211DG4	D	SOIC	8	75	506.6	8	3940	4.32
LM211P	P	PDIP	8	50	506	13.97	11230	4.32
LM211PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM211PW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM211QD	D	SOIC	8	75	507	8	3940	4.32
LM211QDG4	D	SOIC	8	75	507	8	3940	4.32
LM311D	D	SOIC	8	75	507	8	3940	4.32
LM311D	D	SOIC	8	75	506.6	8	3940	4.32
LM311DE4	D	SOIC	8	75	506.6	8	3940	4.32
LM311DE4	D	SOIC	8	75	507	8	3940	4.32
LM311DG4	D	SOIC	8	75	507	8	3940	4.32
LM311DG4	D	SOIC	8	75	506.6	8	3940	4.32
LM311P	P	PDIP	8	50	506	13.97	11230	4.32
LM311PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM311PW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM311PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

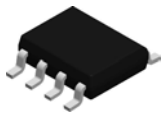


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

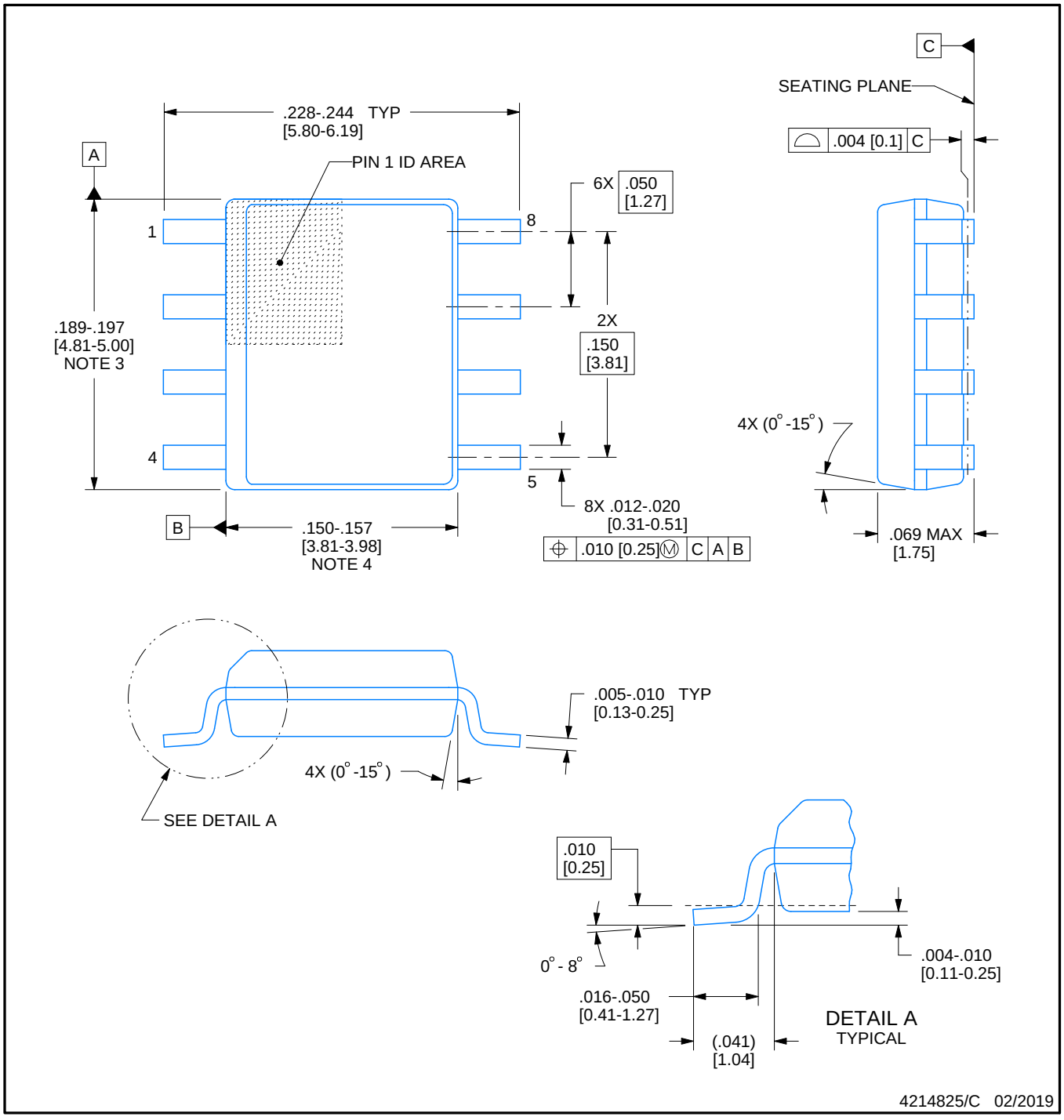


PACKAGE OUTLINE

D0008A

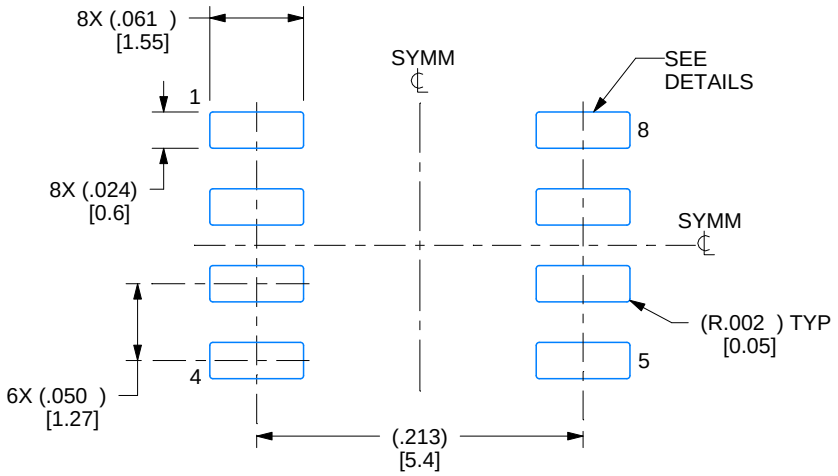
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

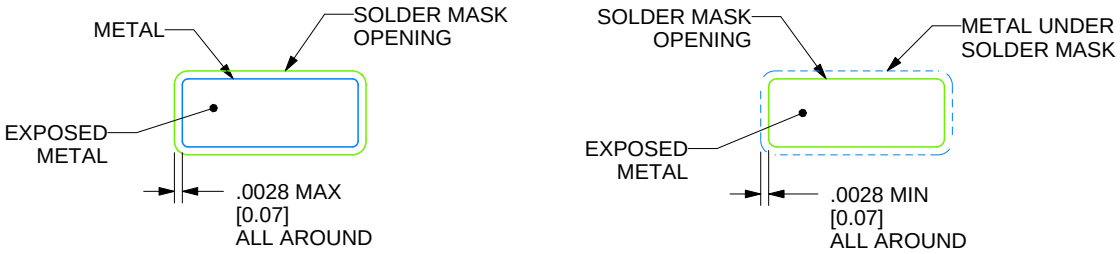


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

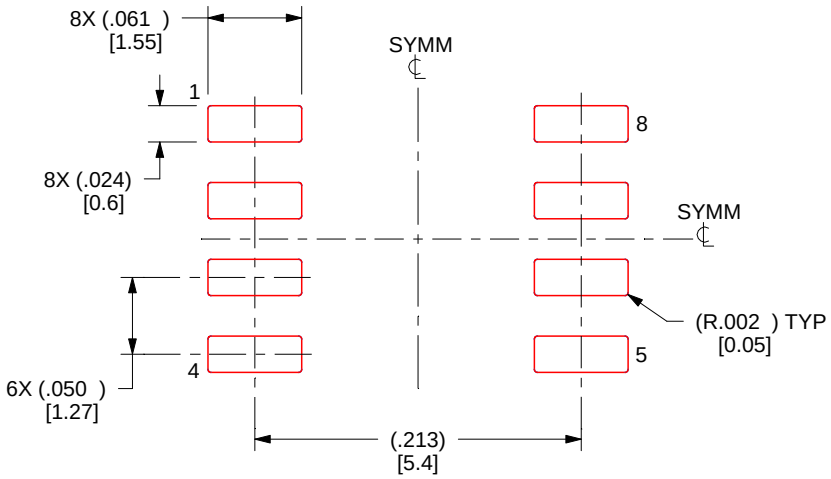
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

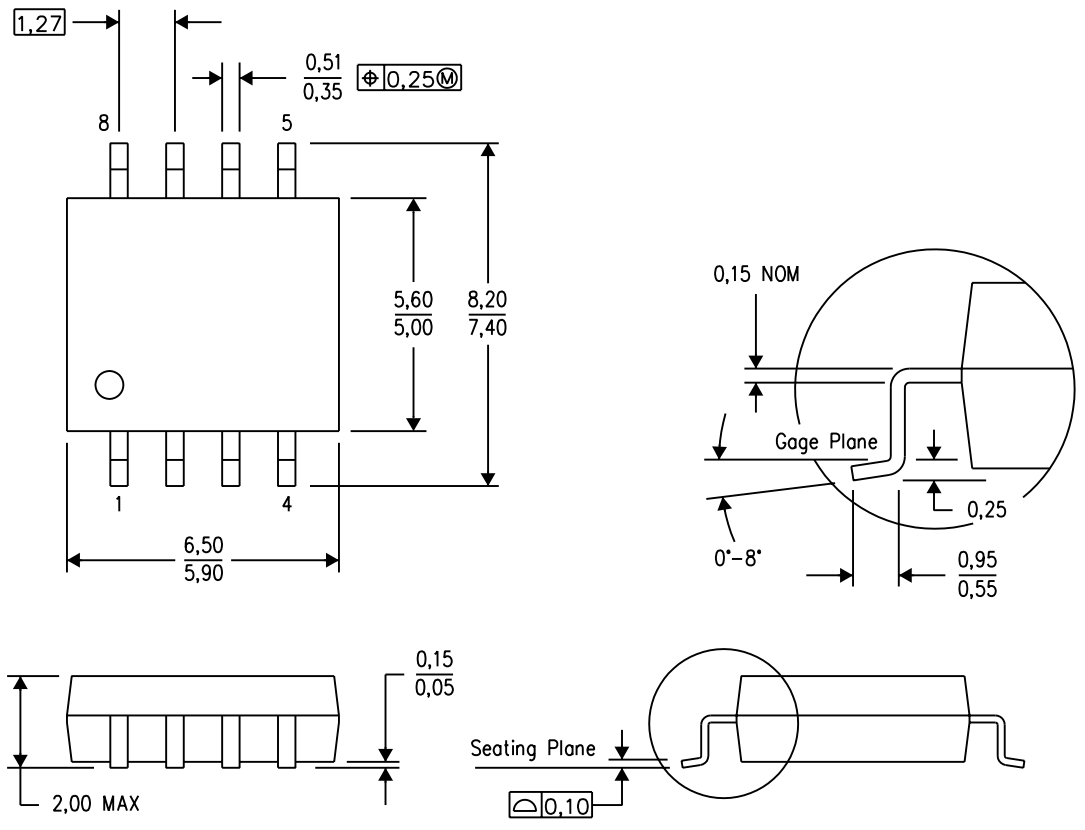
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

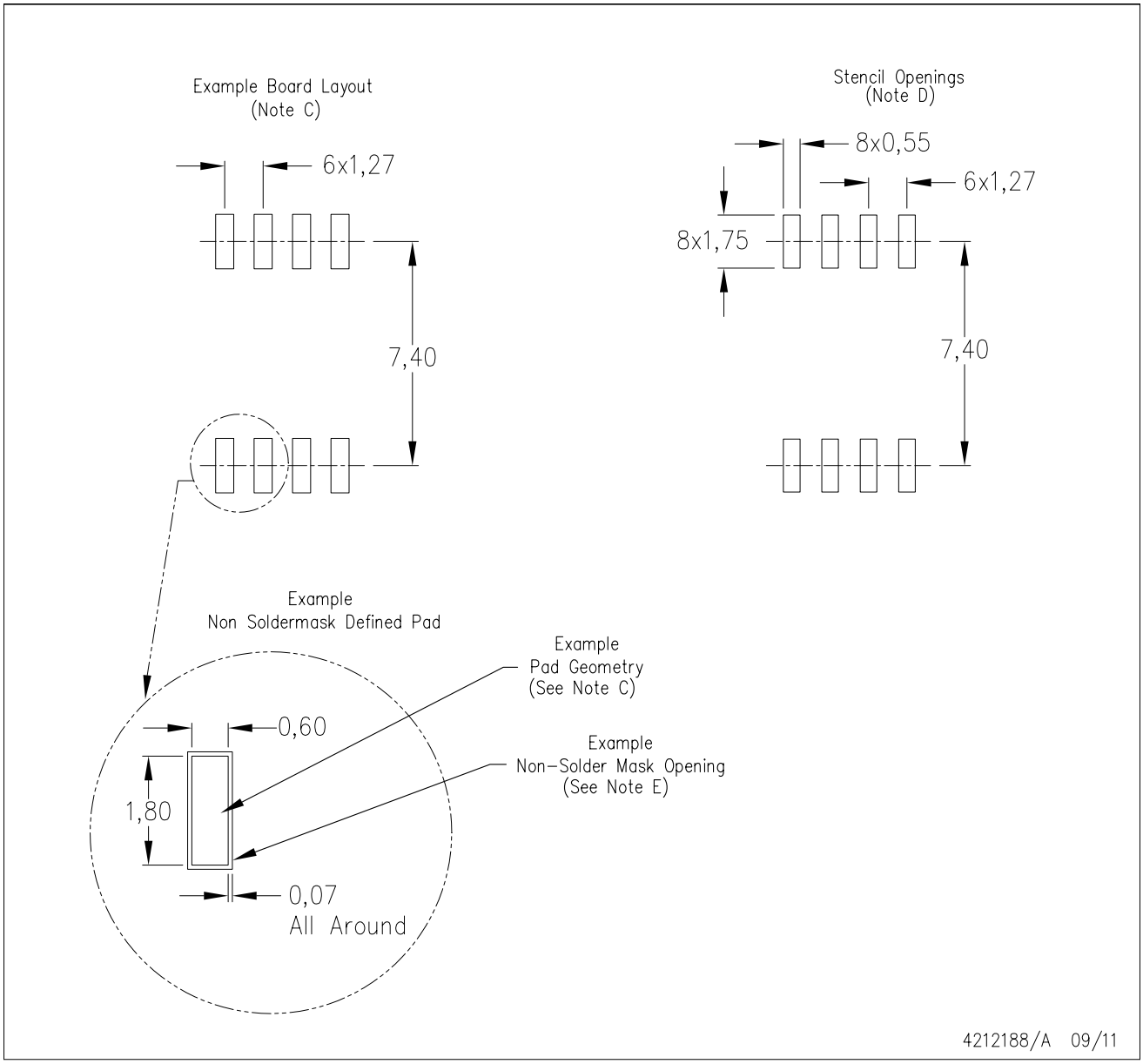
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

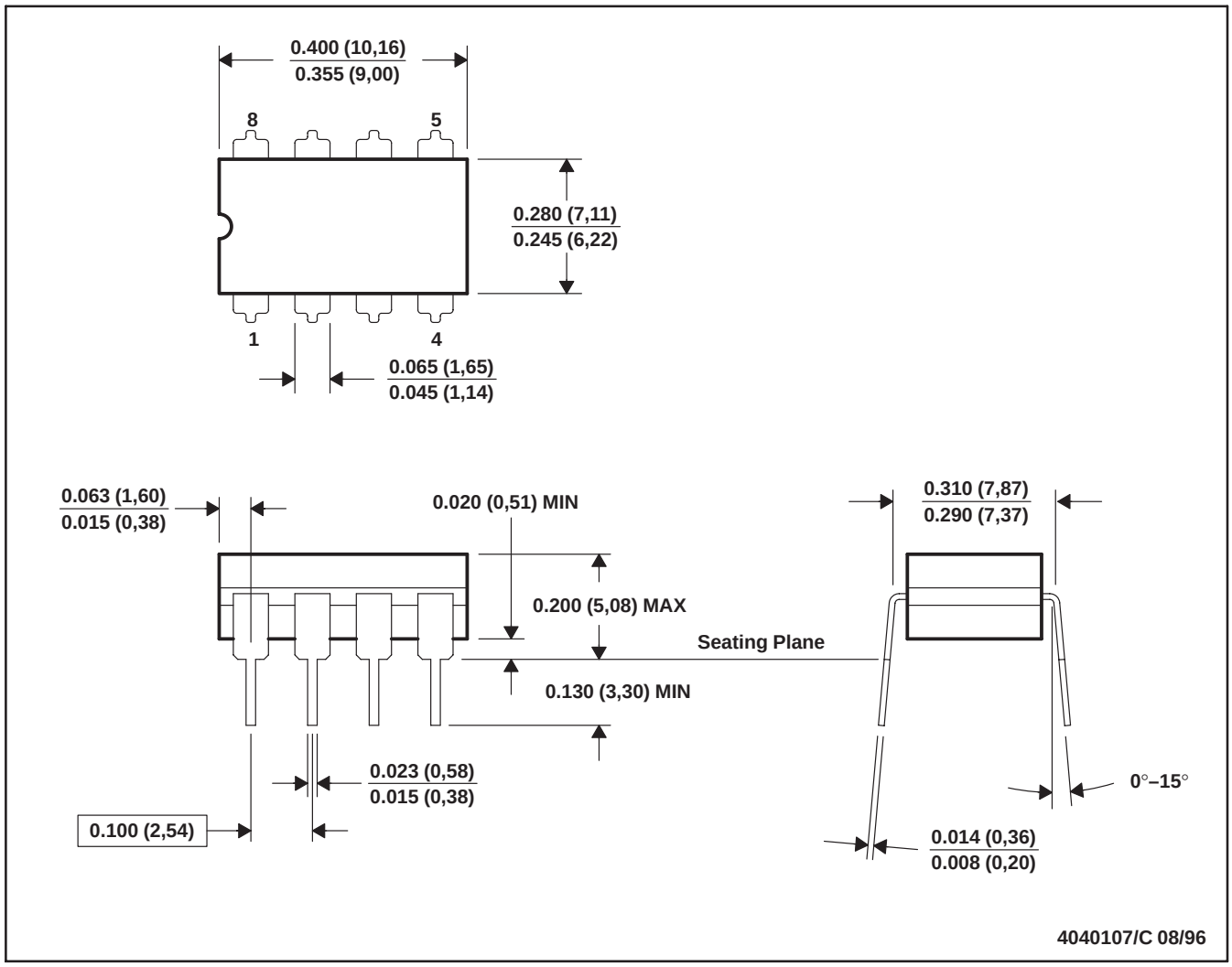
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

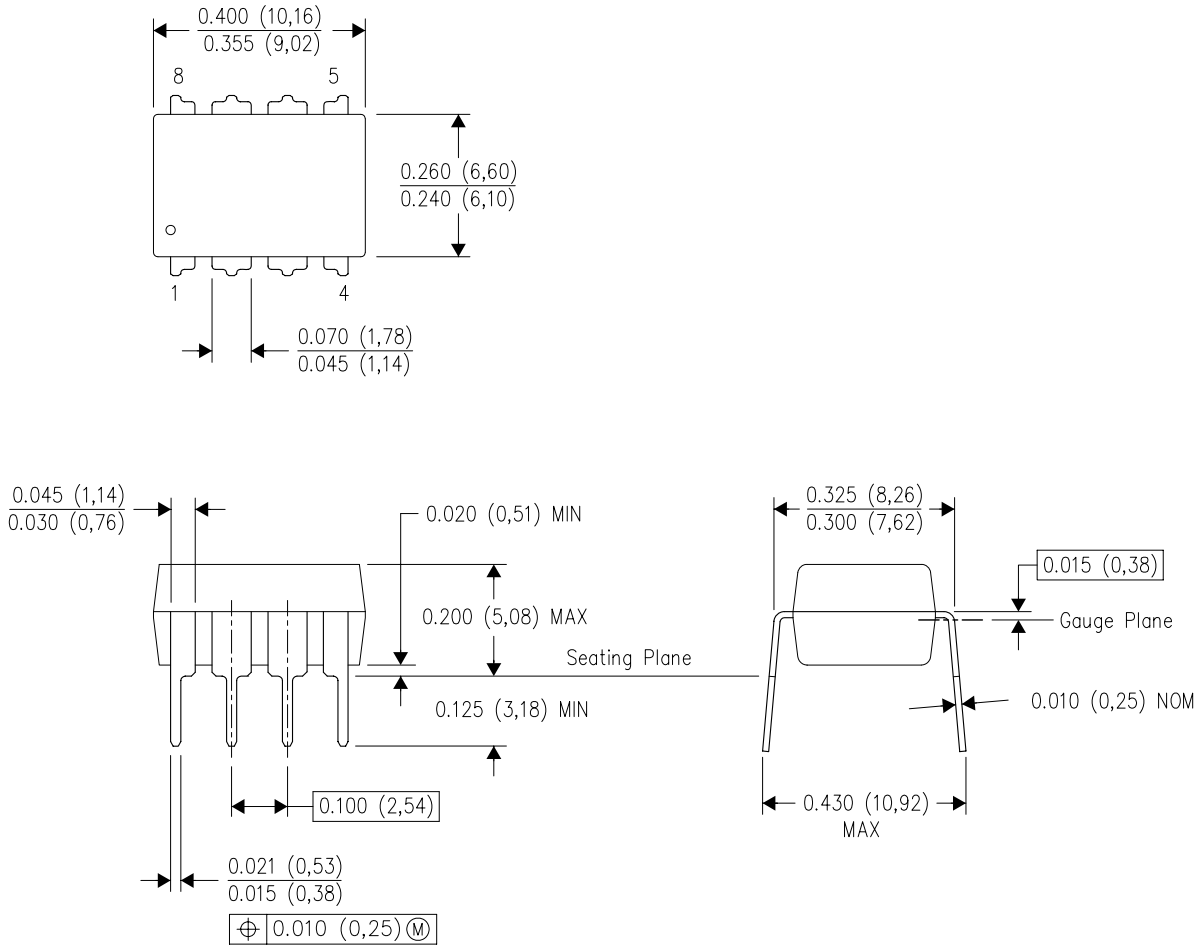
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



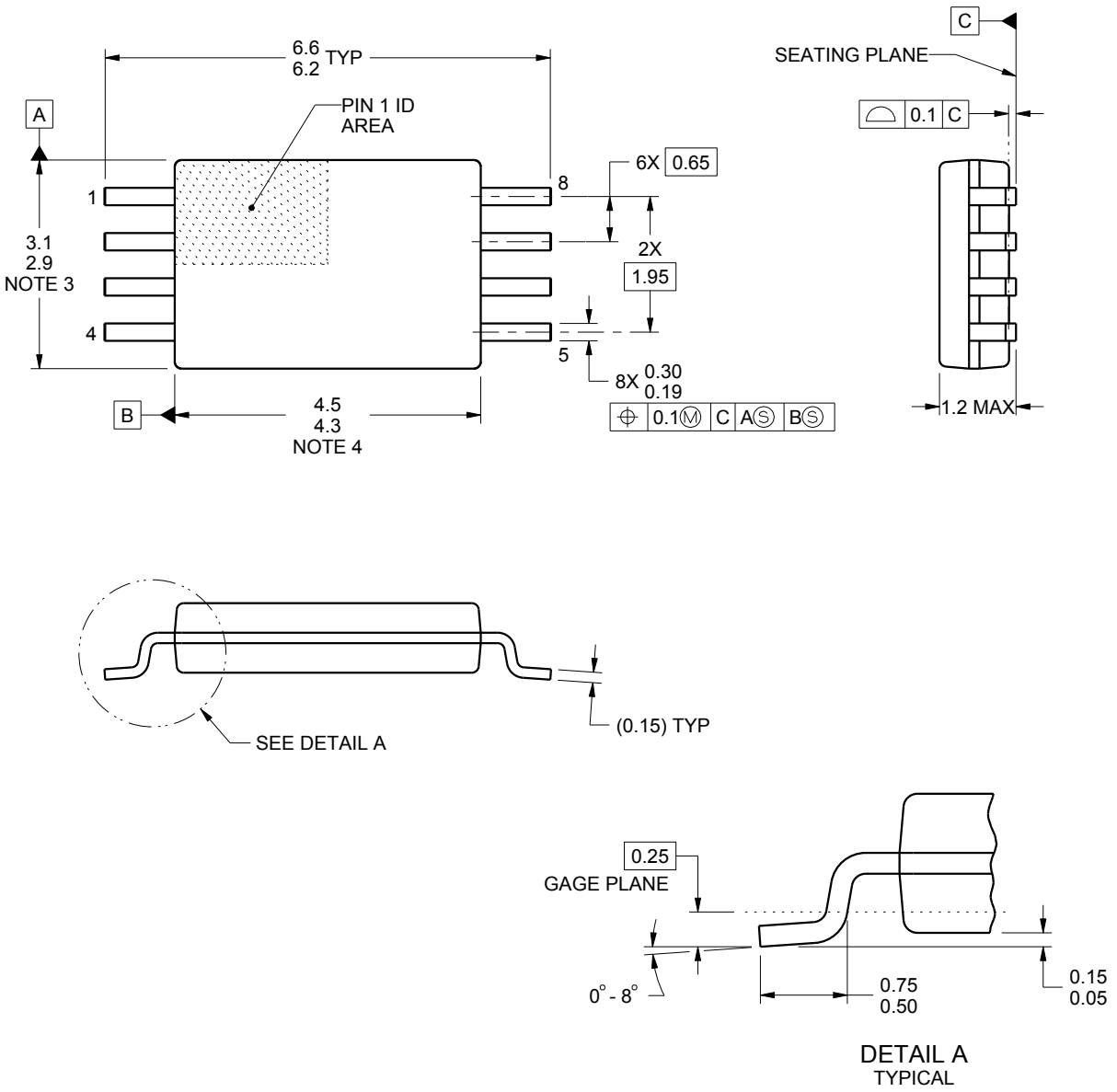
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

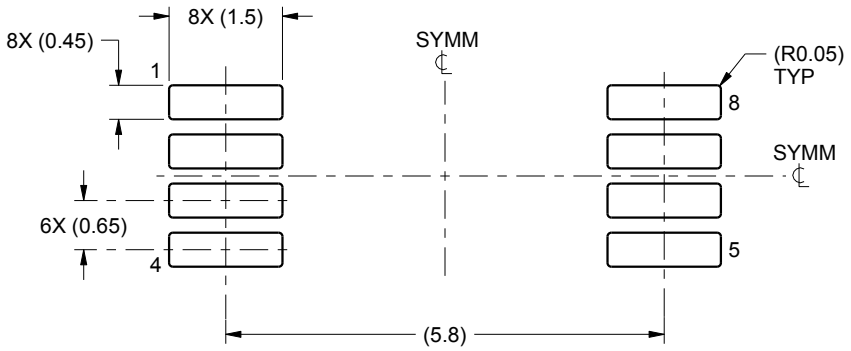
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

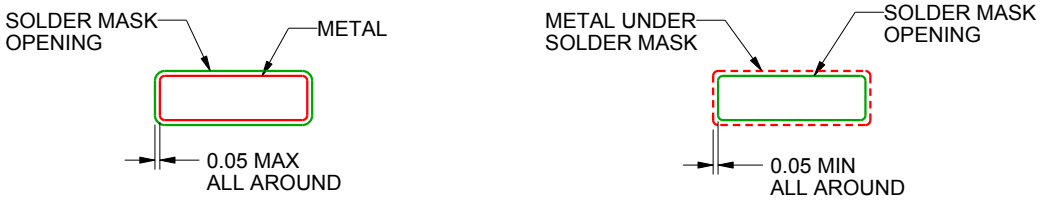


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

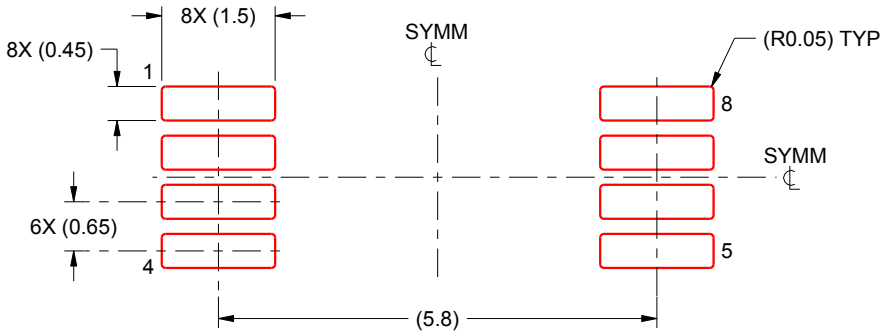


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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