PR8224/PR8224H

High Voltage Green Mode Power Switch

GENERAL DESCRIPTION

PR8224/PR8224H is a highly intergrated current mode PWM power switch. It built in patent High voltage startup, optimized for high performance, exhibit extra low standby power consumption (<50mW).

PWM switching frenquency at normal operation is internally fixed. At no load or light load condition, It operates in hiccup mode to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved. Less than 50mW standby power consumption and very high conversion efficiency is thus achieved. Patent high voltage startup is implemented in PR8224/PR8224H, which features with short startup time and extra low standby current.

PR8224/PR8224H offers rich protection such as: auto-recovery including Cycle-by Cycle current limiting (OCP), over load protection (OLP), VDD under voltage lockout (UVLO), and over temperature protection (OTP). It also provides the protection with latched shut down including VDD over voltage protection. Excellent EMI performance is achieved with PR8224/PR8224H proprietary frequency hiccup technique. The frequency at below 22KHZ is minimized to avoid audible noise during operation.

FEATURES

- Built-in patent High Voltage Startup
- Patent High voltage startup technique
- Extra Low Standby (<50mW)
- Power on Soft Startup
- Frequency spreading to Minimize EMI
- Audible Noise Free Operation
- Fixed 65KHz/130KHz Switching Frequency
- Comprehensive Protection
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Cycle-by-cycle Over Current Protection (OCP)
  - Overload Protection (OLP) with Auto-recovery
  - Over Temperature Protection (OTP) with Latch Shut Down
  - VDD Over Voltage Protection (OVP) with Latch Shut Down

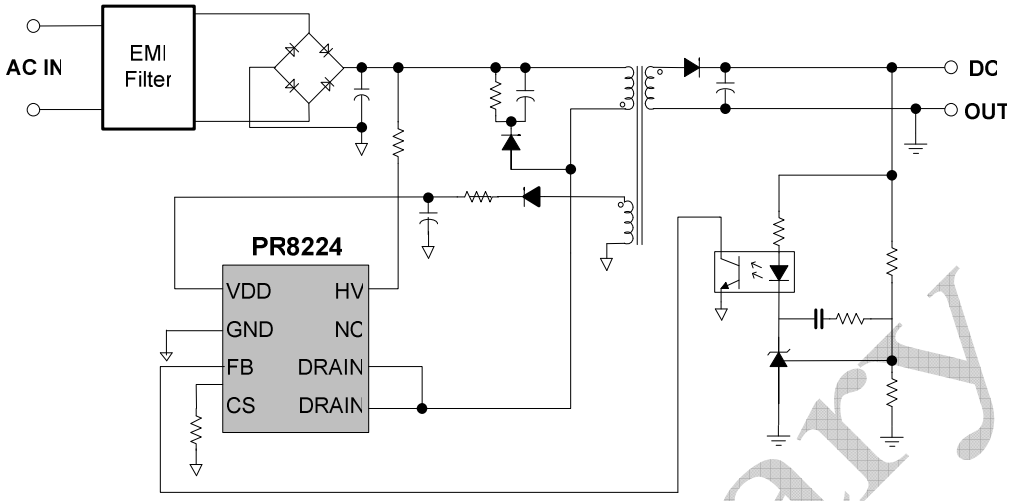
APPLICATIONS

Offline AC/DC Flyback Converter For

- AC/DC Adapter
- PDA Power Supplies
- Digital Cameras and Camcorder Adapter
- VCR, SVR, STB, DVD&DVCD Player SMPS
- Set-Top Box Power
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

TYPICAL APPLICATION

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Output Power Table

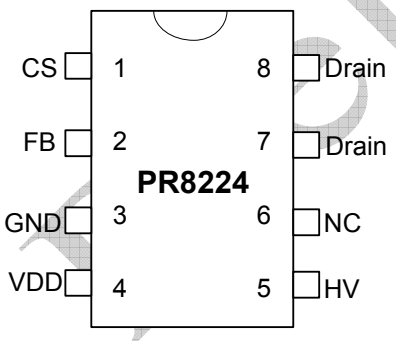
Product	230VAC+/-15%	90-265VAC
	Adapter[1]	Adapter[1]
PR8224/PR8224H	14W	12W

Notes: 1. Maximum pratical continuous power in an Adapter design with sufficient drain pattern as a heat sink, at 40℃ ambient.

GENERAL INFORMATION

Pin Configuration

The PR8224/PR8224H is offered in DIP8 package, shown as below.



Absolute Maximum Ratings

Parameter	Value
Drain Voltage (off state)	-0.3 to BVdss
High-Voltage Pin, HV	-0.3 to 500 V
VDD DC Supply Voltage	-0.3 to 30V
VDD Zener Clamp Voltage[Note]	VDD_Clamp+0.1V
VDD DC Clamp Current	10 mA
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260℃

Note: VDD_Clamp has a nominal value of 30V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device's reliability.

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TERMINAL ASSIGNMENTS

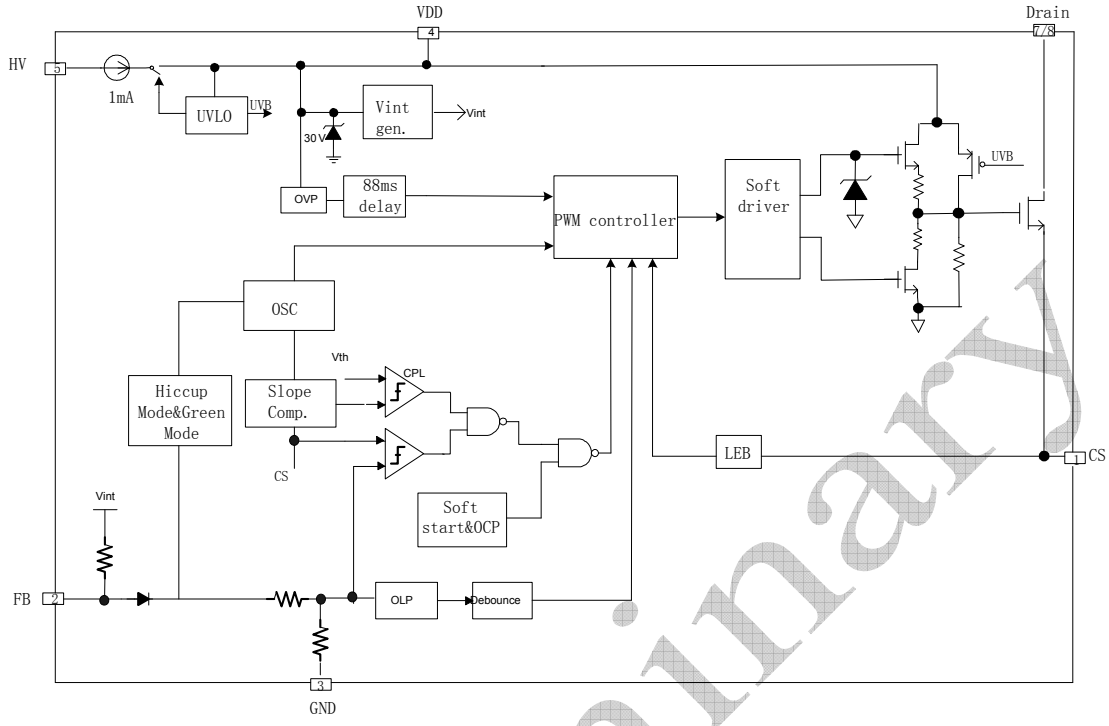
Pin Num	Pin Name	I/O	Description
1	CS	I	Current sense input.
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin.
3	GND	P	Ground
4	VDD	P	Power Supply
5	HV	P	Connected to the line input or bulk capacitor via resistors for startup.
7, 8	Drain	O	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transtormer.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min/Max	Unit
VDD	VDD Supply Voltage	10.5 to 23.5	V
T_A	Operating Ambient Temperature	-20 to 85	℃

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BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

(TA = 25℃, VDD=16V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
IHV	Supply current from HV pin	VDD=2V, HV=100V		1		mA
Leakage	HV pin leakage current after startup	VDD=18V, HV=500V			10	μA
Supply Voltage (VDD)						
Ist	VDD Start up Current	VDD=UVLO_OFF-1 V, measure leakage current into VDD		5	20	μA
I_VDD_Operation	Operation Current	V_{FB}=3V		1.5		mA
	Burst Mode Current	VDD=15V, V_{FB}=1V		0.8		mA
UVLO(ON)	VDD Under Voltage Lockout Enter		6	7	8	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		12.5	13.5	14.5	V
Vpull_up	Pull-up PMOS active			13		V
VDD_Clamp		I_{VDD}=10mA	28	29.5	31	V
OVP_ON	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	24	26	28	V
Vlatch_recovery	Auto release threshold voltage			5		V
Vlatch_release	Latch release threshold			4.2		V
Feedback Input Section(FB Pin)						
VFB_Open	VFB Open Loop Voltage		3.9	4.2		V
Avcs	PWM input gain ΔVFB/ ΔVCS			1.71		V/V
Maximum duty cycle	Max duty cycle @ VDD=18,VFB=3V,VCS=0.3 V		75	80	85	%
Vref_green	The threshold enter green mode			1.4		V
Vref_HH	The threshold exit hiccup mode			0.67		V
Vref_HL	The threshold enter hiccup mode			0.57		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		250		μA
VTH_PL	Power Limiting FB Threshold Voltage			3.5		V
TD_PL	Power limiting Debounce Time		80	88	96	mSec
Z_{FB}_IN	Input Impedance			16		Kohm
Current Sense Input(CS Pin)						
SST	Soft start time			5		ms
T_blanking	Leading edge blanking time			320		ns

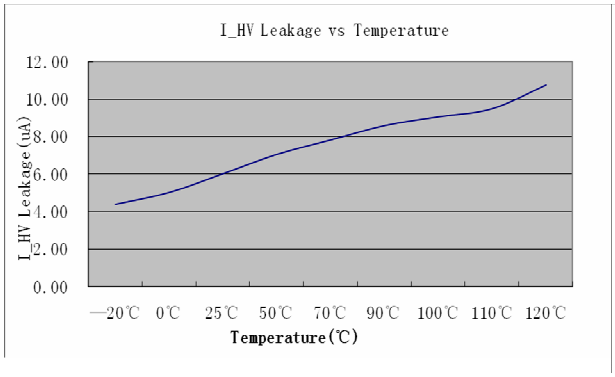
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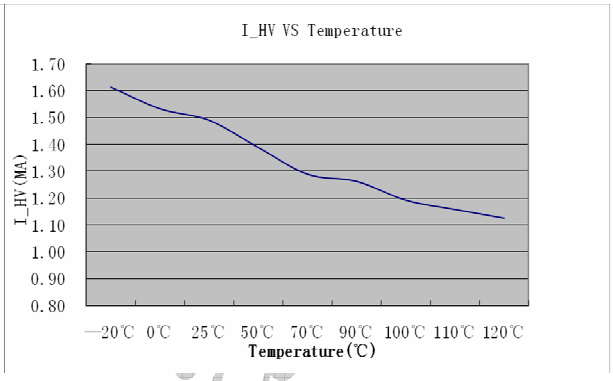
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Z_{SENSE}_IN	Input Impedance			40		Kohm
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		120		nSec
V_{TH}_OC	Current Limiting Threshold Voltage with zero duty cycle		0.72	0.75	0.78	V
Vocp_clamping	Current limiting threshlod at maximum Duty			0.90		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency @ FB=3V	PR8224	60	65	70	KHz
		PR8224H	110	130	150	
△f_OSC	Frequency jittering			+/-4		%
F_shuffling	Shuffling frequency			32		Hz
△f_Temp	Frequency Temperature stability			2		%
△f_VDD	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			22		KHz
MOSFET Section						
BVdss	MOSFET Drain-Source Breakdown voltage		600			V
Rdson	Static, Id=1.0A			5	5.8	Ω
On Chip OTP						
OTP	Over temperature protection trip point with Recommended PCB layout.			145		℃

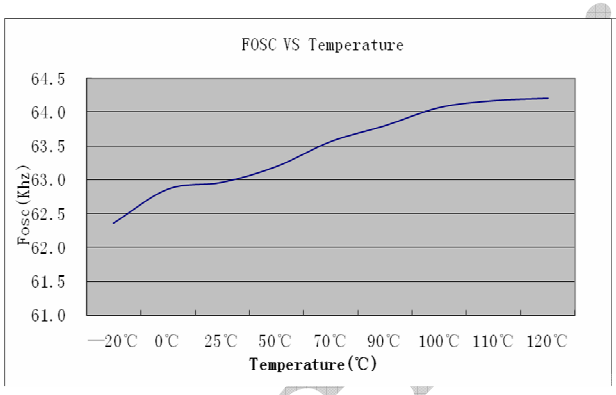
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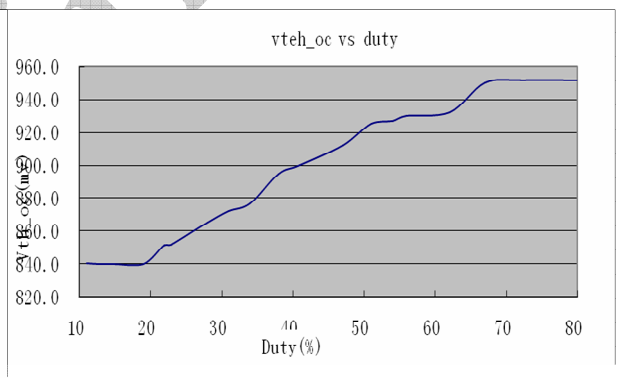
CHARACTERIZATION PLOTS

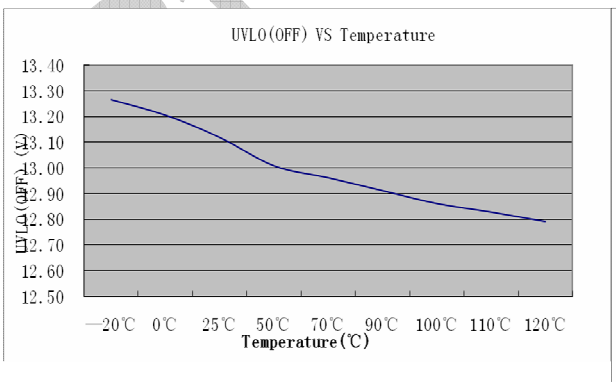
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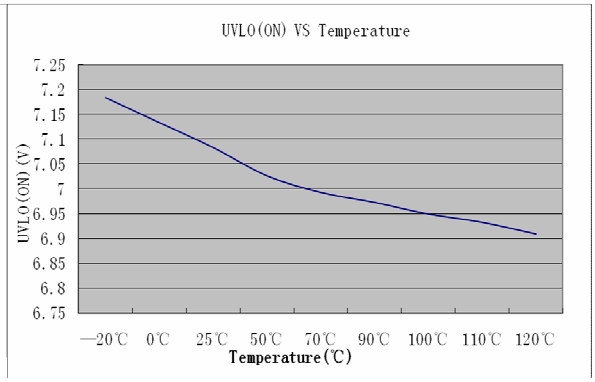












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OPERATION DESCRIPTION

PR8224/PR8224H is a highly integrated current mode PWM Power Switch optimized fo high performance, extra low standby power consumption and cost effective offline flyback converter applications. The 'hiccup mode' control greatly reduces the standby power consumption (less than 50mW) and helps the design easily to meet the international power conservation requirements.

- **Internal High Voltage Startup and Under Voltage Lockout (UVLO)**

PR8224/PR8224H integrates HV startup circuit. During power on state, it provides about 1mA current to charge the capacitor connecting between VDD and Ground from HV pin. When the voltage level ant VDD is higher than UVLO (OFF), the charge current is switched off. At this moment, the VDD capacitor provides current to PR8224/PR8224H until the auxiliary winding of the main transformer starts to provide the operation current.

In general application, a 51KΩ(typical) resistor is recommended to be placed in the high voltage path to limit the current.

- **Operating Current**

The Operating current of PR8224/PR8224H is 1.5mA. Good efficiency is achieved with this low operating current together with the 'hiccup mode' control features. The operation current is greatly reduced at no/light conditions such that extra low standby (less than 50mW) can be achieved.

- **Soft Start**

PR8224/PR8224H features an internal typical 5ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO (OFF), the primary winding current is controlled to be gradually increased to the maximum level. Every restart up is followed by a soft start.

- **Frequency spreading for EMI improvement**

The frequency spreading (switching frequency modulation) is implemented in PR8224/PR8224H. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

- **Green Mode Operation**

PR8224/PR8224H provides green-mode control to reduce the switching frequency in light-load and no-load conditions. $V_{FB,}$ which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage (Vref_green), switching frequency is continuously decreased to the minimum green-mode frequency of around 22 KHz.

- **Extended Burst Mode Operation**

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switching frequency is reduced at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold voltage (Vref_H_L) and device enters Burst Mode control. The gate driver output switches only when FB voltage is higher than the threshold voltage (Vref_H_H) to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audible noise at any loading conditions.

- **Oscillator Operation**

The switching frequency is internally fixed at 65KHz/130KHz. No external frequency setting components are needed for PCB design simplification.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in PR8224/PR8224H current mode PWM control. The switching current is detected by a sense resistor connected to the CS pin. An internal

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leading edge blanking circuit chops off the sensed voltage spikes due to snubber diode reverse recovery and surge gate current of power MOSFET at initial internal power MOSFET on state. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and eliminates the subharmonic oscillation and thus reduces the output ripple voltage.

- **Driver**

The internal power MOSFET in PR8224/PR8224H is driven by a dedicated gate driver for power switching control. Too weak the gate driver results in higher conduction and switch loss of power MOSFET while too strong gate driver results in the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with well controlled output strength and dead time control. The low idle loss and good EMI system design is achieved with this dedicated control scheme.

- **Protection Controls**

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), and Under Voltage Lockout on VDD (UVLO), and latch shutdown features including VDD over voltage protection (OVP).

The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition, when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit shuts down the converter. It restarts when VDD voltage drops below Vth_recovery. For protection with latched shut down mode, control circuit shutdowns (latch) the power MOSFET when VDD Over Voltage condition is detected until VDD drops below Vth_latch (by plug off), and device enters power on restart-up sequence thereafter.

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Package Dimensions

DIP-8L

尺寸 / 标注	最 小（mm）	最 大（mm）	尺寸 / 标注	最 小（mm）	最 大（mm）
A	9.00	9.20	C2	0.50	
A1	1.524		C3	3.3	
A2	0.39	0.53	C4	1.52TYP	
A3	2.54		D	8.20	8.80
A4	0.51TYP		D1	0.20	0.35
A5	0.99TYP		D2	7.62	7.87
B	6.1	6.3	θ1	17° TYP	
C	7.20		θ2	5° TYP	
C1	3.20	3.40			

