普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
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URL: http://www.princeton.com.tw

DESCRIPTION

The PT2257 is an electronic volume controller IC utilizing CMOS technology specially designed for the new generation of AV entertainment products. It has two (2) built-in channels making it ideally suitable for mono and stereo sound applications. The PT2257 provides an I^2C control interface, an attenuation range of 0 to -79dB, low noise, and high channel separation. It is housed in an 8 pins, DIP or SOP package. The PT2257's pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

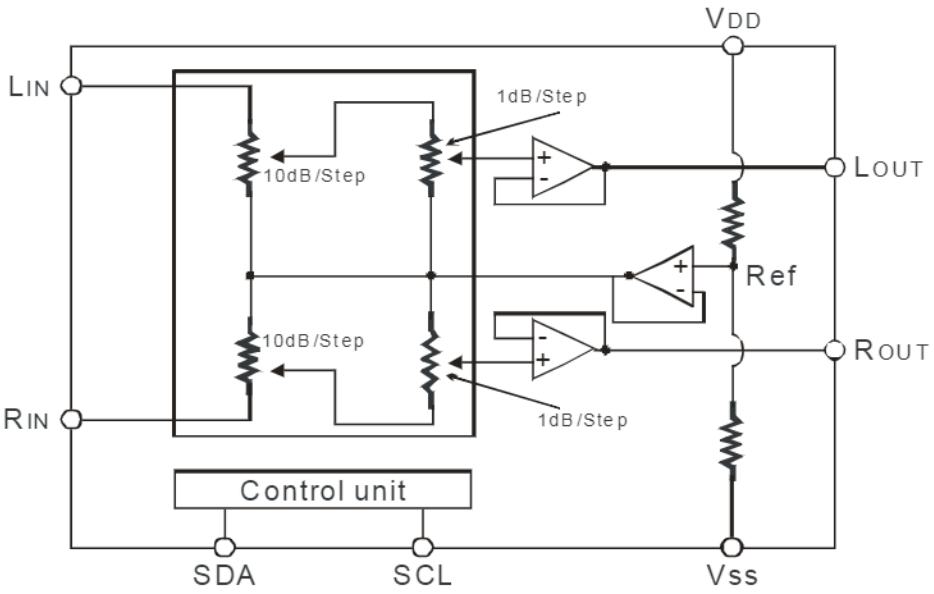
- CMOS technology
- Low power consumption
- Least external components
- Attenuation range: 0 to -79dB at 1dB/step
- Operating voltage: 3 to 9V
- Low Noise, S/N Ratio>100dB (A-weighting)
- Two channel output
- Available in 8 pins, DIP or SOP

APPLICATIONS

- AV surround audio equipment
- Car audio
- Mini compo
- Computer multi-media speaker
- Other audio equipment

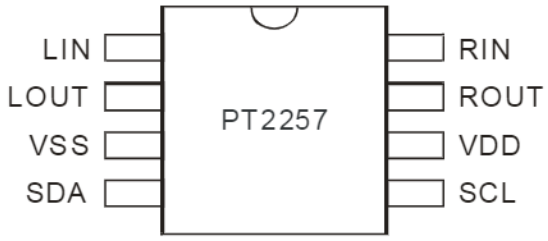
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BLOCK DIAGRAM



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PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
L_{IN}	I	Left input channel Connect a capacitor to audio source	1
L_{OUT}	O	Left output channel Connect a capacitor to audio output	2
V_{SS}	-	Ground	3
SDA	I	I^2C data input	4
SCL	I	I^2C clock input	5
V_{DD}	-	Power supply	6
R_{OUT}	O	Right output channel Connect a capacitor to audio output	7
R_{IN}	I	Right input channel Connect a capacitor to audio source	8

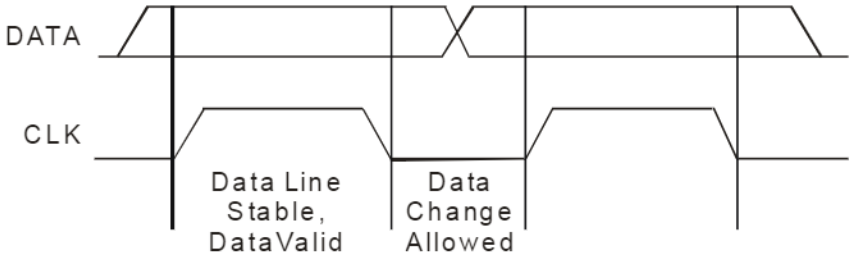
FUNCTION DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2257 via the SDA and SCL. The SDA and SCL make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW States of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

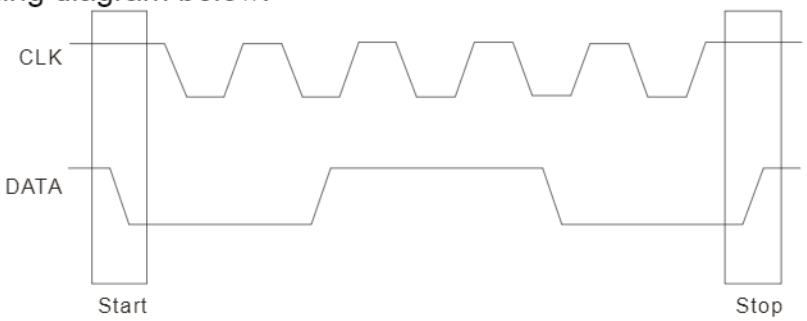
A Start Condition is activated when

1. The SCL is set to HIGH and
2. SDA shifts from HIGH to LOW State.

The Stop Condition is activated when

1. SCL is set to HIGH and
2. SDA shifts from LOW to HIGH State.

Please refer to the timing diagram below.

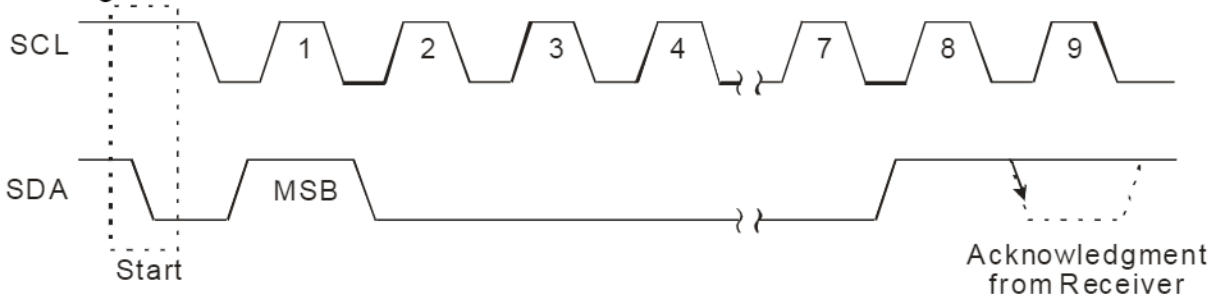


BYTE FORMAT

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the SDA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge Clock Pulse so that the SDA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte; otherwise, the SDA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

TRANSMISSION WITHOUT ACKNOWLEDGE

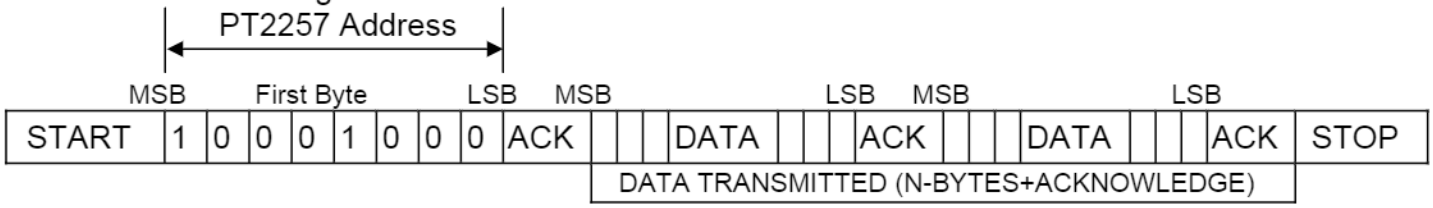
If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and does not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start bit
- A Chip Address Byte=88H
- ACK=Acknowledge bit
- A Data byte
- A Stop bit

Please refer to the diagram below:



Notes:
1. ACK=ACKNOWLEDGE
2. MAX. CLOCK SPEED=100K BITS/S

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SOFTWARE SPECIFICATION

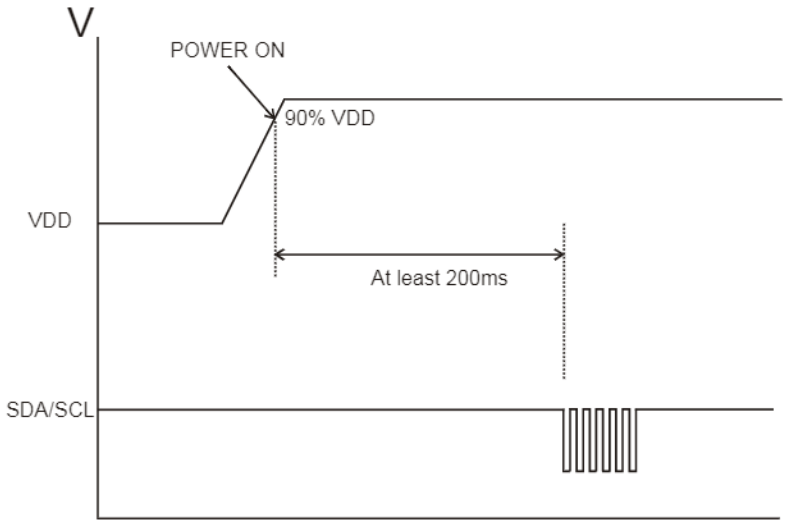
PT2257 ADDRESS

PT2257 Address is shown below:

1 MSB	0	0	0	1	0	0	0 LSB

I^2C BUS INTERFACE START TIME

After Power is turned ON, PT2257 needs to wait for a short time in order to insure stability. The waiting time period for PT2257 to send I^2C Bus Signal is at least 200ms. If the waiting time period is less than 200ms, I^2C Control may fail. Please refer to the diagram below.



DATA BYTES DESCRIPTION

FUNCTION BITS

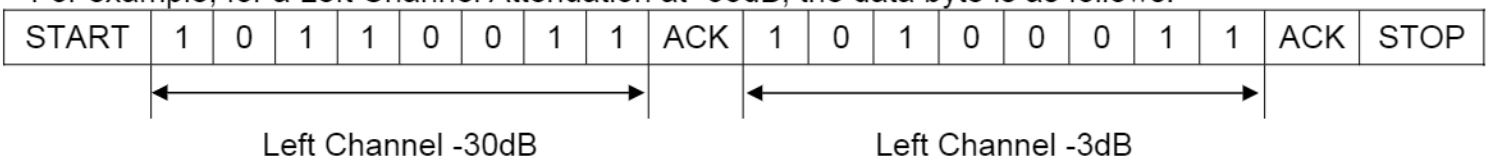
MSB	2	3	4	5	6	7	LSB	Function
1	1	1	1	1	1	1	1	Function OFF (-79dB)
1	1	0	1	A3	A2	A1	A0	2-Channel, -1dB/step
1	1	1	0	0	B2	B1	B0	2-Channel, -10dB/step
1	0	1	0	A3	A2	A1	A0	Left Channel, -1dB/step
1	0	1	1	0	B2	B1	B0	Left Channel, -10dB/step
0	0	1	0	A3	A2	A1	A0	Right Channel, -1dB/step
0	0	1	1	0	B2	B1	B0	Right Channel, -10dB/step
0	1	1	1	1	0	0	M	2-Channel, MUTE When M=1, MUTE=ON When M=0, MUTE=OFF

ATTENUATION UNIT BIT

A3	A2/B2	A1/B1	A0/B0	Attenuation Value (dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/
1	0	0	1	-9/

Where: Ax=-dB/step, Bx=-10dB/step

For example, for a Left Channel Attenuation at -33dB, the data byte is as follows:



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	12	V
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃
Input voltage	V_I	-0.3 to V_{CC}+0.3	V

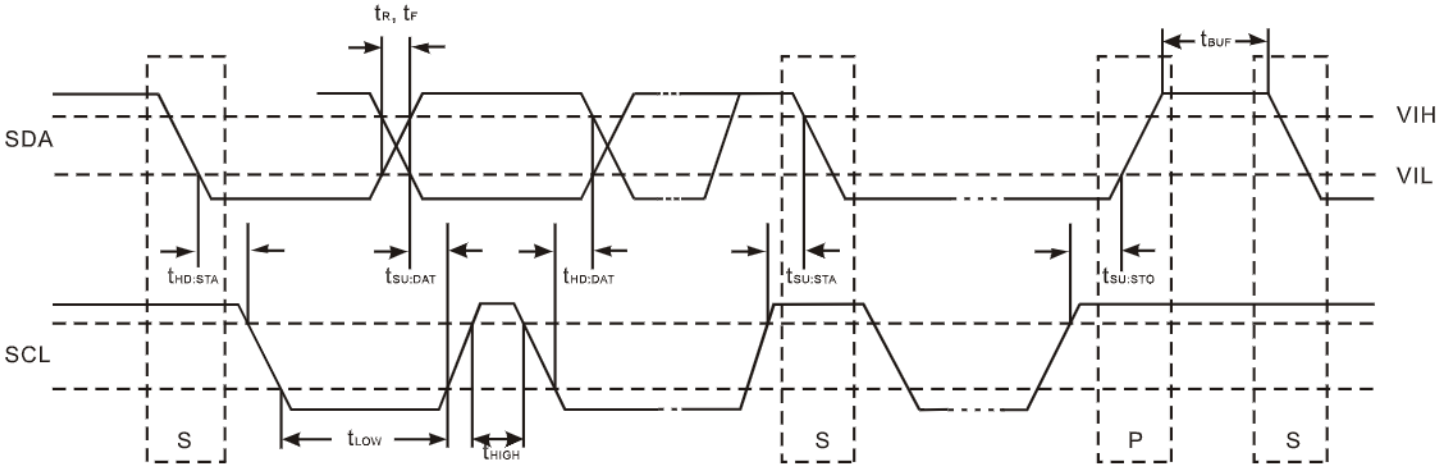
AUDIO SECTION ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating voltage	VDD			3	9	10	V
Operating current	IDD	VDD=9V, V_I=0V		-	9	15	mA
Volume attenuation range	ARANGE	Minimum Attenuation		-0.5	0	-	dB
		Maximum Attenuation		-72	-79	-	
Attenuation step	ASTEP			-	1	-	dB
Joint step gain error	GERR			-	0.5	-	dB
Inter-channel attenuation gain error	CERR			-	0.5	-	dB
Maximum output level	Vomax	VDD=9V, F=1KHz Volume Att=0dB Rload=50K, THD<1%		2.0	2.3	2.5	Vrms
Total harmonic distortion	THD	F =1KHz, Volume Att=0dB, A-weighted Rload=50K	Vout=2Vrms	-	0.07	0.09	%
			Vout=200m Vrms	-	0.003	0.005	
Noise output	No	Vin=GND, MUTE=OFF Volume Att=0dB, A-weighted		-	2	3	μVrms
Signal-to-Noise ratio	SNR	0dB=Vomax, ATT=0dB	22~22KHz	90	100	103	dB
			A-weighted	110	120	123	
Channel separation	CS	Vin=2.5Vrms, F=1KHz,Volume=0dB		100	120	125	dB
Mute attenuation	MUTE	Vin=2.5Vrms, F=1KHz Volume Att=0dB, A-weighted		90	95	97	dB
Frequency response	FR	Vin=1Vrms, Volume Att=-10dB		-	1	1.3	MHz
Input impedance	Rin	F=1KHz		15	20	26	KΩ
Output impedance	Rout	F=1KHz, Vout=100m Vrms		-	100	-	Ω
Minimum load resistance	Rload	VDD=9V, Vo=2Vrms,THD<1%		2	-	-	KΩ

I²C BUS SECTION ELECTRICAL CHARACTERISTICS

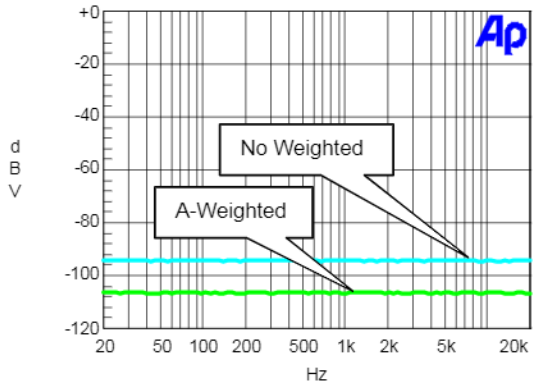
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bus high input level	VIH	VDD=9V	0.4	-	VDD	VDD
Bus low input level	VIL	VDD=9V	0	-	0.2	VDD

BUS LINE TIMING CHARACTERISTICS

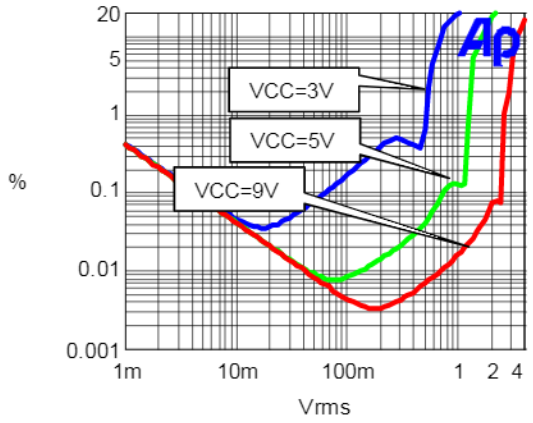


Parameter	Symbol	Condition	Min.	Max.	Unit
Low level input voltage	V_{IL}	VDD=4.0V	-0.5	1.1	V
High level input voltage	V_{IH}	VDD=4.0V	1.6	4.0	V
SCL clock frequency	f_{SCL}		0	100	KHz
Time the bus must be free before a new transmission can start	t_{BUF}		5.0	-	µs
Hold time start condition*	$t_{HD\text{-}STA}$		4.0	-	µs
Clock low period	t_{LOW}		5.0	-	µs
Clock high period	t_{HIGH}		4.0	-	µs
Setup time for start condition **	$t_{SU\text{-}STA}$		5.0	-	µs
Data hold time	$t_{HD\text{-}DAT}$		0	-	µs
Data setup time	$t_{SU\text{-}DAT}$		250	-	ns
Rise time (SDA & SCL Lines)	t_R		-	1000	ns
Fall time (SDA & SCL Lines)	t_F		-	300	ns
Stop condition setup time	$t_{SU\text{-}STO}$		4.0	-	µs

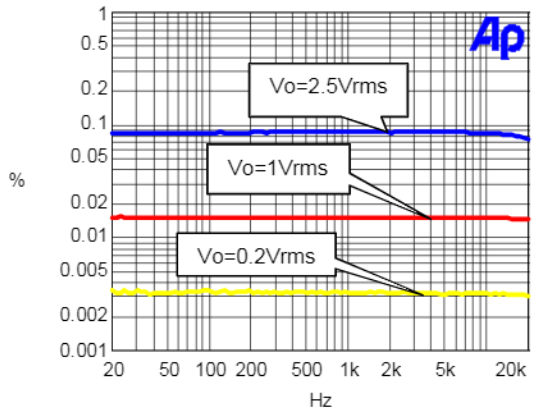
Notes:
1. * = The first clock pulse is generated after this period.
2. ** = This is only relevant for a repeated start condition.



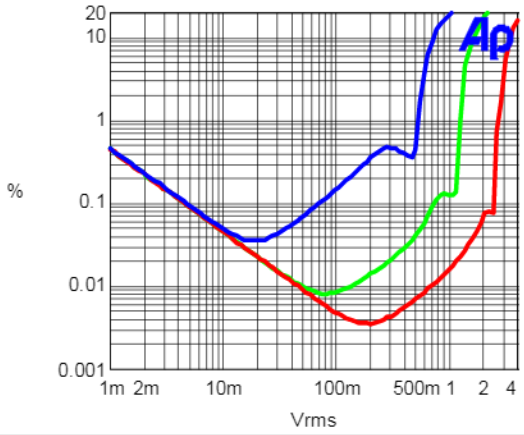
Residual Noise Floor



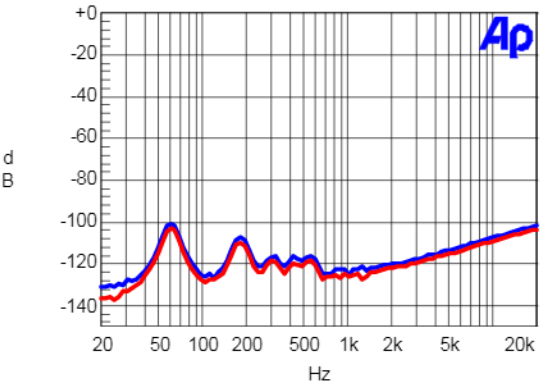
THD vs. Output Level, RL=50KΩ



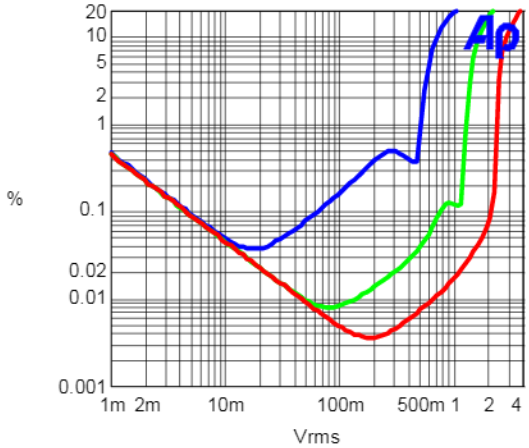
THD vs. Frequency



THD vs. Output Level, RL=5KΩ



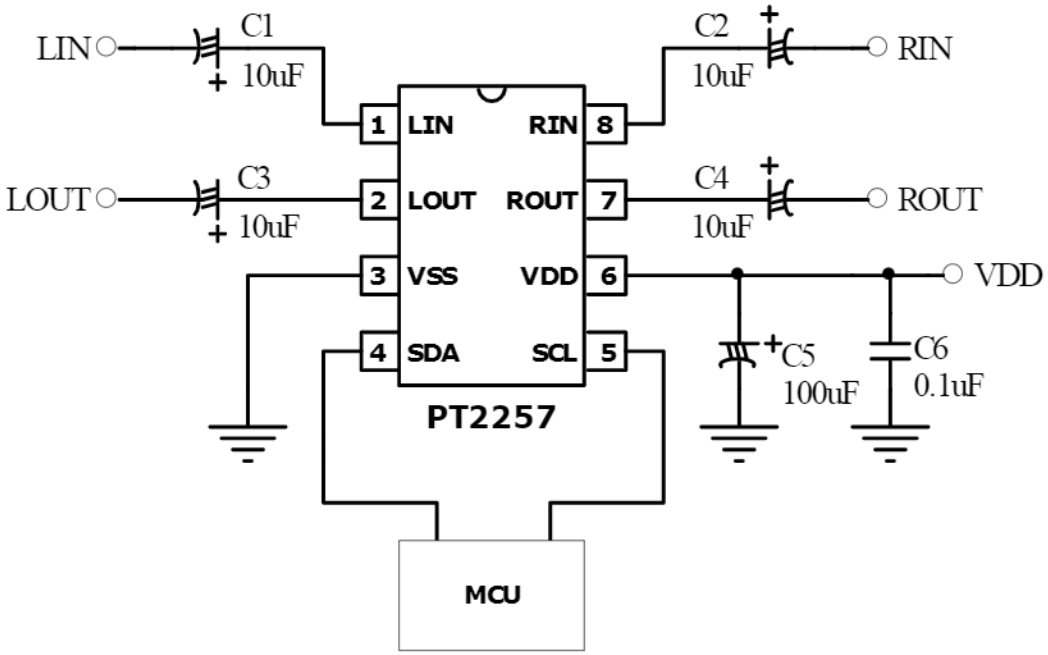
Crosstalk



THD vs. Output Level, RL=2KΩ

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APPLICATION CIRCUIT



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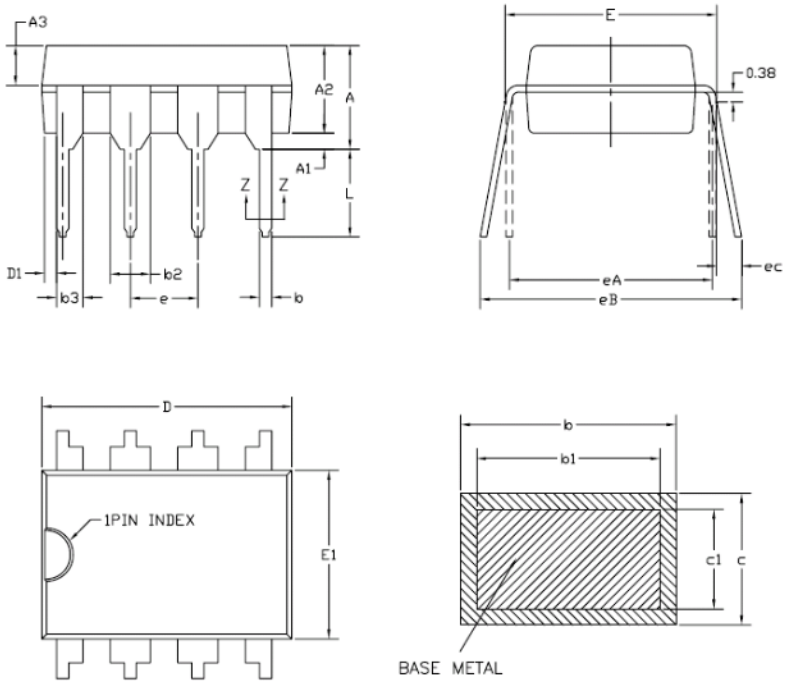
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2257-D	8 Pins, DIP, 300mil	PT2257-D
PT2257-S	8 Pins, SOP, 150mil	PT2257-S

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PACKAGE INFORMATION

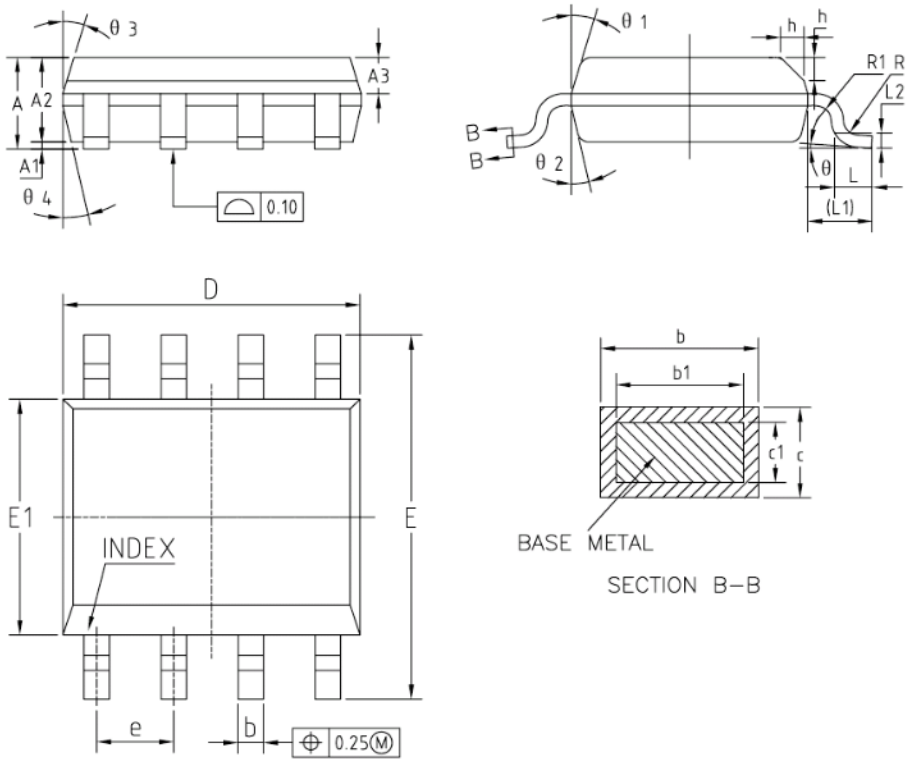
8 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	4.80
A1	0.50	-	-
A2	3.10	3.30	3.50
A3	1.40	1.50	1.60
b	0.38	-	0.55
b1	0.38	0.46	0.51
b2	1.47	1.52	1.57
b3	0.89	0.99	1.09
c	0.21	-	0.35
c1	0.20	0.25	0.30
D	9.10	9.20	9.30
D1	0.13	-	-
E	7.62	7.87	8.25
E1	6.25	6.35	6.45
e	2.54 BSC		
eA	7.62 BSC.		
eB	7.62	8.80	10.90
eC	0.000	-	1.52
L	2.92	3.30	3.81

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8 PINS, SOP, 150 MIL



Symbol	Min.	Typ.	Max.
A	1.35	1.55	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC.	
L	0.45	0.60	0.80
L1		1.04 REF.	
L2		0.25 BSC.	
R	0.07	-	-
R1	0.07		-
h	0.30	0.40	0.50
θ	0°	-	8°
θ1	15°	17°	19°
θ2	11°	13°	15°
θ3	15°	17°	19°
θ4	11°	13°	15°

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AA.

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