TEXAS INSTRUMENTS

TL2842, TL2843, TL2844, TL2845
TL3842, TL3843, TL3844, TL3845

SLVS038I – JANUARY 1989 – REVISED JULY 2016

# TLx84x Current-Mode PWM Controllers

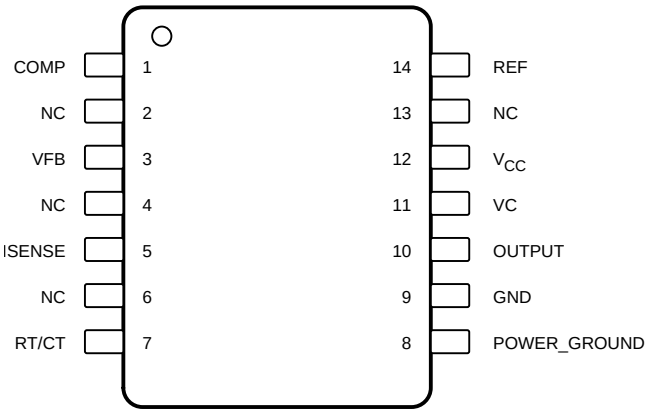
## 1 Features

- Optimized for Off-Line and DC-to-DC Converters
- Low Start-Up Current (< 1 mA)
- Automatic Feed-forward compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load-Response Characteristics
- Undervoltage Lockout With Hysteresis
- Double-Pulse Suppression
- High-Current Totem-Pole Output
- Internally Trimmed Bandgap Reference
- 500-kHz Operation
- Error Amplifier With Low Output Resistance
- Designed to be Interchangeable with UC2842 and UC3842 Series

## 2 Applications

- Switching regulators of any polarity
- Transformer-coupled DC/DC convertors

### Device Pinout Drawing SOIC (14)




Not to scale

## 3 Description

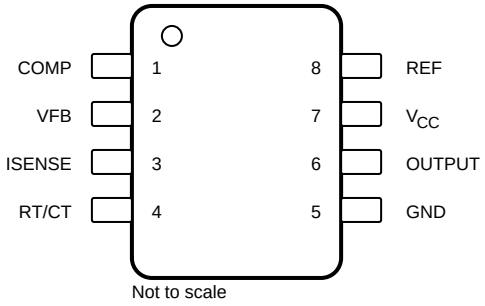
The TL284x and TL384x series of control integrated circuits provide the features that are necessary to implement off-line or DC-to-DC fixed-frequency current-mode control schemes, with a minimum number of external components. Some of the internally implemented circuits are an undervoltage lockout (UVLO), featuring a start-up current of less than 1 mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator (that also provides current-limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

### Device Information(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLx84x | SOIC (8) | 4.90 mm × 3.91 mm |
| | SOIC (14) | 8.65 mm × 3.91 mm |
| | PDIP (8) | 9.81 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Device Pinout Drawing SOIC or PDIP (8)




Not to scale

NC — No internal connection

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

**1 Features** ... 1
**2 Applications** ... 1
**3 Description** ... 1
**4 Revision History** ... 2
**5 Pin Configuration and Functions** ... 3
**6 Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
**7 Detailed Description** ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 9
**8 Application and Implementation** ... 10
8.1 Typical Application ... 10
**9 Power Supply Recommendations** ... 12
**10 Layout** ... 13
10.1 Layout Guidelines ... 13
10.2 Layout Example ... 14
**11 Device and Documentation Support** ... 15
11.1 Receiving Notification of Documentation Updates 15
11.2 Related Links ... 15
11.3 Community Resources ... 15
11.4 Trademarks ... 15
11.5 Electrostatic Discharge Caution ... 15
11.6 Glossary ... 15
**12 Mechanical, Packaging, and Orderable Information** ... 15

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision H (January 2015) to Revision I** — **Page**

- Updated pinout images ... 3
- Changed TL984x to TL384x in *Recommended Operating Conditions* ... 4
- Changed TLx842, TLx844 to TLx842, TLx843 and TLx843, TLx845 to TLx844, TLx845 in *Pulse-Width-Modulator Section* ... 6
- Added *Receiving Notification of Documentation Updates* section and *Community Resources* section ... 15

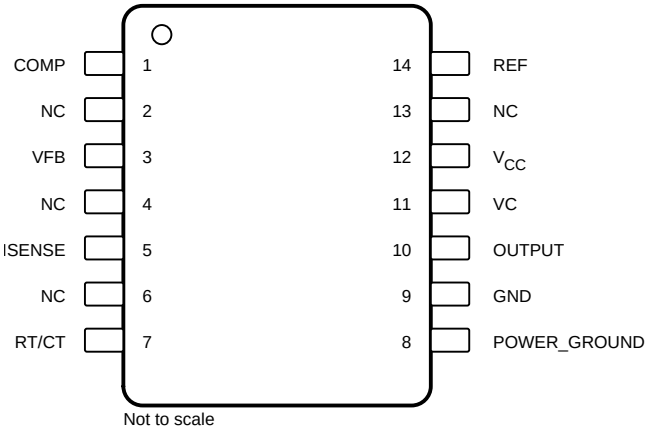
**Changes from Revision G (February 2008) to Revision H** — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1


Copyright © 1989–2016, Texas Instruments Incorporated

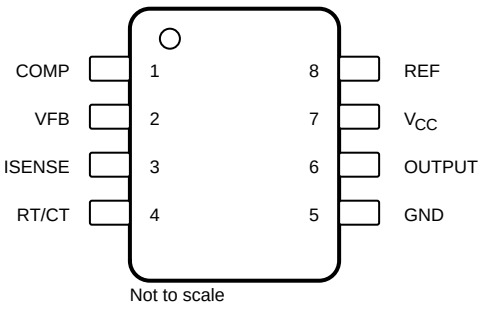
# 5 Pin Configuration and Functions

**D Package**
**14-Pin SOIC**
**Top View**




Not to scale

**D or P Package**
**8-Pin SOIC or PDIP**
**Top View**




Not to scale

NC — No internal connection

**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | D | D or P | | |
| COMP | 1 | 1 | I/O | Error amplifier compensation pin |
| GND | 9 | 5 | — | Device power supply ground terminal |
| ISENSE | 5 | 3 | I | Current sense comparator input |
| NC | 2, 4, 6, 13 | — | — | Do not connect |
| OUTPUT | 10 | 6 | O | PWM Output |
| POWER GROUND | 8 | — | — | Output PWM ground terminal |
| REF | 14 | 8 | O | Oscillator voltage reference |
| RT/CT | 7 | 4 | I/O | Oscillator RC input |
| VC | 11 | — | — | Output PWM positive voltage supply |
| $V_{CC}$ | 12 | 7 | — | Device positive voltage supply |
| VFB | 3 | 2 | I | Error amplifier input |

Copyright © 1989–2016, Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage(2) | Self limiting | | — |
| $V_I$ | Analog input voltage range, VFB and ISENSE | –0.3 | 6.3 | V |
| $V_O$ | Output Voltage | | 35 | V |
| $V_I$ | Input Voltage, VC and D Package only | | 35 | V |
| $I_{CC}$ | Supply current | | 30 | mA |
| $I_O$ | Output current | | ±1 | A |
| | error amplifier output sink current | | 10 | mA |
| $T_J$ | Virtual junction temperature | | 150 | °C |
| | Output energy (capacitive load) | | 5 | µJ |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the device GND pin.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 3000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 3000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ and VC(1) | Supply Voltage | | | | 30 | V |
| $V_I$, RT/CT | Input Voltage | | 0 | | 5.5 | V |
| $V_I$, VFB and ISENSE | Input Voltage | | 0 | | 5.5 | V |
| $V_O$, OUTPUT | Output voltage | | 0 | | 30 | V |
| $V_O$, POWER GROUND(1) | Output voltage | | –0.1 | | 1 | V |
| $I_{CC}$ | Supply current, externally limited | | | | 25 | mA |
| $I_O$ | Average output current | | | | 200 | mA |
| $I_{O(ref)}$ | Reference output current | | | | –20 | mA |
| $f_{OSC}$ | Oscillator frequency | | | 100 | 500 | kHz |
| $T_A$ | Operating free-air temperature | TL284x | –40 | | 85 | °C |
| | | TL384x | 0 | | 70 | |

(1) These recommended voltages for VC and POWER GROUND apply only to the D package.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TLx84x | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | D (SOIC) | P (PDIP) | |
| | | 8 PINS | 14 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97 | 86 | 85 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


Copyright © 1989–2016, Texas Instruments Incorporated

## 6.5 Electrical Characteristics

over operating free-air temperature range, $V_{CC}$ = 15 V[1], $R_T$ = 10 kΩ, $C_T$ = 3.3 nF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS[2] | TL284x | | | TL384x | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP[2] | MAX | MIN | TYP[2] | MAX | |
| **Reference Section** | | | | | | | | | |
| Output voltage | | $I_O$ = 1 mA, $T_A$ = 25°C | 4.95 | 5 | 5.05 | 4.9 | 5 | 5.1 | V |
| Line regulation | | $V_{CC}$ = 12 V to 25 V | | 6 | 20 | | 6 | 20 | mV |
| Load regulation | | $I_O$ = 1 mA to 20 mA | | 6 | 25 | | 6 | 25 | mV |
| Temperature coefficient of output voltage | | | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/°C |
| Output voltage with worst-case variation | | $V_{CC}$ = 12 V to 25 V, $I_O$ = 1 mA to 20 mA | 4.9 | | 5.1 | 4.82 | | 5.18 | V |
| Output noise voltage | | f = 10 Hz to 10 kHz, $T_A$ = 25°C | | 50 | | | 50 | | µV |
| Output-voltage long-term drift | | After 1000 h at $T_A$ = 25°C | | 5 | 25 | | 5 | 25 | mV |
| Short-circuit output current | | | –30 | –100 | –180 | –30 | –100 | –180 | mA |
| **Oscillator Section** | | | | | | | | | |
| Oscillator frequency[3] | | $T_A$ = 25°C | 47 | 52 | 57 | 47 | 52 | 57 | kHz |
| Frequency change with supply voltage | | $V_{CC}$ = 12 V to 25 V | | 2 | 10 | | 2 | 10 | Hz/kHz |
| Frequency change with temperature | | | | 50 | | | 50 | | Hz/kHz |
| peak-to-peak amplitude at RT/CT | | | | 1.7 | | | 1.7 | | V |
| **Error-Amplifier Section** | | | | | | | | | |
| Feedback input voltage | | COMP at 2.5 V | 2.45 | 2.50 | 2.55 | 2.42 | 2.50 | 2.58 | V |
| Input bias current | | | | –0.3 | –1 | | –0.3 | –2 | µA |
| Open-loop voltage amplification | | $V_O$ = 2 V to 4 V | 65 | 90 | | 65 | 90 | | dB |
| Gain-bandwidth product | | | 0.7 | 1 | | 0.7 | 1 | | MHz |
| Supply-voltage rejection ratio | | $V_{CC}$ = 12 V to 25 V | 60 | 70 | | 60 | 70 | | dB |
| Output sink current | | VFB, at 2.7 V, COMP at 1.1 V | 2 | 6 | | 2 | 6 | | mA |
| Output source current | | VFB, at 2.3 V, COMP at 5 V | –0.5 | –0.8 | | –0.5 | –0.8 | | mA |
| Hihg-level output voltage | | VFB, at 2.3 V, $R_L$ = 15 kΩ to GND | 5 | 6 | | 5 | 6 | | V |
| Low-level output voltage | | VFB, at 2.7 V, $R_L$ = 15 kΩ to GND | | 0.7 | 1.1 | | 0.7 | 1.1 | V |
| **Current-sense Section** | | | | | | | | | |
| Voltage amplification | | See[4][5] | 2.85 | 3 | 3.13 | 2.85 | 3 | 3.15 | V/V |
| Current-sense comparator threshold | | COMP at 5 V, see[4] | 0.9 | 1 | 1.1 | 0.9 | 1 | 1.1 | V |
| Supply-voltage rejection ratio | | $V_{CC}$ = 12 V to 25 V, see[4] | | 70 | | | 70 | | dB |
| Input bias current | | | | –2 | –10 | | –2 | –10 | µA |
| Delay time to output | | | | 150 | 300 | | 150 | 300 | ns |
| **Output Section** | | | | | | | | | |
| High-level output voltage | | $I_{OH}$ = –20 mA | 13 | 13.5 | | 13 | 13.5 | | V |
| | | $I_{OH}$ = –200 mA | 12 | 13.5 | | 13 | 13.5 | | |
| Low-level output voltage | | $I_{OH}$ = 20 mA | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| | | $I_{OH}$ = 200 mA | | 1.5 | 2.2 | | 1.5 | 2.2 | |
| Rise time | | $C_L$ = 1 nF, $T_A$ = 25°C | | 50 | 150 | | 50 | 150 | ns |
| fall time | | $C_L$ = 1 nF, $T_A$ = 25°C | | 50 | 150 | | 50 | 150 | ns |
| **Undervoltage-Lockout Section** | | | | | | | | | |
| Start threshold voltage | TLx842, TLx844 | | 15 | 16 | 17 | 14.5 | 16 | 17.5 | V |
| | TLx843, TLx845 | | 7.8 | 8.4 | 9 | 7.8 | 8.4 | 9 | |

(1) Adjust $V_{CC}$ above the start threshold before setting it to 15 V.
(2) All typical values are at TA = 25°C.
(3) Output frequency equals oscillator frequency for the TLx842 and TLx843. Output frequency is one-half the oscillator frequency for the TLx844 and TLx845.
(4) These parameters are measured at the trip point of the latch, with VFB at 0 V.
(5) Voltage amplification is measured between ISENSE and COMP, with the input changing from 0 V to 0.8 V.

Copyright © 1989–2016, Texas Instruments Incorporated

## Electrical Characteristics (continued)

over operating free-air temperature range, $V_{CC}$ = 15 V[1], $R_T$ = 10 kΩ, $C_T$ = 3.3 nF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS[2] | TL284x | | | TL384x | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP[2] | MAX | MIN | TYP[2] | MAX | |
| Minimum operating voltage after startup | TLx842, TLx844 | | 9 | 10 | 11 | 8.5 | 10 | 11.5 | V |
| | TLx843, TLx845 | | 7 | 7.6 | 8.2 | 7 | 7.6 | 8.02 | |
| **Pulse-Width-Modulator Section** | | | | | | | | | |
| Maximum duty cycle | TLx842, TLx843 | | 95% | 97% | 100% | 95% | 97% | 100% | |
| | TLx844, TLx845 | | 46% | 48% | 50% | 46% | 48% | 50% | |
| Minimum duty cycle | | | | | 0% | | | 0% | |
| **Supply Voltage** | | | | | | | | | |
| Start-up current | | | | 0.5 | 1 | | 0.5 | 1 | mA |
| Operating supply current | | VFB and ISENSE at 0 V | | 11 | 17 | | 11 | 17 | mA |
| Limiting voltage | | $I_{CC}$ = 25 mA | | 34 | | | 34 | | V |

## 6.6 Typical Characteristics

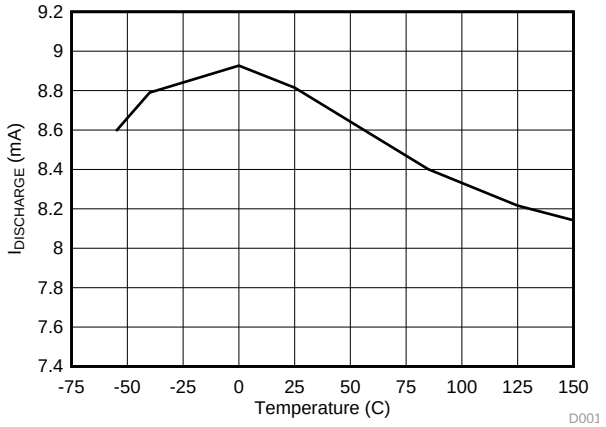



**Figure 1. Oscillator Discharge Current vs Temperature for $V_{IN}$ = 15 V and $V_{OSC}$ = 2V**

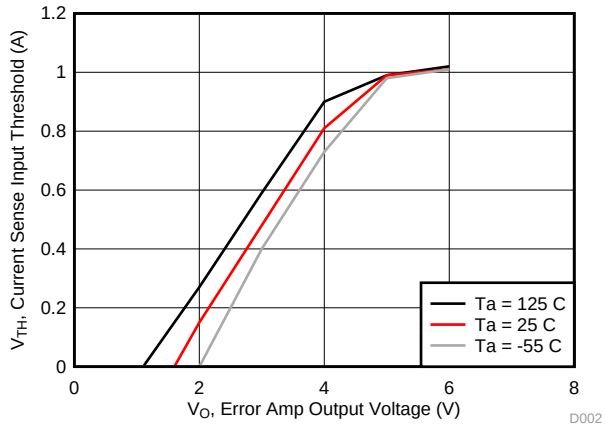



**Figure 2. Current Sense Input Threshold vs Error Amplifier Output Voltage for $V_{IN}$ = 15 V**

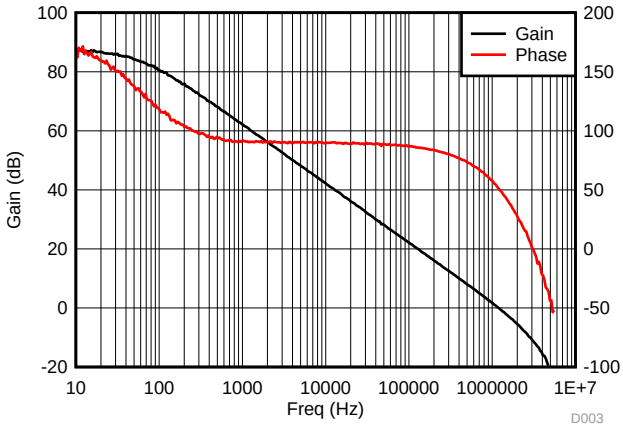



**Figure 3. Error Amplifier Open-Loop Gain and Phase vs Frequency $V_{CC}$ = 15 V, $R_L$ = 100 kΩ, and $T_A$ = 25 °C**

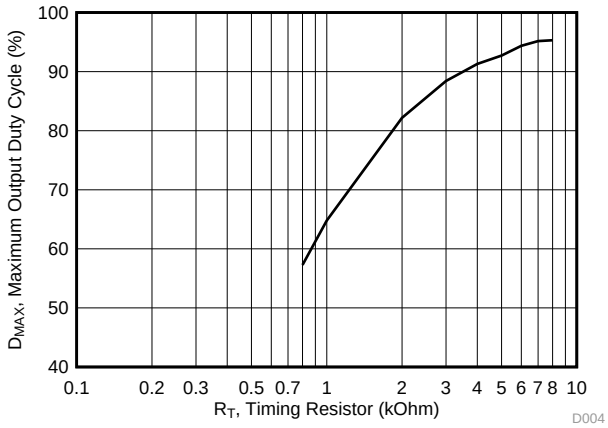



**Figure 4. Max Output Duty Cycle vs Timing Resistor for $V_{CC}$ = 15, $C_T$ = 3.3 nF, $T_A$ = 25 °C**


Copyright © 1989–2016, Texas Instruments Incorporated

## Typical Characteristics (continued)

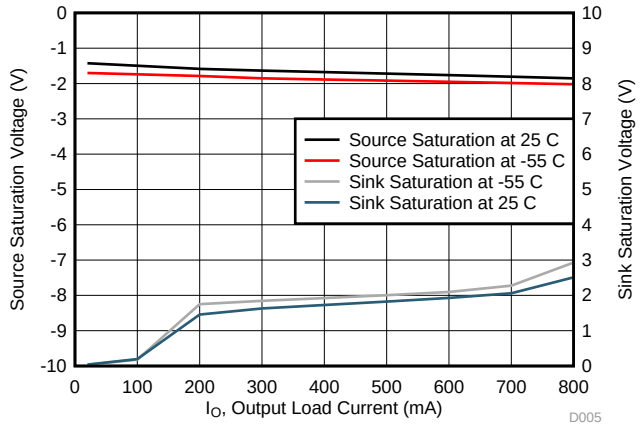



**Figure 5. Output Saturation Voltage vs Load Current for $V_{CC}$ = 15 V with 5-ms Input Pulses**

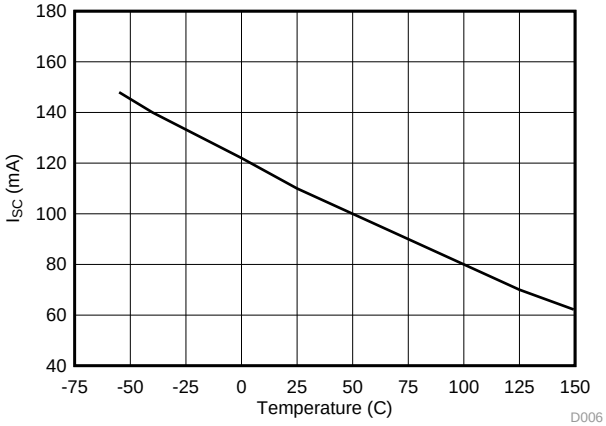



**Figure 6. Reference Short Circuit Current vs Temperature for $V_{IN}$ = 15 V**

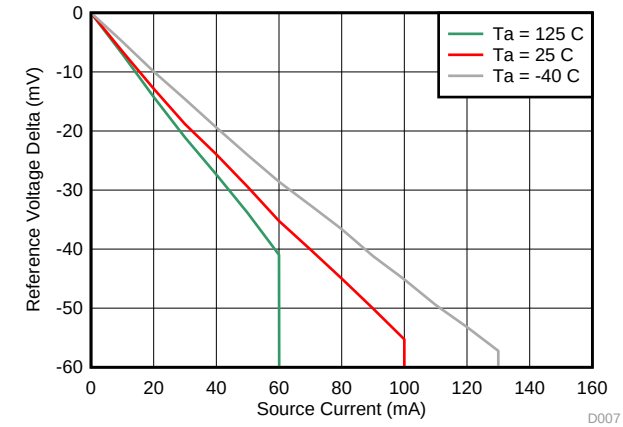



**Figure 7. Reference Voltage vs Source Current**

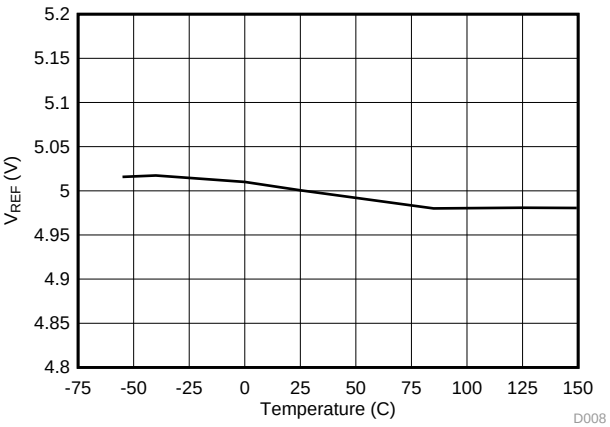



**Figure 8. Reference Voltage vs Temperature**

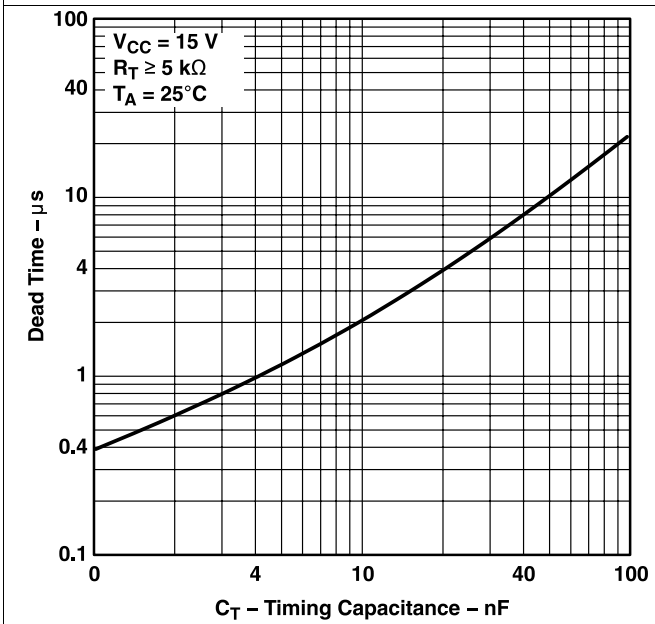



**Figure 9. Dead Time vs Timing Capacitance**

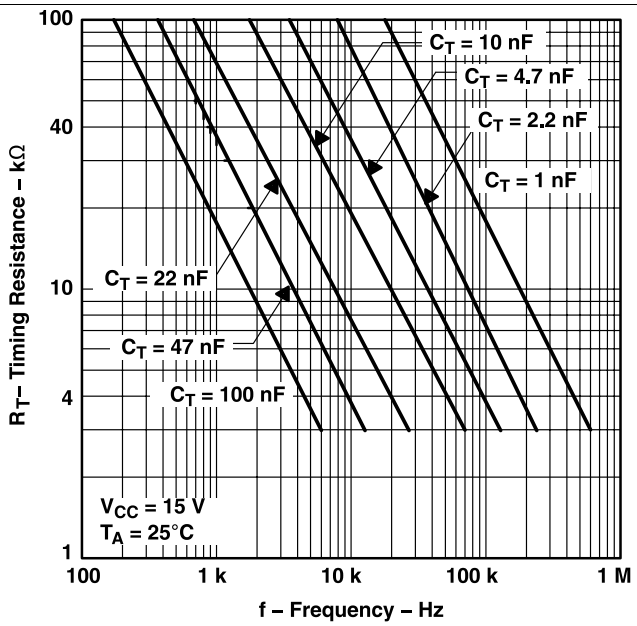



**Figure 10. Timing Resistance vs Frequency**

Copyright © 1989–2016, Texas Instruments Incorporated

# 7 Detailed Description

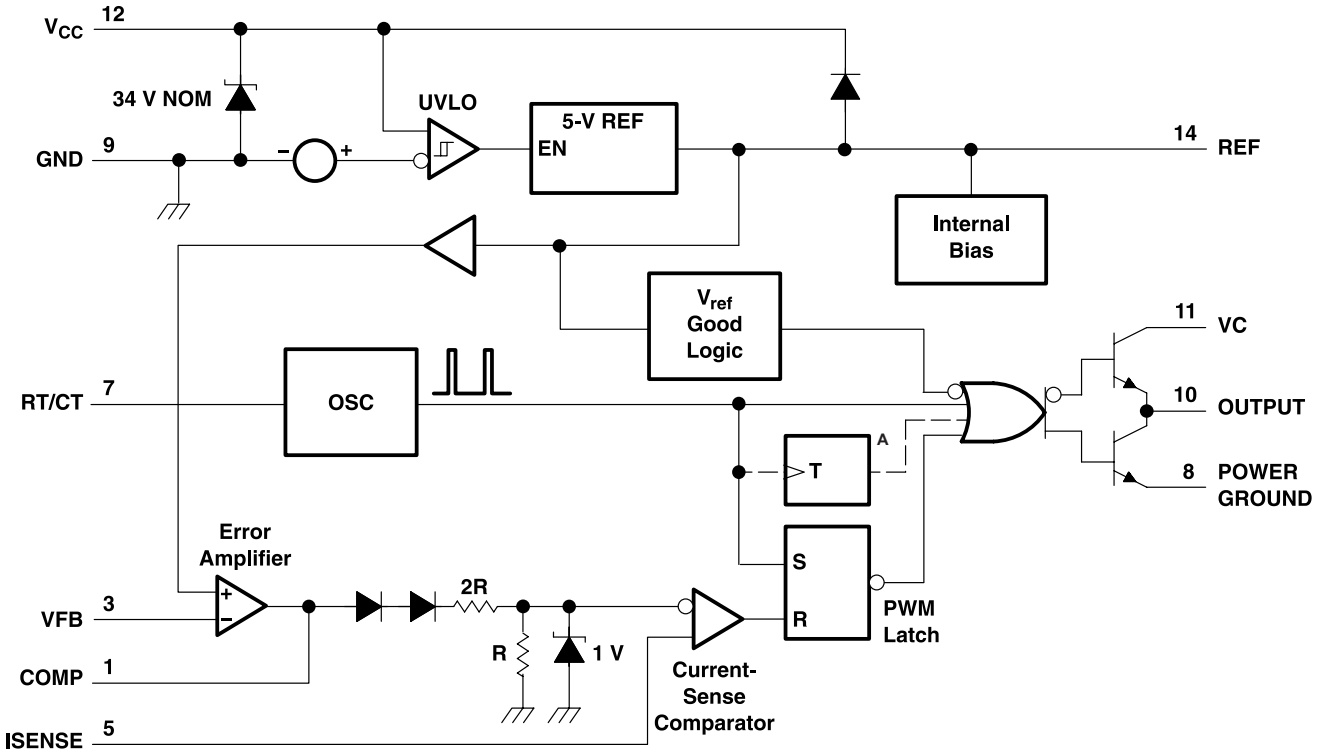
## 7.1 Overview

The TL284x and TL384x series of control integrated circuits provide the features that are necessary to implement off-line or DC-to-DC fixed-frequency current-mode control schemes, with a minimum number of external components. Some of the internally implemented circuits are an undervoltage lockout (UVLO), featuring a start-up current of less than 1 mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator (that also provides current-limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

Major differences between members of these series are the UVLO thresholds and maximum duty-cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the TLx842 and TLx844 devices make them ideally suited to off-line applications. The corresponding typical thresholds for the TLx843 and TLx845 devices are 8.4 V (on) and 7.6 V (off). The TLx842 and TLx843 devices can operate to duty cycles approaching 100%. A duty-cycle range of 0 to 50% is obtained by the TLx844 and TLx845 by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.

The TL284x-series devices are characterized for operation from −40°C to +85°C. The TL384x devices are characterized for operation from 0°C to 70°C.

## 7.2 Functional Block Diagram




A. The toggle flip-flop is present only in TL2844, TL2845, TL3844, and TL3845. Pin numbers shown are for the D (14-pin) package.

## 7.3 Feature Description

### 7.3.1 Pulse-by-Pulse Current Limiting

Pulse-by-pulse limiting is inherent in the control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation


Copyright © 1989–2016, Texas Instruments Incorporated

## Feature Description (continued)

### 7.3.2 Error Amplifier With Low Output Resistance

With a low output resistance, various impedance networks may be used on the compensation pin input for error amplifier feedback.

### 7.3.3 High-Current Totem-Pole Output

The output of the TLx84x devices can sink or source up to 1 A of current.

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Technique

The PWM controller (see Figure 11) can be shut down by two methods: either raise the voltage at ISENSE above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (see *Functional Block Diagram*). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or ISENSE terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling VCC below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.

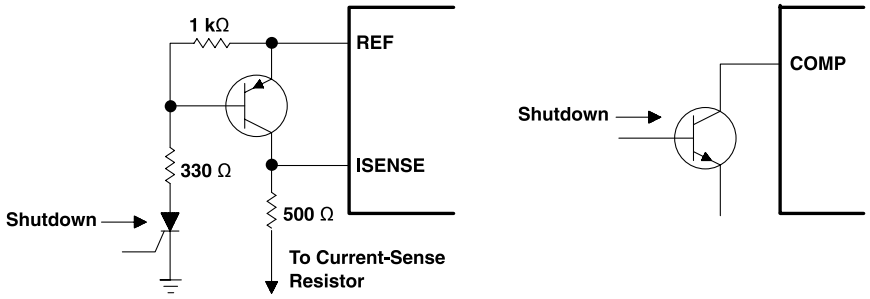



**Figure 11. Shutdown Techniques**

### 7.4.2 Slope Compensation

A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 12).

**NOTE**

Capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

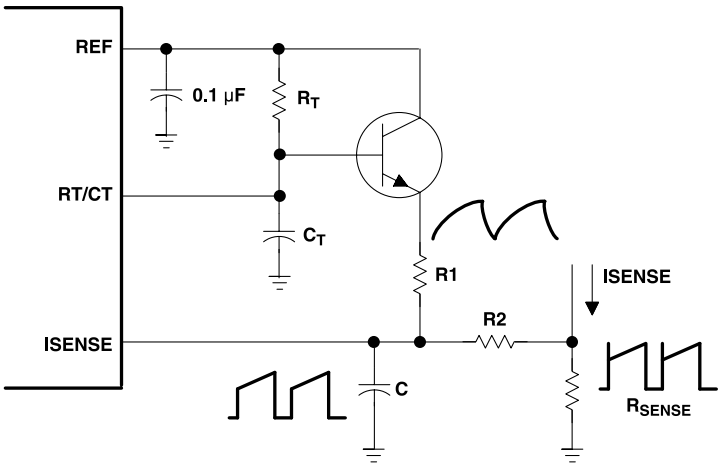



**Figure 12. Slope Compensation**

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Typical Application

The following application is an open-loop laboratory test fixture. This circuit demonstrates the setup and use of the TL284x and TL384x devices and their internal circuitry.

In the open-loop laboratory test fixture (see Figure 13), high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-kΩ potentiometer sample the oscillator waveform and apply an adjustable ramp to the ISENSE terminal.

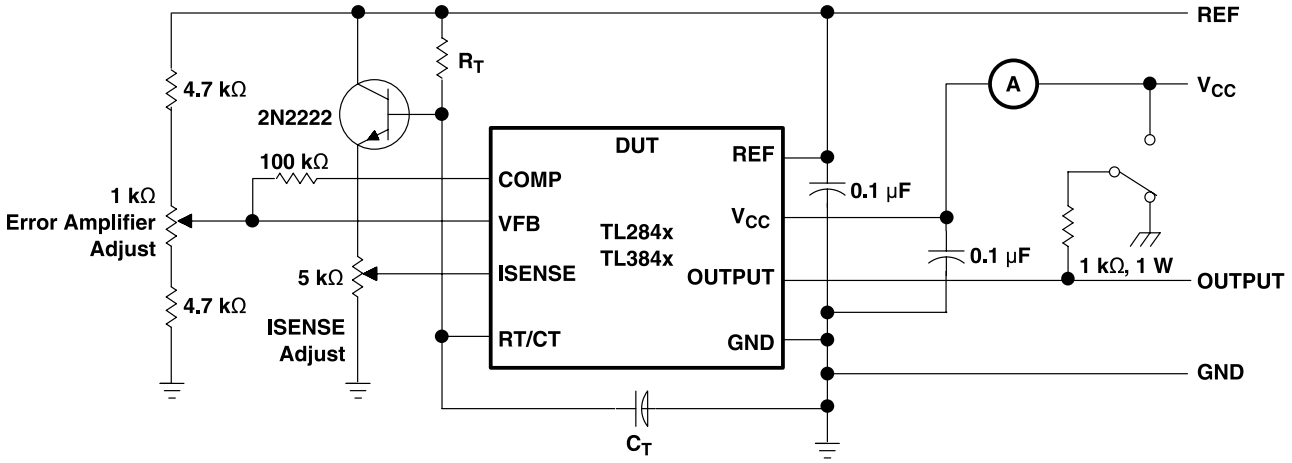



**Figure 13. Open-Loop Laboratory Test Fixture**

### 8.1.1 Design Requirements

The design techniques in the following sections may be used for power supply PWM applications which fall within the following requirements.

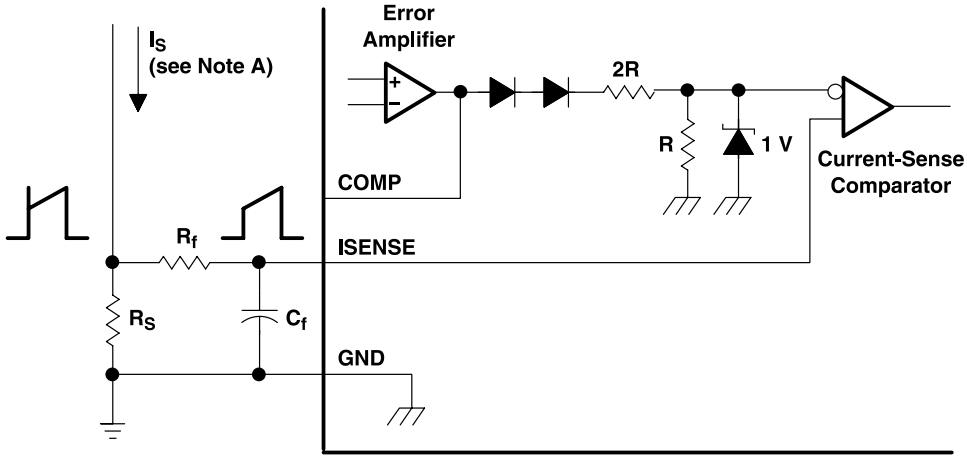
- 500-kHz or lower operation
- 30-V or less output voltage
- 200-mA or less output current


Copyright © 1989–2016, Texas Instruments Incorporated

## Typical Application (continued)

### 8.1.2 Detailed Design Procedure

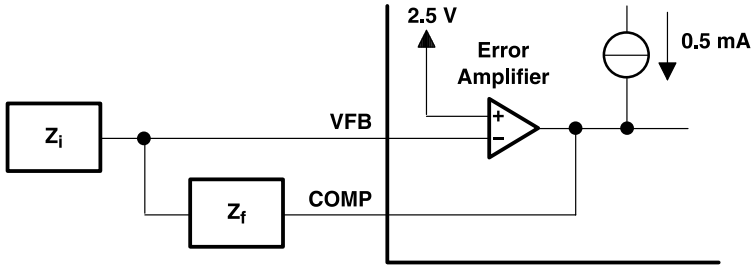
#### 8.1.2.1 Current-Sense Circuit




A. Peak current (IS) is determined by the formula: $I_{S(max)} = \frac{1\ V}{R_S}$ A small RC filter formed by resistor Rf and capacitor Cf may be required to suppress switch transients.

**Figure 14. Current-Sense Circuit Schematic**

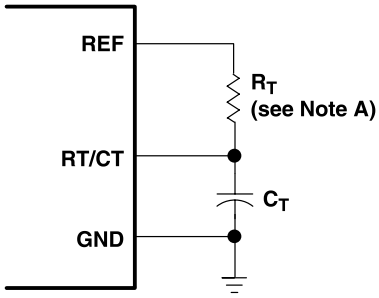
#### 8.1.2.2 Error-Amplifier Configuration




A. Error amplifier can source or sink up to 0.5 mA.

**Figure 15. Error-Amplifier Configuration Schematic**

#### 8.1.2.3 Oscillator Section




A. For $R_T > 5\ k\Omega$: $f \approx \frac{1.72}{R_T C_T}$

**Figure 16. Oscillator Section Schematic**

## Typical Application (continued)

### 8.1.3 Application Curve

The application curve shows oscillator characteristics for chosen capacitor and resistor values.

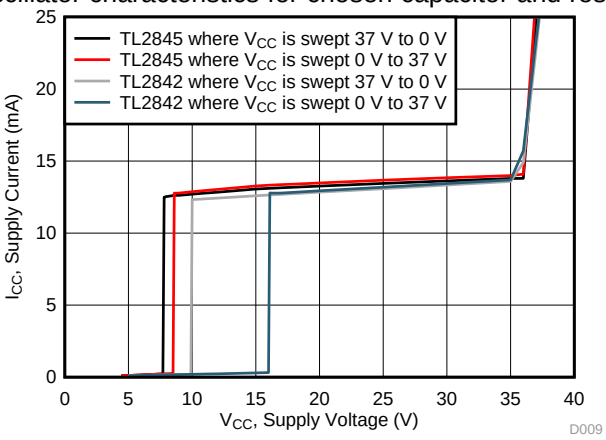



**Figure 17. Supply Current vs Supply Voltage**

## 9 Power Supply Recommendations

See *Recommended Operating Conditions* for the recommended power supply voltages for the TL284x and TL384x devices. TI also recommends to have a decoupling capacitor on the output of the device's power supply to limit noise on the device input.


Copyright © 1989–2016, Texas Instruments Incorporated

# 10 Layout

## 10.1 Layout Guidelines

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

### 10.1.1 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. Also, keep the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

### 10.1.2 Input/Output Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the $V_{CC}$ pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case it should also be positioned as close to the IC as possible. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

### 10.1.3 Compensation Components

External compensation components for stability should also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

### 10.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.

The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace will need to conduct a significant amount of current from one plane to the other.

Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

Copyright © 1989–2016, Texas Instruments Incorporated

## 10.2 Layout Example

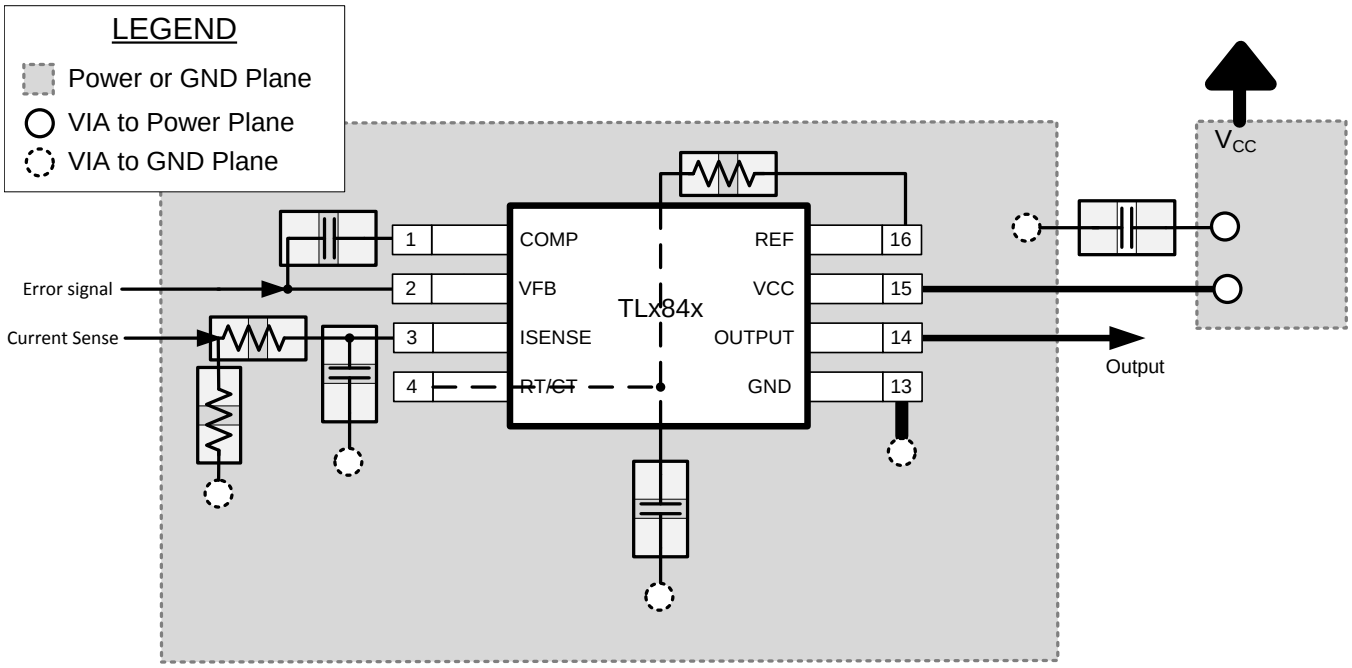



**Figure 18. Layout of D-8 or P Package for TLx84x Devices**


Copyright © 1989–2016, Texas Instruments Incorporated

# 11 Device and Documentation Support

## 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TL2842 | Click here | Click here | Click here | Click here | Click here |
| TL2843 | Click here | Click here | Click here | Click here | Click here |
| TL2844 | Click here | Click here | Click here | Click here | Click here |
| TL2845 | Click here | Click here | Click here | Click here | Click here |
| TL3842 | Click here | Click here | Click here | Click here | Click here |
| TL3843 | Click here | Click here | Click here | Click here | Click here |
| TL3844 | Click here | Click here | Click here | Click here | Click here |
| TL3845 | Click here | Click here | Click here | Click here | Click here |

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 1989–2016, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL2842D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL2842P | Samples |
| TL2843D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DG4-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DRG4-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL2843P | Samples |
| TL2844D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844DRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL2844P | Samples |
| TL2844PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL2844P | Samples |
| TL2845D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL2845D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DG4-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL2845P | Samples |
| TL3842D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842DRE4-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3842P | Samples |
| TL3842PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3842P | Samples |
| TL3843D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3843P | Samples |
| TL3844D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL3844P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3844P | Samples |
| TL3844PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3844P | Samples |
| TL3845D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845D-8 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845DR-8 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3845P | Samples |
| TL3845PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL3845P | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

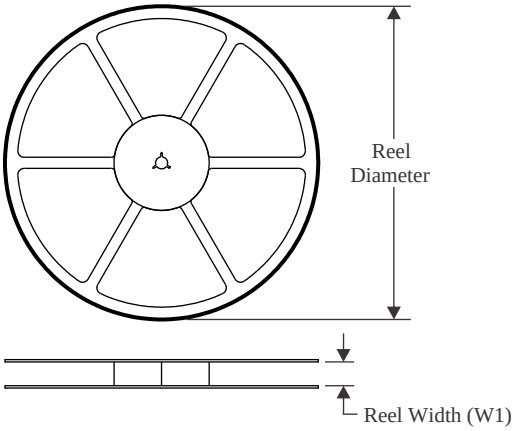
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

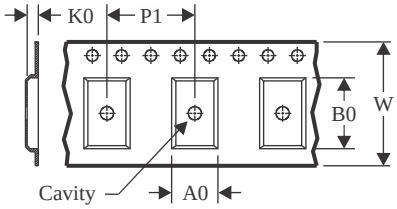
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

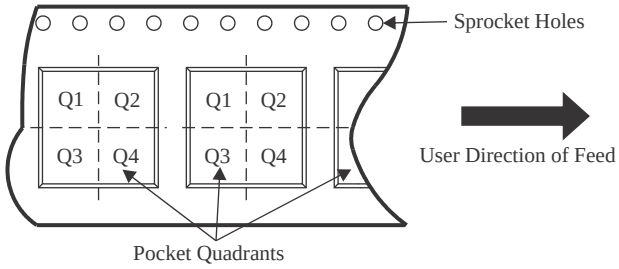



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

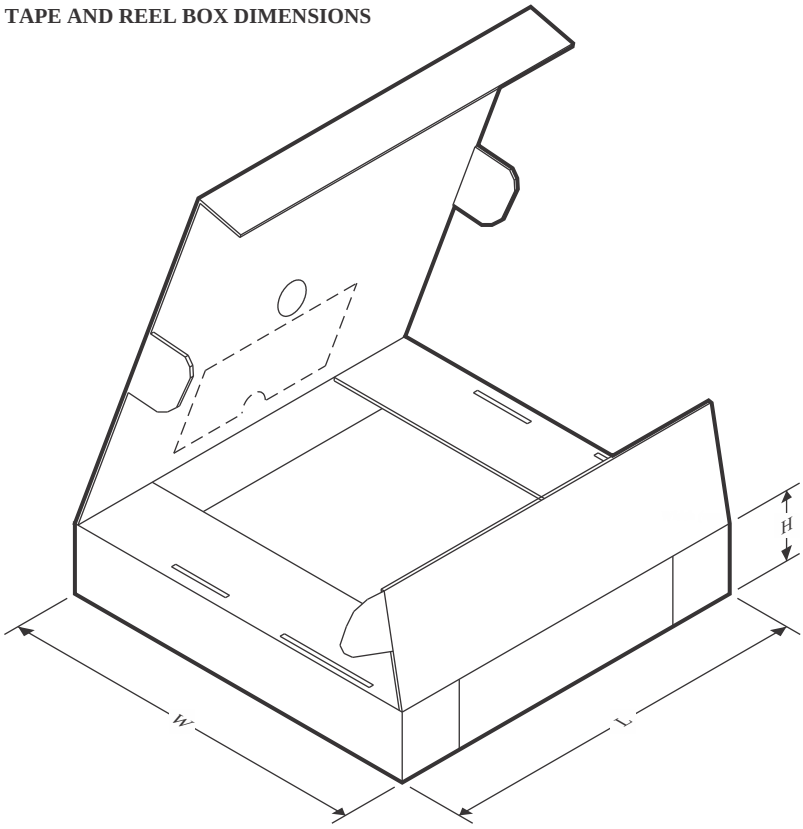



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL2842DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2842DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2843DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2843DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2844DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2845DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2845DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3842DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3842DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3843DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3843DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3844DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL3845DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3845DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

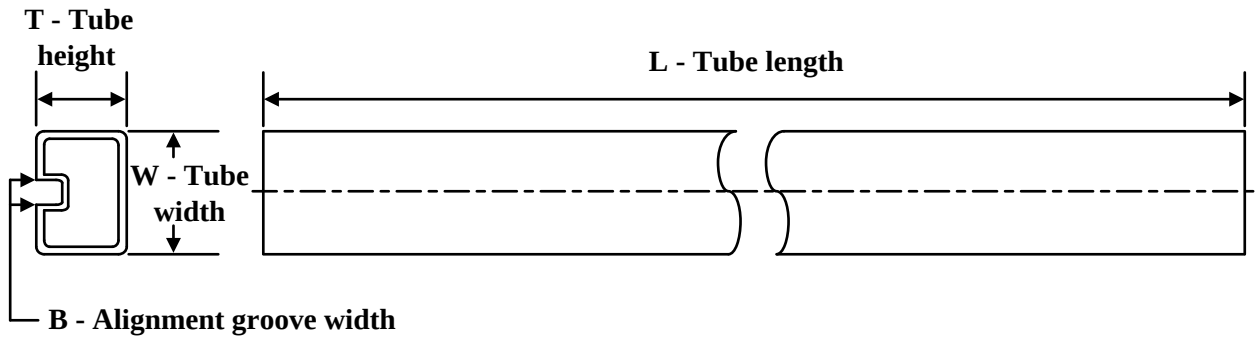
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL2842DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2842DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL2843DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2843DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL2844DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TL2844DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2844DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL2845DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL2845DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3842DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3842DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3843DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3843DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3844DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3844DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TL3844DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL3845DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL3845DR-8 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |

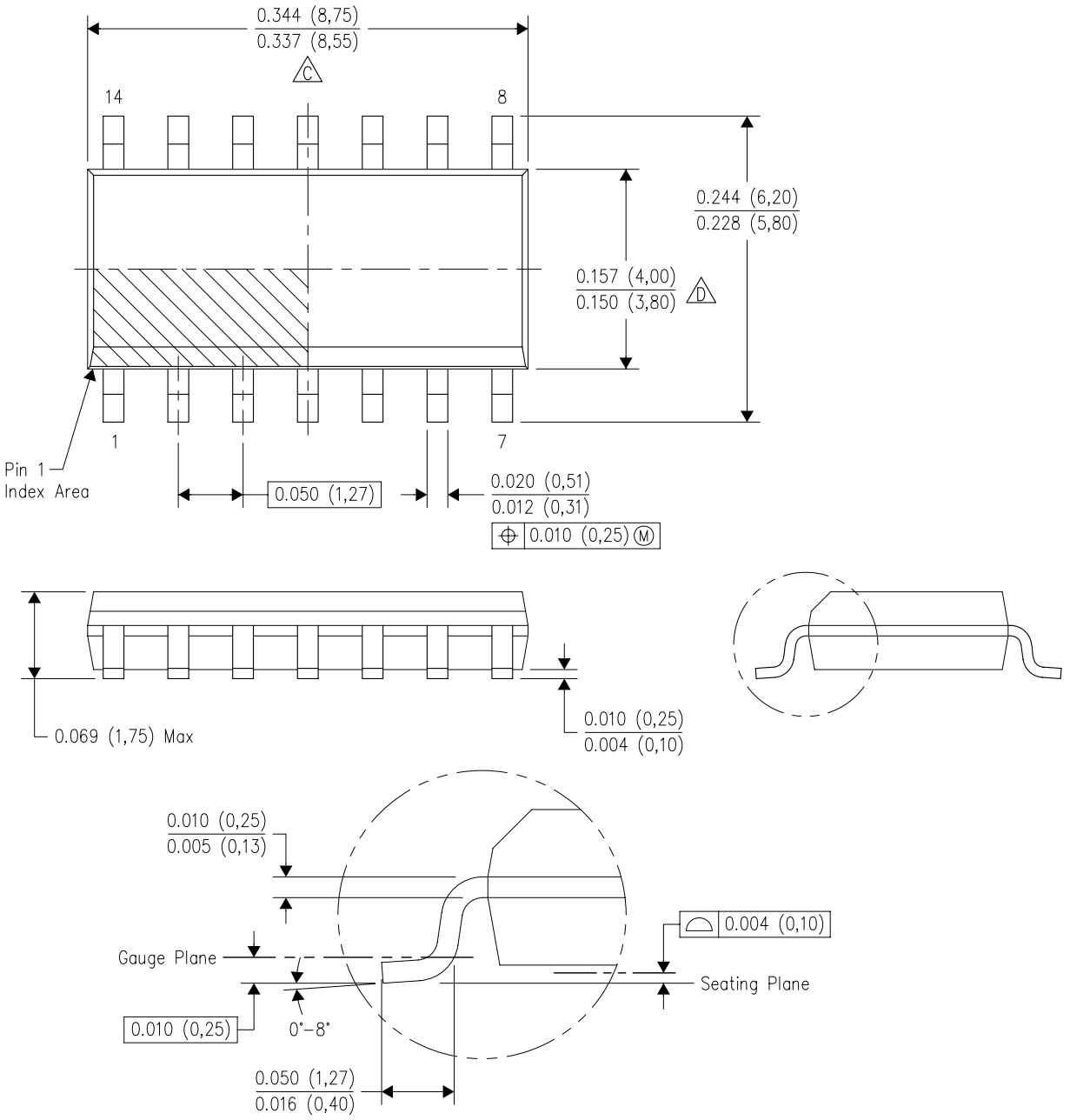
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TL2842D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL2842D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2842P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL2843D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2843DG4-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2843P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL2844D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL2844D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2844P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL2844PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL2845D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL2845D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2845DG4-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL2845P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3842D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3842P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3842PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3843D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL3843D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3843P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3844D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL3844D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3844P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3844PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3845D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL3845D-8 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL3845P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL3845PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

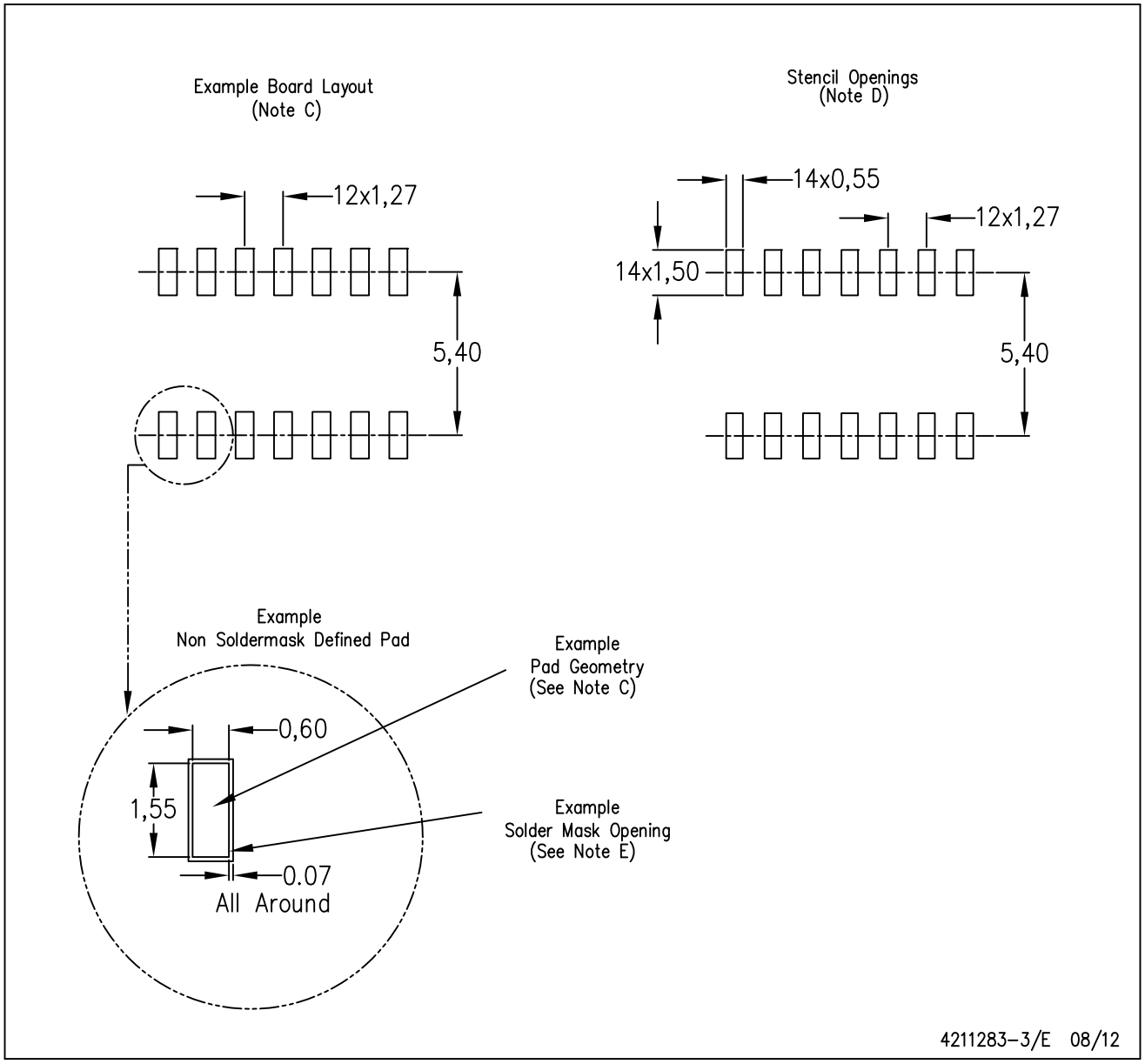
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



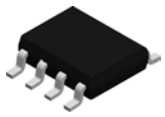

4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

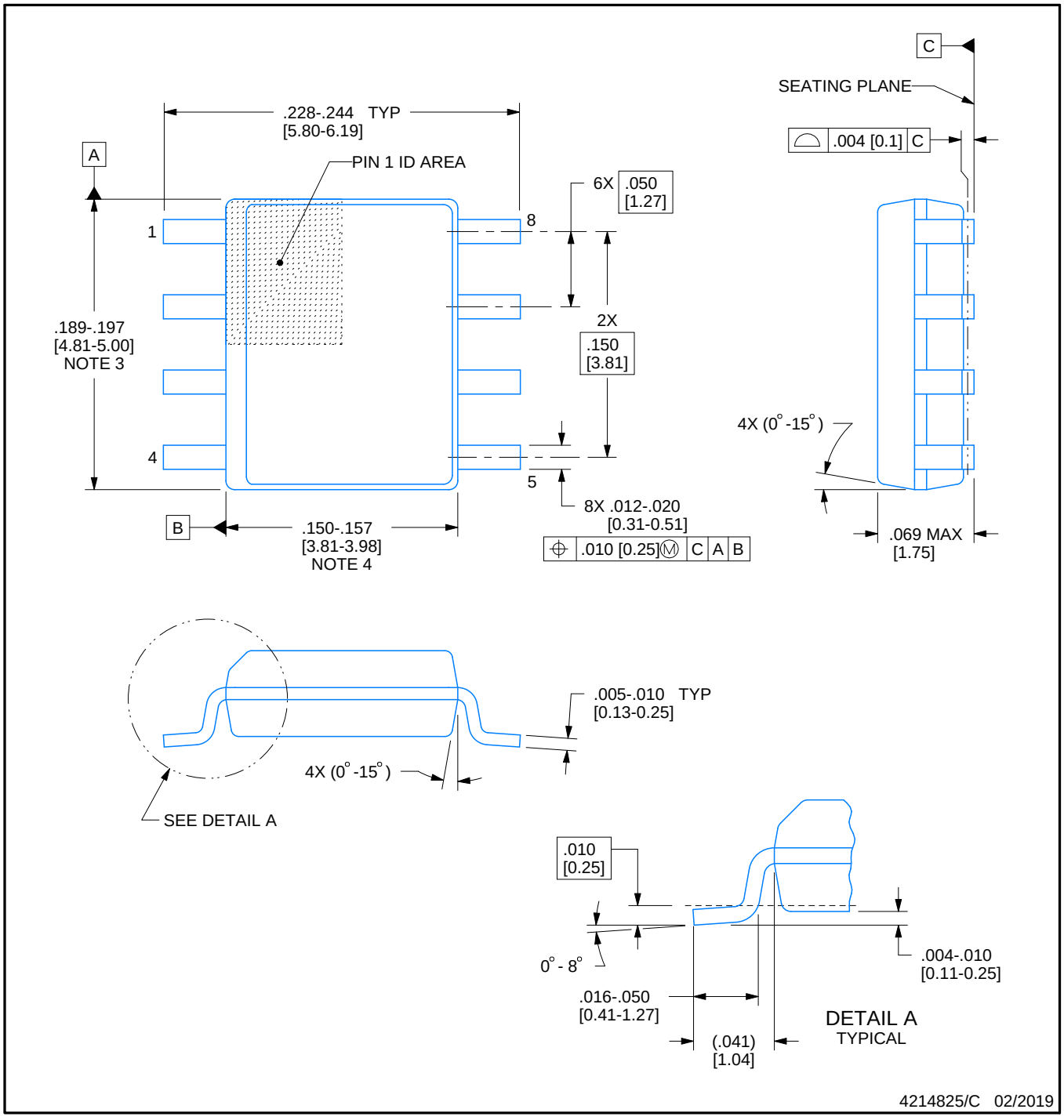


# PACKAGE OUTLINE

## D0008A

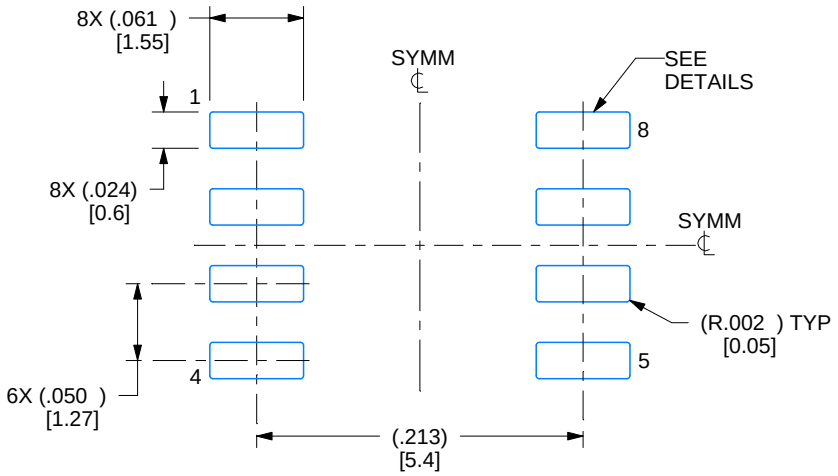
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

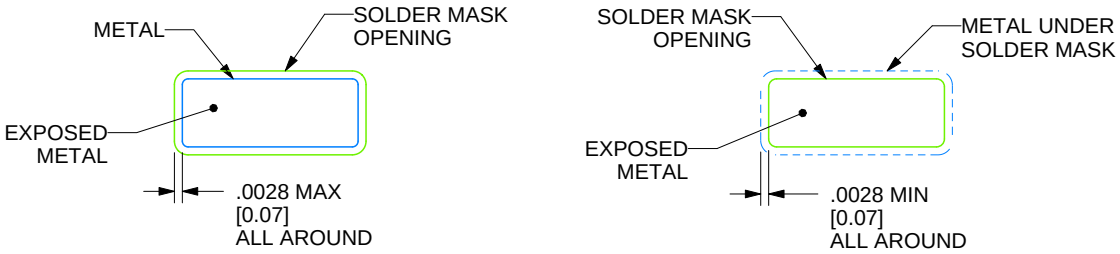



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

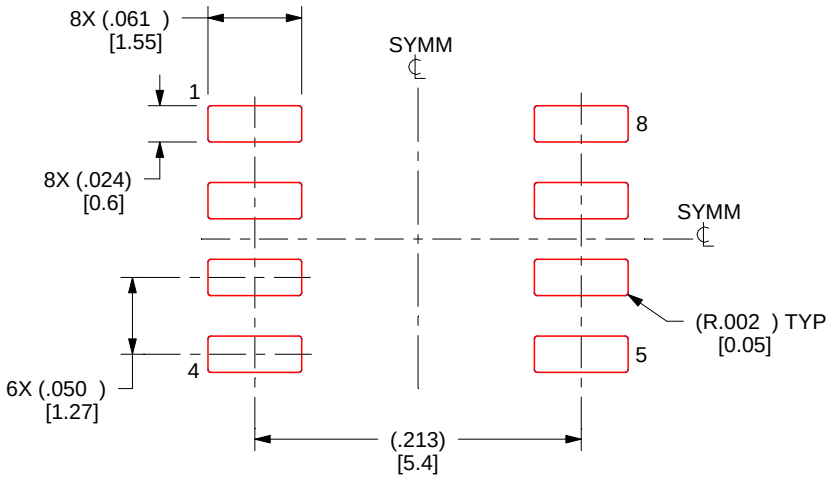
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



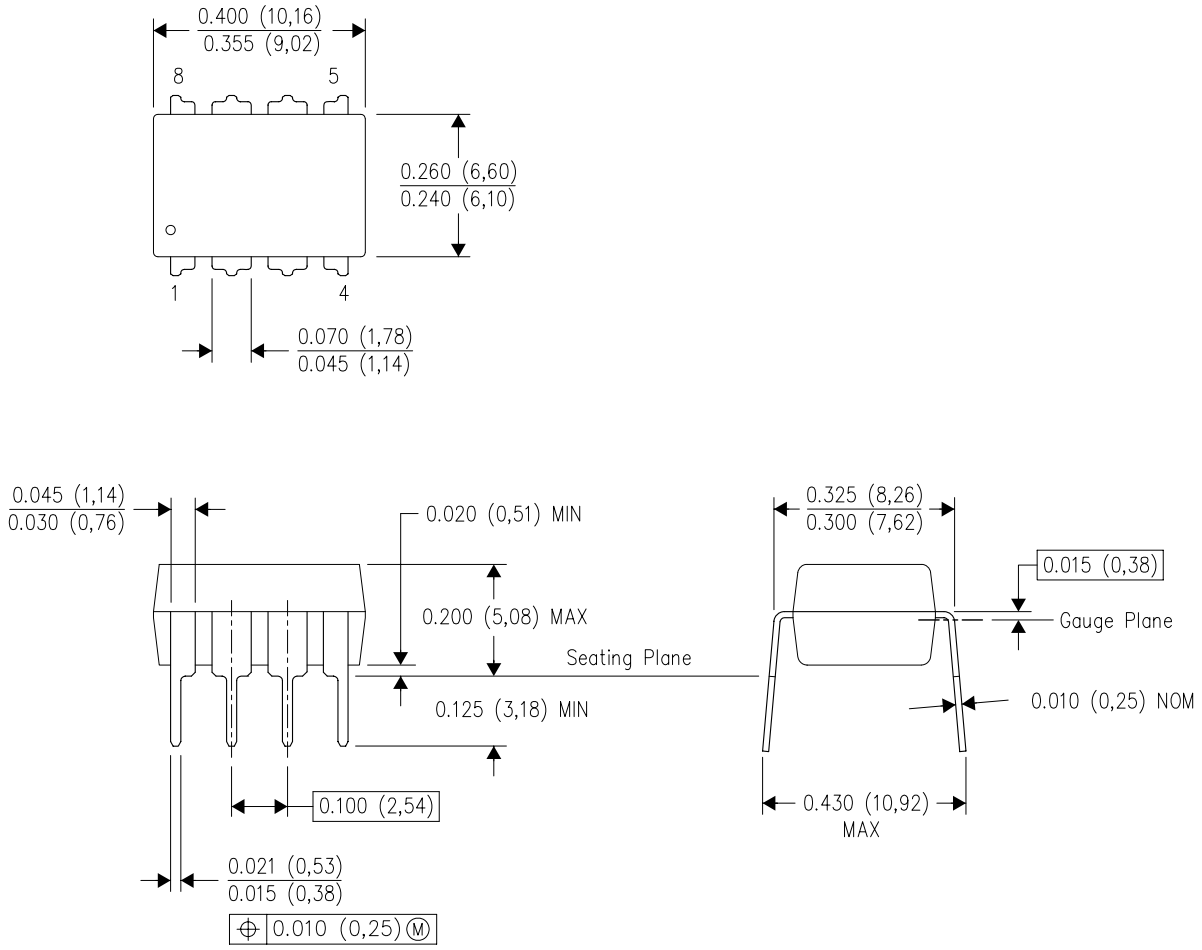

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated