VIPer53 - E

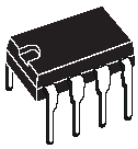
OFF-line primary switch

General features

Type	European (195 - 265Vac)	US / Wide range (85 - 265 Vac)
DIP-8	50W	30W
PowerSO-10™	65W	40W



PowerSO-10



DIP-8

Features

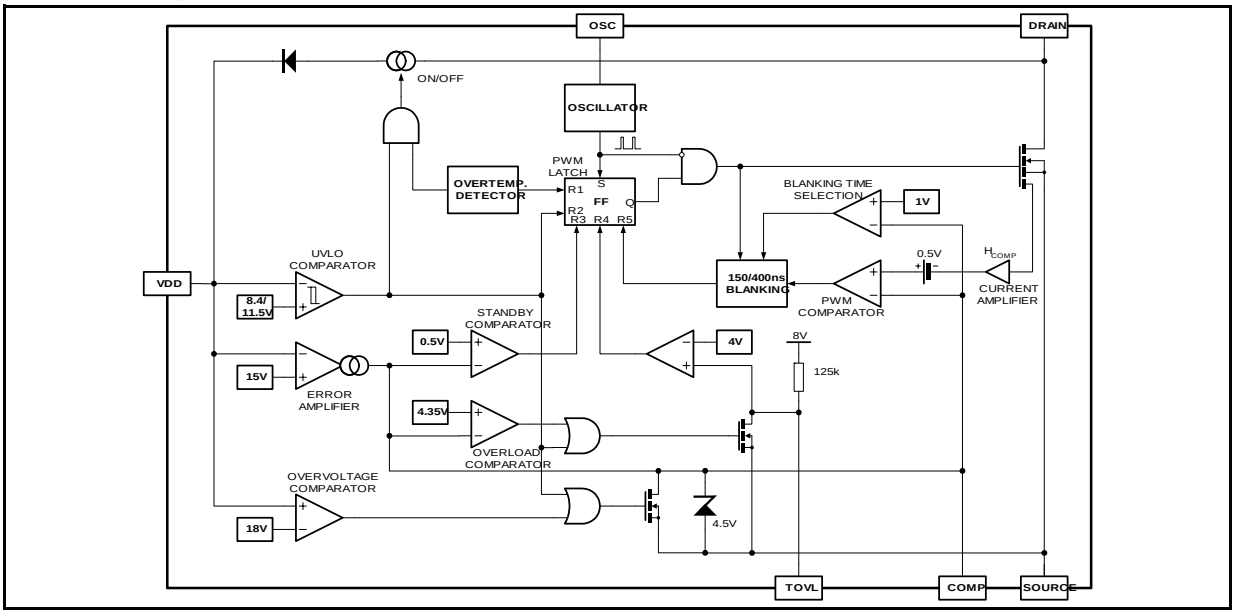
- Switching frequency up to 300kHz
- Current limitation
- Current mode control with adjustable limitation
- Soft start and shut-down control
- Automatic burst mode in standby condition (“Blue Angel“ compliant)
- Undervoltage lockout with Hysteresis
- HIgh voltage star-tup current source
- Overtemperature protection
- Overload and short-circuit control

Description

The VIPer53-E combines an enhanced current mode PWM controller with a high voltage MDMesh Power Mosfet in the same package. Typical applications cover offline power supplies with a secondary power capability ranging up to 30W in wide range input voltage, or 50W in single European voltage range and DIP-8 package, with the following benefits:

- Overload and short circuit controlled by feedback monitoring and delayed device reset.
- Efficient standby mode by enhanced pulse skipping.
- Primary regulation or secondary loop failure protection through high gain error amplifier.

Block diagram



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1 Electrical data

1.1 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DS}	Continuous drain source voltage (T_J= 25 ... 125°C) (1)	-0.3 ... 620	V
I_D	Continuous drain current	Internally limited	A
V_{DD}	Supply voltage	0 ... 19	V
V_{OSC}	OSC input voltage range	0 ... V_{DD}	V
I_{COMP} I_{TOVL}	COMP and TOVL input current range (1)	-2 ... 2	mA
V_{ESD}	Electrostatic discharge: Machine model (R = 0Ω; C = 200pF) Charged device model	 200 1.5	 V kV
T_J	Junction operating temperature	Internally limited	°C
T_C	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. In order to improve the ruggedness of the device versus eventual drain overvoltages, a resistance of 1kΩ should be inserted in series with the TOVL pin.\

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter		PowerSO-10 (1)	DIP-8 (2)	Unit
R_{thJC}	Thermal Resistance Junction-case	Max	2	20	°C/W
R_{thJA}	Thermal Resistance Ambient-case	Max	60	80	°C/W

1. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 mm thick) connected to the DRAIN pin.
2. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 mm thick) connected to the device tab.

2 Electrical characteristics

T_J = 25°C, V_{DD} = 13V, unless otherwise specified

Table 3. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source voltage	I_D = 1mA; V_{COMP} = 0V	620			V
I_{DSS}	Off state drain current	V_{DS} = 500V; V_{COMP} = 0V; T_J = 125°C			150	µA
$R_{DS(on)}$	Static drain-source On state resistance	I_D = 1A; V_{COMP} = 4.5V; V_{TOVL} = 0V T_J = 25°C T_J = 100°C		0.9	 1 1.7	 Ω Ω
t_{fv}	Fall time	I_D = 0.2A; V_{IN} = 300V (1)		100		ns
t_{rv}	Rise time	I_D = 1A; V_{IN} = 300V (1)		50		ns
C_{oss}	Drain capacitance	V_{DS} = 25V		170		pF
C_{Eon}	Effective output capacitance	200V < V_{DSon} < 400V (2)		60		pF

1. On clamped inductive load
2. This parameter can be used to compute the energy dissipated at turn on E_{ton} according to the initial drain to source voltage V_{DSon} and the following formula:

$$E_{ton} = \frac{1}{2} \cdot C_{Eon} \cdot 300^2 \cdot \left(\frac{V_{DSon}}{300}\right)^{1.5}$$

Table 4. Oscillator section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{OSC1}	Oscillator frequency initial accuracy	R_T = 8kΩ; C_T = 2.2nF *Figure 12 on page 12*	95	100	105	kHz
F_{OSC2}	Oscillator frequency total variation	R_T = 8kΩ; C_T = 2.2nF *Figure 16 on page 14* V_{DD} = V_{DDon} ... V_{DDovp}; T_J = 0 ... 100°C	93	100	107	kHz
V_{OSChi}	Oscillator peak voltage			9		V
V_{OSClo}	Oscillator valley voltage			4		V

Table 5. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DSstart}$	Drain voltage starting threshold	V_{DD} = 5V; I_{DD} = 0mA		34	50	V
I_{DDch1}	Startup charging current	V_{DD} = 0 ... 5V; V_{DS} = 100V *Figure 5 on page 10*		-12		mA
I_{DDch2}	Startup charging current	V_{DD} = 10V; V_{DS} = 100V *Figure 5.*		-2		mA
$I_{DDchoff}$	Startup charging current in thermal shutdown	V_{DD} = 5V; V_{DS} = 100V *Figure 7.* $T_J > T_{SD} - T_{HYST}$	0			mA
I_{DD0}	Operating supply current not switching	F_{sw} = 0kHz; V_{COMP} = 0V		8	11	mA
I_{DD1}	Operating supply current switching	F_{sw} = 100kHz		9		mA
V_{DDoff}	V_{DD} undervoltage shutdown threshold	*Figure 5 on page 10*	7.5	8.4	9.3	V
V_{DDon}	V_{DD} startup threshold	*Figure 5.*	10.2	11.5	12.8	V
V_{DDhyst}	V_{DD} threshold hysteresis	*Figure 5.*	2.6	3.1		V
V_{DDovp}	V_{DD} Overvoltage shutdown threshold	*Figure 5.*	17	18	19	V

Table 6. Error amplifier section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DDreg}	V_{DD} regulation point	I_{COMP} = 0mA *Figure 11. on page 11*	14.5	15	15.5	V
ΔV_{DDreg}	V_{DD} regulation point total variation	I_{COMP} = 0mA; T_J = 0 ... 100°C		2		%
G_{BW}	Unity gain bandwidth	From Input = V_{DD} to Output = V_{COMP} I_{COMP} = 0mA *Figure 14* and *15*		700		kHz
AV_{OL}	Voltage gain	I_{COMP} = 0mA *Figure 14* and *15*	40	45		dB
G_m	DC transconductance	V_{COMP} = 2.5V *Figure 11.*	1	1.4	1.8	mS
V_{COMPlo}	Output low level	I_{COMP} = -0.4mA; V_{DD} = 16V		0.2		V
V_{COMPhi}	Output high level	I_{COMP} = 0.4mA; V_{DD}=14V(1)		4.5		V
I_{COMPlo}	Output sinking current	V_{COMP} = 2.5V; V_{DD} = 16V *Figure 11. on page 11*		-0.6		mA
I_{COMPhi}	Output sourcing current	V_{COMP} = 2.5V; V_{DD}= 14V *Figure 11.*		0.6		mA

1. In order to insure a correct stability of the error amplifier, a capacitor of 10nF (minimum value: 8nF) should always be present on the COMP pin.

Table 7. PWM comparator section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
H_{COMP}	ΔV_{COMP} / ΔI_{DPEAK}	V_{COMP} = 1 ... 4 V *Figure 10.* dI_D/dt = 0	1.7	2	2.3	V/A
V_{COMPos}	V_{COMP} Offset	dI_D/dt = 0 *Figure 10. on page 11*		0.5		V
I_{Dlim}	Peak drain current limitation	I_{COMP} = 0mA; V_{TOVL} = 0V *Figure 10.* dI_D/dt = 0	1.7	2	2.3	A
I_{Dmax}	Drain current capability	V_{COMP} = $V_{COMPovl}$; V_{TOVL} = 0V dI_D/dt = 0	1.6	1.9	2.3	A
t_d	Current sense delay to Turn-Off	I_D = 1A		250		ns
V_{COMPbl}	V_{COMP} blanking time change threshold	*Figure 6 on page 10*		1		V
t_{b1}	Blanking time	V_{COMP} < V_{COMPBL} *Figure 6.*	300	400	500	ns
t_{b2}	Blanking time	V_{COMP} > V_{COMPBL} *Figure 6.*	100	150	200	ns
t_{ONmin1}	Minimum On time	V_{COMP} < V_{COMPBL}	450	600	750	ns
t_{ONmin2}	Minimum On time	V_{COMP} > V_{COMPBL}	250	350	450	ns
$V_{COMPoff}$	V_{COMP} Shutdown Threshold	*Figure 9 on page 11*		0.5		V

Table 8. Overload protection section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{COMPovl}$	V_{COMP} overload threshold	I_{TOVL} = 0mA (1) *Figure 4 on page 9*		4.35		V
$V_{DIFFovl}$	V_{COMPhi} to $V_{COMPovl}$ voltage difference	V_{DD} = V_{DDoff} ... V_{DDreg}; I_{TOVL}= 0mA *Figure 4.* (1)	50	150	250	mV
V_{OVLth}	V_{TOVL} overload threshold	*Figure 4.*		4		V
t_{OVL}	Overload delay	C_{OVL} = 100nF *Figure 4.*		8		ms

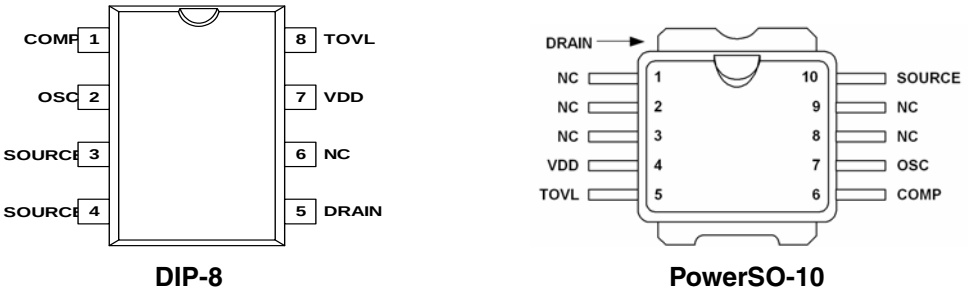
1. $V_{COMPovl}$ is always lower than V_{COMPhi}

Table 9. Over temperature Protection Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{SD}	Thermal shutdown temperature	*Figure 7 on page 10*	140	160		°C
T_{HYST}	Thermal shutdown hysteresis	*Figure 7 on page 10*		40		°C

3 Pin connections and function

Figure 1. Pin connection (top view)



DIP-8 PowerSO-10

Figure 2. Current and voltage conventions

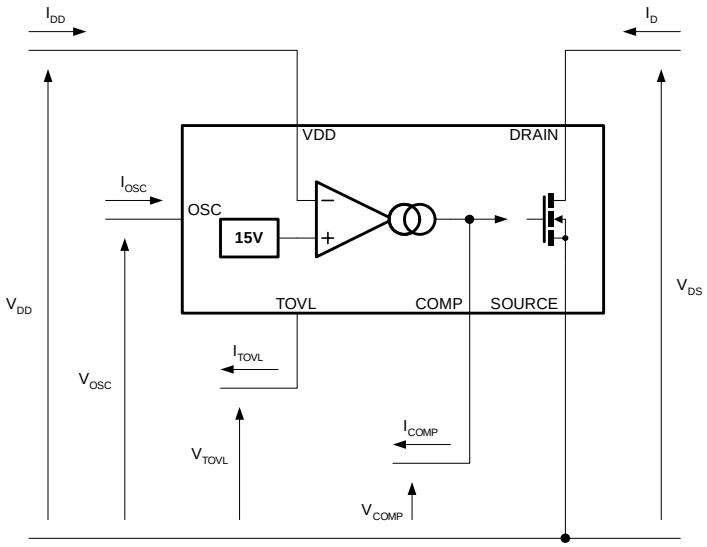


Table 10. Pin function

Pin Name	Pin function
V_{DD}	Power supply of the control circuits. Also provides the charging current of the external capacitor during start-up. The functions of this pin are managed by four threshold voltages: - VDDon: Voltage value at which the device starts switching (Typically 11.5 V). - VDDoff: Voltage value at which the device stops switching (Typically 8.4 V). - VDDreg: Regulation voltage point when working in primary feedback (Trimmed to 15 V). - VDDovp: Triggering voltage of the overvoltage protection (Trimmed to 18 V).
SOURCE	Power MOSFET source and circuit ground reference.
DRAIN	Power MOSFET drain. Also used by the internal high voltage current source during the start-up phase to charge the external V_{DD} capacitor.
COMP	Input of the current mode structure, and output of the internal error amplifier. Allows the setting of thedynamic characteristic of the converter through an external passive network. The useful voltage range extends from 0.5V to 4.5V. The Power MOSFET is always off below 0.5V, and the overload protection is triggered if the voltage exceeds 4.35V. This action is delayed by the timing capacitor connected tothe TOVL pin.
TOVL	Allows the connection of an external capacitor for delaying the overload protection, which is triggered by a voltage on the COMP pin higher than 4.35V.
OSC	Allows the setting of the switching frequency through an external Rt-Ct network.

4 Operation pictures

Figure 3. Rise and fall time

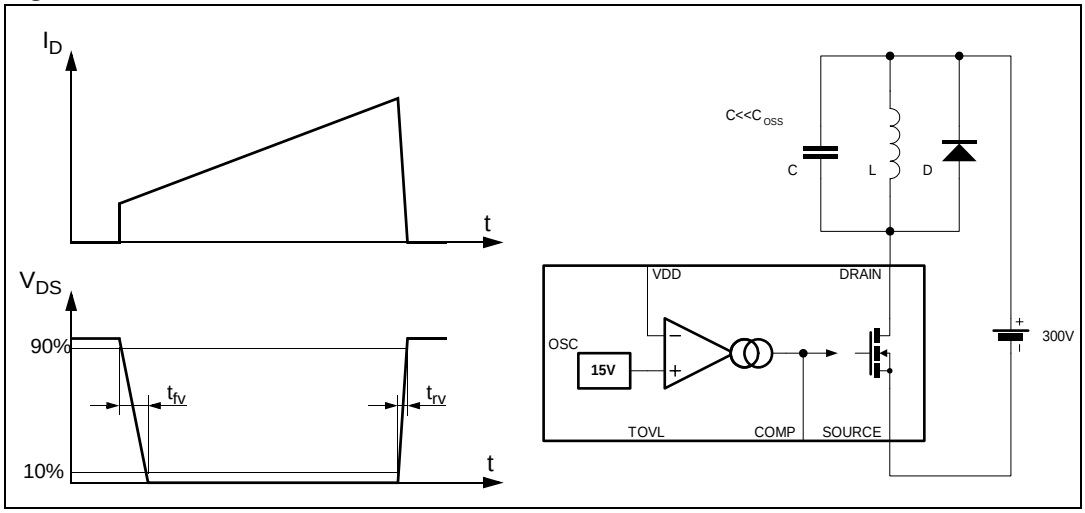


Figure 4. Overloaded event

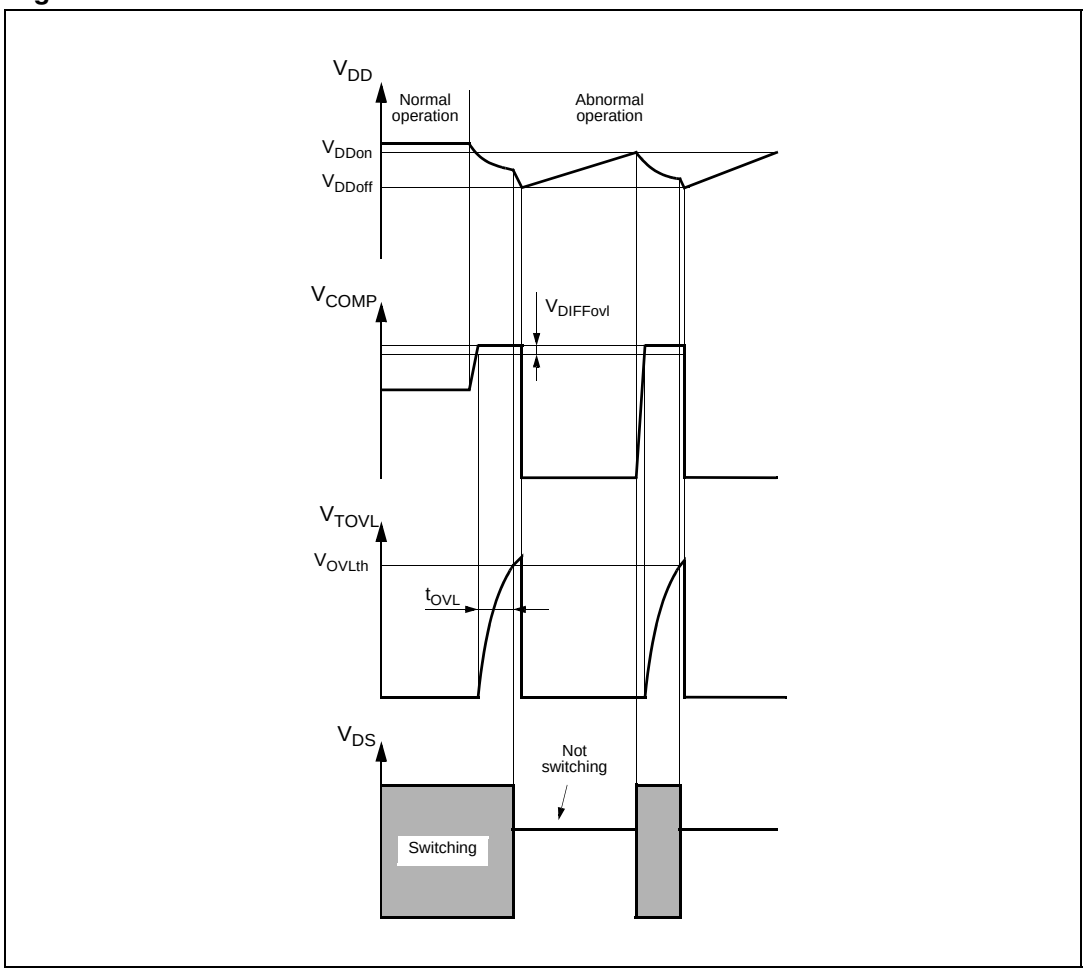


Figure 5. Start-up V_{DD} current

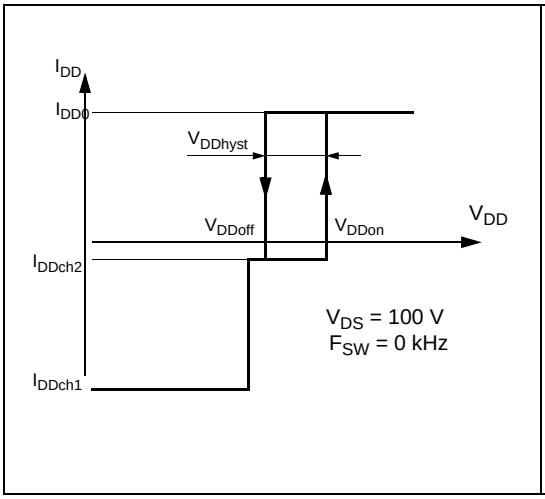


Figure 6. Blanking time

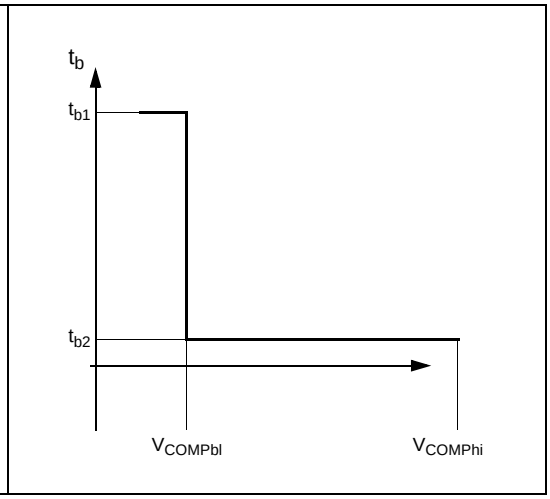


Figure 7. Thermal shutdown

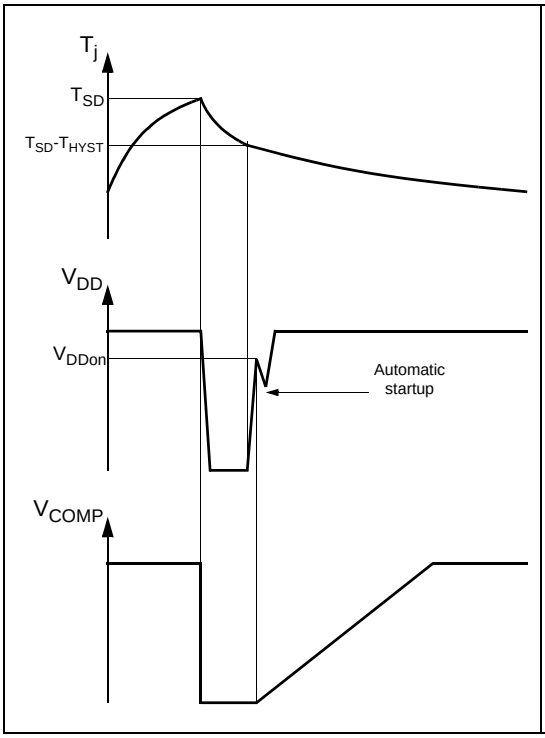


Figure 8. Overvoltage event

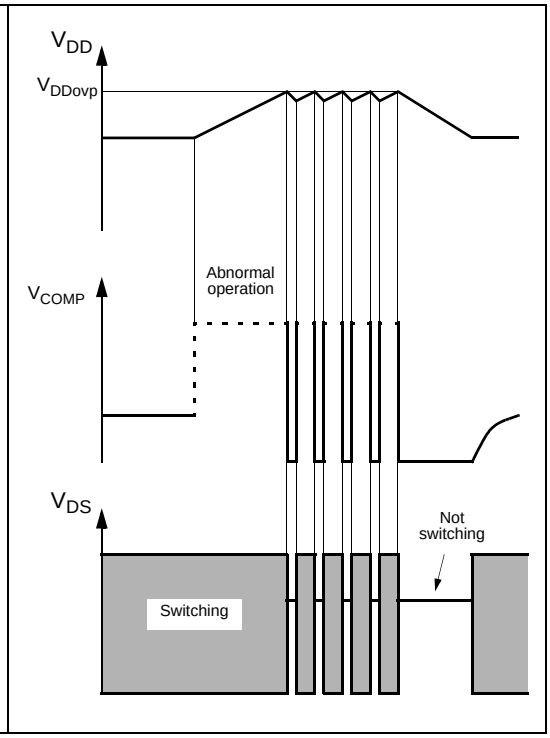


Figure 9. Shutdown action

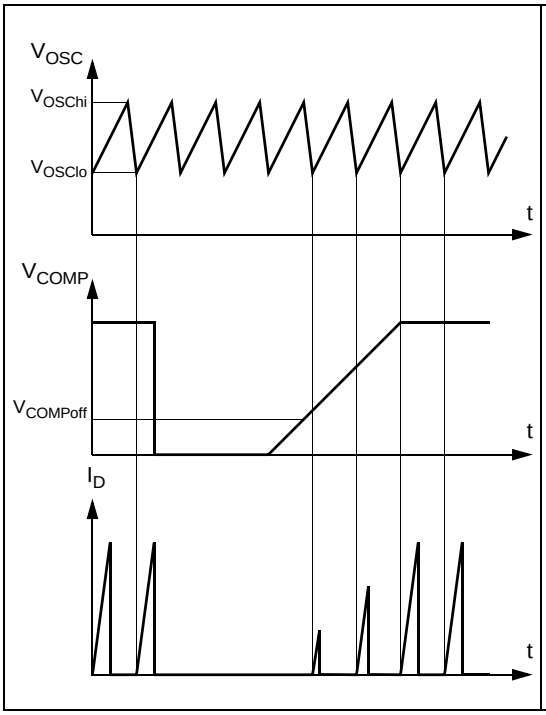


Figure 10. Comp pin gain and offset

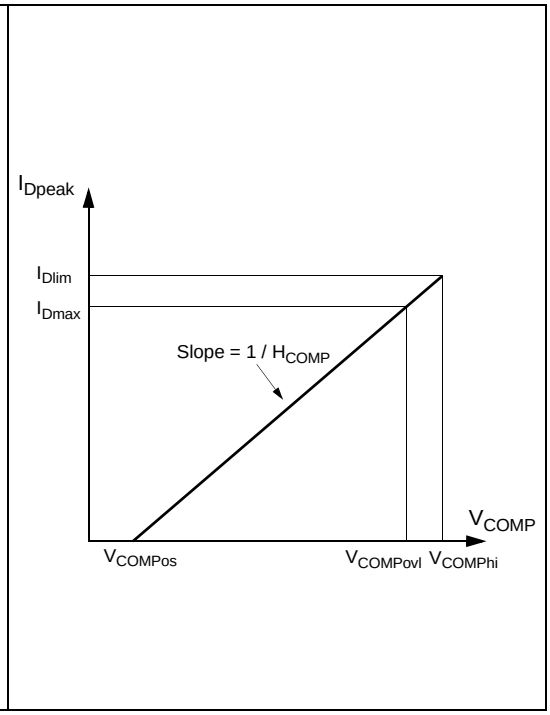


Figure 11. Output characteristics

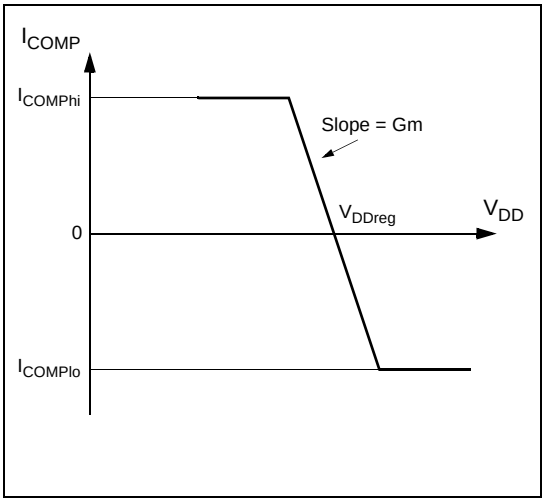
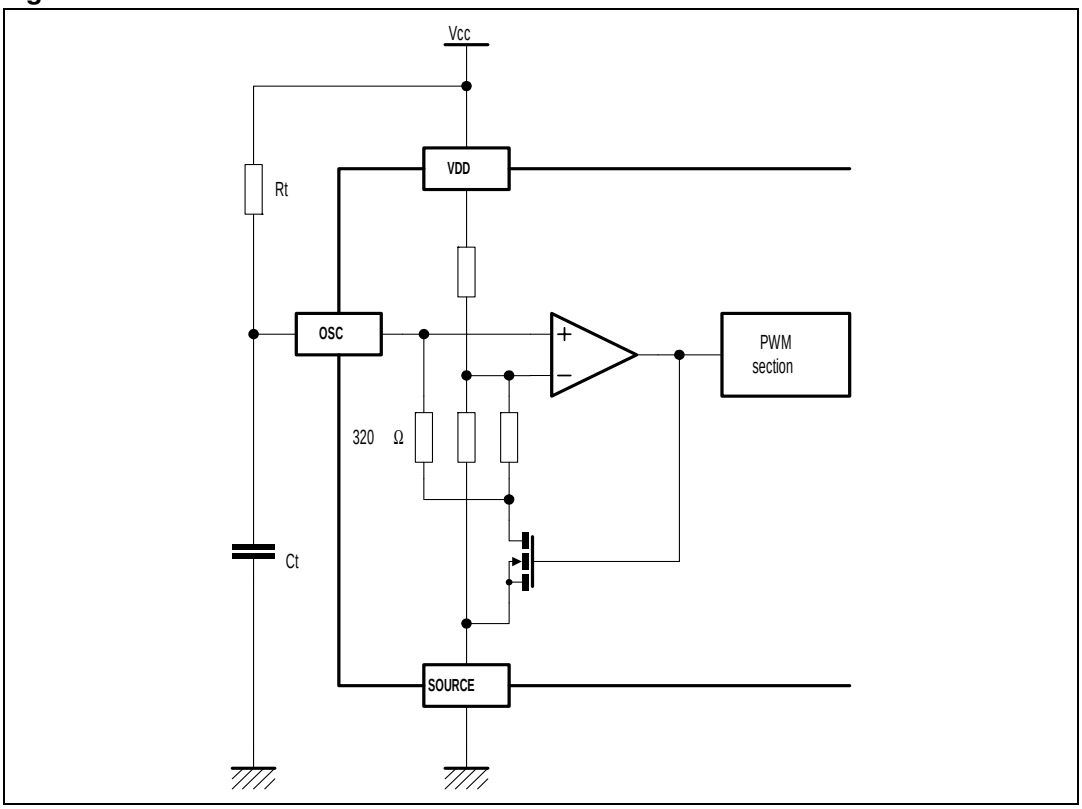


Figure 12. Oscillator schematic



The switching frequency settings shown on the graphic here below is valid within the following boundaries:

$R_t > 2k\Omega$

$F_{SW} = 300kHz$

Figure 13. Oscillator settings

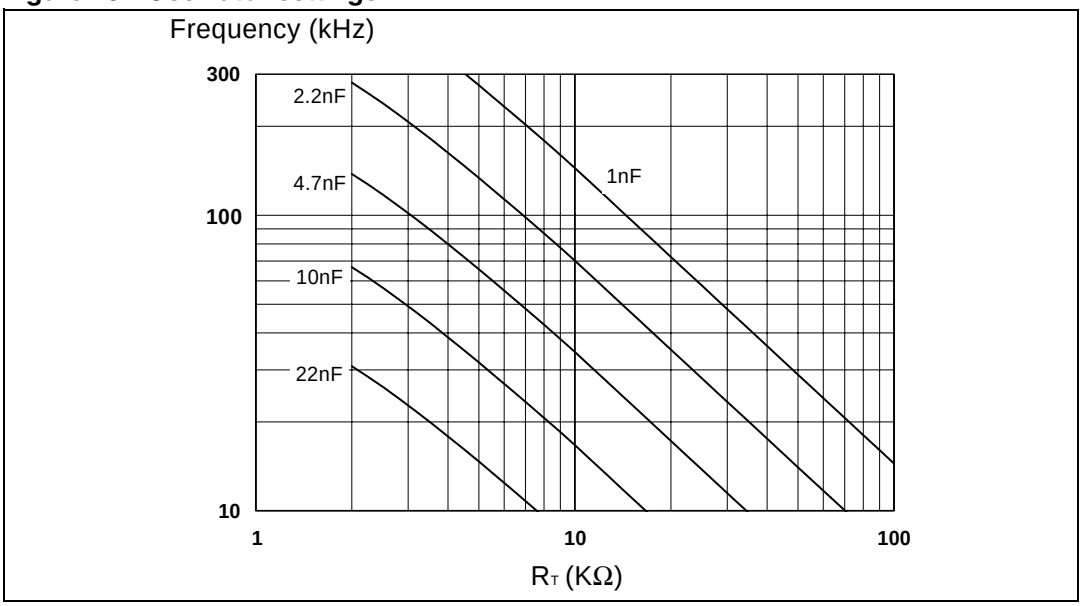
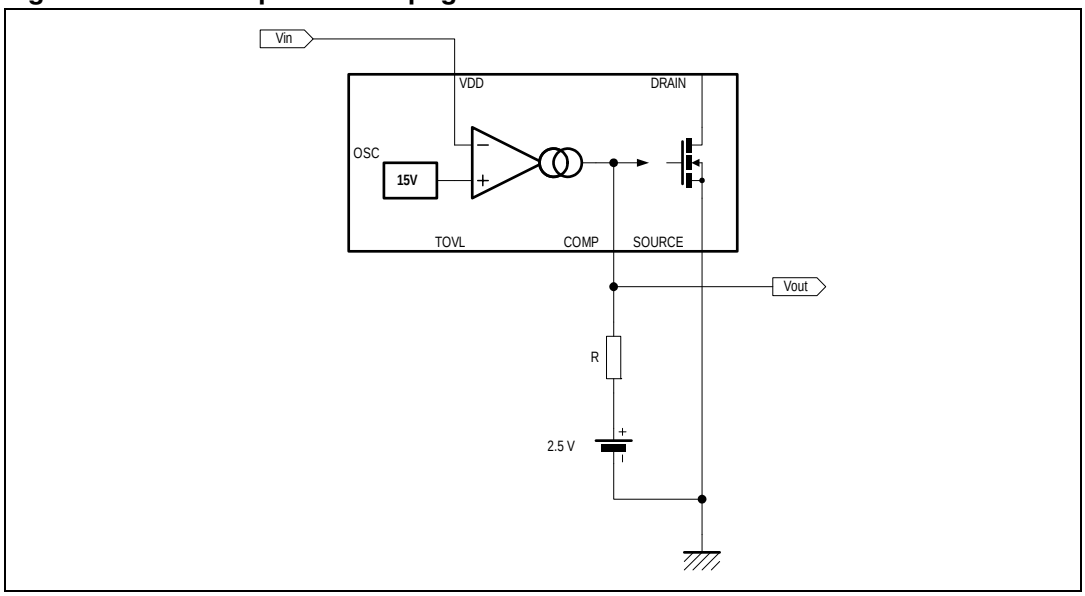


Figure 14. Error amplifier test cpfiguration



This configuration is for test purpose only. In order to insure a correct stability of the error amplifier, a capacitor of 10nF (minimum value: 8nF) should be always connected between COMP pin and ground. See figures *Figure 18*, *19* and *22*.

Figure 15. Error amplifier transfer function

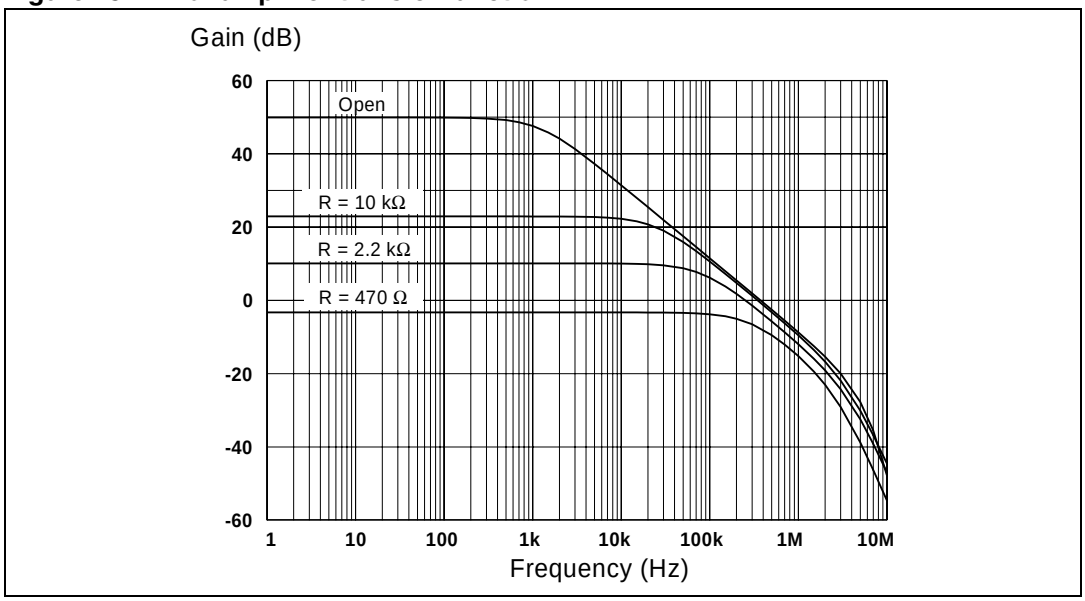


Figure 16. Typical frequency variation vs. junction temperature

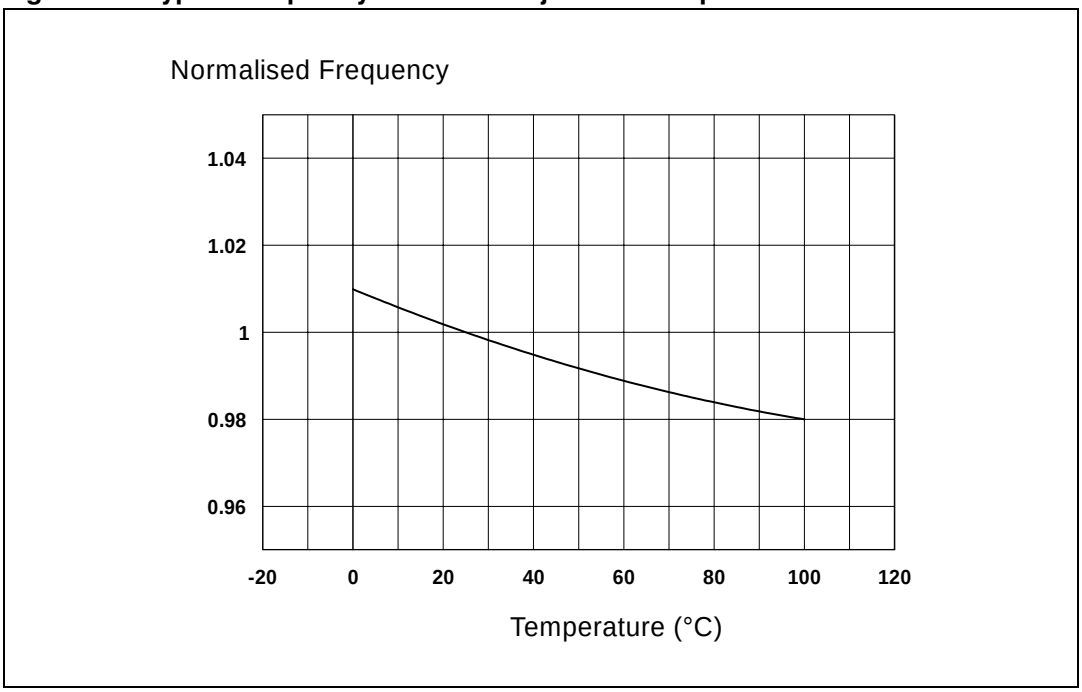
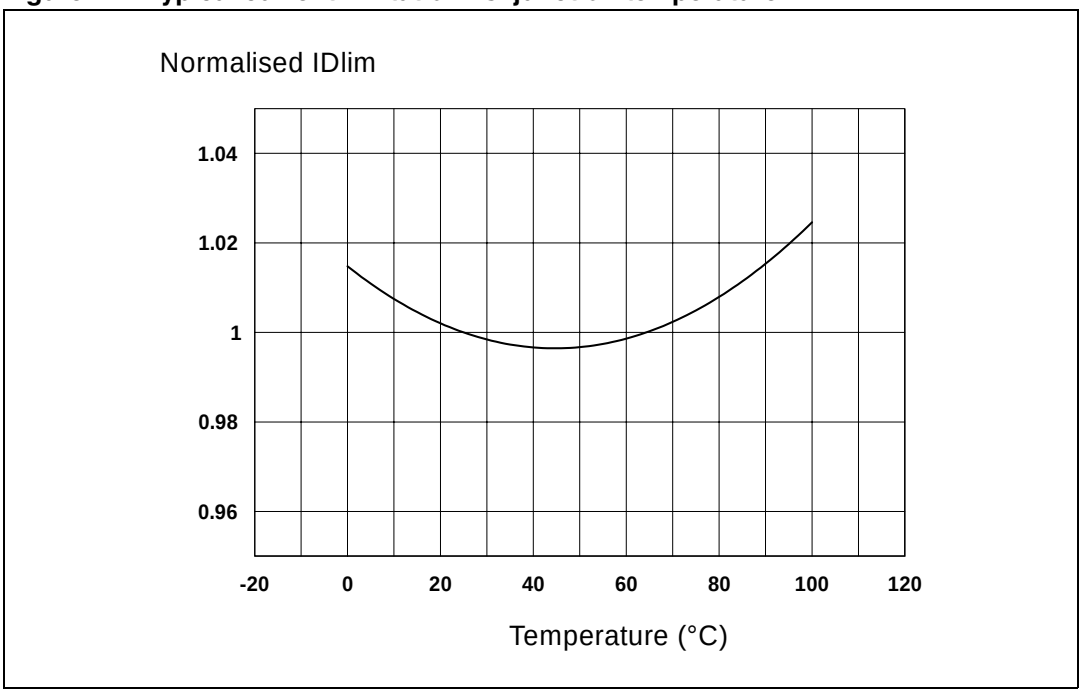
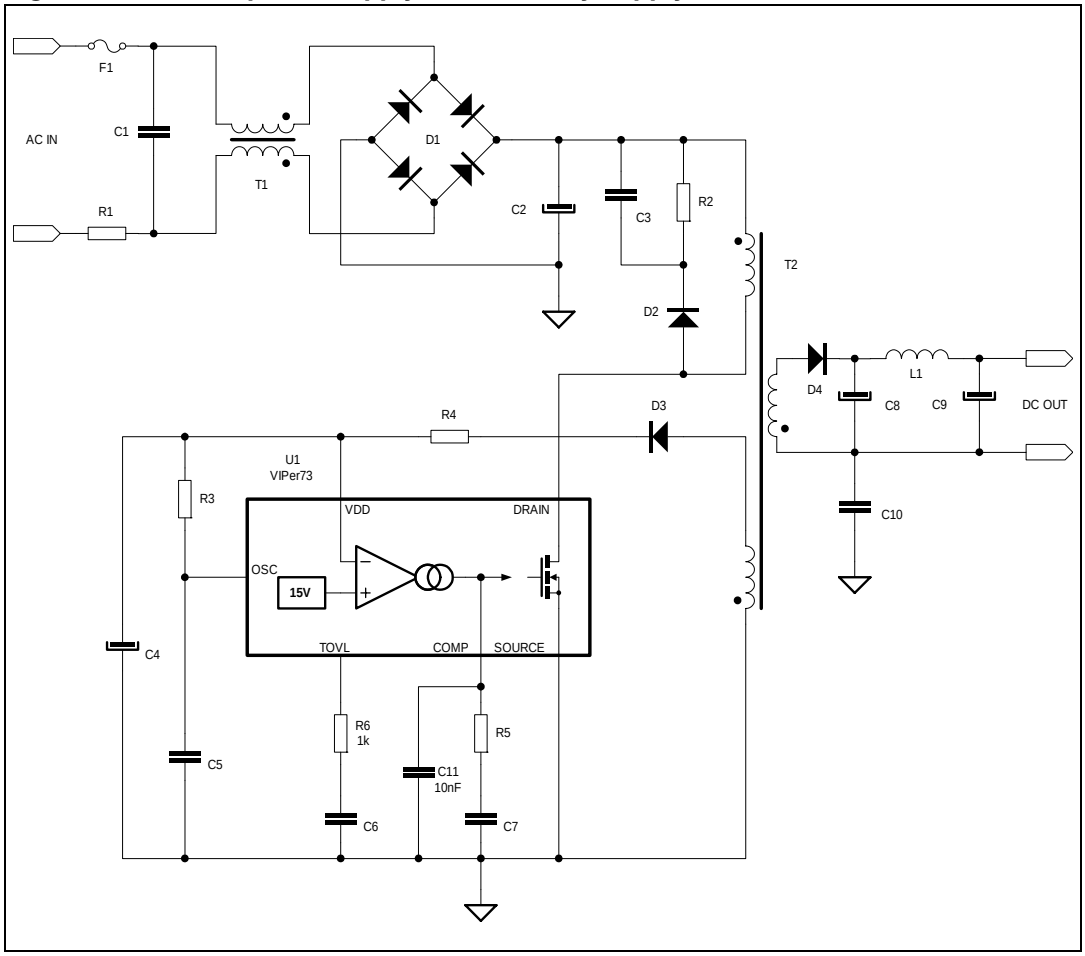


Figure 17. Typical current limitation vs. junction temperature



5 Primary regulation configuration example

Figure 18. Off line power supply with auxiliary supply feedback



The schematic on *Figure 18* delivers a fixed output voltage by using the internal error amplifier of the device in a primary feedback configuration. The primary auxiliary winding provides a voltage to the V_{DD} pin, and is automatically regulated at 15V, due to the internal error amplifier connected to this pin. The secondary voltage has to be adjusted through the turn ratio of the transformer between auxiliary and secondary.

The error amplifier of the VIPer53 is a transconductance type: its output is a current proportional to the difference of voltage between the V_{DD} pin and the internally trimmed 15V reference (i.e., the error voltage). As the transconductance value is set at a relatively low value to control the overall loop gain and ensure stability, this current has to be integrated by a capacitor (C7 in *Figure 18*). When the steady state operation is reached, this capacitor blocks any DC current from the COMP pin and imposes a “nil” error voltage. Therefore, the V_{DD} voltage is accurately regulated to 15V.

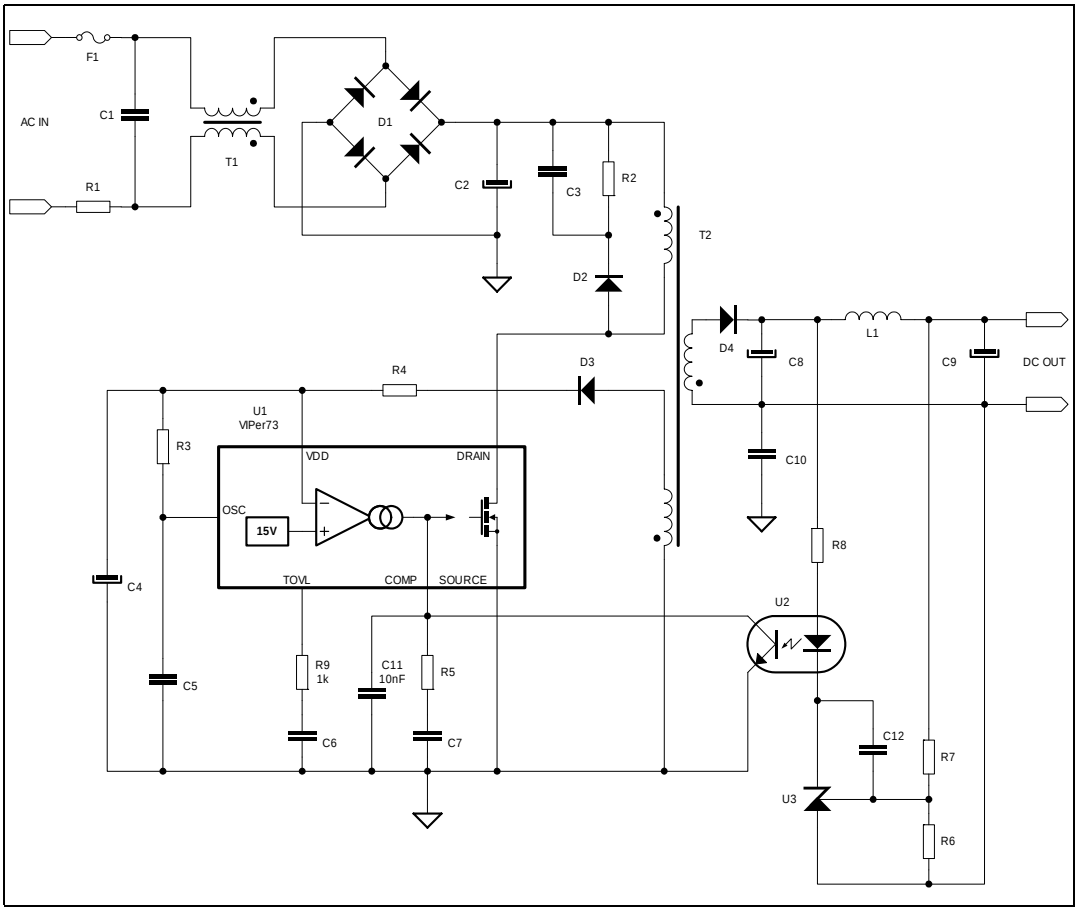
This results in a good load regulation, which depends only on transformer coupling and output diodes impedance. The current mode structure takes care of all incoming voltage changes, thus providing at the same time an excellent line regulation.

The switching frequency can be set to any value through the choice of R3 and C5. This allows to optimize the efficiency of the converter by adopting the best compromise between switching losses, EMI (Lower with low switching frequencies) and transformer size (Smaller with high switching frequencies). For an output power of a few watts, typical switching frequencies between 20kHz and 40kHz because of the small size of the transformer. For higher power, 70kHz to 130kHz are generally chosen.

The R5 compensation resistor value sets the dynamic behavior of the converter. It can be adjusted to provide the best compromise between stability and recovery time with fast load changes.

6 Secondary feedback configuration example

Figure 19. Off line power supply with optocoupler feedback



When a more accurate output voltage is needed, the way is to monitor it directly secondary side, and drive the PWM controller through an optocoupler as shown on *Figure 17.*

The optocoupler is connected in parallel with the compensation network on the COMP pin. The design of the auxiliary winding that the VDD voltage is always lower than the internal 15V reference. The internal error amplifier will therefore be saturated in the high state, and because of its transconductance nature, will deliver a constant biasing current of 0.6mA to the optotransistor. This current does not depend on the compensation voltage, and so it does not depend on the output load either. Consequently, the gain of the optocoupler ensures consequently a constant biasing of the TL431 device (U3) which is in charge of secondary regulation. If the optocoupler gain is sufficiently low, no additional components are required to ensure a minimum current biasing of U3. Also, the low biasing current value avoid any ageing of the optocoupler.

The constant current biasing can be used to simplify the secondary circuit: Instead of a TL431, a simple zener and resistance network in series with the optocoupler diode can insure a good secondary regulation. As the current flowing in this branch remains constant for the same reason as above, typical load regulation of 1% can be achieved from zero to full output current with this simple configuration.

Since the dynamic characteristics of the converter are set on the secondary side through components associated to U3, the compensation network has only a role of gain stabilization for the optocoupler, and its value can be freely chosen. R5 can be set to a fixed value of 1kΩ, offering the possibility of using C7 as a soft start capacitor: When starting up the converter, the VIPer53 device delivers a constant current of 0.6 mA on the COMP pin, creating a constant voltage of 0.6V in R5 and a rising slope across C7. This voltage shape, together with the operating range of 0.5V to 4.5V provides a soft start-up of the converter. The rising speed of the output voltage can be set through the value of C7. The C4 and C6 values must be adjusted accordingly in order to ensure a correct start-up.

7 Current mode topology

The VIPer53-E implements the conventional current mode control method for regulating the output voltage. This kind of feedback includes two nested regulation loops:

The inner loop controls the peak primary current cycle by cycle. When the Power MOSFET output transistor is on, the inductor current (primary side of the transformer) is monitored with a SenseFET technique and converted into a voltage. When Vs reaches V_{COMP}, the power switch is turned off. This structure is completely integrated as shown on the Block Diagram *on page 1*, with the current amplifier, the PWM comparator, the blanking time function and the PWM latch. The following formula gives the peak current in the Power MOSFET according to the compensation voltage:

Equation 1

$$I_{Dpeak} = \frac{V_{COMP} - V_{COMPos}}{H_{COMP}}$$

The outer loop defines the level at which the inner loop regulates peak current in the power switch. For this purpose, V_{COMP} is driven by the feedback network (TL431 through an optocoupler in secondary feedback configuration, see *Figure 19 on page 17*) and is sets accordingly the peak drain current for each switching cycle.

As the inner loop regulates the peak primary current in the primary side of the transformer, all input voltage changes are compensated for before impacting the output voltage. This results in an improved line regulation, instantaneous correction to line changes, and better stability for the voltage regulation loop.

Current mode topology also provides a good converter start-up control. The compensation voltage can be controlled to increase slowly during the start-up phase, so the peak primary current will follow this soft voltage slope to provide a smooth output voltage rise, without any overshoot. The simpler voltage mode structure which only controls the duty cycle, leads generally to high current at start-up with the risk of transformer saturation.

An integrated blanking filter inhibits the PWM comparator output for a short time after the integrated Power MOSFET is switched on. This function prevents anomalous or premature termination of the switching pulse in the case of current spikes caused by primary side transformer capacitance or secondary side rectifier reverse recovery time when working in continuous mode.

8 Standby mode

The device offers a special feature to address the low load condition. The corresponding function described hereafter consists of reducing the switching frequency by going into burst mode, with the following benefits:

– It reduces the switching losses, thus providing low consumption on the mains lines. The device is compliant with “Blue Angel” and other similar standards, requiring less than 0.5 W of input power when in standby.

– It allows the regulation of the output voltage, even if the load corresponds to a duty cycle that the device is not able to generate because of the internal blanking time, and associated minimum turn on.

For this purpose, a comparator monitores the COMP pin voltage, and maintains the PWM latch and the Power MOSFET in the Off state as long as V_{COMP} remains below 0.5V (See Block Diagram *on page 1*). If the output load requires a duty cycle below the one defined by the minimum turn on of the device, the V_{COMP} net decreases its voltage until it reaches this 0.5V threshold ($V_{COMPoff}$). The Power MOSFET can be completely Off for some cycles, and resumes normal operation as soon as V_{COMP} is higher than 0.5V. The output voltage is regulated in burst mode. The corresponding ripple is not higher than the nominal one at full load.

In addition, the minimum turn on time which defines the frontier between normal operation and burst mode changes according to V_{COMP} value. Below 1.0V (V_{COMPbl}), the blanking time increases to 400ns, whereas for higher voltages, it is 150ns *Figure 6 on page 10* The minimum turn on times resulting from these values are respectively 600 ns and 350 ns, when taking into account internal propagation time. This brutal change induces an hysteresis between normal operation and burst mode as shown on *Figure 20 on page 21*.

When the output power decreases, the system reaches point 2 where V_{COMP} equals V_{COMPbl}. The minimum turn-on time passes immediately from 350ns to 600ns, exceeding the effective turn-on time that should be needed at this output power level. Therefore the regulation loop will quickly drive V_{COMP} to $V_{COMPoff}$ (Point 3) in order to pass into burst mode and to control the output voltage. The corresponding hysteresis can be seen on the switching frequency which passes from F_{SWnom} which is the normal switching frequency set by the components connected to the OSC pin and to FSWstby. Note: This frequency is actually an equivalent number of switching pulses per second, rather than a fixed switching frequency since the device is working in burst mode.

As long as the power remains below P_{RST} the output of the regulation loop remains stuck at V_{COMPsd} and the converter works in burst mode. Its “density” increases (i.e. the number of missing cycles decreases) as the power approaches P_{RST} and finally resumes normal operation at point 1. The hysteresis cannot be seen on the switching frequency, but it can be seen in the sudden surge of the COMP pin voltage from point 3 to point 1 at that power level.

The power points value P_{RST} and P_{STBY} are defined by the following formulas:

Equation 2

$$P_{RST} = \frac{1}{2} \bullet F_{SWnom} \bullet (tb_1 + td)^2 \bullet V^2IN \bullet \frac{1}{Lp}$$

Equation 3

$$P_{STBY} = \frac{1}{2} \bullet F_{SWnom} \bullet Ip^2(V_{COMPbl}) \bullet Lp$$

Where $Ip(V_{COMPbl}^2)$ is the peak Power MOSFET current corresponding to a compensation voltage of V_{COMPbl} (1V).

Note: The power point PSTBY where the converter is going into burst mode does not depend on the input voltage.

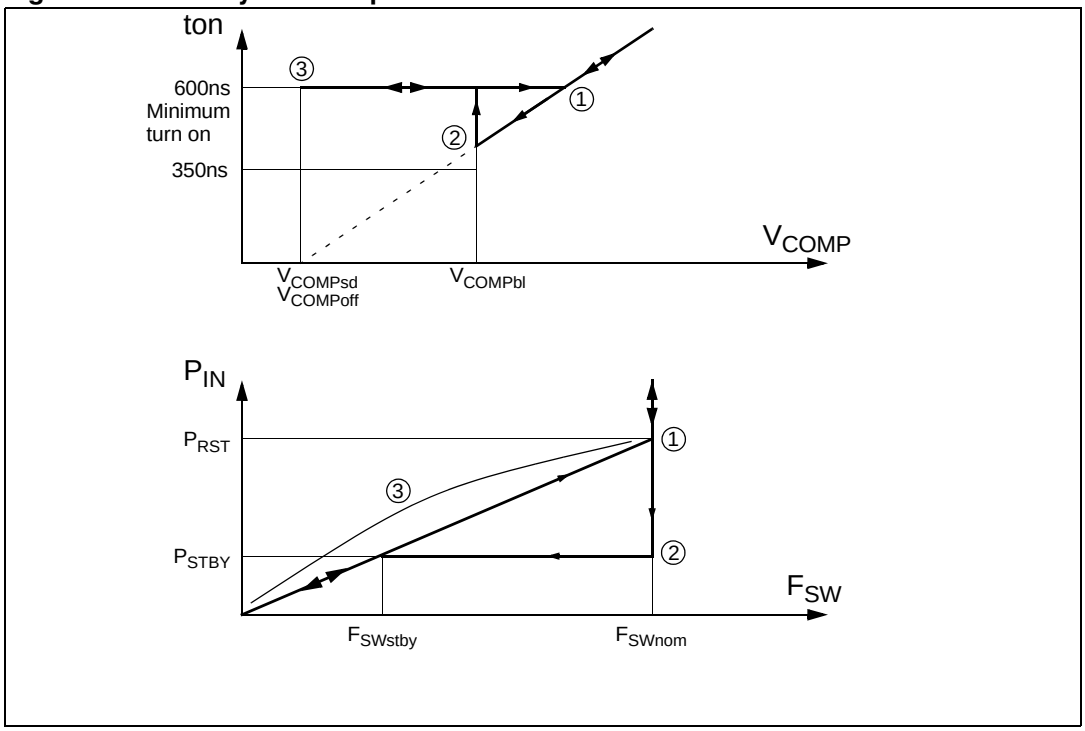
The standby frequency F_{SWstby} is given by:

Equation 4

$$P_{SWstby} = \frac{P_{STBY}}{P_{RST}} \bullet F_{SWnom}$$

The ratio between the nominal and standby switching frequencies can be as high as 4, depending on the Lp value and input voltage.

Figure 20. Standby mode implementation



9 High voltage Start-up current source

An integrated high voltage current source provides a bias current from the DRAIN pin during the start-up phase. This current is partially absorbed by internal control circuits in standby mode with reduced consumption, and also supplies the external capacitor connected to the V_{DD} pin. As soon as the voltage on this pin reaches the high voltage threshold V_{DDon} of the UVLO logic, the device turns into active mode and starts switching. The start-up current generator is switched off, and the converter should normally provide the needed current on the V_{DD} pin through the auxiliary winding of the transformer, as shown on *Figure 19 on page 17*.

The external capacitor C_{VDD} on the V_{DD} pin must be sized according to the time needed by the converter to start-up, when the device starts switching. This time tss depends on many parameters, including transformer design, output capacitors, soft start feature, and compensation network implemented on the COMP pin and possible secondary feedback circuit.

The following formula can be used for defining the minimum capacitor needed:

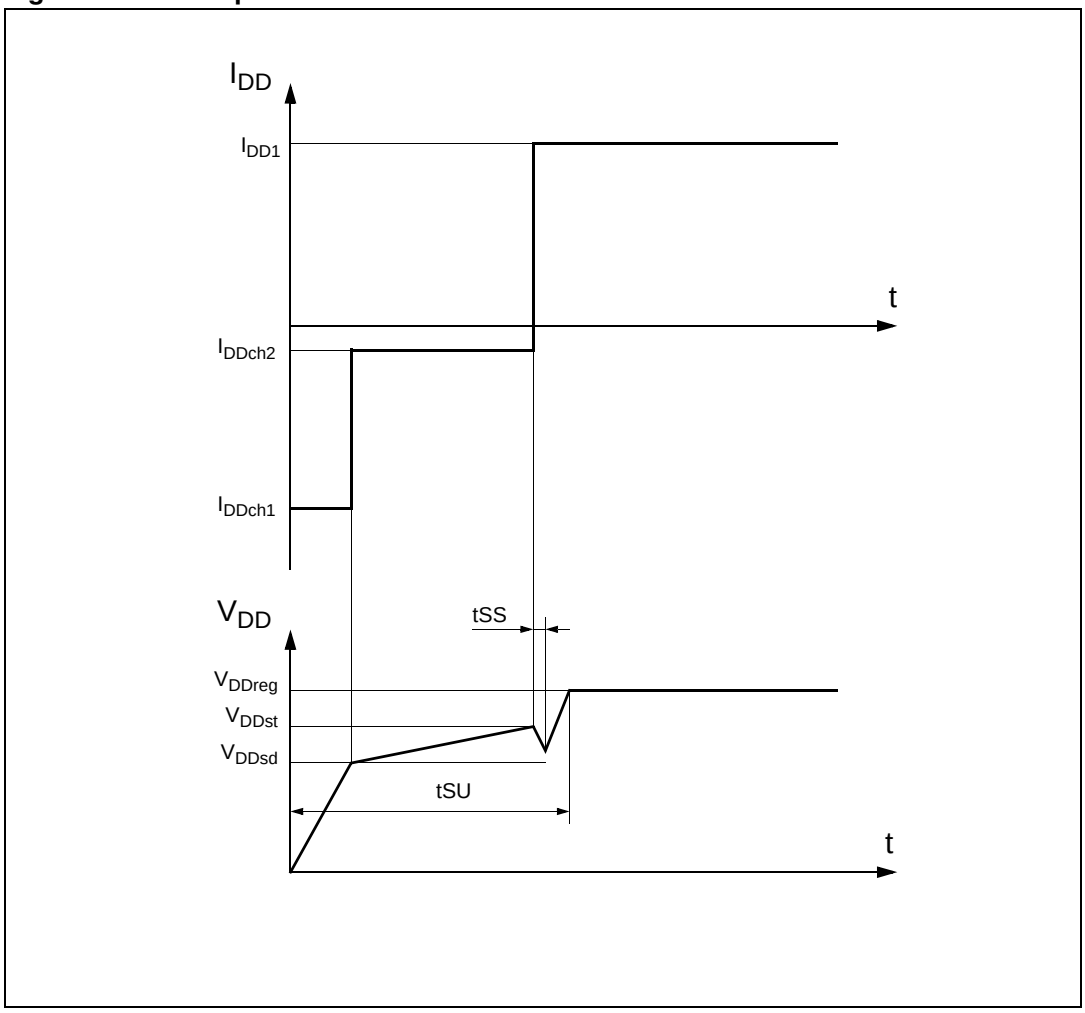
Equation 5

$$C_{VDD} > \frac{I_{DD1} \cdot tss}{V_{DDhyst}}$$

Figure 21 on page 23 shows a typical start-up event. V_{DD} starts from 0V with a charging current I_{DDch1} at about 9 mA. When about V_{DDoff} is reached, the charging current is reduced down to I_{DDch2} which is about 0.6mA. This lower current leads to a slope change on the V_{DD} rise. Device starts switching for V_{DD} equal to V_{DDon}, and the auxiliary winding delivers some energy to V_{DD} capacitor after the start-up time tss.

The charging current change at V_{DDoff} allows a fast complete start-up time t_{SDU}, and maintains a low restart duty cycle. This is especially useful for short circuits and overloads conditions, as described in the following section.

Figure 21. Start-up waveforms



10 Short-circuit and overload protection

A $V_{COMPovl}$ threshold of about 4.35V has been implemented on the COMP pin. When V_{COMP} goes above this level, the capacitor connected on the TOVL pin begins to charge. When reaching typically V_{OVLth} (4V), the internal MOSFET driver is disabled and the device stops switching. This state is latched because of to the regulation loop which maintains the COMP pin voltage above the $V_{COMPovl}$ threshold. Since the V_{DD} pin does not receive any more energy from the auxiliary winding, its voltage drops down until it reaches V_{DDoff} and the device is reset, recharging the V_{DD} capacitor for a new restart cycle. Note: If VCOMP drops below the $V_{COMPovl}$ threshold for any reason during the VDD drop, the device resumes switching immediately.

The device enters an endless restart sequence if the overload or short circuit condition is maintained. The restart duty cycle D_{RST} is defined as the time ratio for which the device tries to restart, thus delivering its full power capability to the output. In order to keep the whole converter in a safe state during this event, D_{RST} must be kept as low as possible, without compromising the real start-up of the converter. A typical value of about 10% is generally sufficient. For this purpose, both V_{DD} and TOVL capacitors can be used to satisfy the following conditions:

Equation 6

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot tss$$

Equation 7

$$C_{VDD} > 8 \cdot 10^{4} \cdot \left(\frac{1}{D_{RST}} - 1\right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

Refer to the previous start-up section for the definition of tss, and C_{VDD} must also be checked against the limit given in this section. The maximum value of the two calculus will be adopted.

All this behavior can be observed on *Figure 8 on page 10*. In *Figure 10 on page 11* the value of the drain current Id for $V_{COMP} = V_{COMPovl}$ is shown. The corresponding parameter I_{Dmax} is the drain current to take into account for design purposes. Since I_{Dmax} represents the maximum value for which the overload protection is not triggered, it defines the power capability of the power supply.

11 Transconductance error amplifier

The VIPer53-E includes a transconductance error amplifier. Transconductance Gm is the change in output current I_{COMP} versus change in input voltage V_{DD}. Thus:

Equation 8

$$Gm = \frac{\partial I_{COMP}}{\partial V_{DD}}$$

The output impedance Z_{COMP} at the output of this amplifier (COMP pin) can be defined as:

Equation 9

$$Z_{COMP} = \frac{\partial V_{COMP}}{\partial I_{COMP}} = \frac{1}{Gm} \cdot \frac{\partial V_{COMP}}{\partial V_{DD}}$$

This last equation shows that the open loop gain A_{VOL} can be related to Gm and Z_{COMP}:

Equation 10

$$A_{VOL} = Gm \cdot Z_{COMP}$$

where Gm value for VIPer53 is typically 1.4mA/V.

Gm is well defined by specification, but $Z_{COMP,}$ and therefore $A_{VOL,}$ are subject to large tolerances. An impedance Z must be connected between the COMP pin and ground in order to accurately define the transfer function F of the error amplifier, the following equation, very similar to the one above:

Equation 11

$$F(s) = Gm \cdot Z(s)$$

The error amplifier frequency response is shown in .0 for different values of a simple resistance connected on the COMP pin. The unloaded transconductance error amplifier shows an internal Z_{COMP} of about 140KΩ More complex impedances can be connected on the COMP pin to achieve different compensation methods. A capacitor provides an integrator function, thus eliminating the DC static error, and a resistance in series leads to a flat gain at higher frequency, introducing a zero level and ensuring a correct phase margin. This configuration illustrated in *Figure 22*, for the schematic and *Figure 23 on page 28* for the error amplifier transfer function for a typical set of values of C_{COMP} and R_{COMP}

Note that a 10nF capacitor (8nF, minimum value) should always be connected to the COMP pin to ensure a correct stability of the internal error amplifier.

The complete converter open loop transfer function can be built from both power cell and error amplifier transfer functions. A theoretical example can be seen in *Figure 24* for a discontinuous mode flyback loaded by a simple resistor, regulated from primary side (no

optocoupler, the internal error amplifier is fully used for regulation). A typical schematic corresponding to this situation can be seen on *Figure 18*.

The transfer function of the power cell is represented as G(s) in *Figure 24* lexhibits a pole which depends on the output load and on the output capacitor value. As the load of a converter may change, two curves are shown for two different values of output resistance value, R_{L1} and R_{L2}. A zero at higher frequency values then appears, due to the output capacitor ESR. Note: The overall transfer function does not depend on the input voltage because of the current mode control.

The error amplifier has a fixed behavior, similar to the one shown in *Figure 23*. Its bandwidth is to avoid injection of high frequency noise in the current mode section. A zero due to the R_{COMP}-C_{COMP} network is set at the same value as the maximum load R_{L2} pole.

The total transfer function is shown as F(s). G(s) at the bottom of *Figure 24*. For maximum load (plain line), the load pole is exactly compensated by the zero of the error amplifier, and the result is a perfect first order decreasing until it reaches the zero of the output capacitor ESR. The error amplifier cut-off then definitely any further spurious noise or resonance from disturbing the regulation loop.

The point where the complete transfer function has a unity gain is known as the regulation bandwidth and has:

- The higher it is, the faster the reaction will be to an eventual load change, and the smaller the output voltage change will be.
- The phase shift in the complete system at this point has to be less than 135° to ensure good stability. Generally, a first-order slope gives 90° of phase shift, and a second-order gives 180°.

In *Figure 24*, the unity gain is reached in a first order slope, so the stability is ensured.

The dynamic load regulation is improved by increasing the regulation bandwidth, but some limitations have to be respected: As the transfer function above the zero due the capacitor ESR is not reliable (The ESR itself is not well specified, and other parasitic effects may take place), the bandwidth should always be lower than the minimum of F_C and ESR zero.

As the highest bandwidth is obtained with the highest output power (Plain line with R_{L2} load in *Figure 24*), the above criteria will be checked for this condition and allows to define the value of R_{COMP} as the error amplifier gain depends only on this value for this frequency range. The following formula can be derived:

Equation 12

$$R_{COMP} = \sqrt{\frac{P_{OUT2}}{P_{MAX}}} \cdot \frac{F_{BW2} \cdot R_{L2} \cdot C_{OUT}}{Gm}$$

With: $P_{OUT2} = \frac{V_{OUT}^2}{R_{L2}}$ and: $P_{MAX} = \frac{1}{2} \cdot L_P \cdot I_{LIM}^2 \cdot F_{SW}$

The lowest load gives another condition for stability: The frequency F_{BW1} must not encounter the second order slope generated by the load pole and the integrator part of the error amplifier. This condition can be met by adjusting the C_{COMP} value:

Equation 13

$$C_{COMP} > \frac{R_{L1} \cdot C_{OUT}}{6.3 \cdot Gm \cdot R_{COMP}^2} \cdot \sqrt{\frac{P_{OUT1}}{P_{MAX}}}$$

With: $P_{OUT1} = \frac{V_{OUT}^2}{R_{L1}}$

The above formula gives a minimum value for C_{COMP}. It can be then increased to provide a natural soft start function as this capacitor is charged by the error amplifier current capacity I_{COMPhi} at start-up.

Figure 22. Typical compensation network

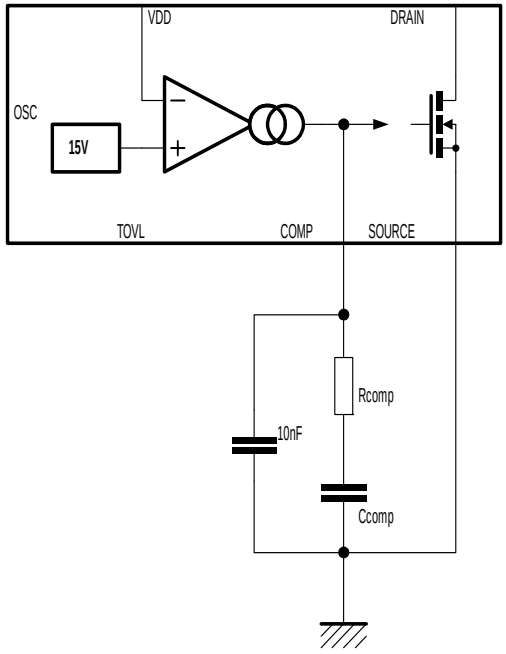


Figure 23. Typical transfer functions

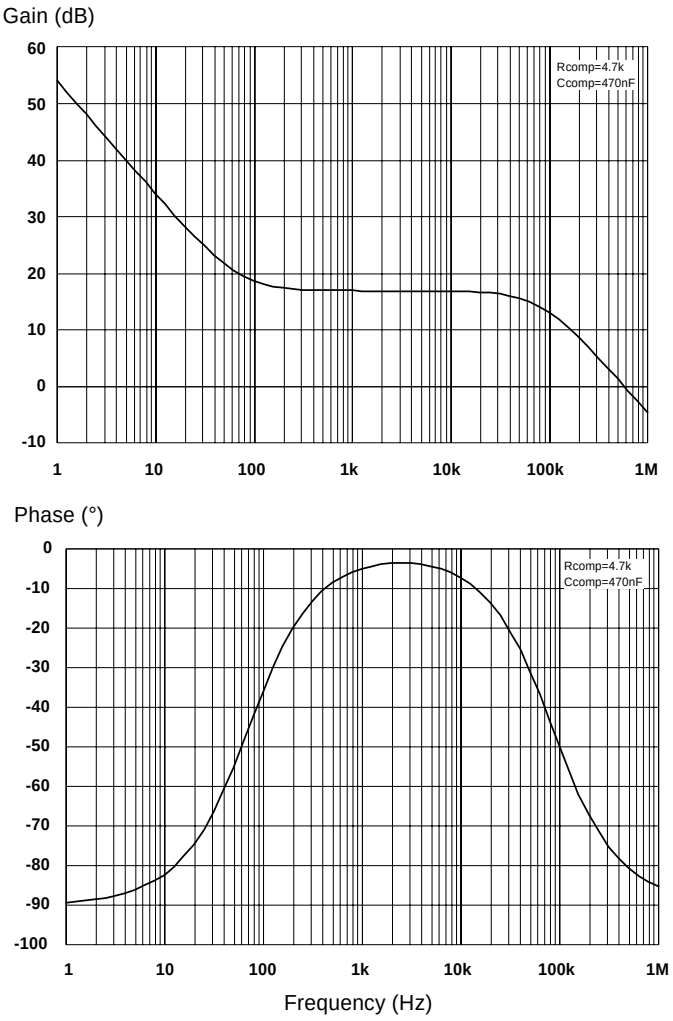
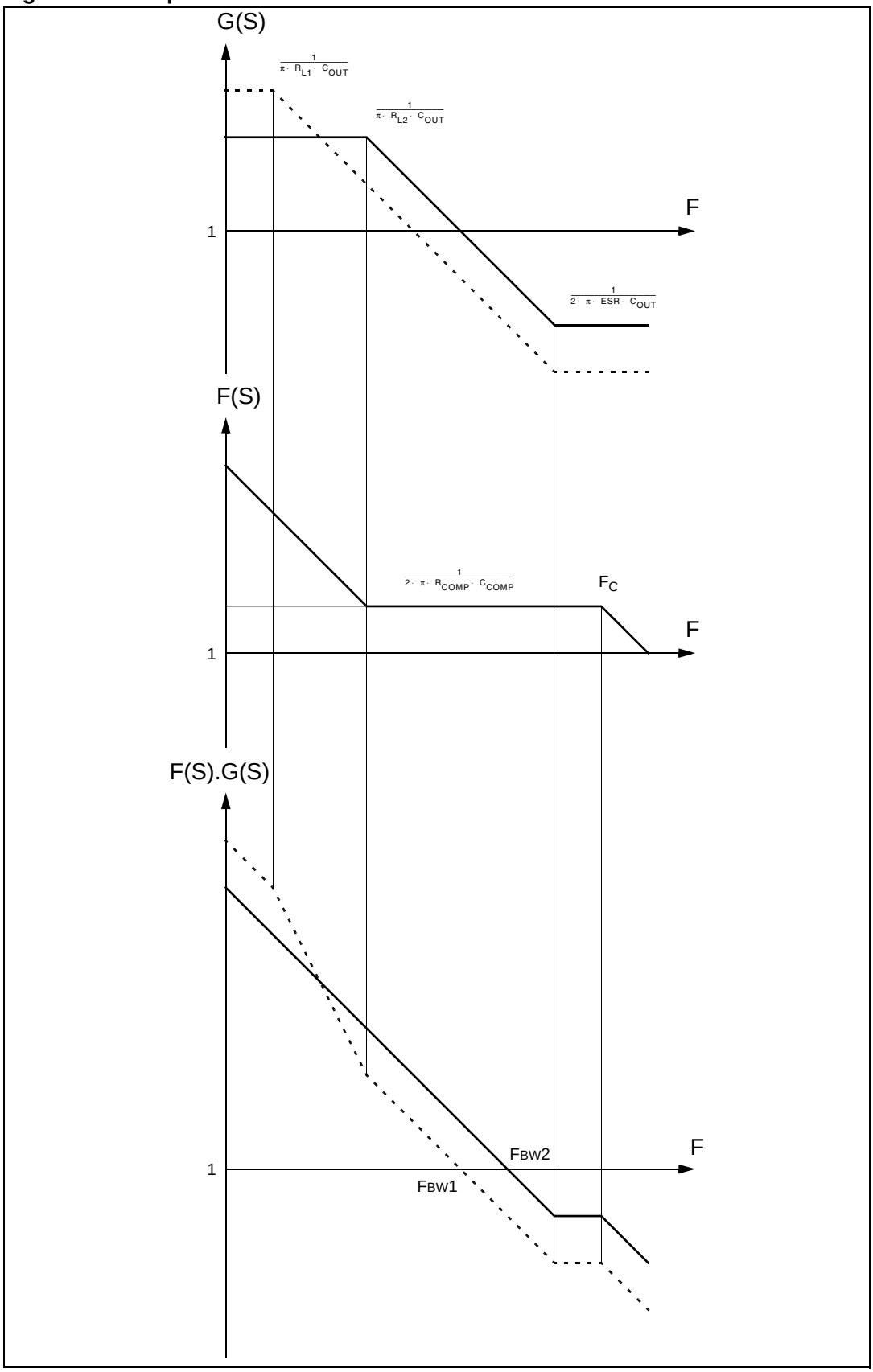


Figure 24. Complete converter transfer function



12 Special recommendations

As steted in the error amplifier section, a capacitor of 10nF capacitor (minimum value: 8nF) should always be connected to the COMP pin to ensure correct stability of the internal error amplifier *Figure 18*, *19* and *22*.

In order to improve the ruggedness of the device versus eventual drain overvoltages, a resistance of 1kΩ should be inserted in series with the TOVL pin, as shown on *Figure 18*, *Figure 19 on page 17*.

Note that, this resistance does not impact the overload delay, as its value is negligible prior to the internal pull-up resistance (about 125kΩ).

13 Software implementation

All the above considerations and some others are included included in ST design software which provides all of the needed components around the VIPer device for specified output configurations, and is available on www.st.com.

14 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 11. DIP8 mechanical data

Dimensions			
Ref.	Databook (mm)		
	Nom.	Min	Max
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81
Package Weight	Gr. 470		

Figure 25. Package dimensions

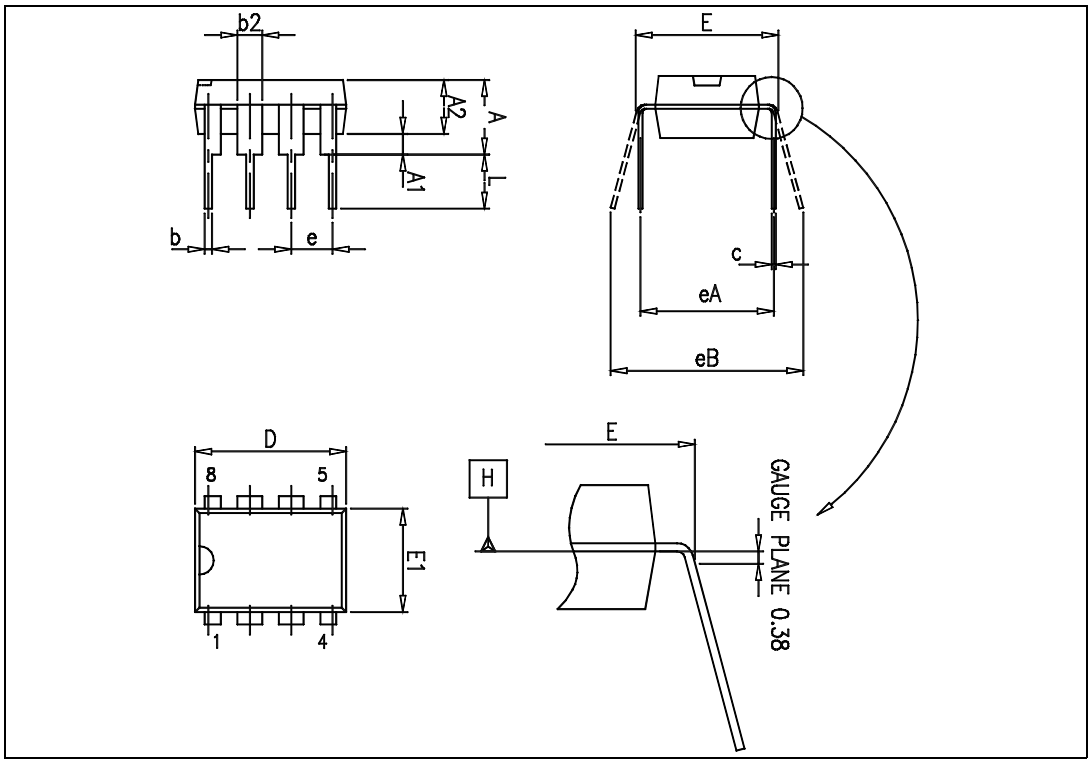
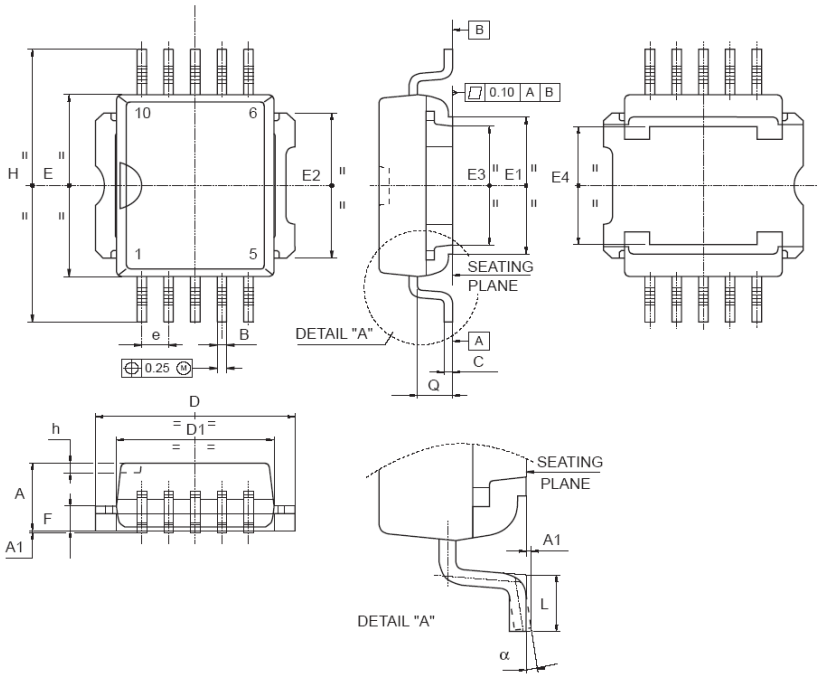


Table 12. PowerSO-10 mechanical data

Dimensions			
Ref.	Databook (mm)		
	Nom.	Min	Max
A	3.35		3.65
A1	0.00		0.10
B	0.40		0.60
c	0.35		0.55
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E1	7.20		7.40
E2	7.20		7.60
E3	6.10		6.35
E4	5.90		6.10
e		1.27	
F	1.25		1.35
H	13.80		14.40
h		0.50	
L	1.20		1.80
q		1.70	
α	0°		8°

Figure 26. Package dimensions



15 Order codes

Table 13. Order codes

Part Number	Package	Shipment
VIPer53DIP-E	DIP-8	Tube
VIPer53SP-E	PowerSO-10	Tube
VIPer53SPTR - E	PowerSO-10	Tape and reel

16 Revision history

Table 14. Revision history

Date	Revision	Changes
13-Nov-2006	1	Initial release.

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