74HC00; 74HCT00

Quad 2-input NAND gate

Rev. 04 — 11 January 2010 Product data sheet

1. General description

The 74HC00; 74HCT00 are high-speed Si-gate CMOS devices that comply with JEDEC standard no. 7A. They are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC00; 74HCT00 provides a quad 2-input NAND function.

2. Features

- Input levels:
  - For 74HC00: CMOS level
  - For 74HCT00: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC00N	−40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT00N				
74HC00D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT00D				
74HC00DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT00DB				
74HC00PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT00PW				
74HC00BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT00BQ				

NXP founded by Philips

4. Functional diagram

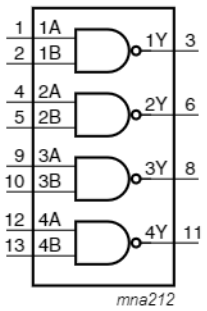


Fig 1. Logic symbol

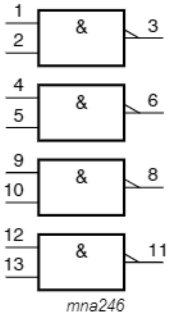


Fig 2. IEC logic symbol

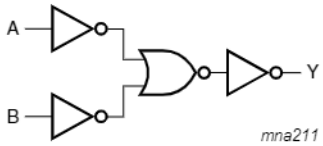


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

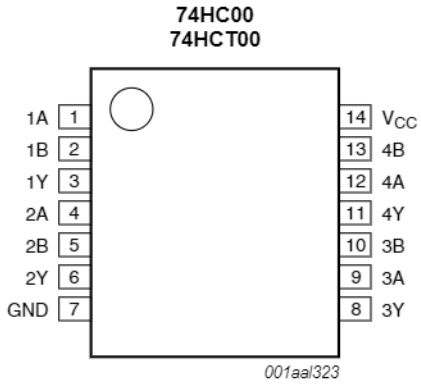
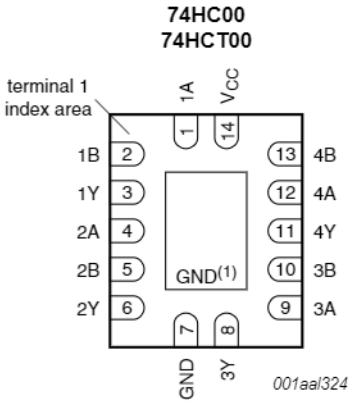


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14



Transparent top view

(1) The substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input. It is recommended that no connection is made at all.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

© NXP B.V. 2010. All rights reserved.

6. Functional description

Table 3. Function table[1]

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation		[2]			
	DIP14 package			-	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages			-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC00			74HCT00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C

© NXP B.V. 2010. All rights reserved.

Table 5. Recommended operating conditions *...continued*

Voltages are referenced to GND (ground = 0 V) ...continued

Symbol	Parameter	Conditions	74HC00			74HCT00			Unit
			Min	Typ	Max	Min	Typ	Max	
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC00										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	-	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	-	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	-	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	-	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	-	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	-	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	-	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	-	4.32	-	3.84	-	3.7	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	-	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	-	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	-	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

© NXP B.V. 2010. All rights reserved.

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT00										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	-	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA	-	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.15	-	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} – 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	150	-	-	675	-	735	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; *for load circuit see Figure 7.*

Symbol	Parameter	Conditions		25 °C			–40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC00									
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V_{CC} = 2.0 V		-	25	-	115	135	ns
		V_{CC} = 4.5 V		-	9	-	23	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	7	-	-	-	ns
		V_{CC} = 6.0 V		-	7	-	20	23	ns
t_t	transition time	see Figure 6	[2]						
		V_{CC} = 2.0 V		-	19	-	95	110	ns
		V_{CC} = 4.5 V		-	7	-	19	22	ns
		V_{CC} = 6.0 V		-	6	-	16	19	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC}	[3]	-	22	-	-	-	pF

© NXP B.V. 2010. All rights reserved.

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for load circuit see Figure 7.

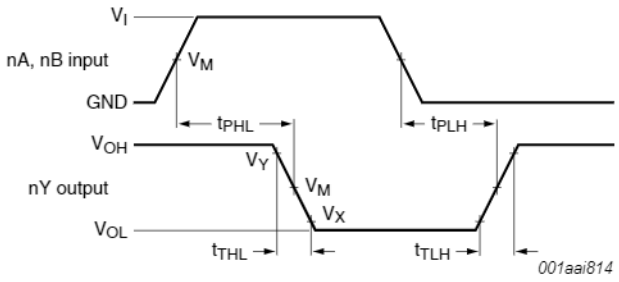
Symbol	Parameter	Conditions		25 °C			−40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HCT00									
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V_{CC} = 4.5 V		-	12	-	24	29	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	10	-	-	-	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 6	[2]	-	-	-	29	22	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} − 1.5 V	[3]	-	22	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



Measurement points are given in Table 9.

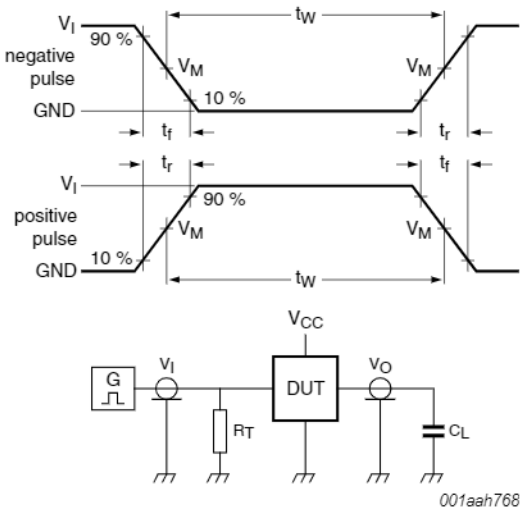
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC00	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT00	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

© NXP B.V. 2010. All rights reserved.



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 7. Load circuitry for measuring switching times

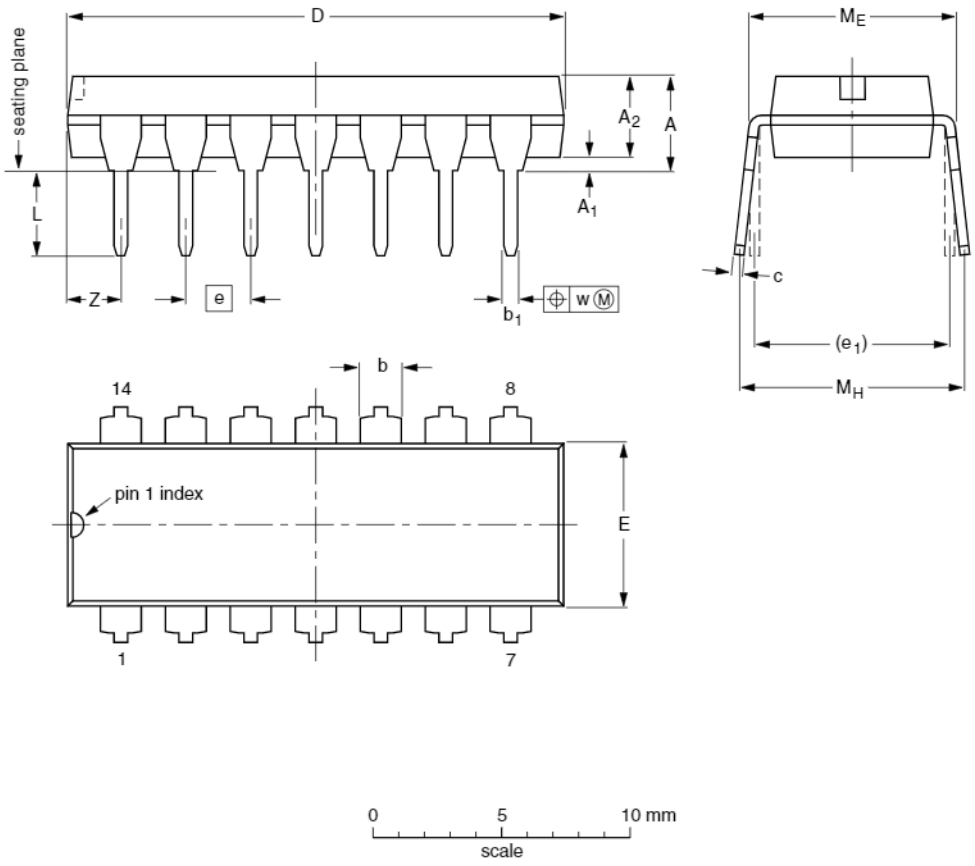
Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC00	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT00	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

© NXP B.V. 2010. All rights reserved.

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

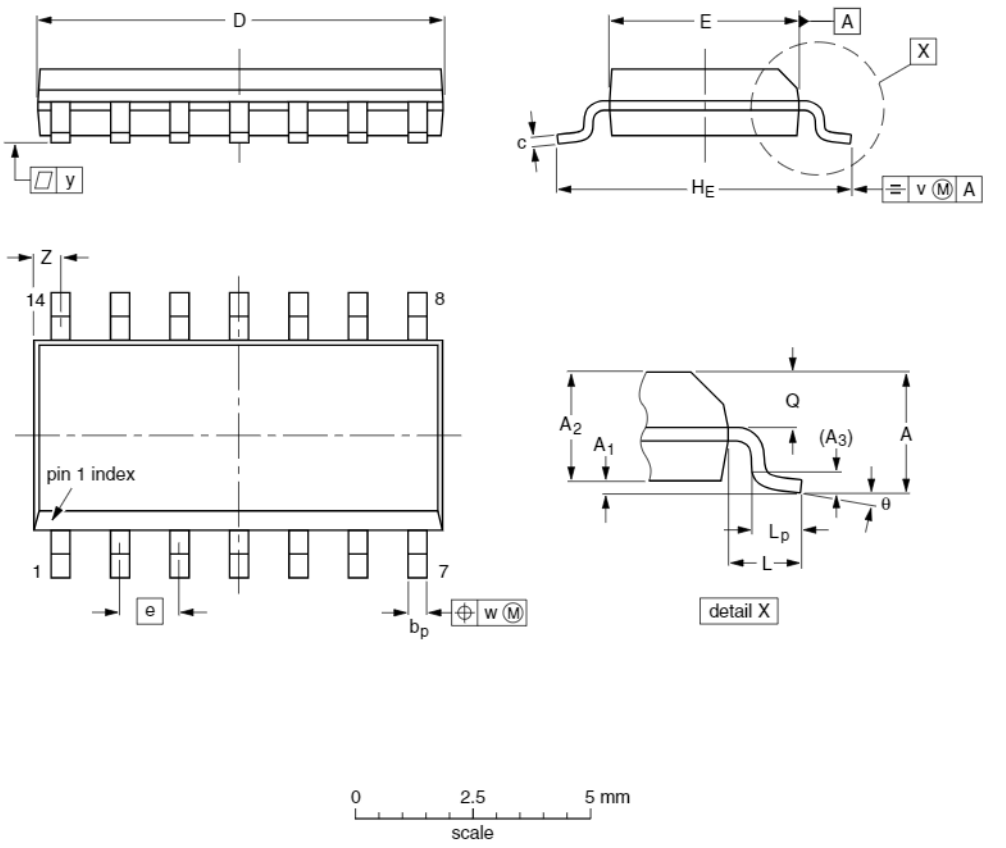
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 8. Package outline SOT27-1 (DIP14)

© NXP B.V. 2010. All rights reserved.

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

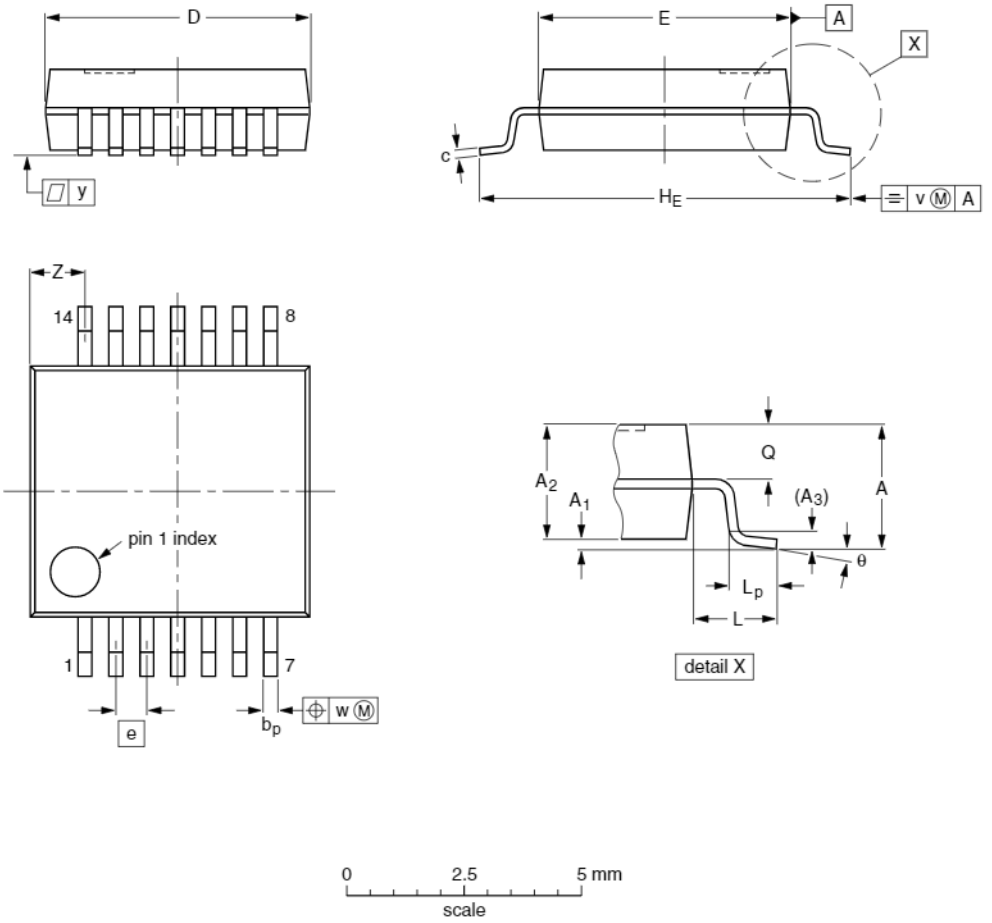
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

© NXP B.V. 2010. All rights reserved.

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

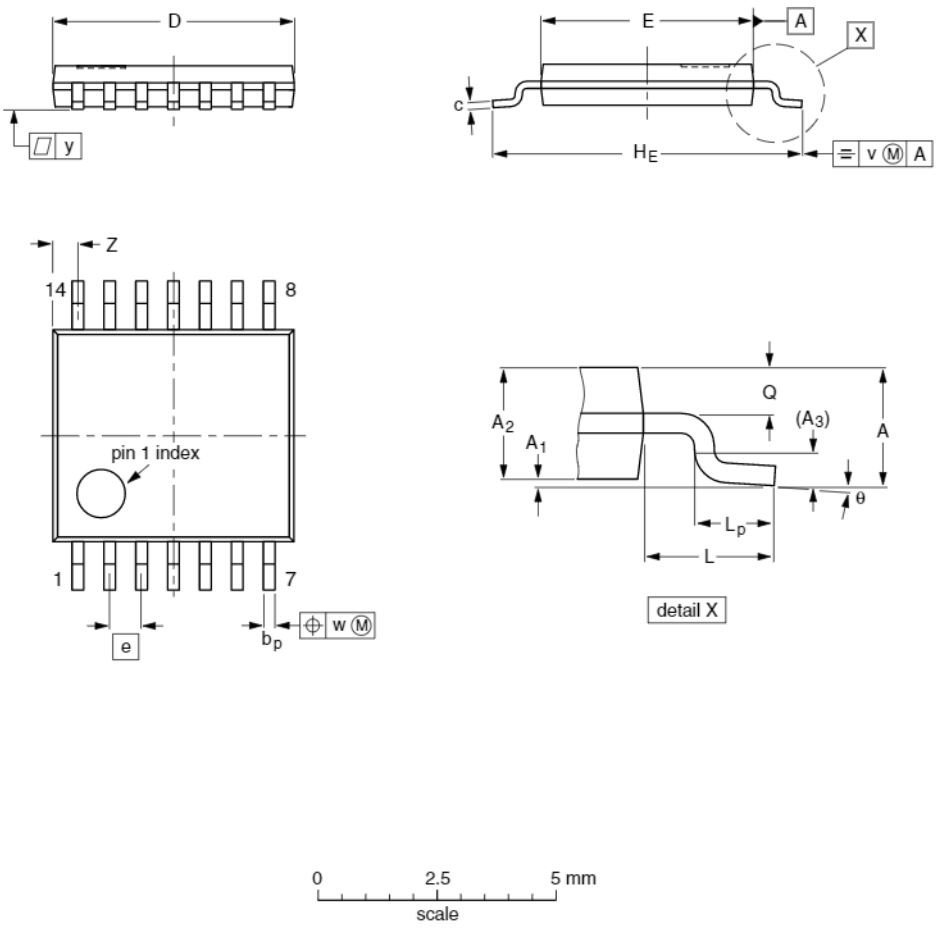
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT337-1 (SSOP14)

© NXP B.V. 2010. All rights reserved.

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

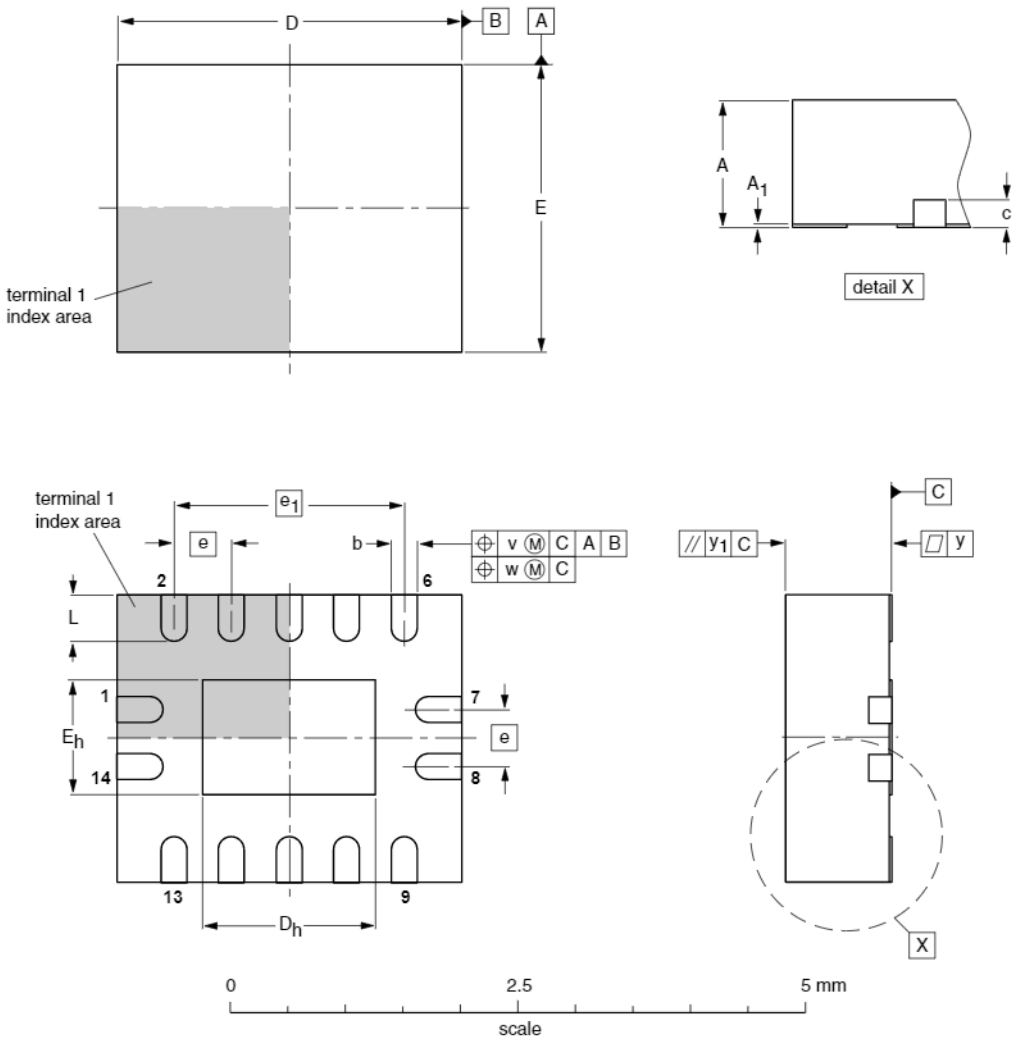
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

© NXP B.V. 2010. All rights reserved.

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 12. Package outline SOT762-1 (DHVQFN14)

© NXP B.V. 2010. All rights reserved.

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT00_4	20100111	Product data sheet	-	74HC_HCT00_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT00_3	20030630	Product data sheet	-	74HC_HCT00_CNV_2
74HC_HCT00_CNV_2	19970826	Product specification	-	-

© NXP B.V. 2010. All rights reserved.

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2010. All rights reserved.

17. Contents

1 General description 1
2 Features 1
3 Ordering information 1
4 Functional diagram 2
5 Pinning information 2
5.1 Pinning 2
5.2 Pin description 2
6 Functional description 3
7 Limiting values 3
8 Recommended operating conditions 3
9 Static characteristics 4
10 Dynamic characteristics 5
11 Waveforms 6
12 Package outline 8
13 Abbreviations 13
14 Revision history 13
15 Legal information 14
15.1 Data sheet status 14
15.2 Definitions 14
15.3 Disclaimers 14
15.4 Trademarks 14
16 Contact information 14
17 Contents 15

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 January 2010
Document identifier: 74HC_HCT00_4

founded by

PHILIPS