TL081, TL081A, TL081B, TL081H
TL082, TL082A, TL082B, TL082H
TL084, TL084A, TL084B, TL084H
SLOS081M – FEBRUARY 1977 – REVISED DECEMBER 2021

TL08xx FET-Input Operational Amplifiers

1 Features

- High slew rate: 20 V/µs (TL08xH, typ)
- Low offset voltage: 1 mV (TL08xH, typ)
- Low offset voltage drift: 2 µV/°C
- Low power consumption: 940 µA/ch (TL08xH, typ)
- Wide common-mode and differential voltage ranges
  - Common-mode input voltage range includes V_{CC+}
- Low input bias and offset currents
- Low noise: V_n = 18 nV/√Hz (typ) at f = 1 kHz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage: ±2.25 V to ±20 V, 4.5 V to 40 V

2 Applications

- Solar energy: string and central inverter
- Motor drives: AC and servo drive control and power stage modules
- Single phase online UPS
- Three phase UPS
- Pro audio mixers
- Battery test equipment

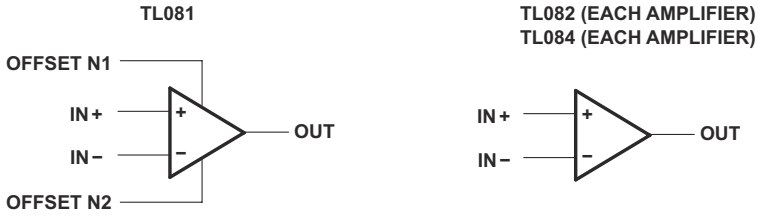
3 Description

The TL08xH (TL081H, TL082H, and TL084H) family of devices are the next-generation versions of the industry-standard TL08x (TL081, TL082, and TL084) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), high slew rate (20 V/µs), and common-mode input to the positive supply. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL08xH devices to be used in the most rugged and demanding applications.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TL081x	PDIP (8)	9.59 mm × 6.35 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SO (8)	6.20 mm × 5.30 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (5)	1.60 mm × 1.20 mm
TL082x	PDIP (8)	9.59 mm × 6.35 mm
	SO (8)	6.20 mm × 5.30 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (8)	2.90 mm × 1.60 mm
	TSSOP (8)	4.40 mm × 3.00 mm
TL082M	CDIP (8)	9.59 mm × 6.67 mm
	LCCC (20)	8.89 mm × 8.89 mm
TL084x	PDIP (14)	19.30 mm × 6.35 mm
	SO (14)	10.30 mm × 5.30 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOT-23 (14)	4.20 mm × 2.00 mm
	TSSOP (14)	5.00 mm × 4.40 mm
TL084M	CDIP (14)	19.56 mm × 6.92 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Symbols

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....4
6 Specifications....10
6.1 Absolute Maximum Ratings: TL08xH....10
6.2 Absolute Maximum Ratings: All Other Devices....10
6.3 ESD Ratings: TL08xH....10
6.4 ESD Ratings: All Other Devices....11
6.5 Recommended Operating Conditions: TL08xH....11
6.6 Recommended Operating Conditions: All Other Devices....11
6.7 Thermal Information for Single Channel: TL081H....11
6.8 Thermal Information for Dual Channel: TL082H....11
6.9 Thermal Information for Quad Channel: TL084H....12
6.10 Thermal Information: All Other Devices....12
6.11 Electrical Characteristics: TL08xH....13
6.12 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI....15
6.13 Electrical Characteristics for TL08xM and TL084x....16
6.14 Switching Characteristics....17
6.15 Dissipation Rating Table....17
6.16 Typical Characteristics: TL08xH....18
6.17 Typical Characteristics: All Other Devices....25
7 Parameter Measurement Information....28
8 Detailed Description....29
8.1 Overview....29
8.2 Functional Block Diagram....29
8.3 Feature Description....29
8.4 Device Functional Modes....30
9 Applications and Implementation....31
9.1 Application Information....31
9.2 Typical Applications....31
9.3 System Examples....32
10 Power Supply Recommendations....34
11 Layout....35
11.1 Layout Guidelines....35
11.2 Layout Examples....35
12 Device and Documentation Support....36
12.1 Receiving Notification of Documentation Updates....36
12.2 Support Resources....36
12.3 Trademarks....36
12.4 Electrostatic Discharge Caution....36
12.5 Glossary....36
13 Mechanical, Packaging, and Orderable Information....36

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (July 2021) to Revision M (December 2021) — **Page**

- Corrected DCK pinout diagram and table in *Pin Configurations and Functions* section....4

Changes from Revision K (June 2021) to Revision L (July 2021) — **Page**

- Deleted preview note from TL081H SOIC (8), SOT-23 (5), and SC70 (5) packages throughout the data sheet....1

Changes from Revision J (November 2020) to Revision K (June 2021) — **Page**

- Deleted VSSOP (8) package references throughout data sheet....1
- Deleted preview note from TL082H SOIC (8), SOT-23 (8), and TSSOP (8) packages throughout the data sheet....1
- Added DBV, DCK, and D packages to TL081H in *Pin Configuration and Functions* section....4
- Added ESD information for TL082H....10
- Added D, DCK, and DBV package thermal information in Thermal Information for Single Channel: TL081H section....11
- Added D, DDF, and PW package thermal information in Thermal Information for Dual Channel: TL082H section....11
- Added I_B and I_{OS} specification for single channel DCK and DBV package....13
- Added I_Q spec for TL081H and TL082H....13
- Removed *Related Links* section from *Device and Documentation Support* section....36

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Changes from Revision I (May 2015) to Revision J (November 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Added TL08xH devices throughout the data sheet....1
- Added features for TL08xH to the *Features* section....1
- Added link to applications in the *Applications* section....1
- Added TL08xH in the *Description* section....1
- Added TL08xH in the *Device Information* table....1
- Updated pinout diagrams and pinout tables in *Pin Configurations and Functions* section....4
- Added TSSOP, VSSOP and DDF packages to TL082x in *Pin Configuration and Functions* section....4
- Added DYY package to TL084x in *Pin Configuration and Functions* section....4
- Added *Typical Characteristics:TL08xH* section in *Specifications* section....18
- Removed Table of Graphs in *Typical Characteristics: All Other Devices* section....25
- Removed references to obsolete documentation....35

Changes from Revision H (January 2014) to Revision I (May 2015) **Page**

- Added *Applications* section, *Device Information* table, Pin Functions table, Thermal Information table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, ESD information, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Added *Applications*....1
- Moved *Typical Characteristics* into *Specifications* section....25

Changes from Revision G (September 2004) to Revision H (January 2014) **Page**

- Deleted *Ordering Information* table....1

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5 Pin Configuration and Functions

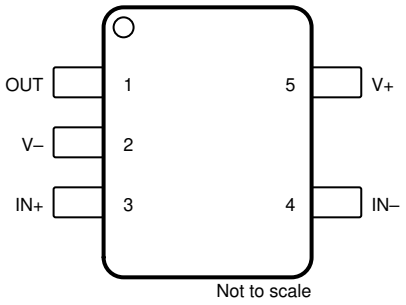


Figure 5-1. TL081H DBV Package
5-Pin SOT-23
(Top View)

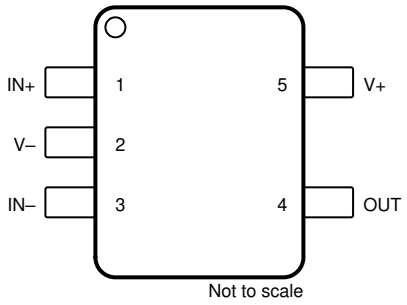
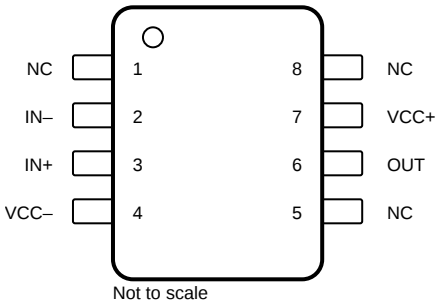


Figure 5-2. TL081H DCK Package
5-Pin SC70
(Top View)



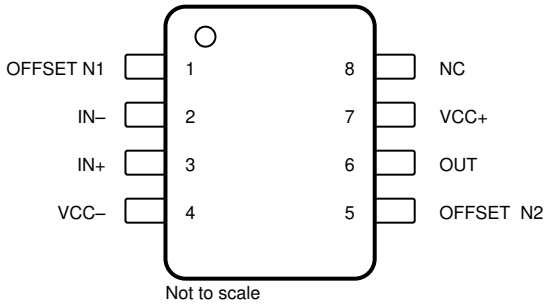
NC- no internal connection

Figure 5-3. TL081H D Package
8-Pin SOIC
(Top View)

Table 5-1. Pin Functions: TL081H

PIN				I/O	DESCRIPTION
NAME	DBV	DCK	D		
IN–	4	3	2	I	Inverting input
IN+	3	1	3	I	Noninverting input
NC	—	—	8	—	Do not connect
NC	—	—	1	—	Do not connect
NC	—	—	5	—	Do not connect
OUT	1	4	6	O	Output
VCC–	2	2	4	—	Power supply
VCC+	5	5	7	—	Power supply

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NC- no internal connection

Figure 5-4. TL081x D, P, and PS Package
8-Pin SOIC, PDIP, and SO
(Top View)

Table 5-2. Pin Functions: TL081x

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC–	4	—	Power supply
VCC+	7	—	Power supply

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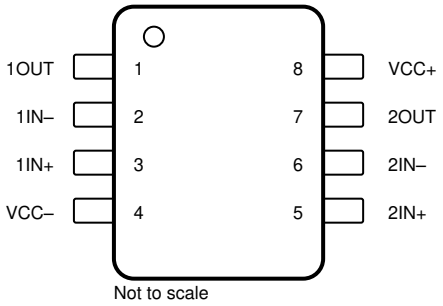
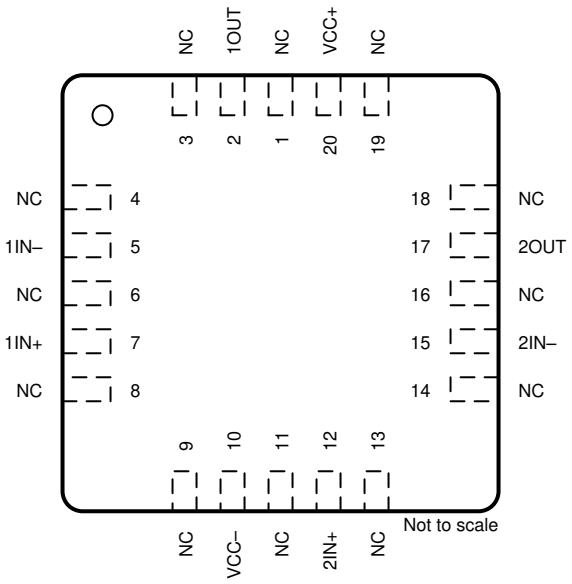


Figure 5-5. TL082x D, DDF, DGK, JG, P, PS, and PW Package 8-Pin SOIC, SOT-23 (8), VSSOP, CDIP, PDIP, SO, and TSSOP (Top View)

Table 5-3. Pin Functions: TL082x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC–	4	—	Power supply
VCC+	8	—	Power supply

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NC- no internal connection

Figure 5-6. TL082 FK Package
20-Pin LCCC
(Top View)

Table 5-4. Pin Functions: TL082x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN–	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC–	10	—	Power supply
VCC+	20	—	Power supply

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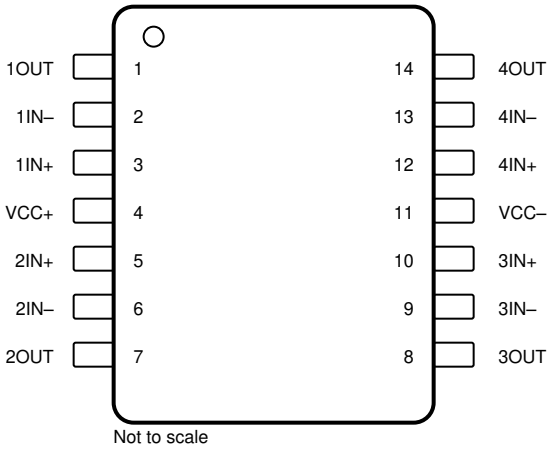
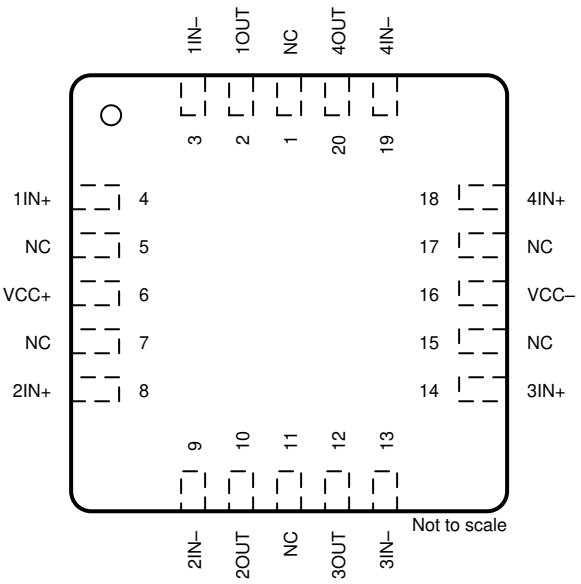


Figure 5-7. TL084x D, N, NS, PW, J, and DYY Package 14-Pin SOIC, PDIP, SO, TSSOP, CDIP, and SOT-23 (14) (Top View)

Table 5-5. Pin Functions: TL084x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN–	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN–	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
V_{CC-}	11	—	Power supply
V_{CC+}	4	—	Power supply

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NC- no internal connection

Figure 5-8. TL084 FK Package
20-Pin LCCC
(Top View)

Table 5-6. Pin Functions: TL084x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN–	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN–	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC–	16	—	Power supply
VCC+	6	—	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings: TL08xH

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, $V_S = (V_{CC+}) - (V_{CC-})$		0	42	V
Signal input pins	Common-mode voltage (3)	$(V_{CC-}) - 0.5$	$(V_{CC+}) + 0.5$	V
	Differential voltage (3)		$V_S + 0.2$	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 Absolute Maximum Ratings: All Other Devices

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC+} - V_{CC-}	Supply voltage(2)	-18	18	V
V_{ID}	Differential input voltage(3)	-30	+30	V
V_I	Input voltage(2) (4)	-15	+15	V
	Duration of output short circuit(5)	Unlimited		
	Continuous total power dissipation	See *Section 6.15*		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.3 ESD Ratings: TL08xH

			VALUE	UNIT
TL084H				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
TL082H and TL081H				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.4 ESD Ratings: All Other Devices

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.5 Recommended Operating Conditions: TL08xH

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V_{CC+}) – (V_{CC–})$	4.5	40	V
V_I	Input voltage range	$(V_{CC–}) + 2$	$(V_{CC+}) + 0.1$	V
T_A	Specified temperature	–40	125	°C

6.6 Recommended Operating Conditions: All Other Devices

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		$V_{CC–} + 4$	$V_{CC+} – 4$	V
T_A	Ambient temperature	TL08xM	–55	125	°C
		TL08xQ	–40	125	
		TL08xI	–40	85	
		TL08xC	0	70	

6.7 Thermal Information for Single Channel: TL081H

THERMAL METRIC [1]		TL081H			UNIT
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.8	217.5	212.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.6	113.1	111.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.3	63.8	79.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.8	34.8	51.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.5	63.5	79.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.8 Thermal Information for Dual Channel: TL082H

THERMAL METRIC [1]		TL082H			UNIT
		D (SOIC)	DDF (SOT-23)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.8	181.5	200.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.2	112.5	89.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.4	98.2	131.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	36.8	17.2	22.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.6	97.6	129.3	°C/W

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6.8 Thermal Information for Dual Channel: TL082H (continued)

THERMAL METRIC (1)		TL082H			UNIT
		D (SOIC)	DDF (SOT-23)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.9 Thermal Information for Quad Channel: TL084H

THERMAL METRIC (1)		TL084H			UNIT
		D (SOIC)	DYY (2) (SOT-23)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	TBD	134.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	TBD	62.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.2	TBD	77.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.8	TBD	13.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.8	TBD	77.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for TL084H.

6.10 Thermal Information: All Other Devices

THERMAL METRIC(1)		TL08xxx											UNIT
		D (SOIC)		FK (LCCC)	J (CDIP)		N (PDIP)		NS (SO)		PW (TSSOP)		
		8 PIN	14 PIN	20 PIN	8 PIN	14 PIN	8 PIN	14 PIN	8 PIN	14 PIN	8 PIN	14 PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	86				85	80	95	76	150	113	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance			5.61	15.05	14.5							

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.11 Electrical Characteristics: TL08xH

For $V_S = (V_{CC+}) – (V_{CC–}) = 4.5$ V to 40 V (±2.25 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±4	mV
			T_A = –40°C to 125°C			±5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±2		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 5 V to 40 V, $V_{CM} = V_S / 2$	T_A = –40°C to 125°C		±1	±10	µV/V
	Channel separation	f = 0 Hz			10		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±120	pA
			DCK and DBV packages		±1	±300	pA
			T_A = –40°C to 125°C (1)			±5	nA
I_{OS}	Input offset current				±0.5	±120	pA
			DCK and DBV packages		±0.5	±250	pA
			T_A = –40°C to 125°C (1)			±5	nA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			37		$nV/\sqrt{Hz}$
		f = 10 kHz			21		
i_N	Input current noise	f = 1 kHz			80		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			$(V_{CC–}) + 1.5$		(V_{CC+})	V
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < $(V_{CC+}) – 1.5$ V		100	105		dB
CMRR	Common-mode rejection ratio		T_A = –40°C to 125°C	95			dB
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < (V_{CC+})		90	105		dB
CMRR	Common-mode rejection ratio		T_A = –40°C to 125°C	80			dB
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 2		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, $(V_{CC–}) + 0.3$ V < V_O < $(V_{CC+}) – 0.3$ V	T_A = –40°C to 125°C	118	125		dB
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, R_L = 2 kΩ, $(V_{CC–}) + 1.2$ V < V_O < $(V_{CC+}) – 1.2$ V	T_A = –40°C to 125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			20		V/µs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.63		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.56		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.91		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.48		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20 pF			56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns

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6.11 Electrical Characteristics: TL08xH (continued)

For $V_S = (V_{CC+}) – (V_{CC–}) = 4.5$ V to 40 V (±2.25 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion + noise	$V_S = 40$ V, $V_O = 6\ V_{RMS}$, G = +1, f = 1 kHz			0.00012		%
EMIRR	EMI rejection ratio	f = 1 GHz			53		dB
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	$V_S = 40$ V, $R_L = 10$ kΩ		115	210	mV
			$V_S = 40$ V, $R_L = 2$ kΩ		520	965	
		Negative rail headroom	$V_S = 40$ V, $R_L = 10$ kΩ		105	215	
			$V_S = 40$ V, $R_L = 2$ kΩ		500	1030	
I_{SC}	Short-circuit current				±26		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1 MHz, $I_O = 0$ A			125		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$I_O = 0$ A			937.5	1125	μA
		$I_O = 0$ A, (TL081H)			960	1156	
		$I_O = 0$ A	$T_A = –40°C$ to 125°C			1130	
		$I_O = 0$ A, (TL082H)				1143	
		$I_O = 0$ A, (TL081H)				1160	
	Turn-On Time	At $T_A = 25°C$, $V_S = 40$ V, V_S ramp rate > 0.3 V/μs			60		μs

(1) Max I_B and I_{os} data is specified based on characterization results.

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6.12 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		μV/°C
I_{IO}	Input offset current(2)	V_O = 0	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current(2)	V_O = 0	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			15			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$/ΔV_{IO})	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and –40°C to 85°C for TL08_I.

(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-52. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

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6.13 Electrical Characteristics for TL08xM and TL084x

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current(2)	V_O = 0	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current(2)	V_O = 0	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		25	200		V/mV
			Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-52. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

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6.14 Switching Characteristics

$V_{CC±}$ = ±15 V, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, see Figure 7-1		8[1]	13		V/µs
		V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, T_A = −55°C to 125°C, see Figure 7-1		5[1]			
t_r	Rise-time	V_I = 20 V, R_L = 2 kΩ, C_L = 100 pF, see Figure 7-1			0.05		µs
	overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	R_S = 20 Ω	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, A_{VD} = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ, f = 1 kHz			0.003%		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

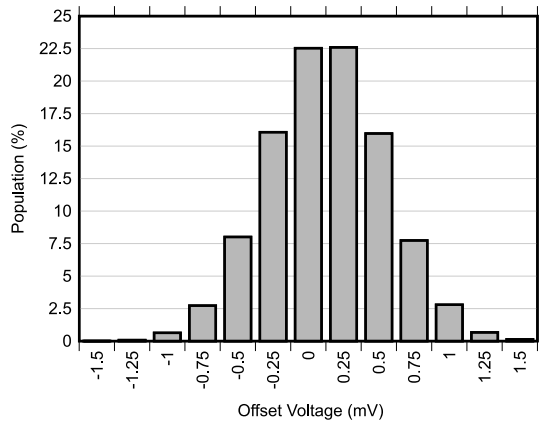
6.15 Dissipation Rating Table

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 m/W	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 m/W	546 mW	210 mW

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6.16 Typical Characteristics: TL08xH

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



T_A = 25°C

Figure 6-1. Offset Voltage Production Distribution

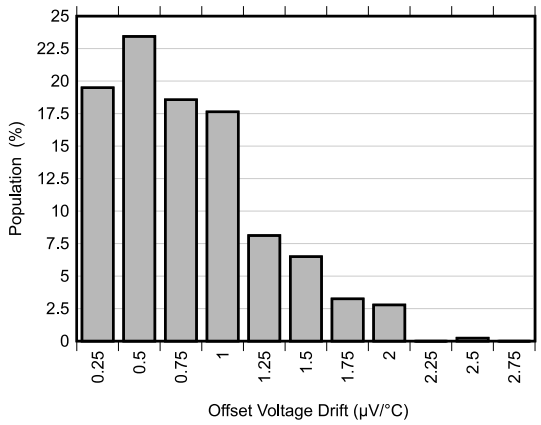
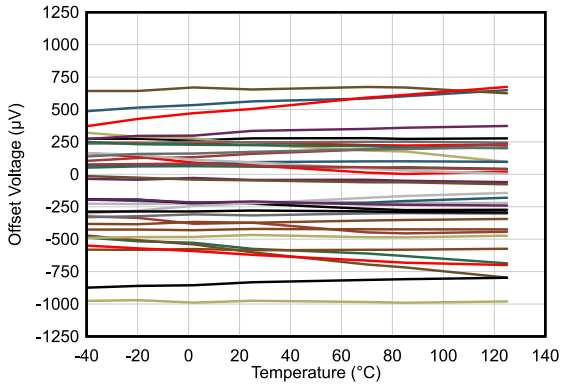
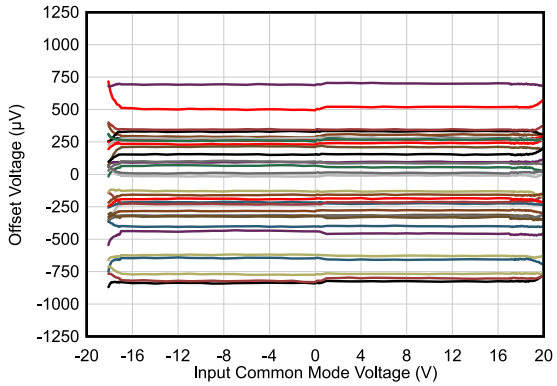


Figure 6-2. Offset Voltage Drift Distribution



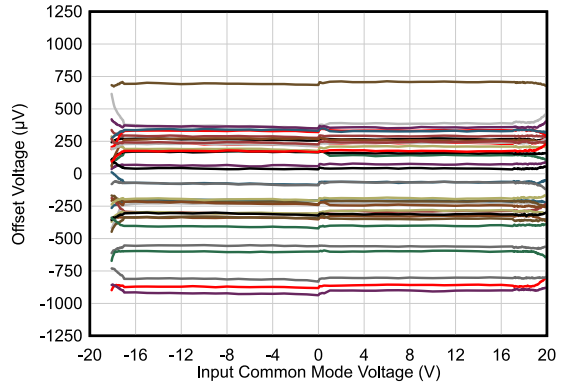
V_{CM} = V_S / 2

Figure 6-3. Offset Voltage vs Temperature



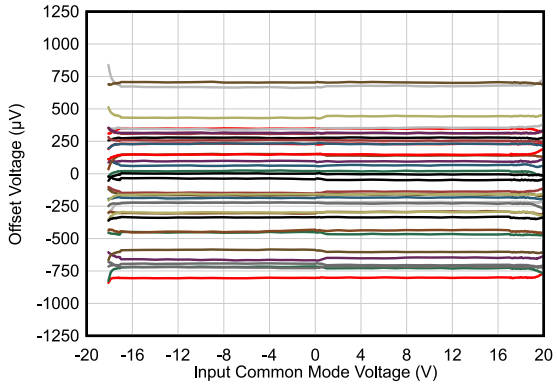
T_A = 25°C

Figure 6-4. Offset Voltage vs Common-Mode Voltage



T_A = 125°C

Figure 6-5. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Figure 6-6. Offset Voltage vs Common-Mode Voltage

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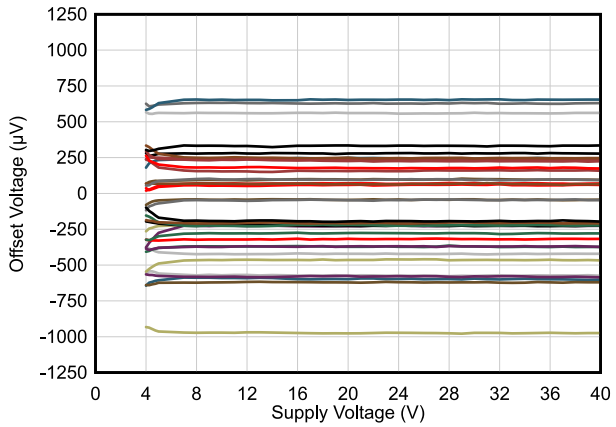


Figure 6-7. Offset Voltage vs Power Supply

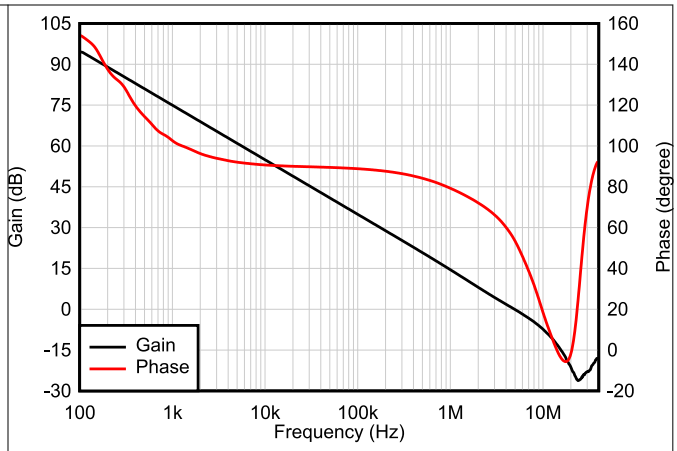


Figure 6-8. Open-Loop Gain and Phase vs Frequency

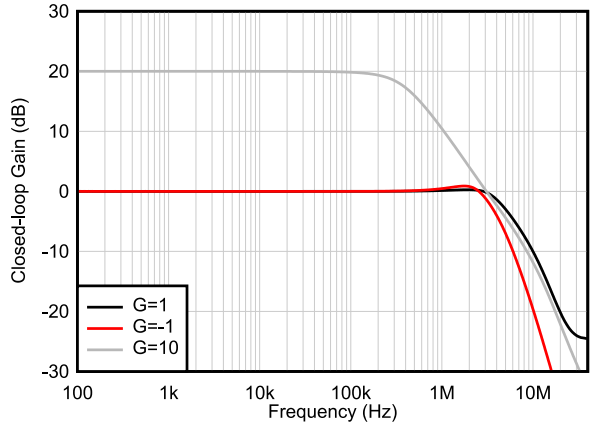


Figure 6-9. Closed-Loop Gain vs Frequency

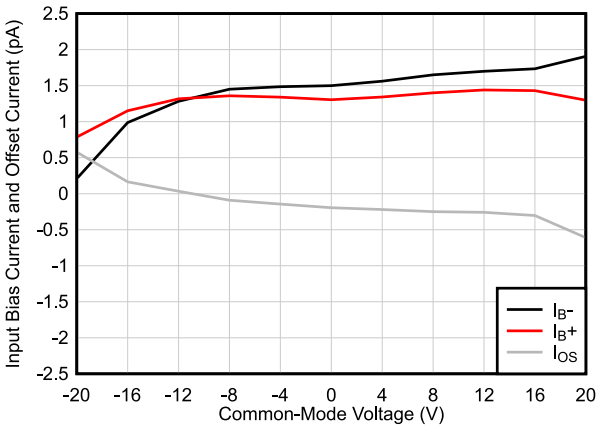


Figure 6-10. Input Bias Current vs Common-Mode Voltage

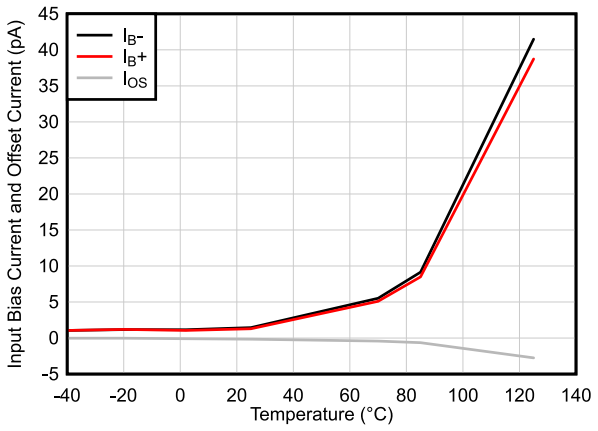


Figure 6-11. Input Bias Current vs Temperature

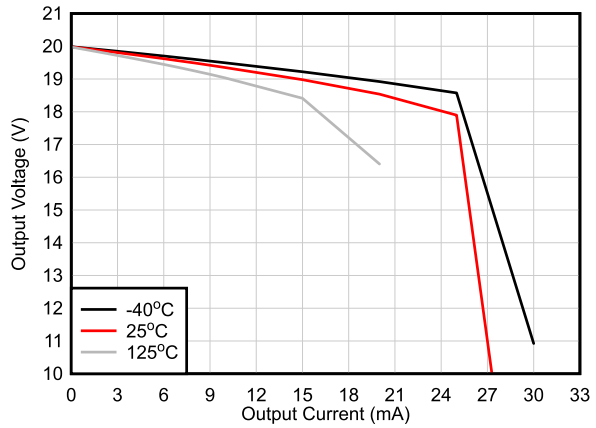


Figure 6-12. Output Voltage Swing vs Output Current (Sourcing)

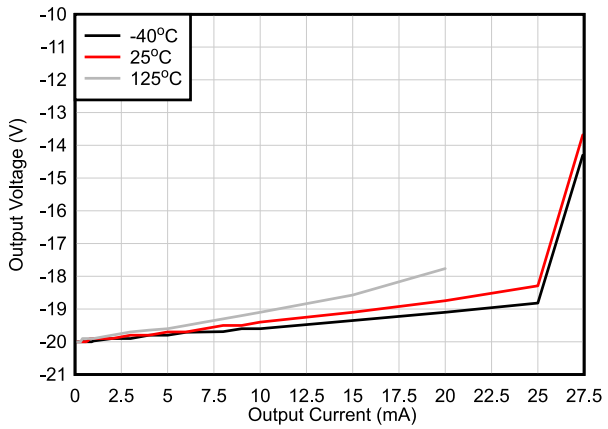


Figure 6-13. Output Voltage Swing vs Output Current (Sinking)

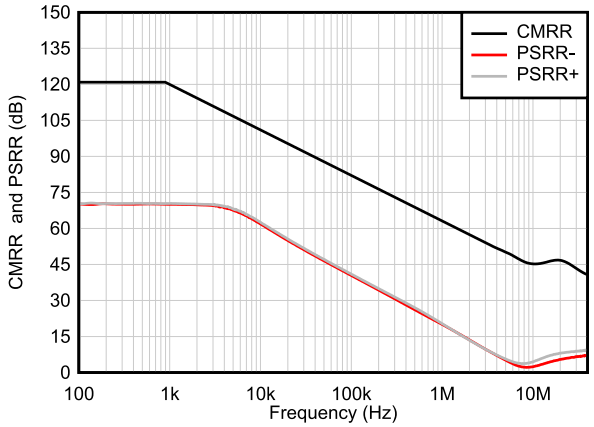
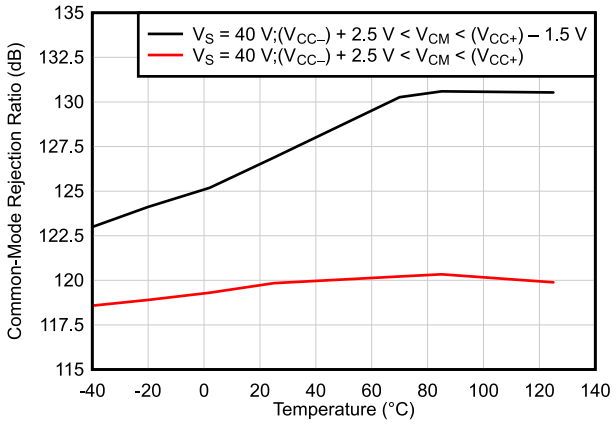
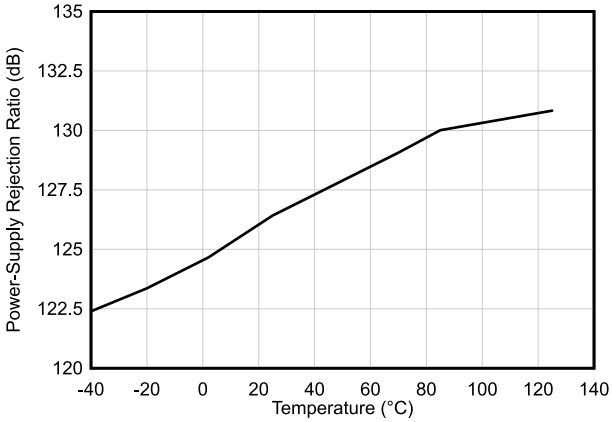


Figure 6-14. CMRR and PSRR vs Frequency



f = 0 Hz

Figure 6-15. CMRR vs Temperature (dB)



f = 0 Hz

Figure 6-16. PSRR vs Temperature (dB)

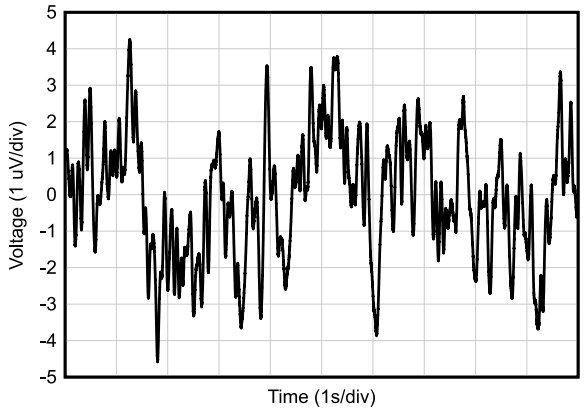


Figure 6-17. 0.1-Hz to 10-Hz Noise

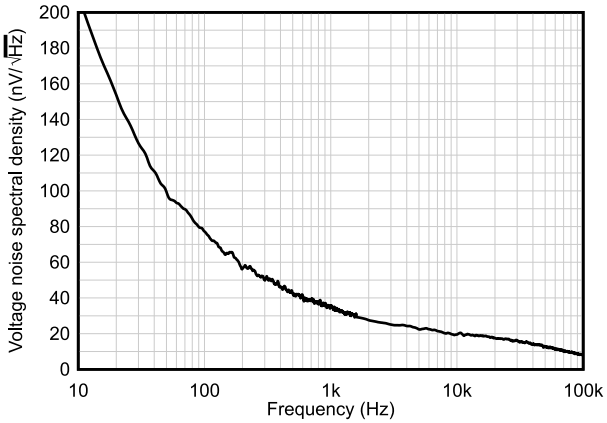
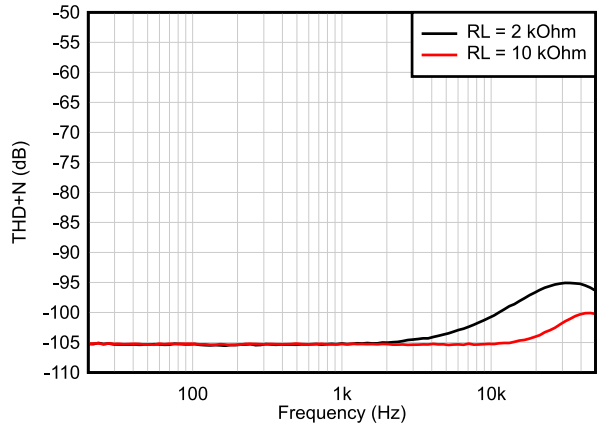


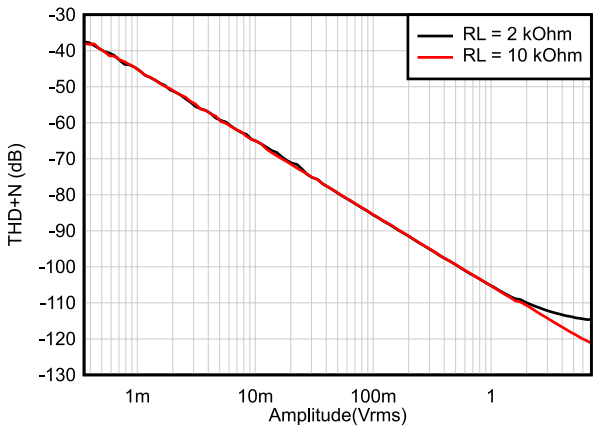
Figure 6-18. Input Voltage Noise Spectral Density vs Frequency

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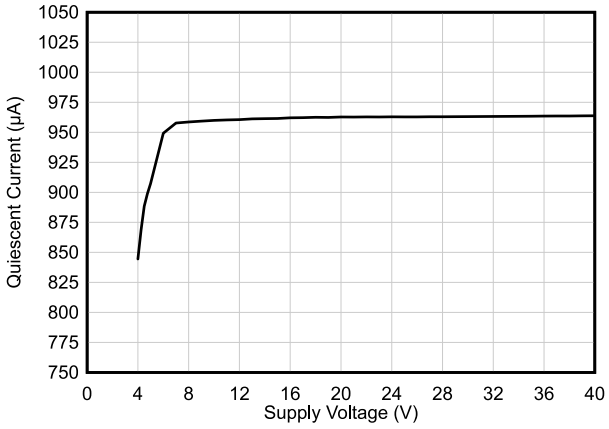
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

Figure 6-19. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

Figure 6-20. THD+N vs Output Amplitude



V_{CM} = V_S / 2

Figure 6-21. Quiescent Current vs Supply Voltage

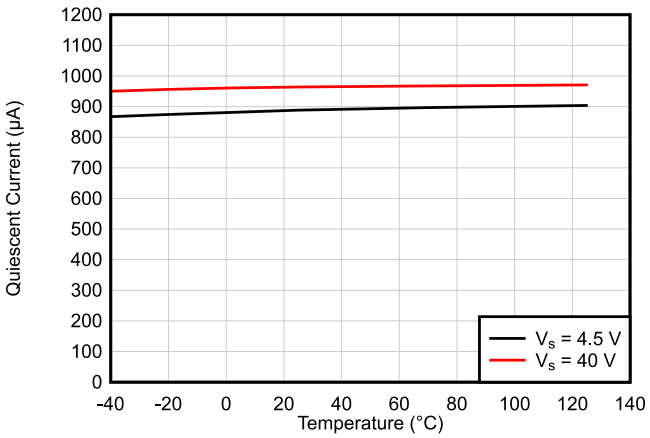


Figure 6-22. Quiescent Current vs Temperature

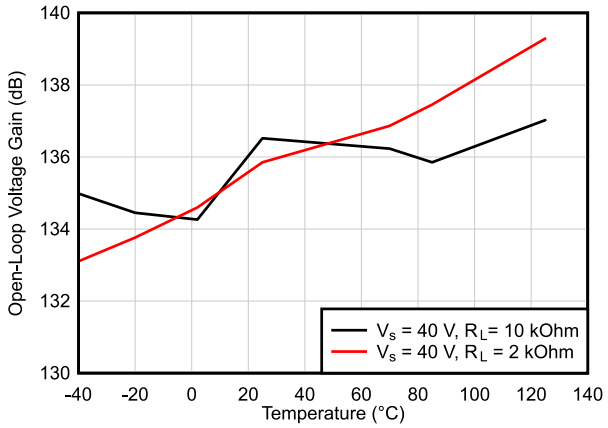


Figure 6-23. Open-Loop Voltage Gain vs Temperature (dB)

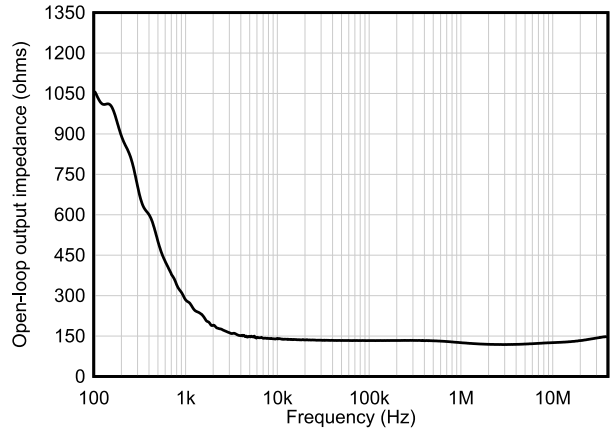
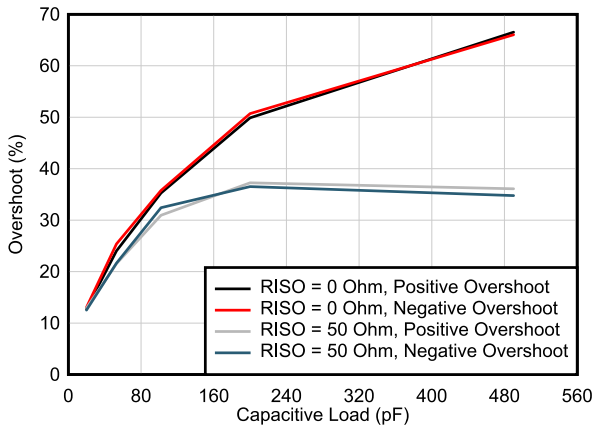
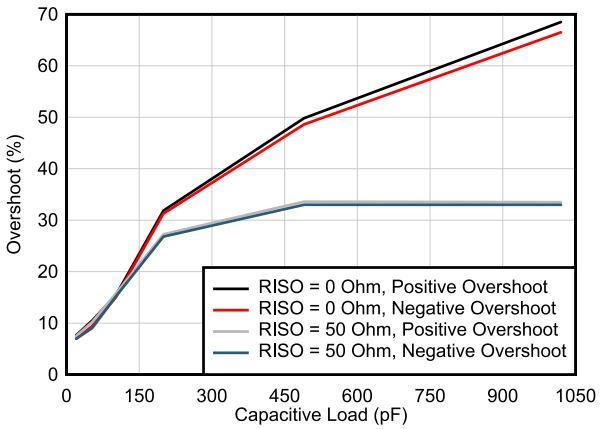


Figure 6-24. Open-Loop Output Impedance vs Frequency



G = –1, 25-mV output step

Figure 6-25. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

Figure 6-26. Small-Signal Overshoot vs Capacitive Load

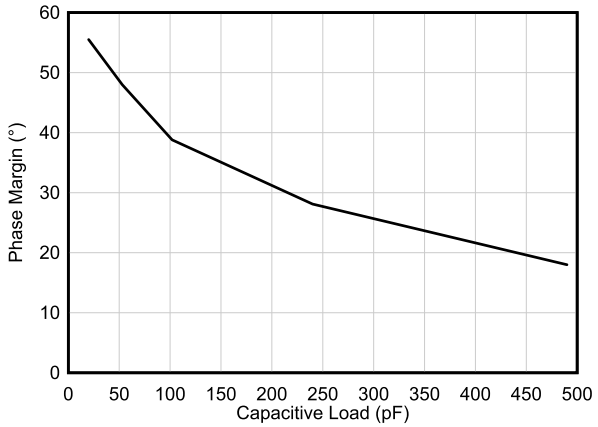
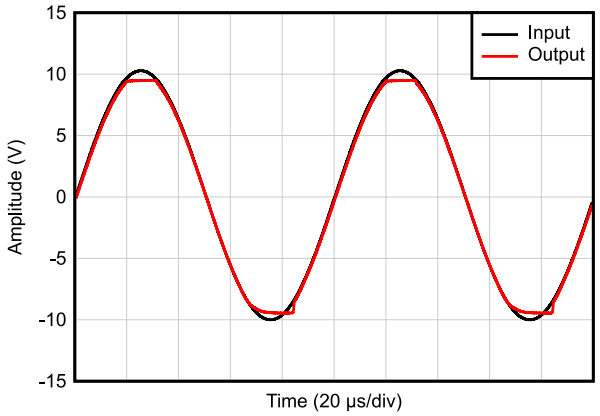
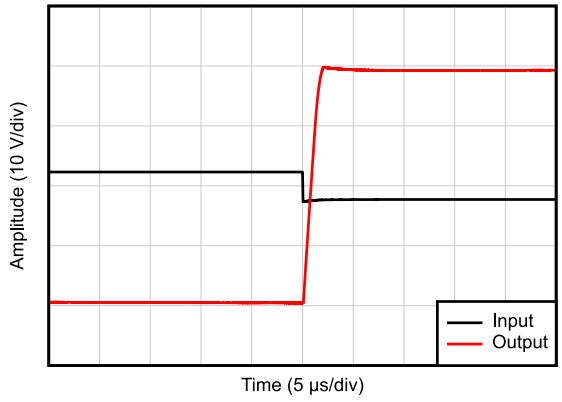


Figure 6-27. Phase Margin vs Capacitive Load



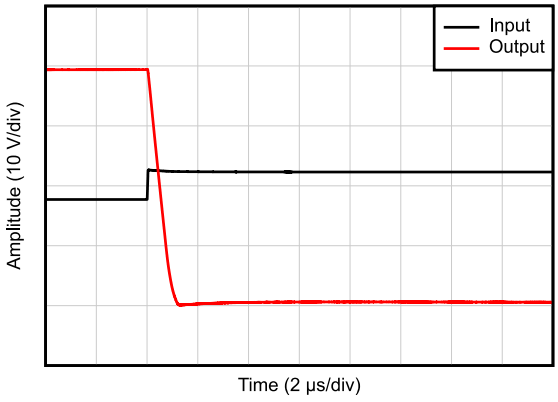
V_S = ±10 V, V_{IN} = V_{OUT}

Figure 6-28. No Phase Reversal



G = –10

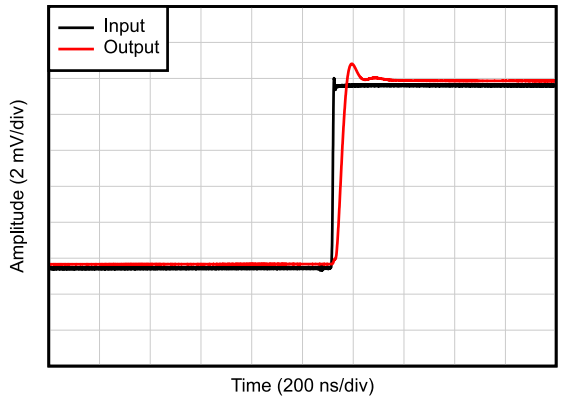
Figure 6-29. Positive Overload Recovery



G = –10

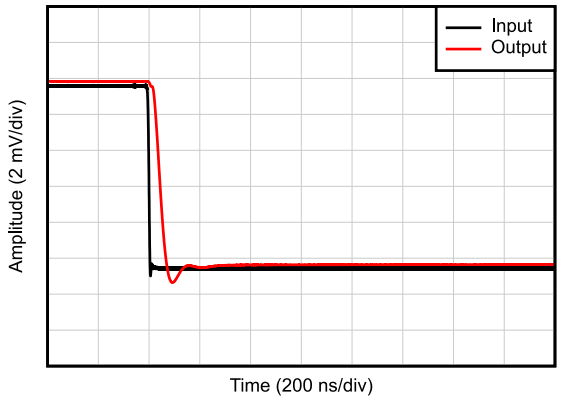
Figure 6-30. Negative Overload Recovery

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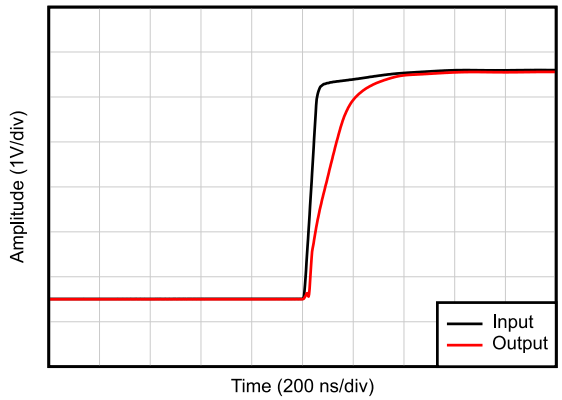
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-31. Small-Signal Step Response, Rising



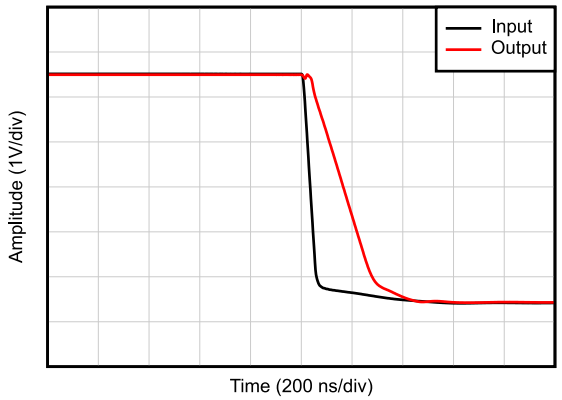
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-32. Small-Signal Step Response, Falling



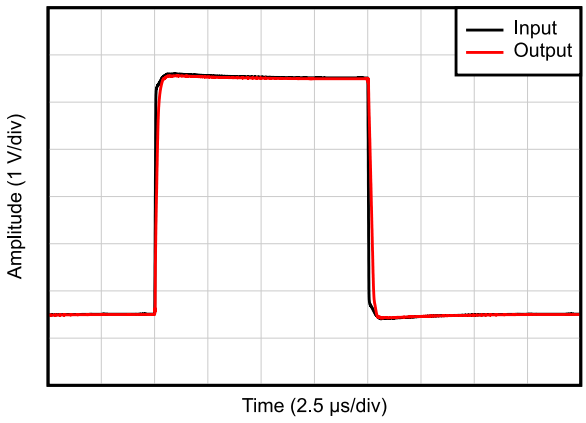
C_L = 20 pF, G = 1

Figure 6-33. Large-Signal Step Response (Rising)



C_L = 20 pF, G = 1

Figure 6-34. Large-Signal Step Response (Falling)



C_L = 20 pF, G = 1

Figure 6-35. Large-Signal Step Response

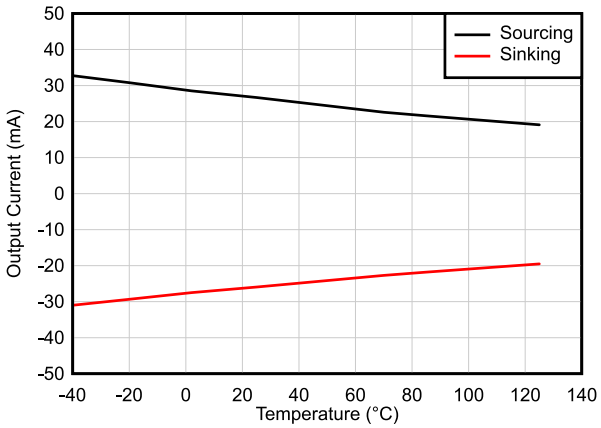


Figure 6-36. Short-Circuit Current vs Temperature

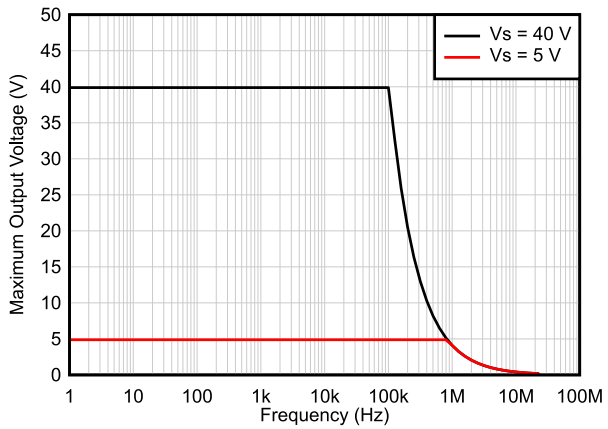


Figure 6-37. Maximum Output Voltage vs Frequency

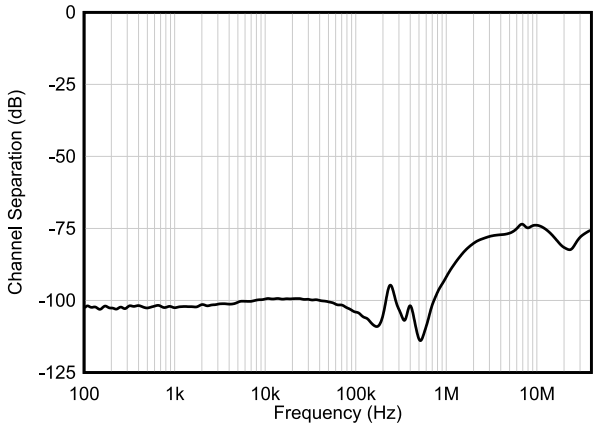


Figure 6-38. Channel Separation vs Frequency

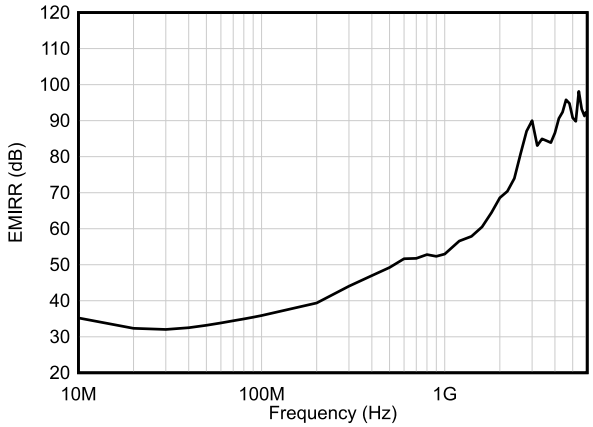


Figure 6-39. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

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6.17 Typical Characteristics: All Other Devices

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in Section 7.

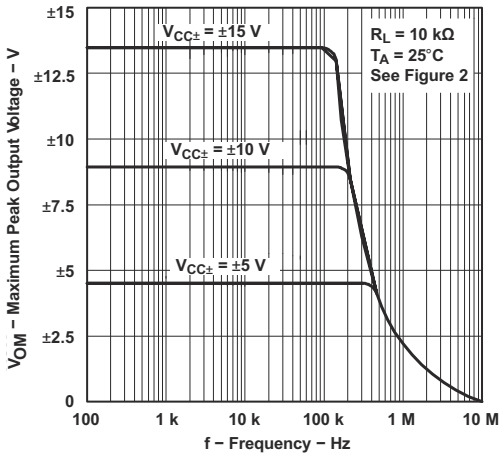


Figure 6-40. Maximum Peak Output Voltage vs Frequency

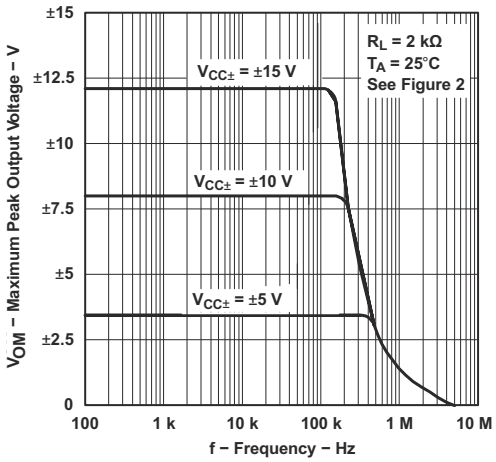


Figure 6-41. Maximum Peak Output Voltage vs Frequency

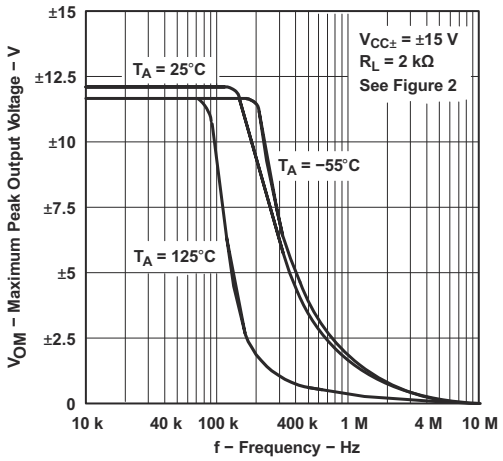


Figure 6-42. Maximum Peak Output Voltage vs Frequency

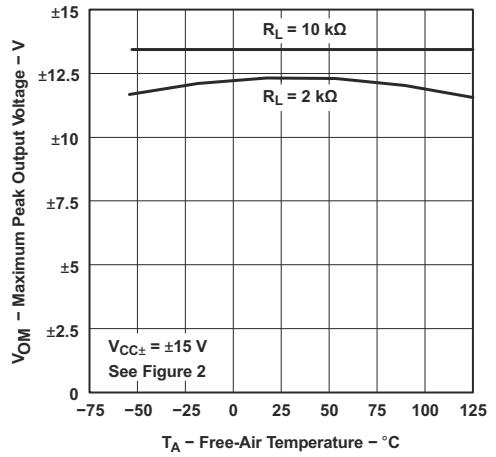


Figure 6-43. Maximum Peak Output Voltage vs Free-Air Temperature

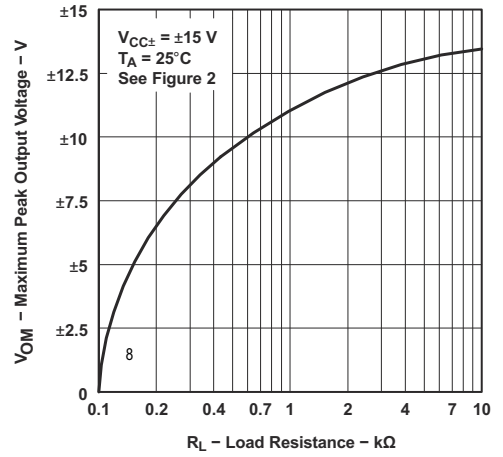


Figure 6-44. Maximum Peak Output Voltage vs Load Resistance

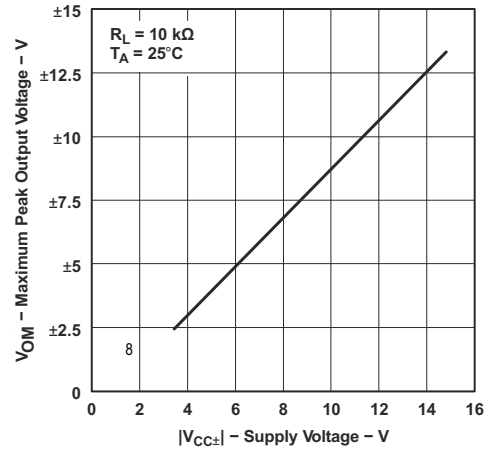


Figure 6-45. Maximum Peak Output Voltage vs Supply Voltage

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6.17 Typical Characteristics: All Other Devices (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in Section 7.

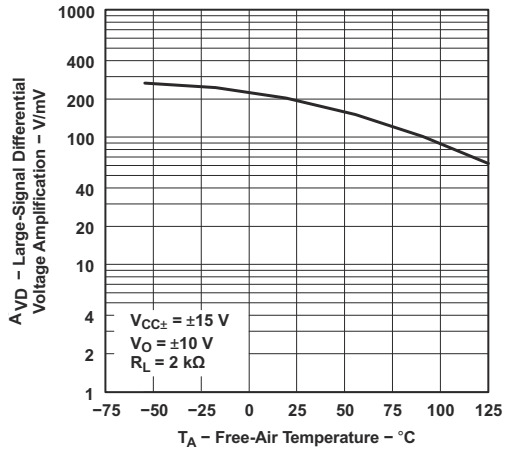


Figure 6-46. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

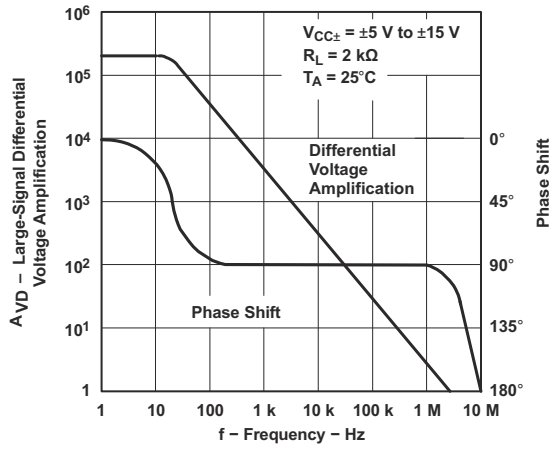


Figure 6-47. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

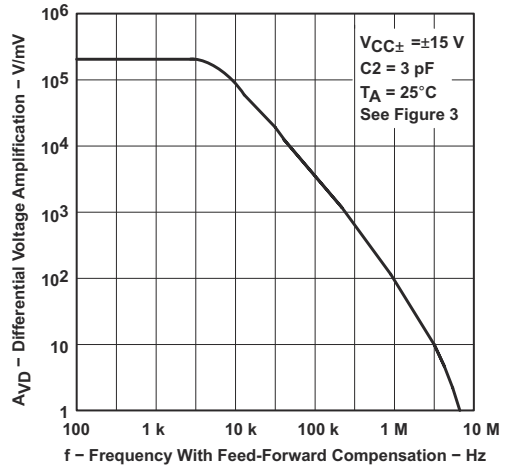


Figure 6-48. Differential Voltage Amplification vs Frequency with Feed-Forward Compensation

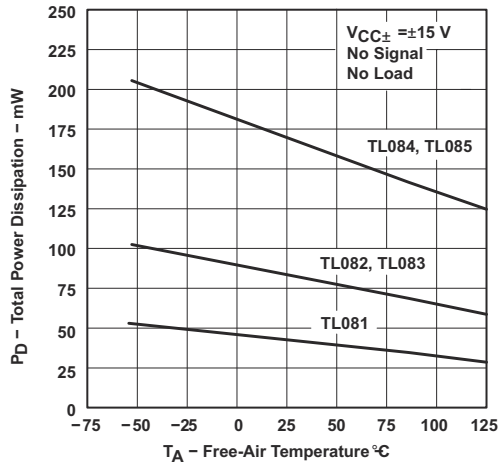


Figure 6-49. Total Power Dissipation vs Free-Air Temperature

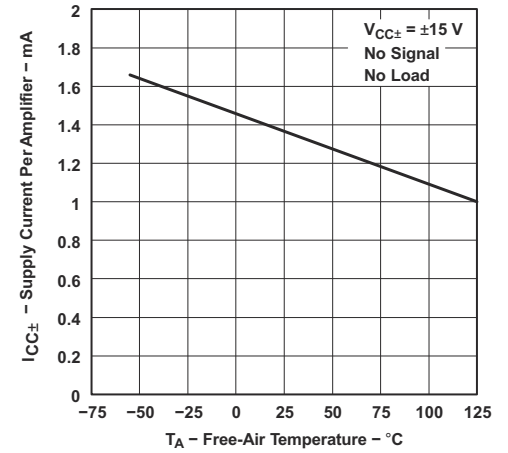


Figure 6-50. Supply Current per Amplifier vs Free-Air Temperature

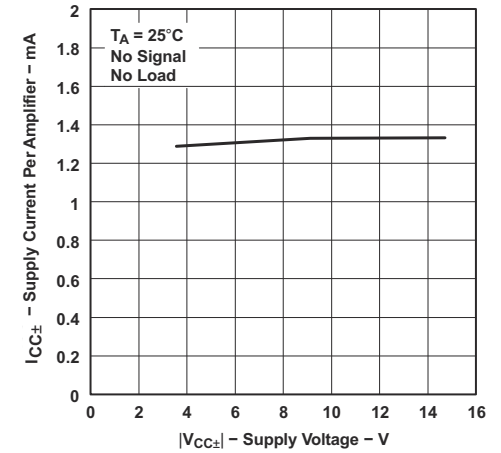


Figure 6-51. Supply Current per Amplifier vs Supply Voltage

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6.17 Typical Characteristics: All Other Devices (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in Section 7.

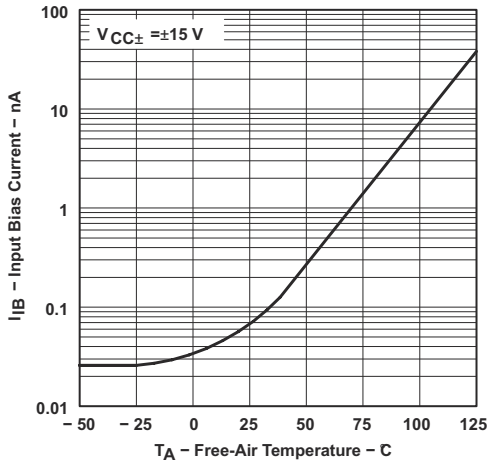


Figure 6-52. Input Bias Current vs Free-Air Temperature

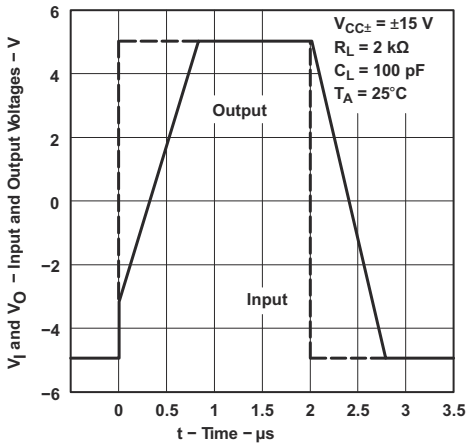


Figure 6-53. Voltage-Follower Large-Signal Pulse Response

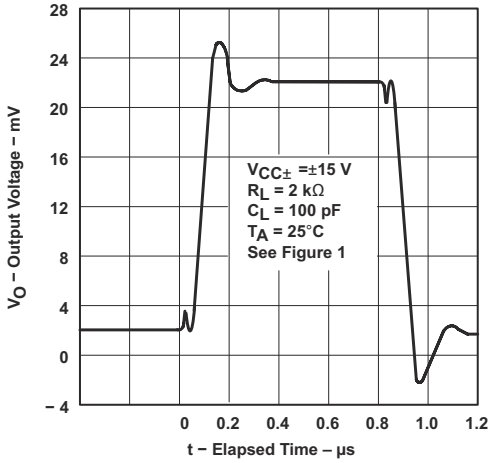


Figure 6-54. Output Voltage vs Elapsed Time

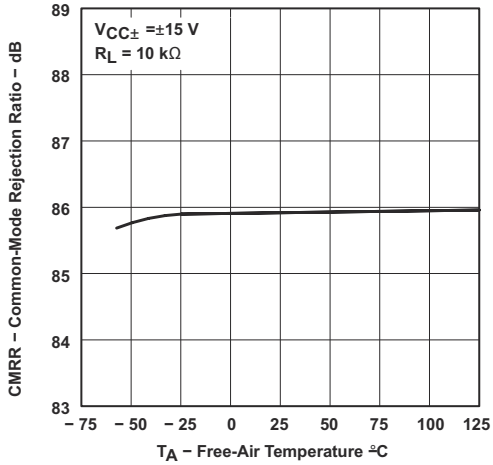


Figure 6-55. Common-Mode Rejection Ratio vs Free-Air Temperature

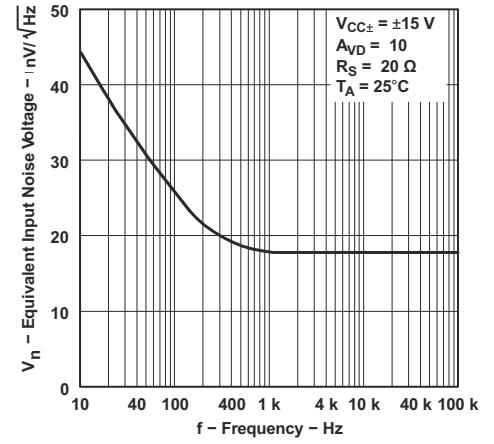


Figure 6-56. Equivalent Input Noise Voltage vs Frequency

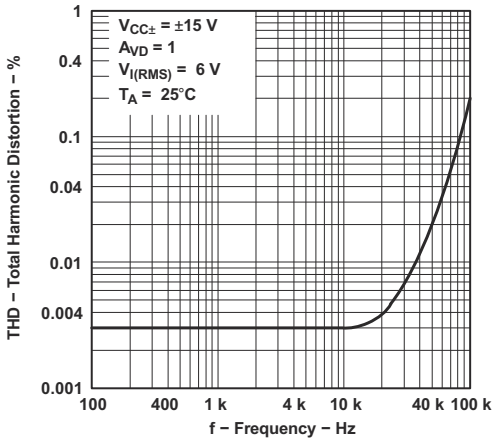


Figure 6-57. Total Harmonic Distortion vs Frequency

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7 Parameter Measurement Information

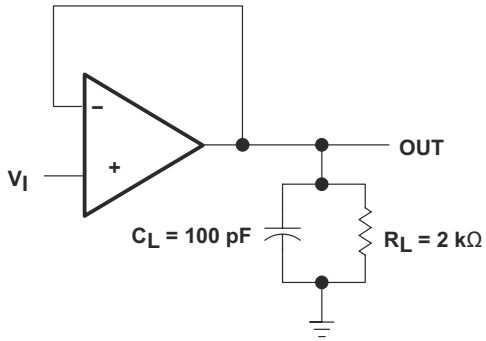


Figure 7-1. Test Figure 1

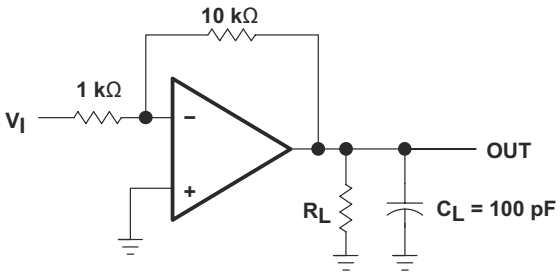


Figure 7-2. Test Figure 2

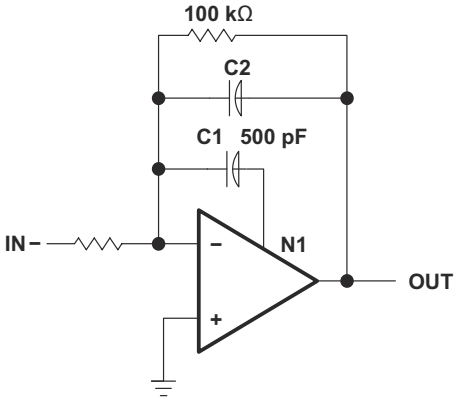


Figure 7-3. Test Figure 3

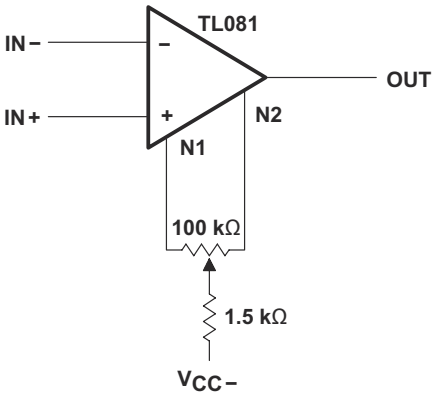


Figure 7-4. Test Figure 4

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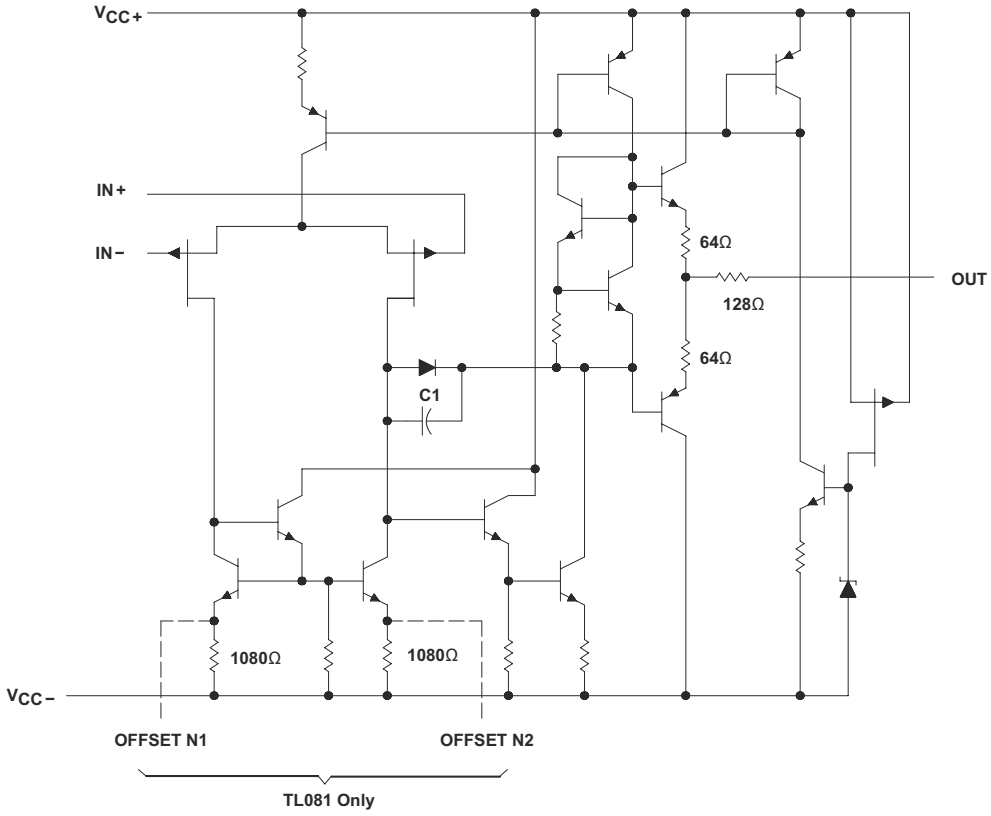
8 Detailed Description

8.1 Overview

The TL08xH family (TL081H, TL082H, and TL084H) is the next-generation family of the industry standard TL08x (TL081, TL082, and TL084) high-voltage general purpose amplifiers. These devices provide outstanding value for cost-sensitive applications requiring high slew rate with high voltage signals, such as motor drive and inverter systems.

A robust MUX-friendly input stage enhances flexibility in design, with common-mode voltage range extending to the positive rail as well as improved settling time in multi-channel applications. Low offset voltage (1 mV, typ) and low offset voltage drift (2 µV/°C) allows the TL08xH family to be used in rugged applications requiring precision current and voltage sensing. High voltage operation (up to 40 V) and high slew rate (20 V/µs) make the TL08xH family a premier choice for high-voltage applications with fast transients.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices will add little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/µs slew rate.

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8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

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9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

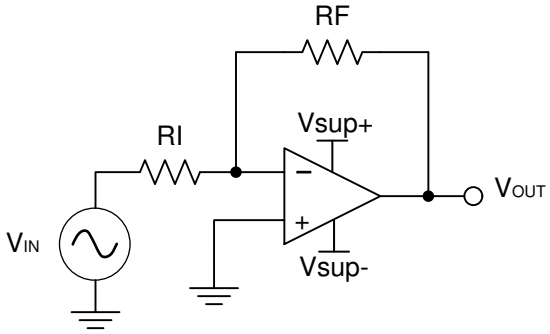


Figure 9-1. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \tag{3}$$

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9.2.1.3 Application Curve

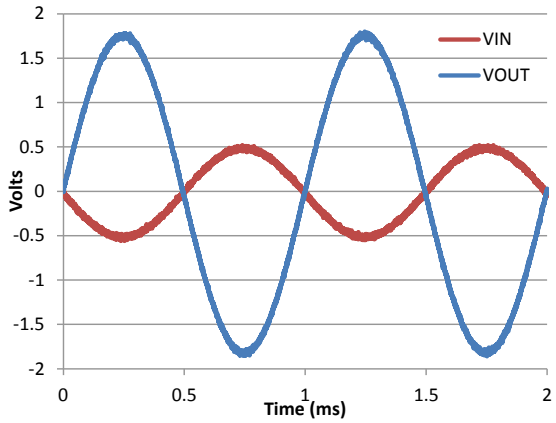


Figure 9-2. Input and Output Voltages of the Inverting Amplifier

9.3 System Examples

9.3.1 General Applications

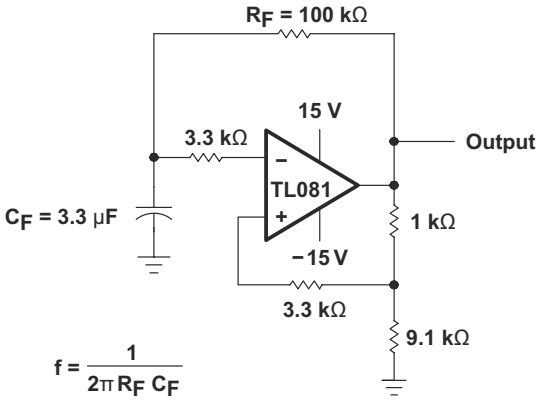


Figure 9-3. 0.5-Hz Square-Wave Oscillator

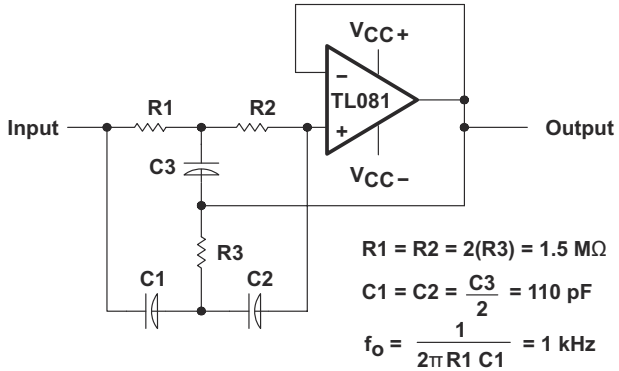


Figure 9-4. High-Q Notch Filter

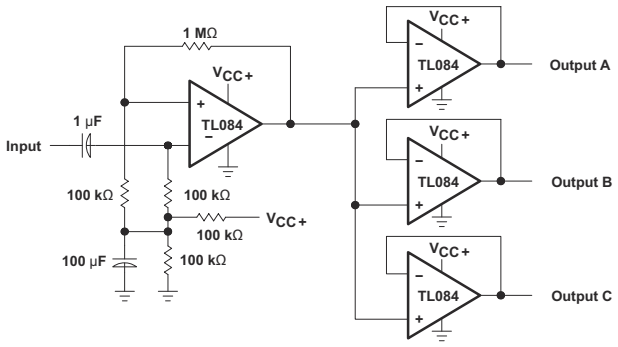
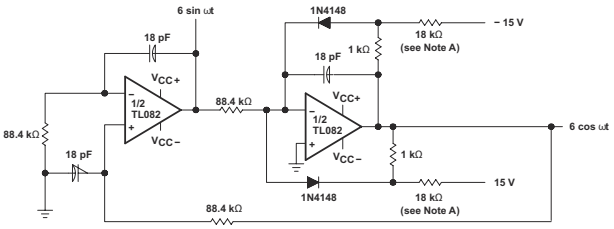


Figure 9-5. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

Figure 9-6. 100-kHz Quadrature Oscillator

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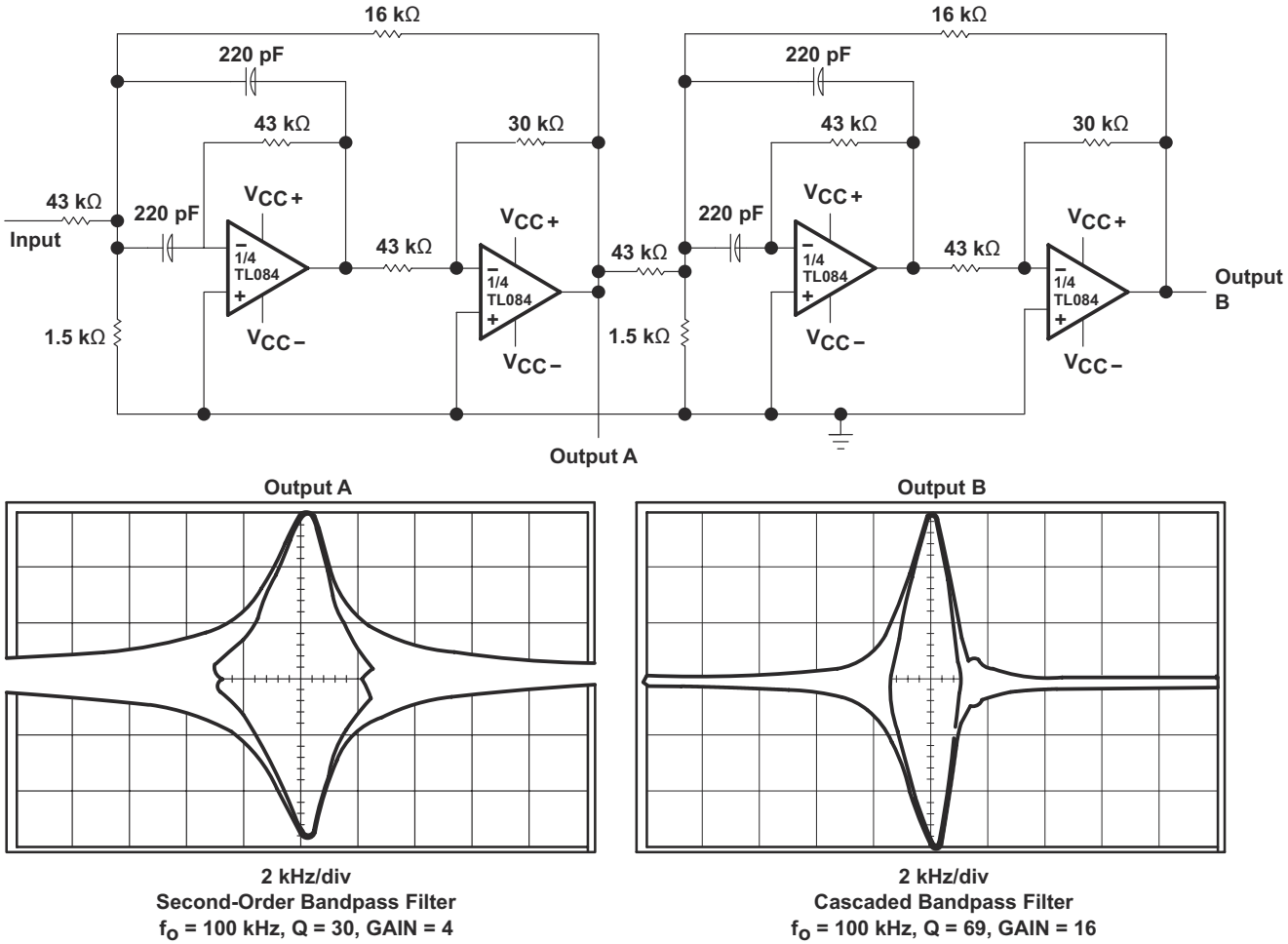


Figure 9-7. Positive-Feedback Bandpass Filter

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see Section 6.2).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to Section 11.

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11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Section 11.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

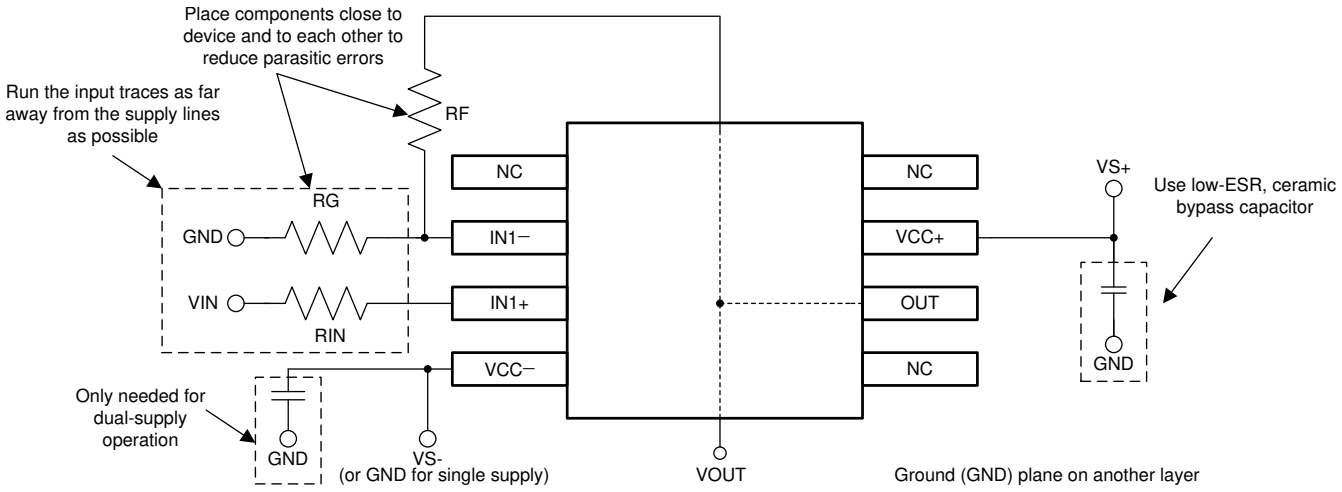


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

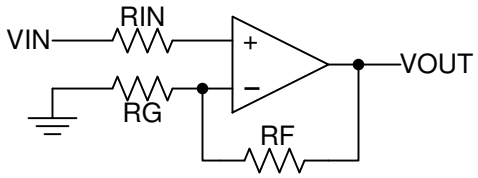


Figure 11-2. Operational Amplifier Schematic for Noninverting Configuration

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851501Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
5962-9851501QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
5962-9851503Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	Samples
5962-9851503QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	Samples
TL081ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	
TL081ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	Samples
TL081BCD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	
TL081BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	
TL081CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples
TL081CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples
TL081CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	Samples
TL081HIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T81V	Samples
TL081HIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1IP	Samples
TL081HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL081D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL081ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	
TL081IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL081IP	Samples
TL082ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	
TL082ACDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	
TL082ACDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	
TL082ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	Samples
TL082ACPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	Samples
TL082BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082BCPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	
TL082CDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	
TL082CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	Samples
TL082CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082CPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPW	LIFEBUY	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082HIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082F	Samples
TL082HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082D	Samples
TL082HIPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082HPW	Samples
TL082ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	
TL082IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	
TL082IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples
TL082IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
TL082MJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL082MJG	Samples
TL082MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
TL084ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084ACDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084ACN	Samples
TL084ACNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples
TL084BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084BCNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	Samples
TL084CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084HIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084HID	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084HIDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY	Samples
TL084HIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084PW	Samples
TL084ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084INE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084MFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL084MFK	Samples
TL084MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	Samples
TL084MJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL084MJ	Samples
TL084MJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	Samples
TL084QD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

- Catalog : TL082, TL084
- Automotive : TL082-Q1, TL082-Q1
- Military : TL082M, TL084M

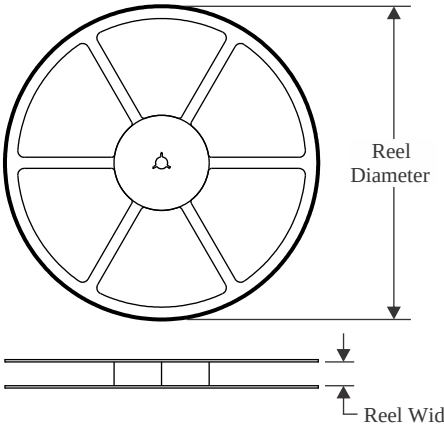
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

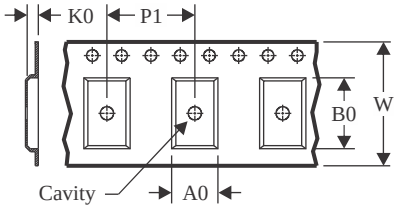
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

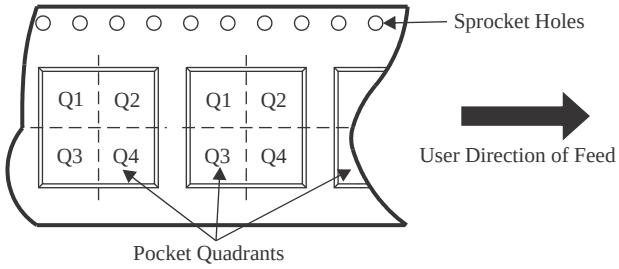


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

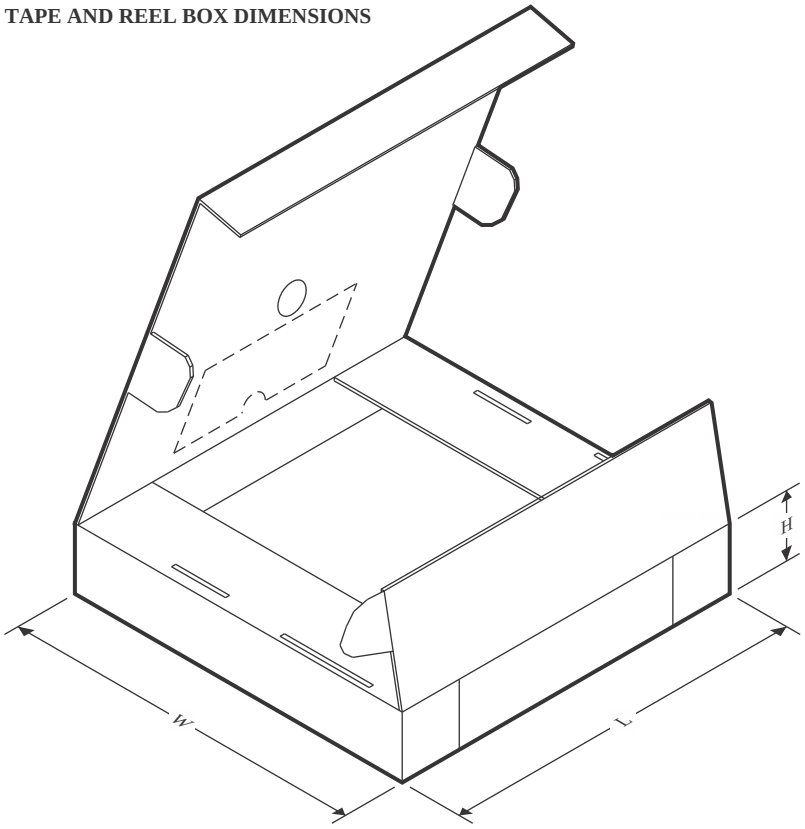


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL081HIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL081HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL081HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL082HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL084HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

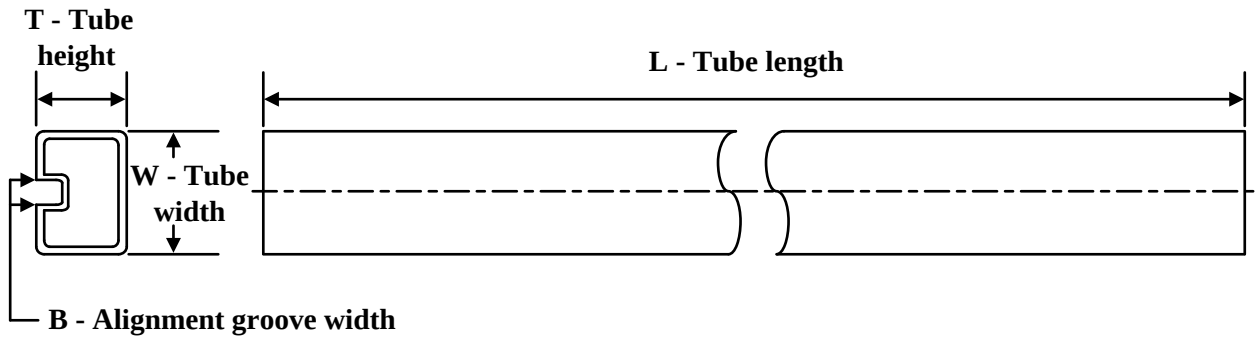


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL081BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL081CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL081CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL081HIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL081HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL081HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL081IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL082ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL082ACPSR	SO	PS	8	2000	356.0	356.0	35.0
TL082BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL082CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL082CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL082CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL082HIDR	SOIC	D	8	3000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082HIPWR	TSSOP	PW	8	3000	356.0	356.0	35.0
TL082IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL082IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL082IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL084ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TL084ACDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084ACNSR	SO	NS	14	2000	356.0	356.0	35.0
TL084BCDR	SOIC	D	14	2500	340.5	336.1	32.0
TL084CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084CDR	SOIC	D	14	2500	340.5	336.1	32.0
TL084CDRG4	SOIC	D	14	2500	340.5	336.1	32.0
TL084CNSR	SO	NS	14	2000	356.0	356.0	35.0
TL084CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084HIDR	SOIC	D	14	2500	356.0	356.0	35.0
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL084HIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084IDR	SOIC	D	14	2500	340.5	336.1	32.0
TL084QDR	SOIC	D	14	2500	350.0	350.0	43.0
TL084QDRG4	SOIC	D	14	2500	350.0	350.0	43.0

TUBE



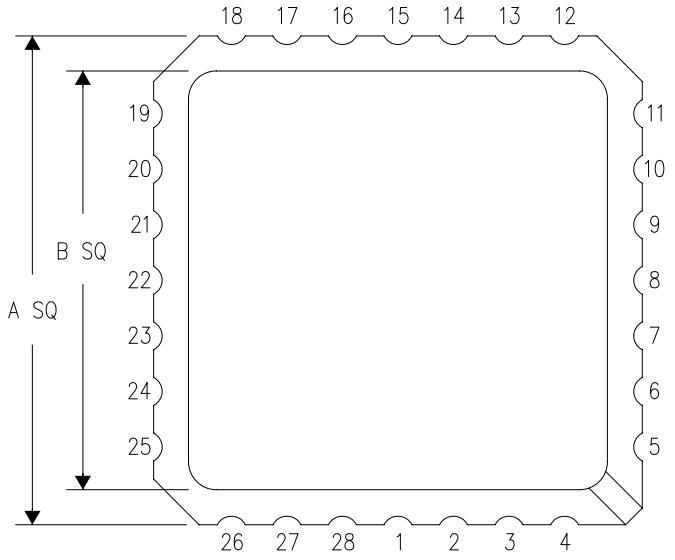
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9851501Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9851503Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
TL081ACD	D	SOIC	8	75	507	8	3940	4.32
TL081ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL081BCD	D	SOIC	8	75	507	8	3940	4.32
TL081BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL081CD	D	SOIC	8	75	507	8	3940	4.32
TL081CP	P	PDIP	8	50	506	13.97	11230	4.32
TL081CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL081ID	D	SOIC	8	75	507	8	3940	4.32
TL081IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082ACD	D	SOIC	8	75	507	8	3940	4.32
TL082ACD	D	SOIC	8	75	506.6	8	3940	4.32
TL082ACDE4	D	SOIC	8	75	506.6	8	3940	4.32
TL082ACDE4	D	SOIC	8	75	507	8	3940	4.32
TL082ACDG4	D	SOIC	8	75	506.6	8	3940	4.32
TL082ACDG4	D	SOIC	8	75	507	8	3940	4.32
TL082ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL082BCD	D	SOIC	8	75	507	8	3940	4.32
TL082BCDE4	D	SOIC	8	75	507	8	3940	4.32
TL082BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL082BCPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL082CD	D	SOIC	8	75	506.6	8	3940	4.32
TL082CD	D	SOIC	8	75	507	8	3940	4.32
TL082CDE4	D	SOIC	8	75	507	8	3940	4.32
TL082CDE4	D	SOIC	8	75	506.6	8	3940	4.32
TL082CP	P	PDIP	8	50	506	13.97	11230	4.32
TL082CPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TL082ID	D	SOIC	8	75	506.6	8	3940	4.32

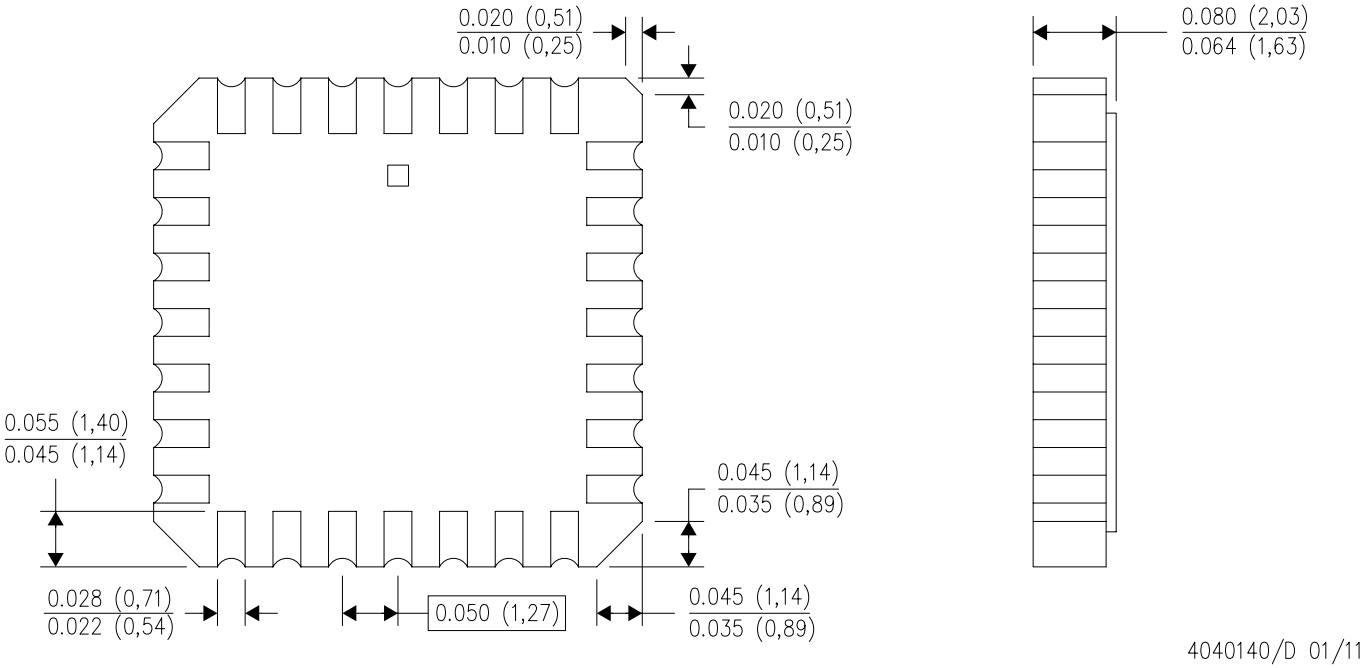
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL082ID	D	SOIC	8	75	507	8	3940	4.32
TL082IDG4	D	SOIC	8	75	507	8	3940	4.32
TL082IDG4	D	SOIC	8	75	506.6	8	3940	4.32
TL082IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL082MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TL084ACD	D	SOIC	14	50	507	8	3940	4.32
TL084ACD	D	SOIC	14	50	506.6	8	3940	4.32
TL084ACDE4	D	SOIC	14	50	507	8	3940	4.32
TL084ACDE4	D	SOIC	14	50	506.6	8	3940	4.32
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCD	D	SOIC	14	50	507	8	3940	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084CD	D	SOIC	14	50	507	8	3940	4.32
TL084CD	D	SOIC	14	50	506.6	8	3940	4.32
TL084CDE4	D	SOIC	14	50	506.6	8	3940	4.32
TL084CDE4	D	SOIC	14	50	507	8	3940	4.32
TL084CDG4	D	SOIC	14	50	506.6	8	3940	4.32
TL084CDG4	D	SOIC	14	50	507	8	3940	4.32
TL084CN	N	PDIP	14	25	506	13.97	11230	4.32
TL084CN	N	PDIP	14	25	506	13.97	11230	4.32
TL084CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TL084CPWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
TL084ID	D	SOIC	14	50	507	8	3940	4.32
TL084IN	N	PDIP	14	25	506	13.97	11230	4.32
TL084INE4	N	PDIP	14	25	506	13.97	11230	4.32
TL084MFK	FK	LCCC	20	1	506.98	12.06	2030	NA
TL084MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TL084QD	D	SOIC	14	50	505.46	6.76	3810	4
TL084QDG4	D	SOIC	14	50	505.46	6.76	3810	4

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

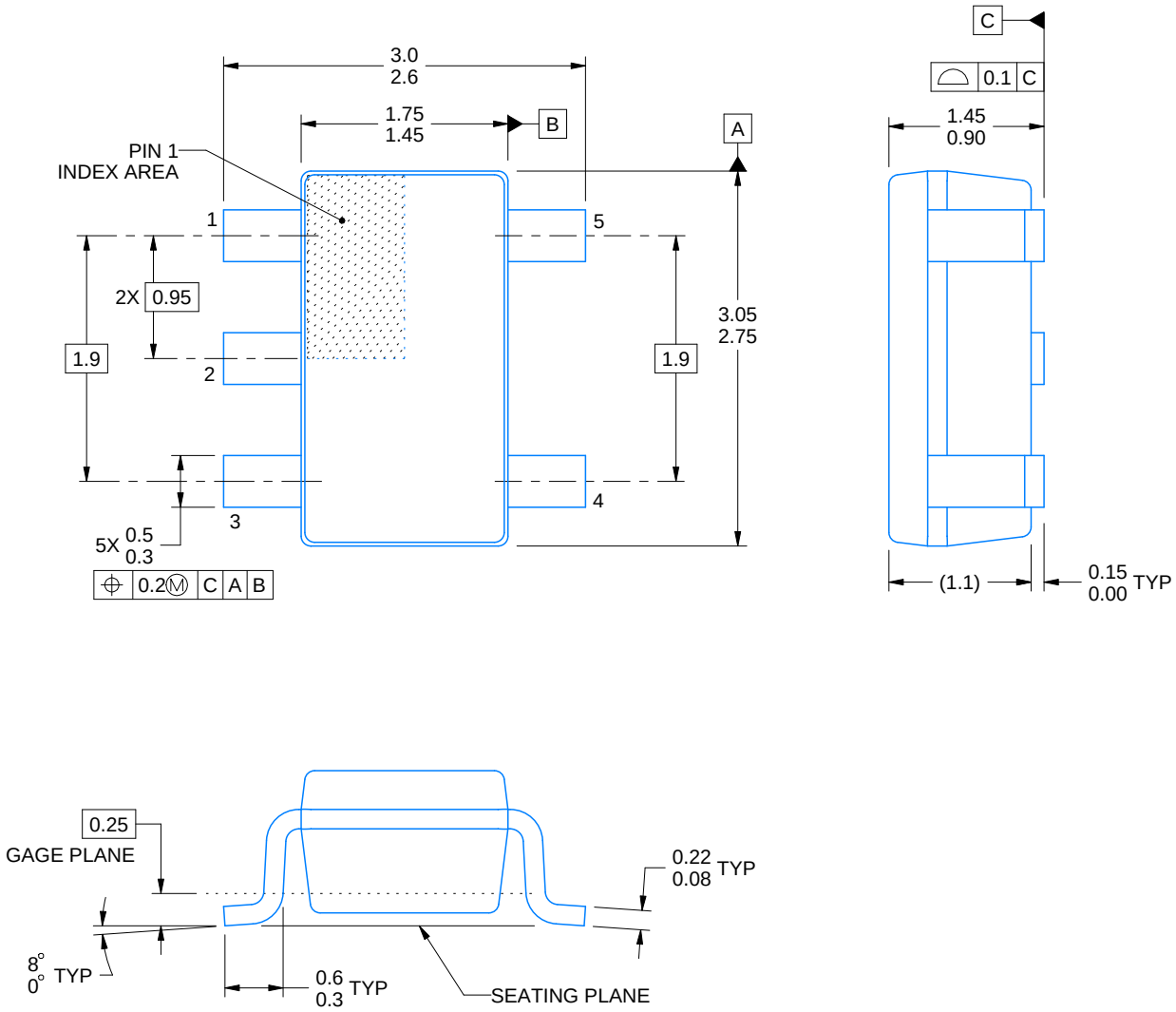
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

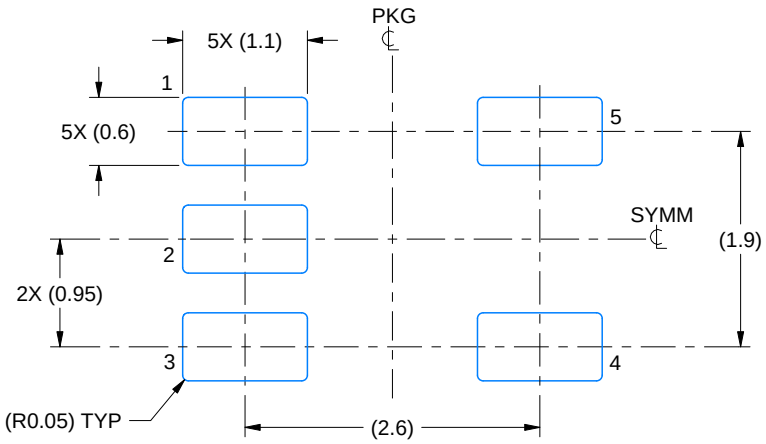
SMALL OUTLINE TRANSISTOR



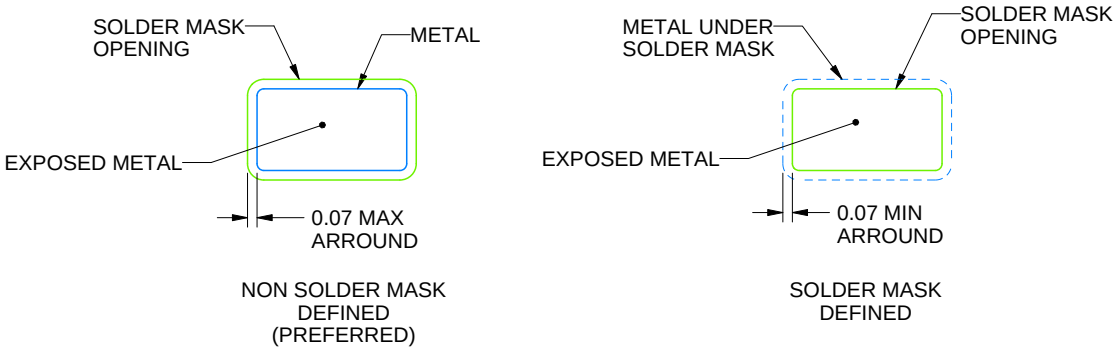
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

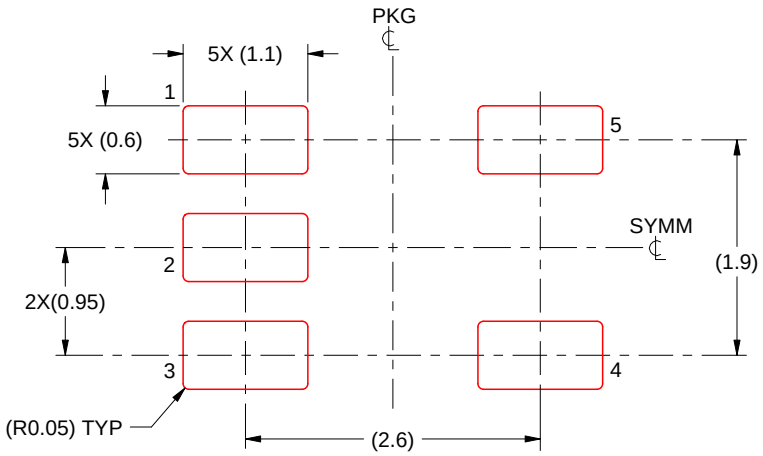


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

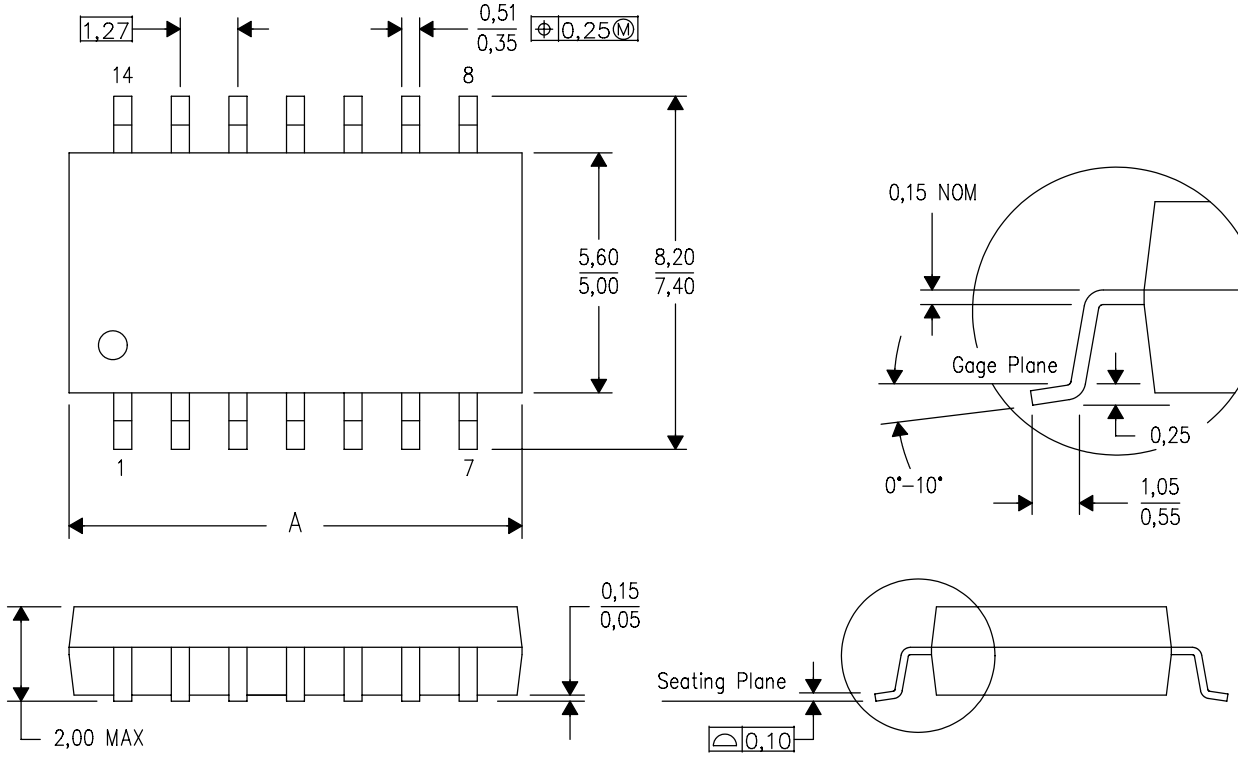
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

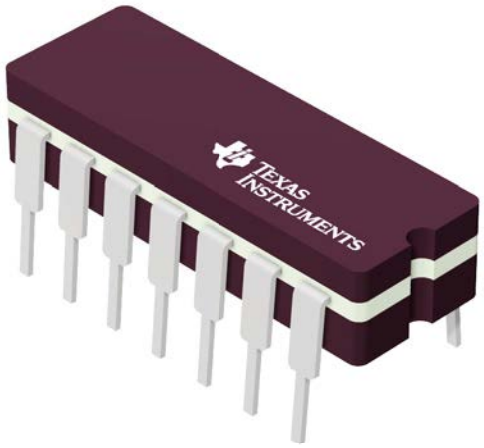
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

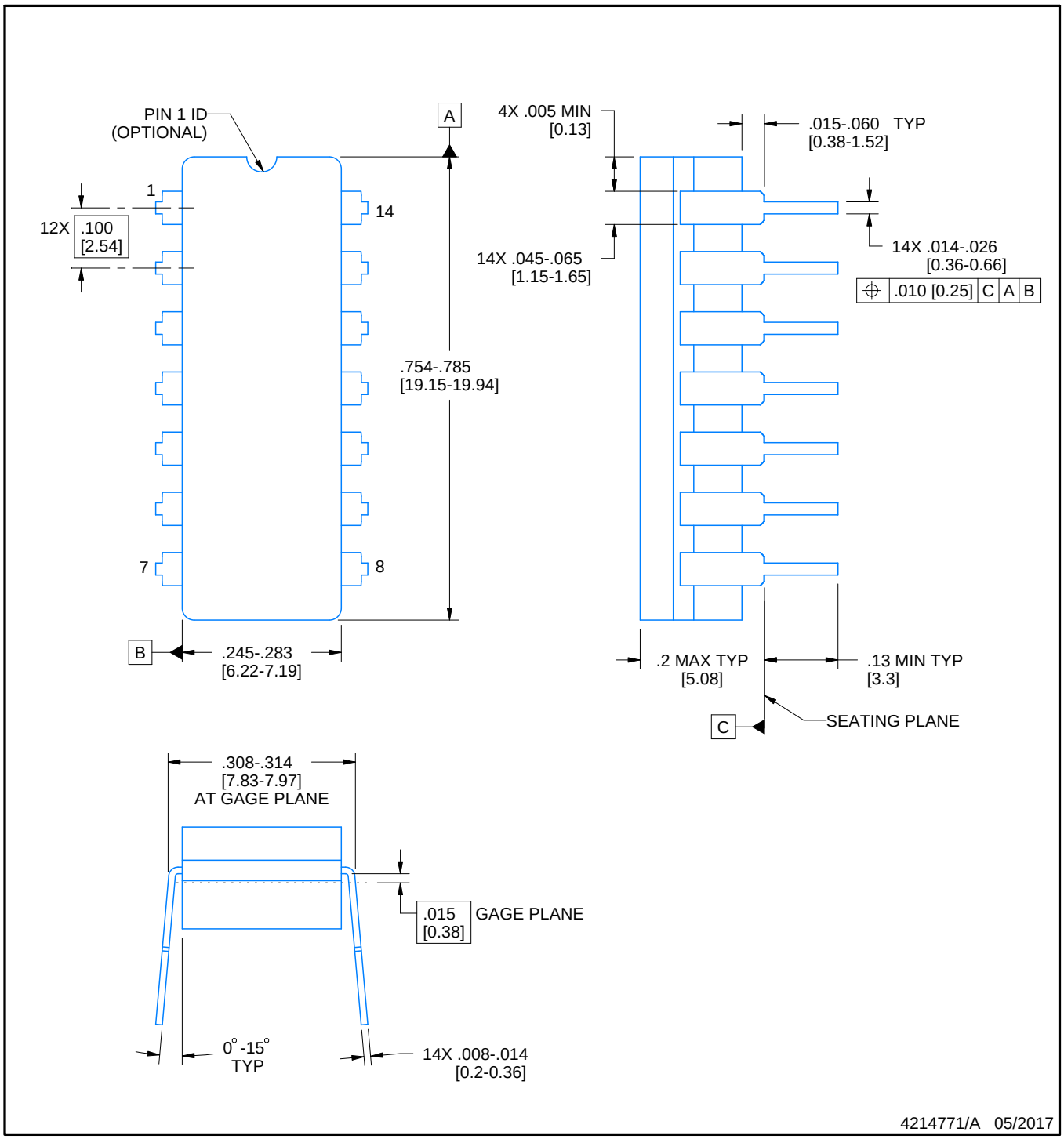


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

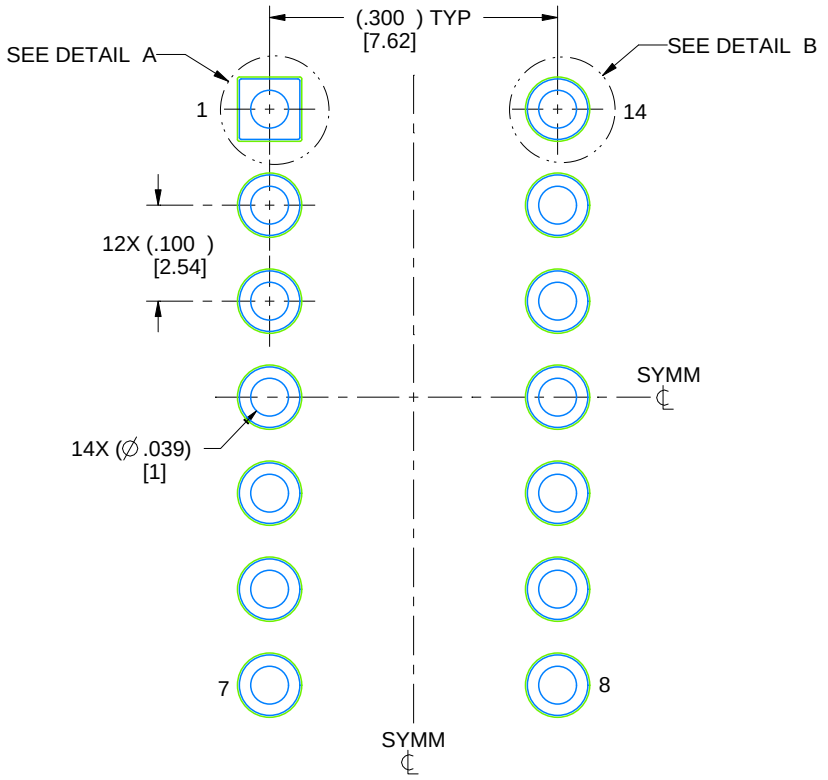
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

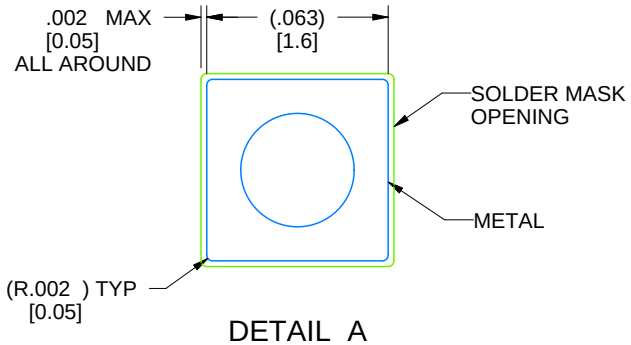
J0014A

CDIP - 5.08 mm max height

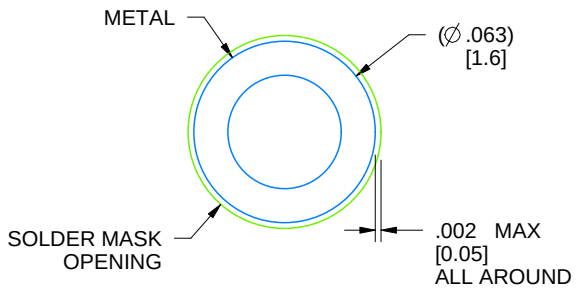
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



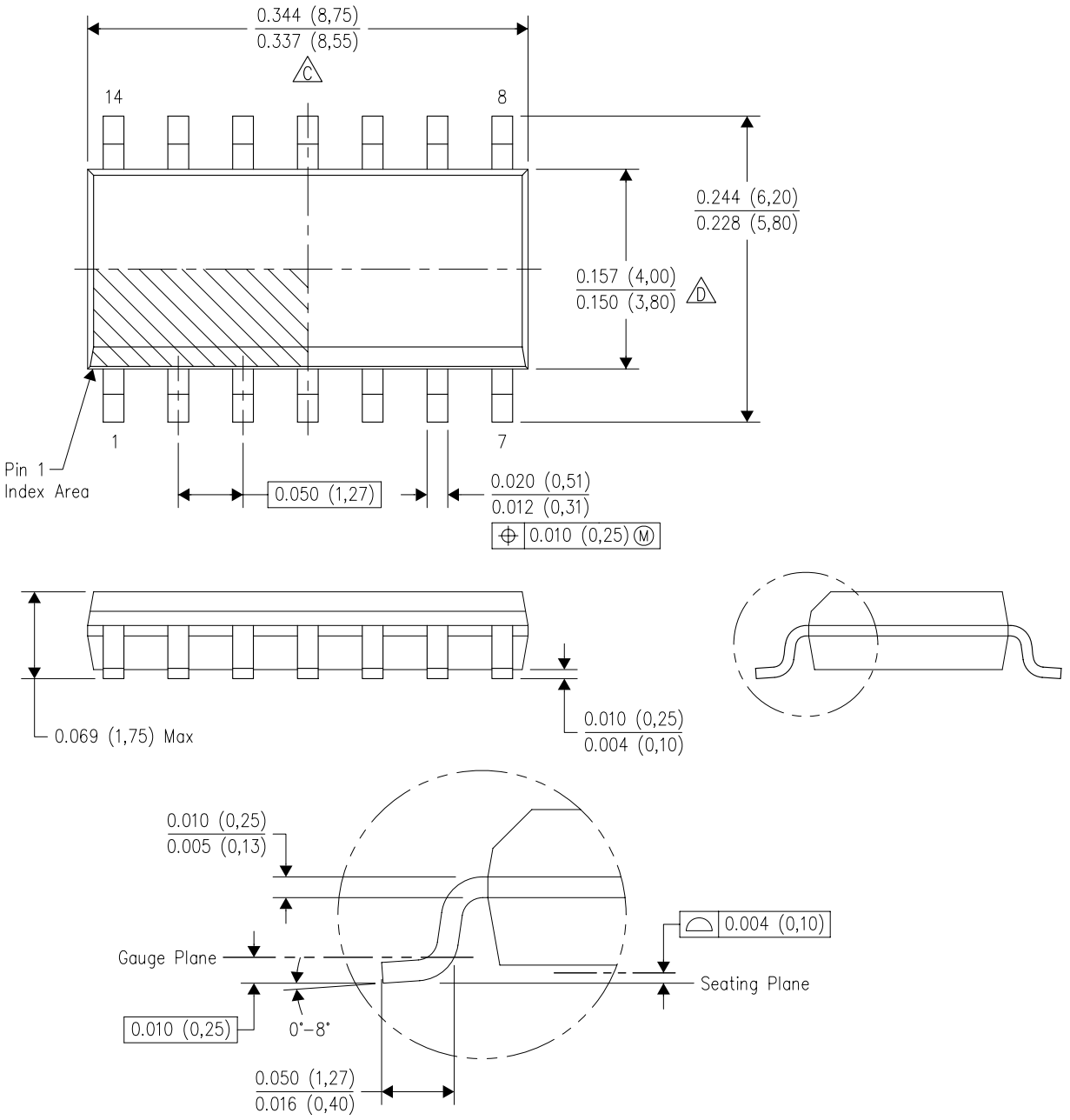
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

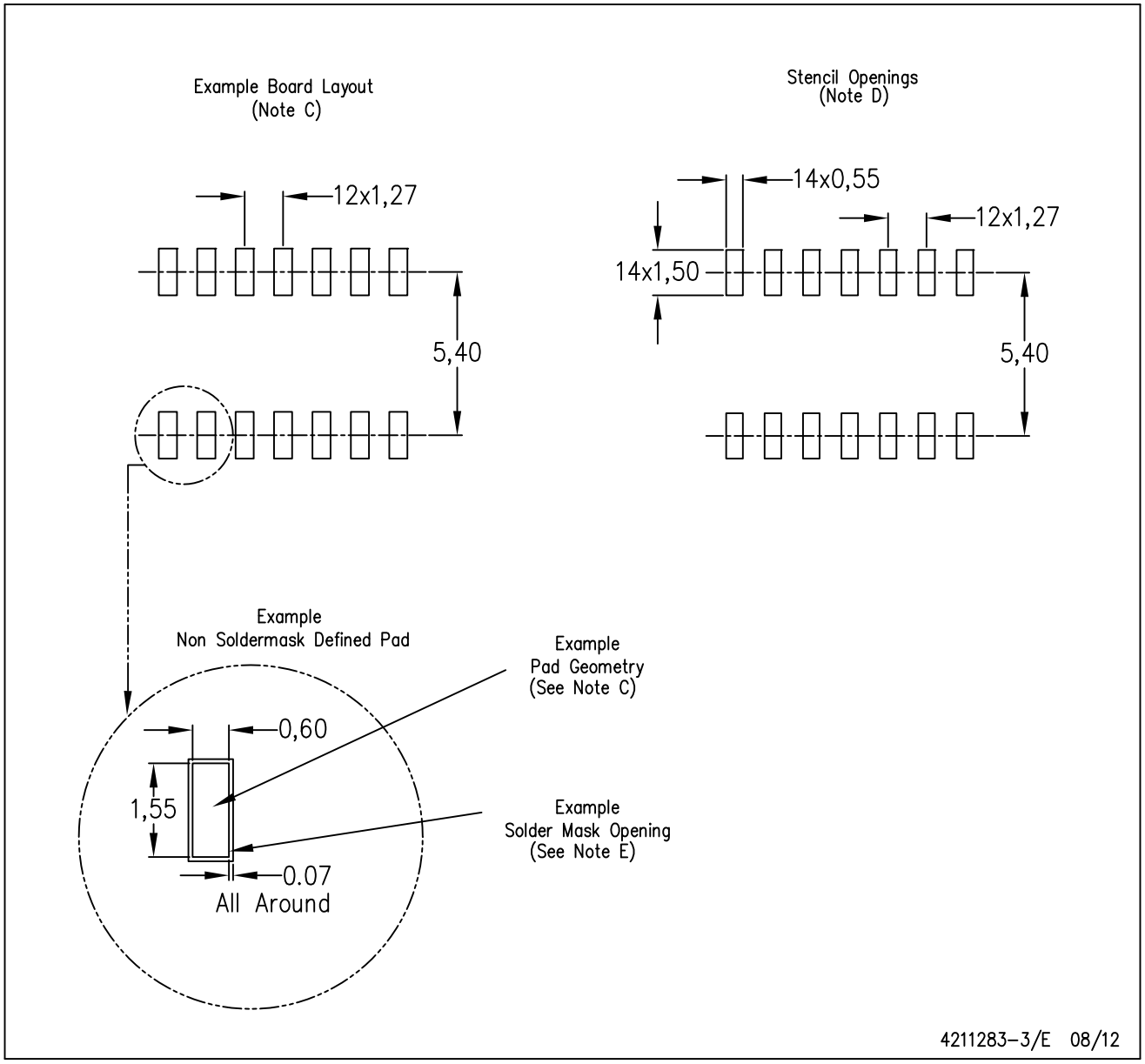
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

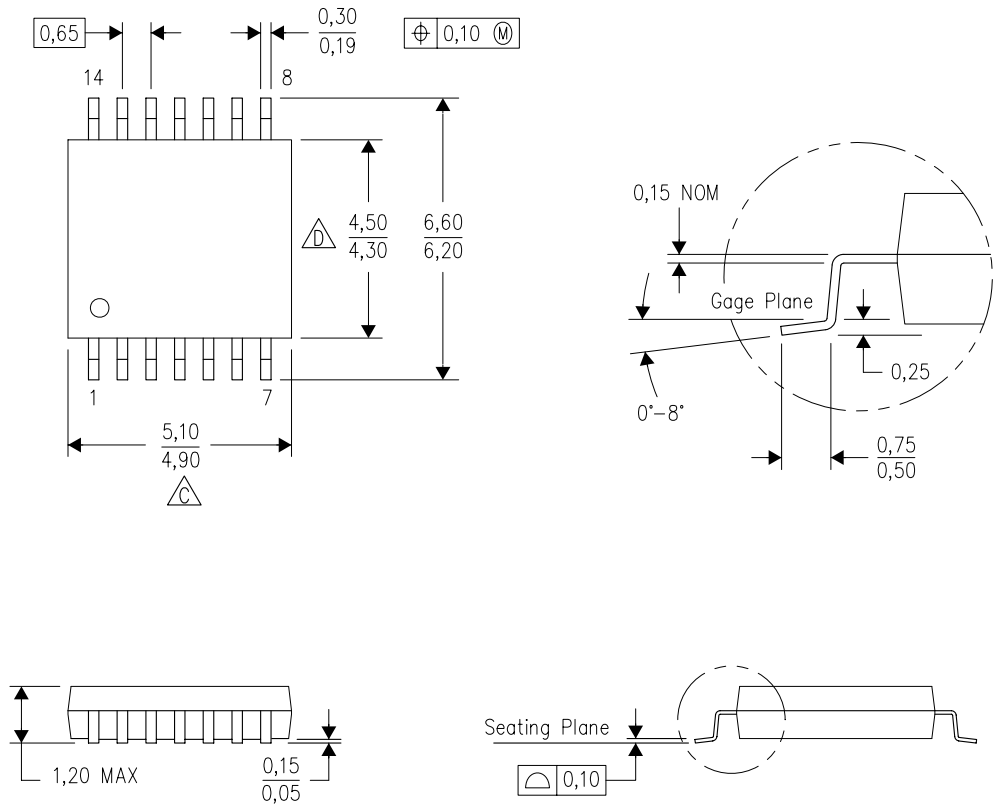
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

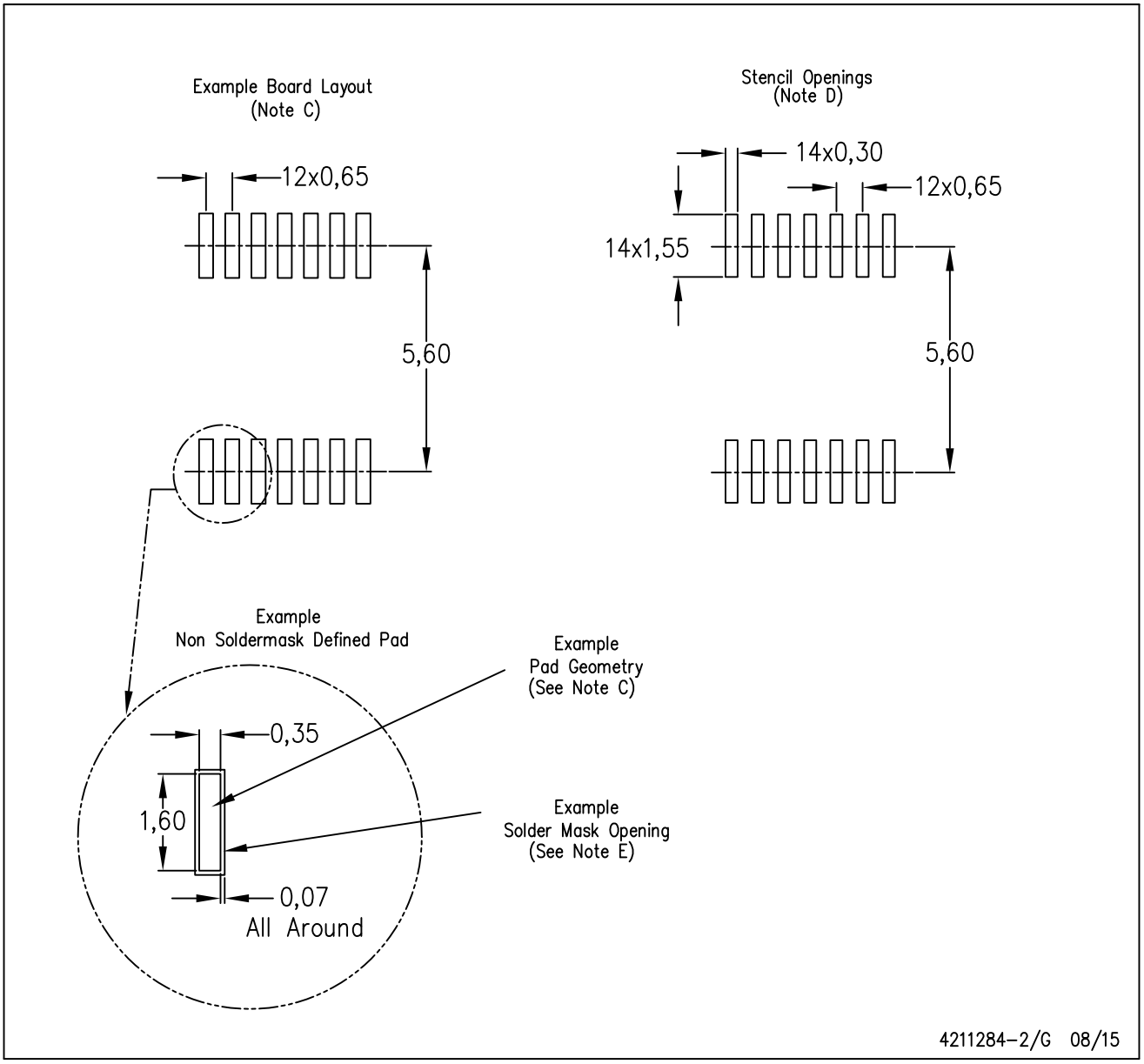
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



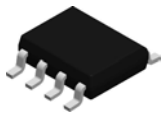
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

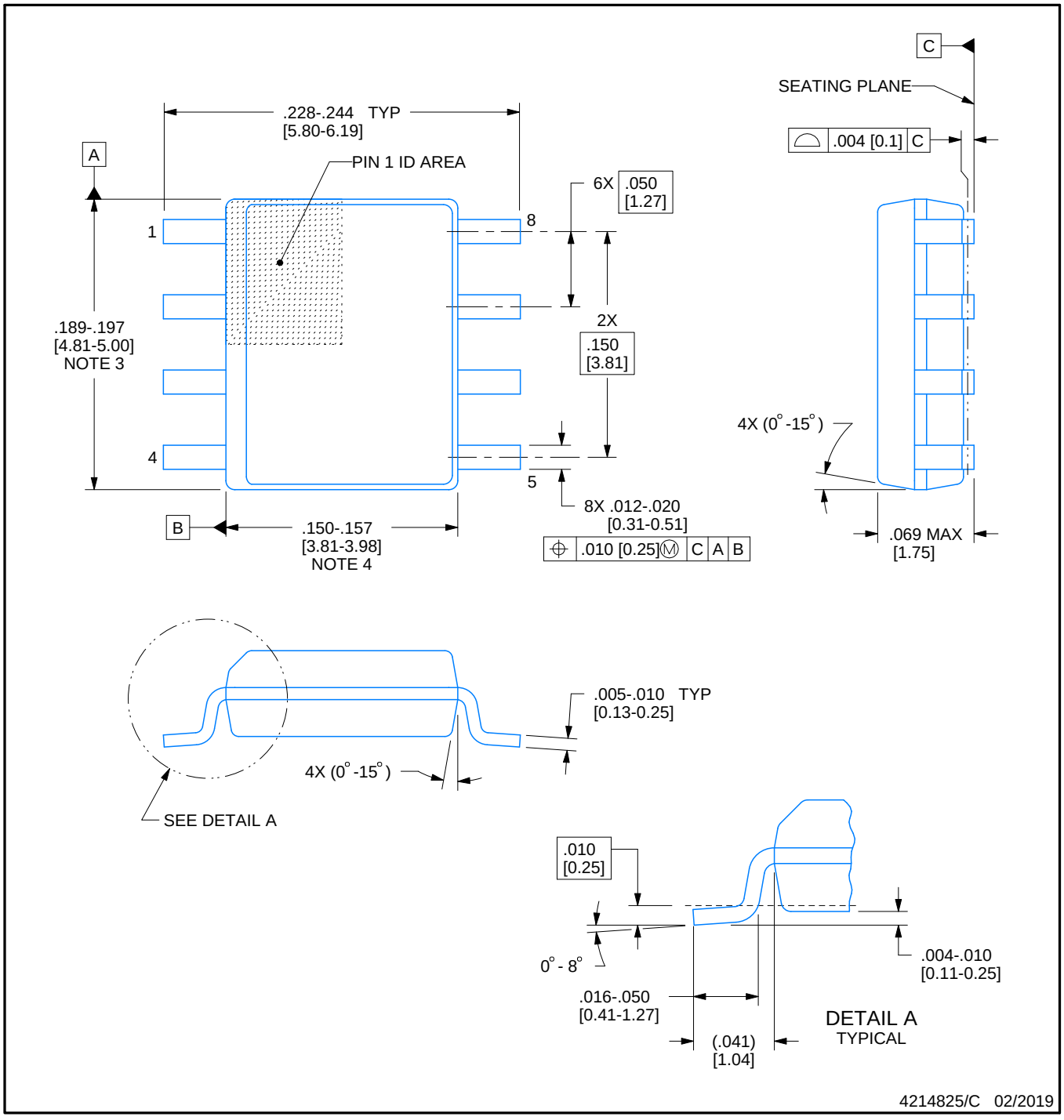


PACKAGE OUTLINE

D0008A

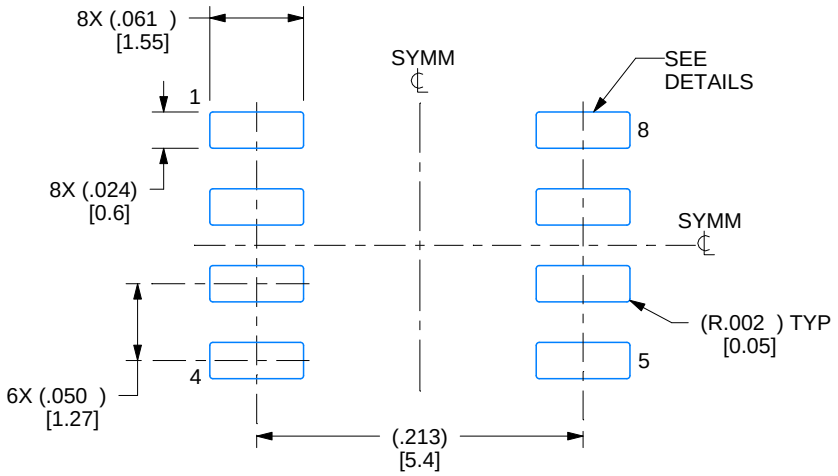
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

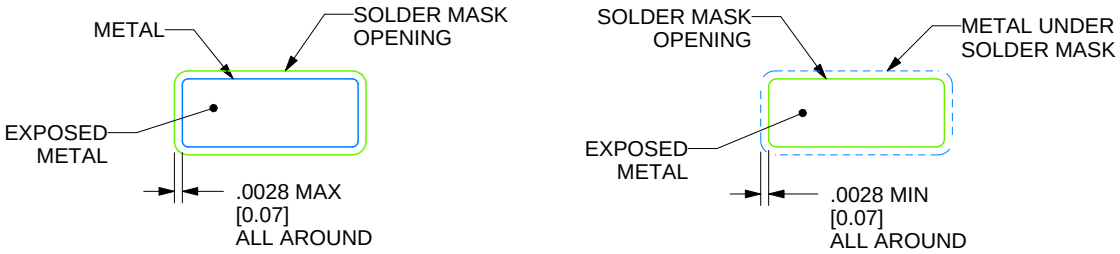


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

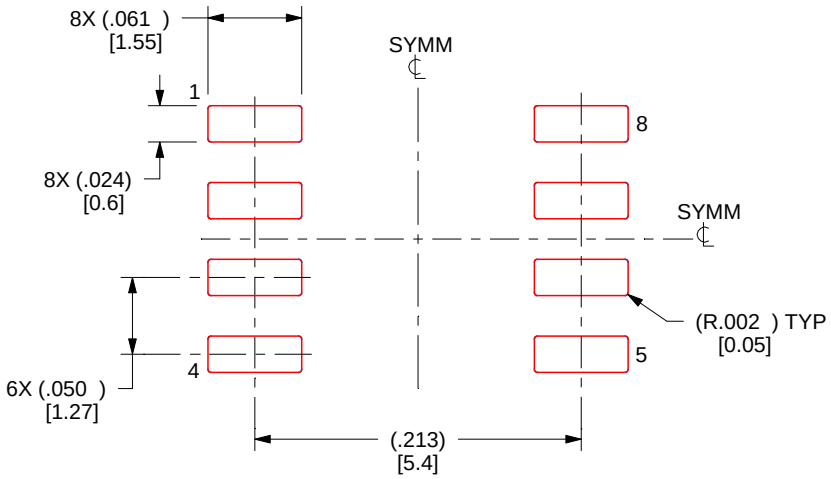
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

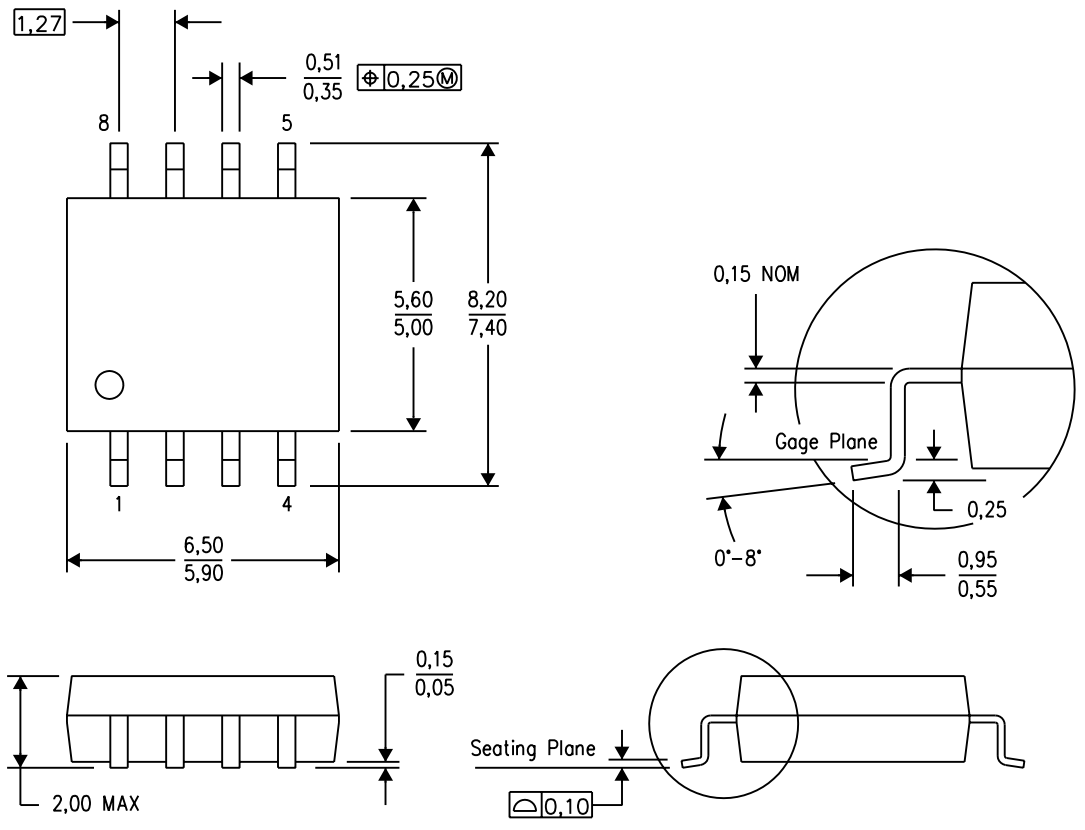
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

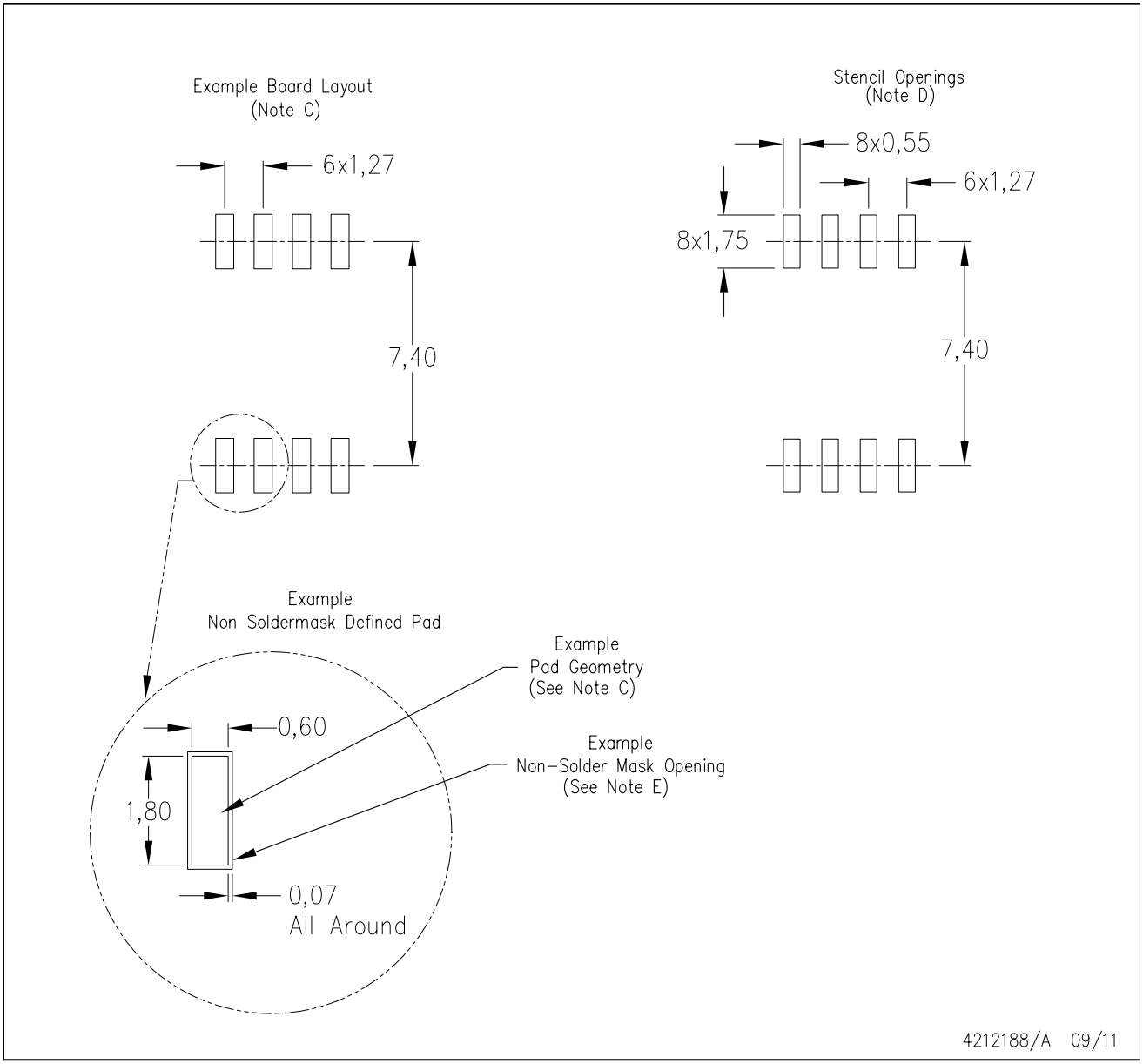
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

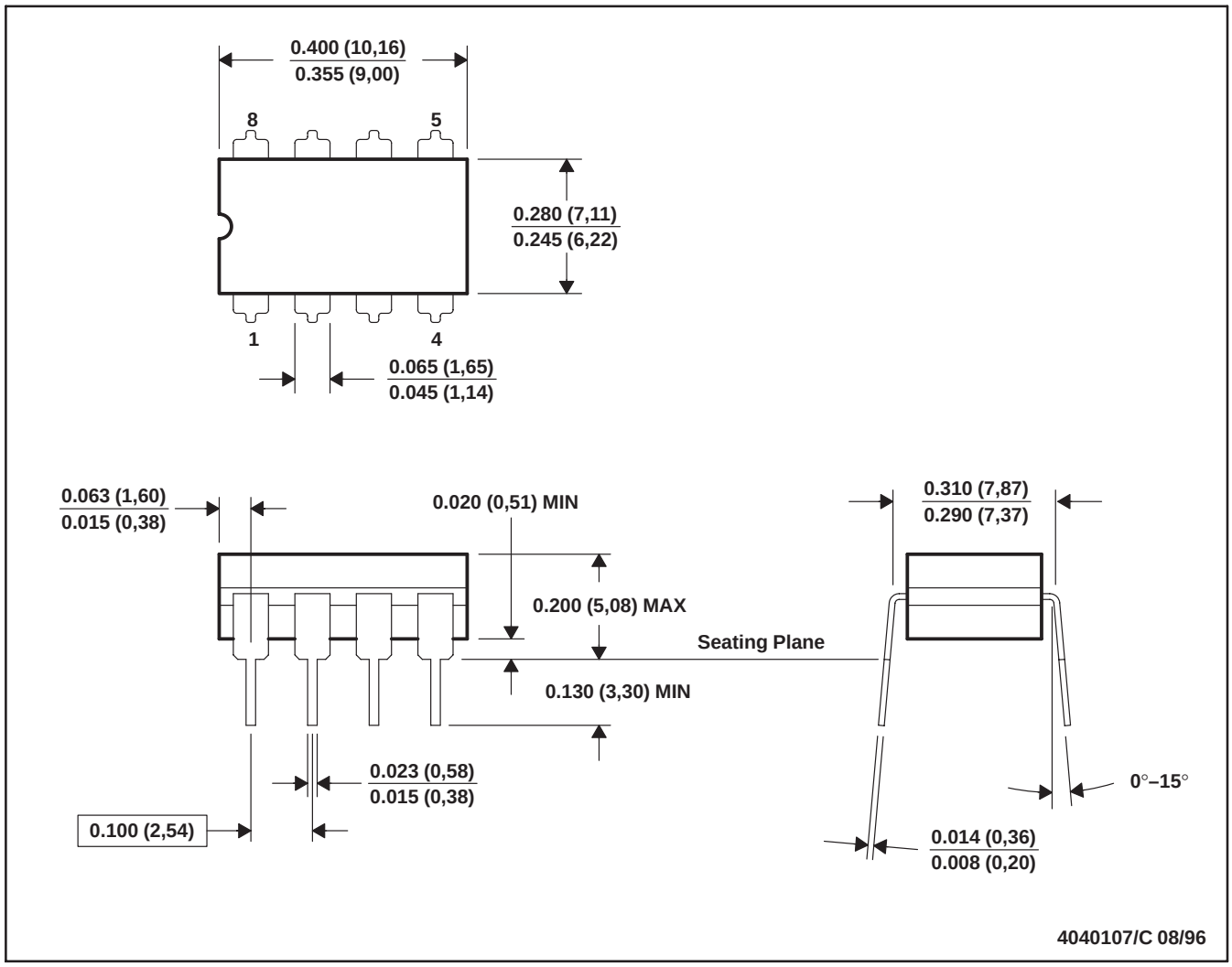
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

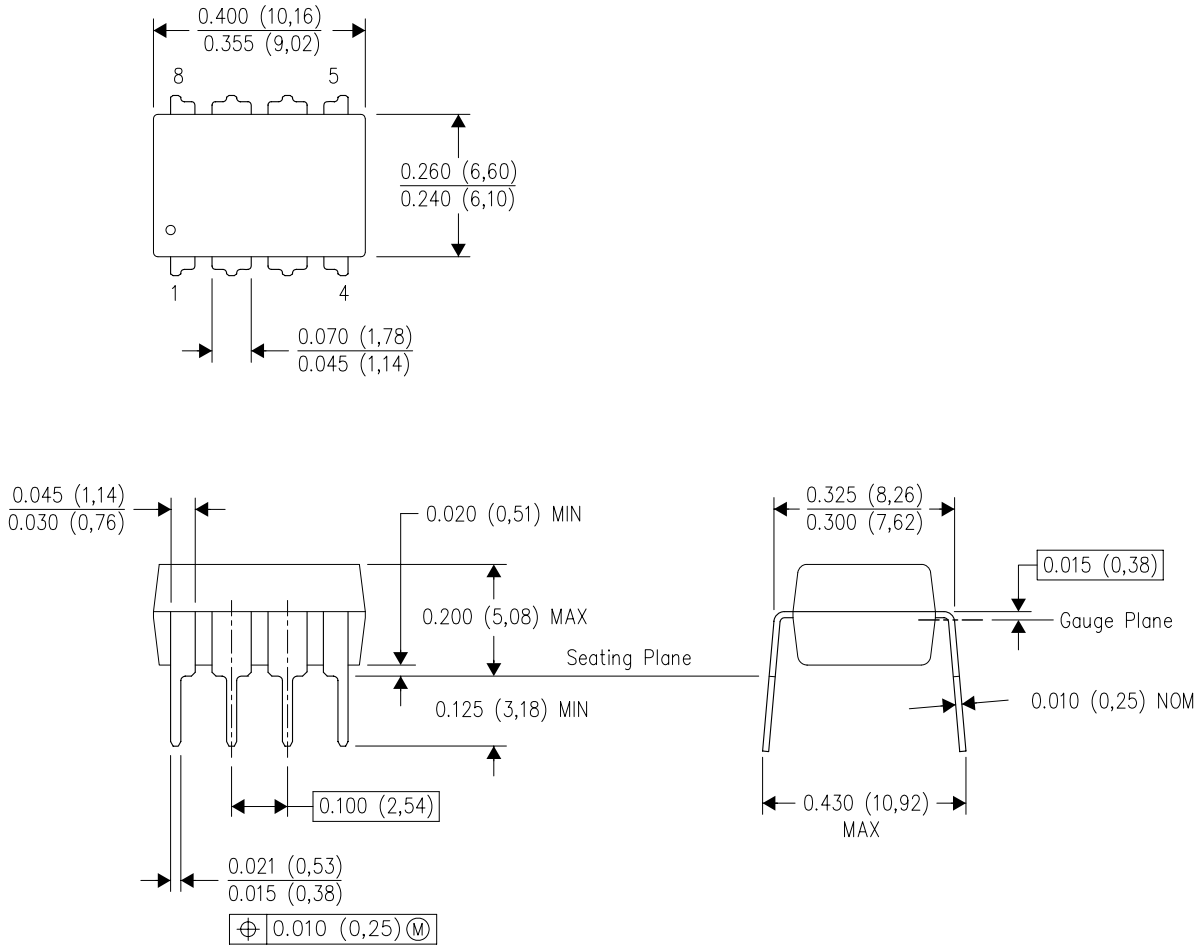
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

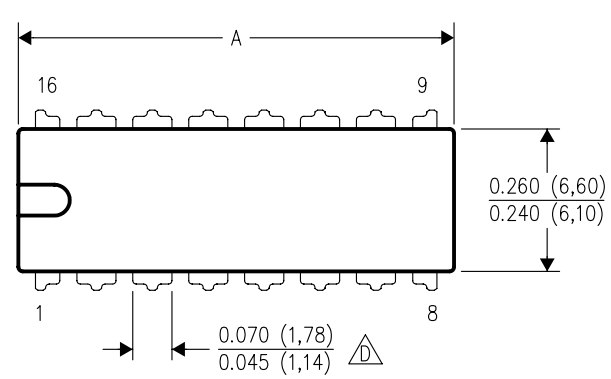


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

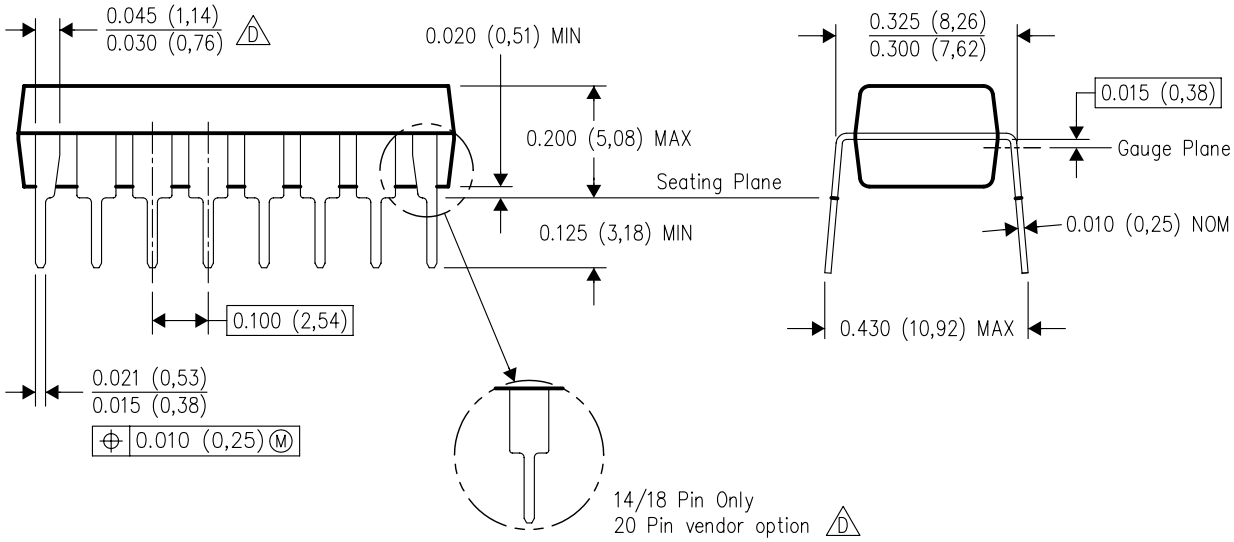
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

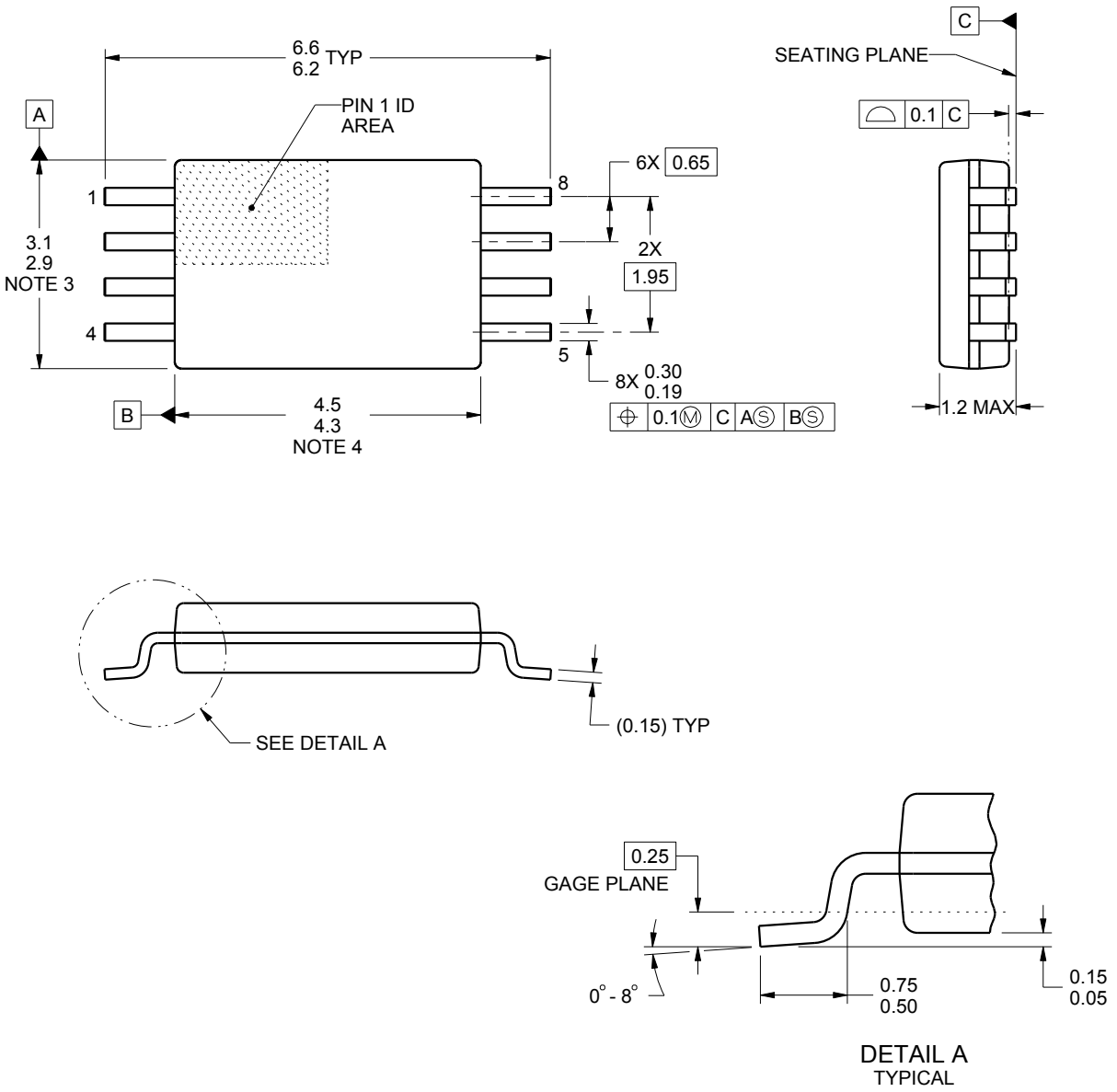
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0008A

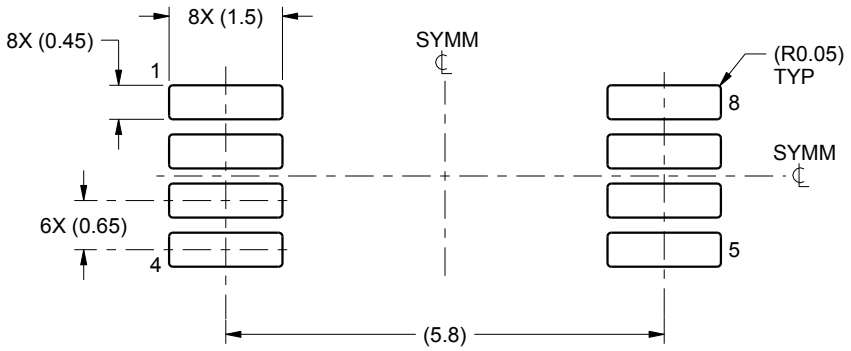
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

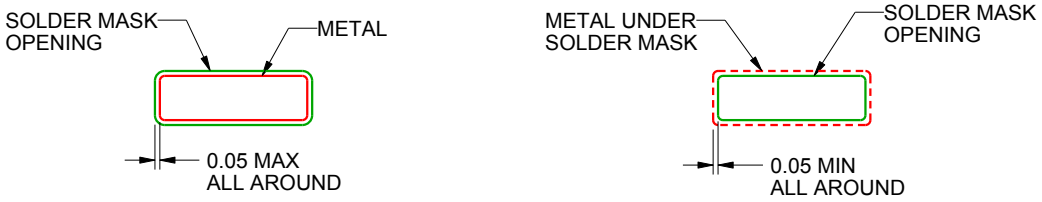


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

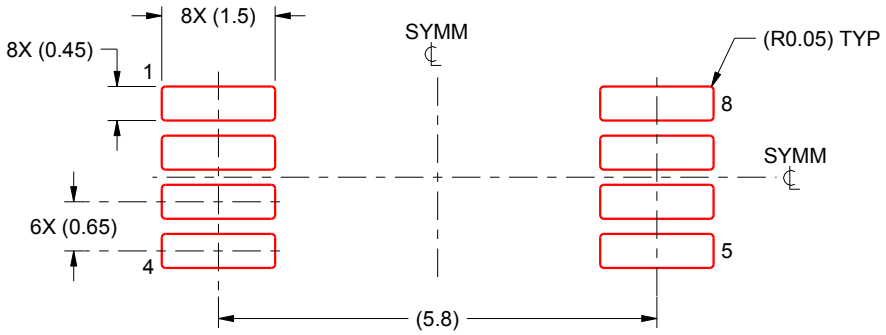


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



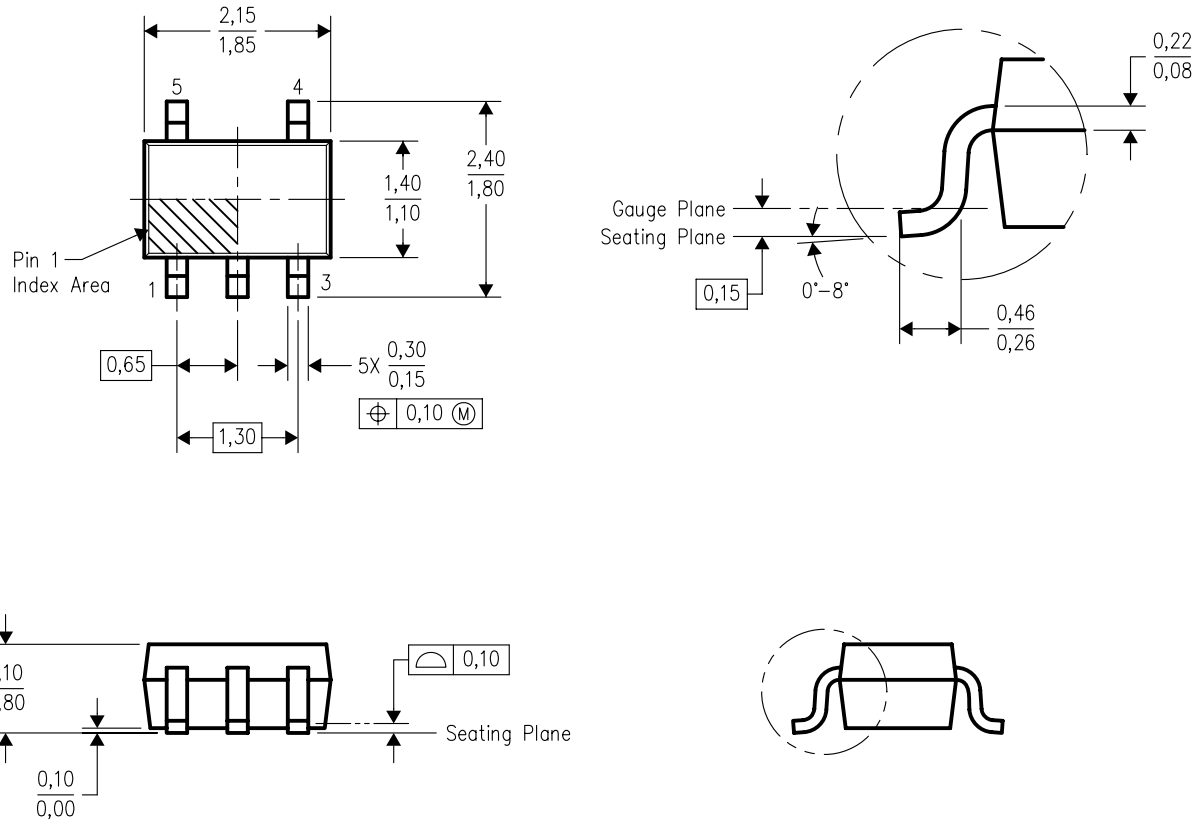
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

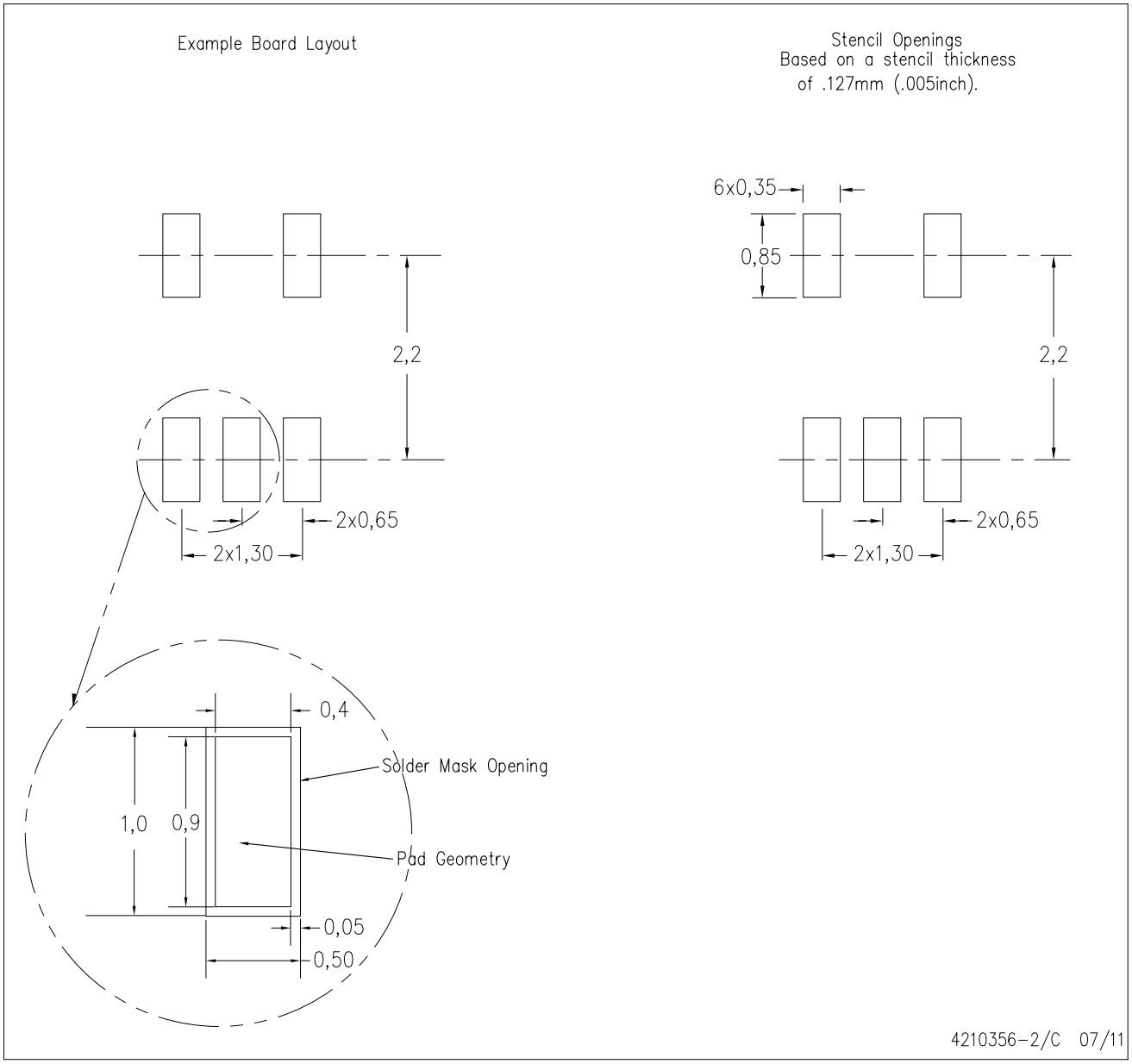
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



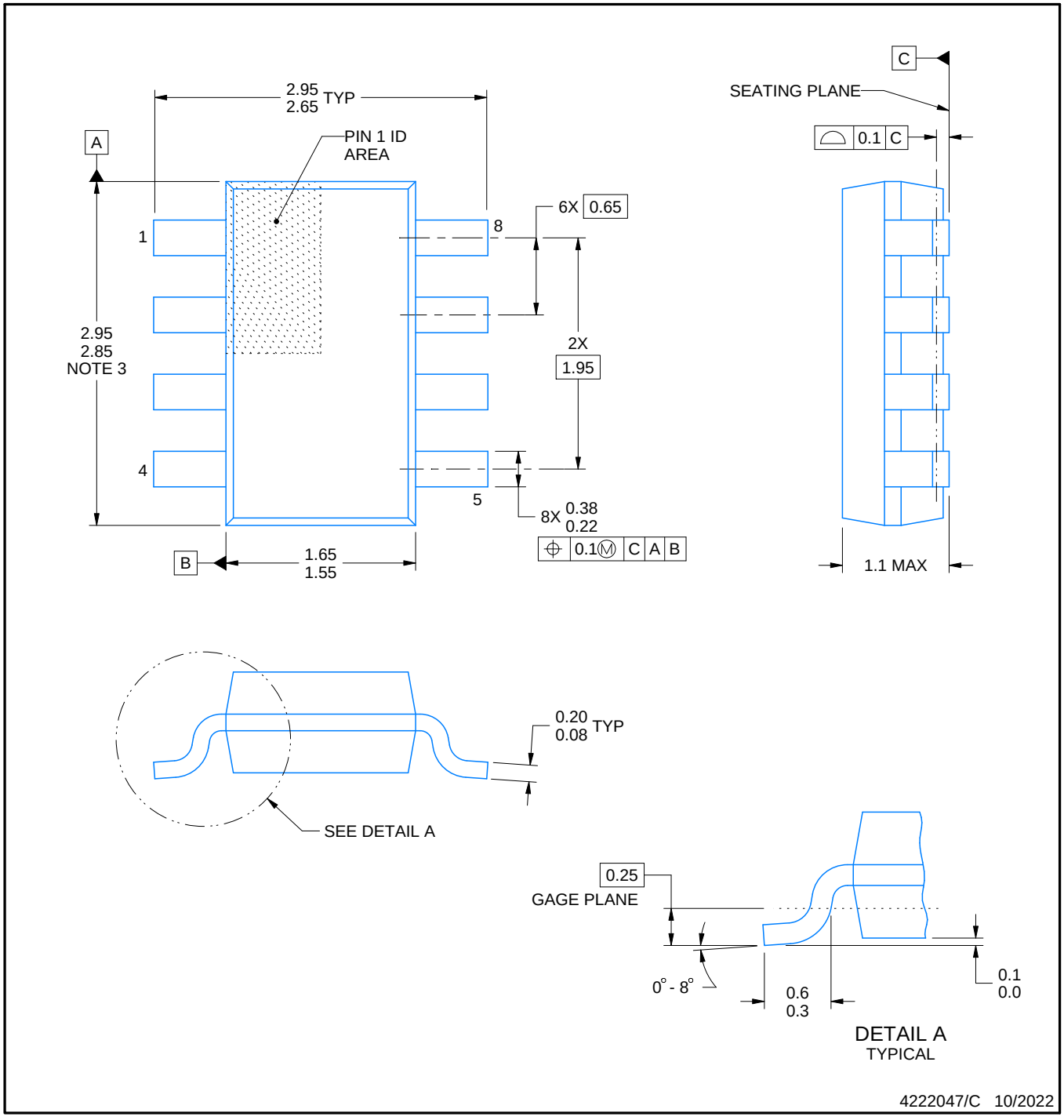
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DDF0008A

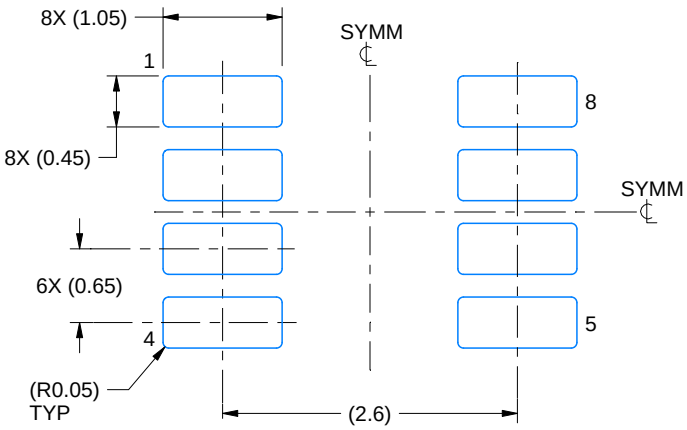
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

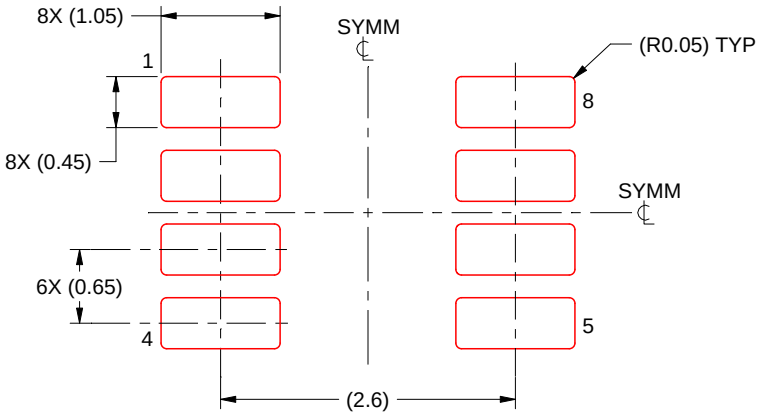
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

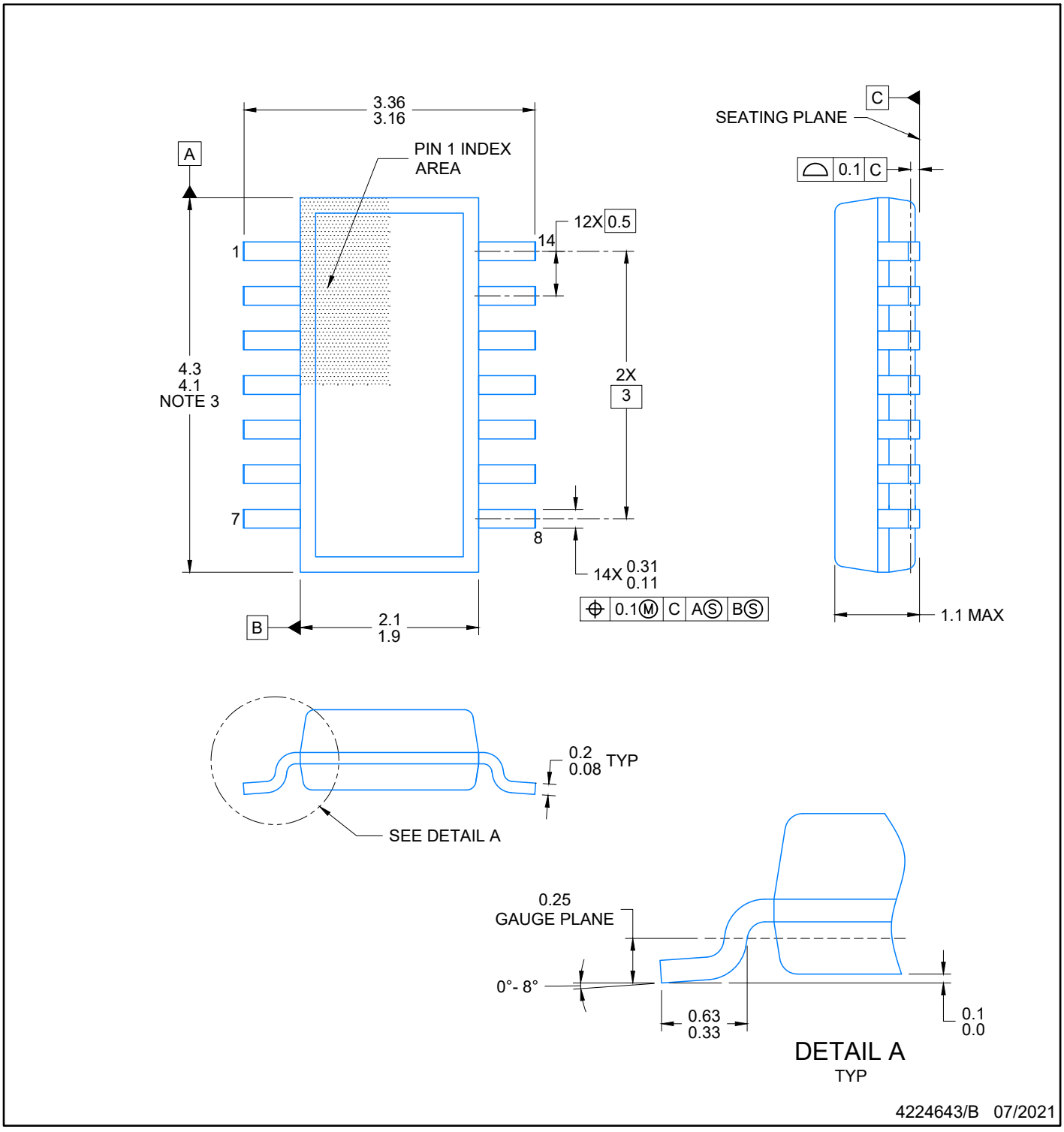
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

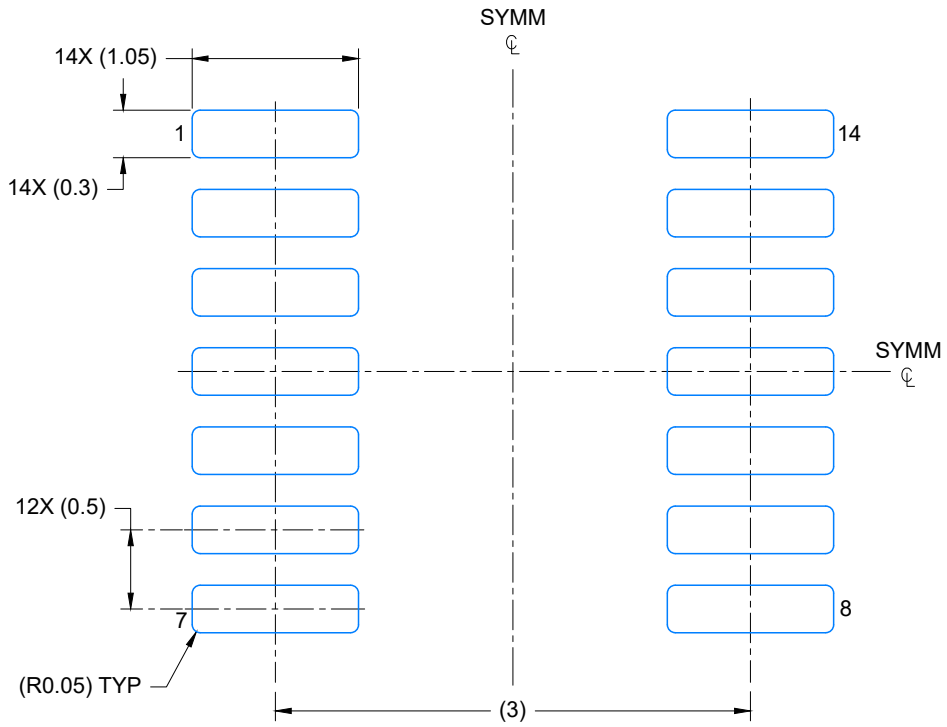
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

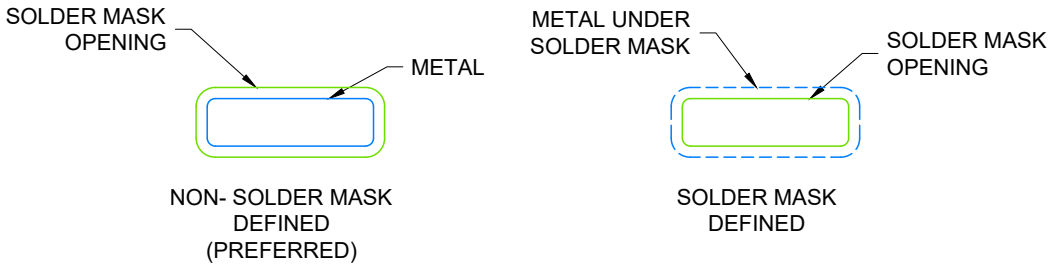


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

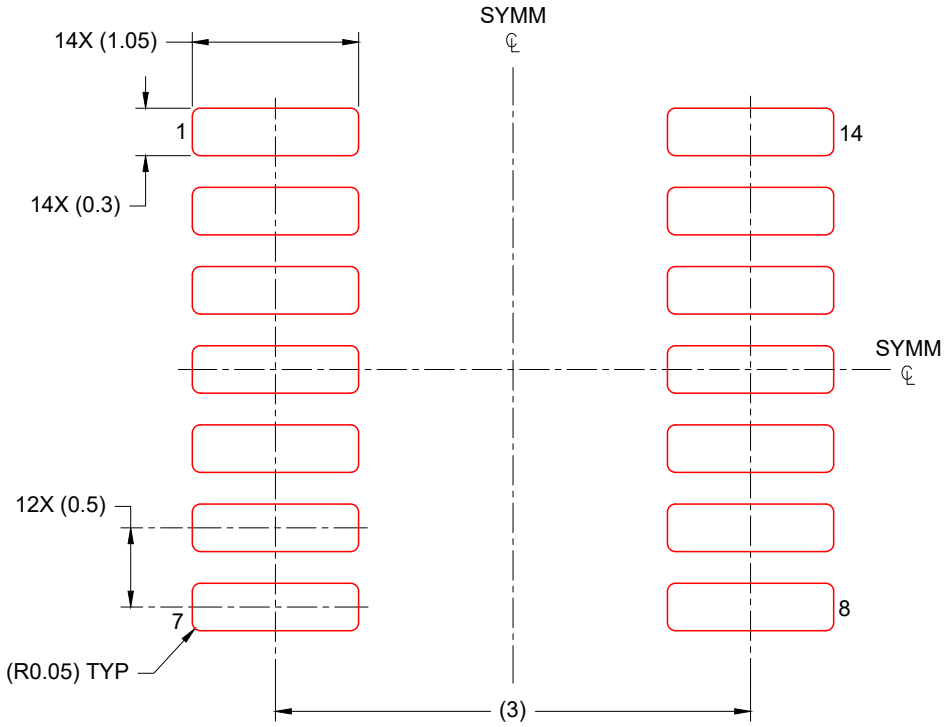


SOLDER MASK DETAILS

4224643/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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