TS04

4-Channel Self Calibration Capacitive Touch Sensor

SPECIFICATION V2.0

1 Specification

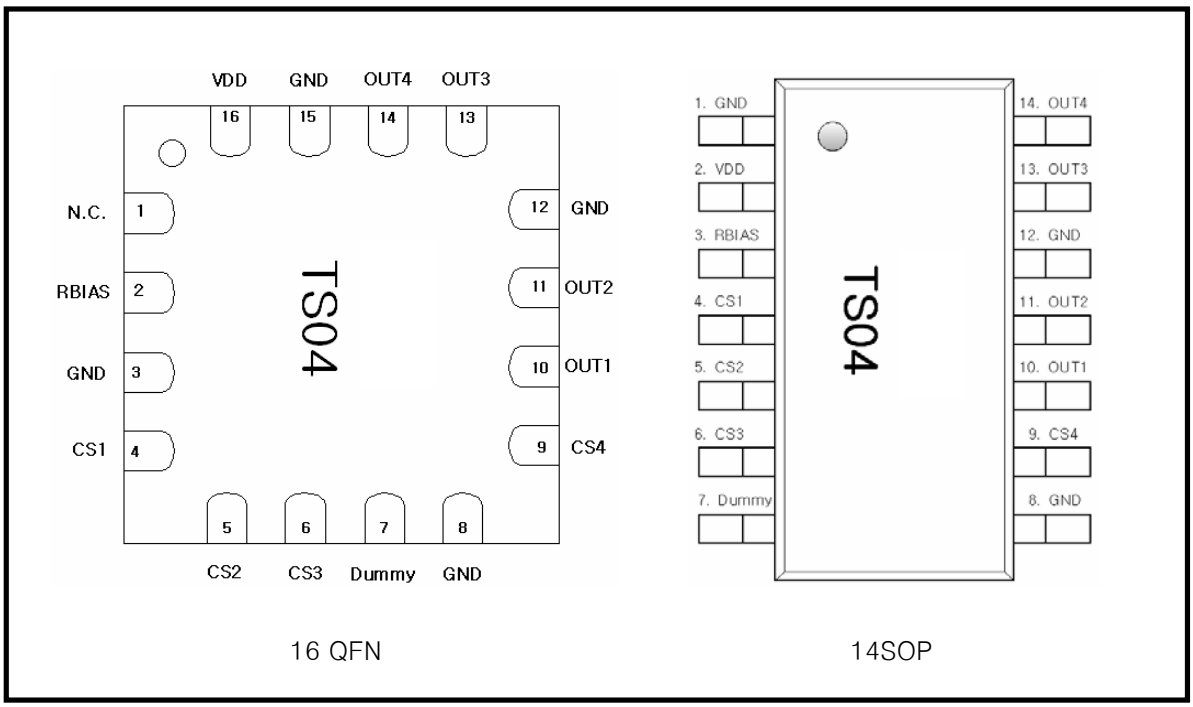
1.1 General Feature

- 4-Channel capacitive sensor with auto sensitivity calibration
- Parallel output interface
- Independently adjustable sensitivity with external capacitor
- Adjustable internal frequency with external resister
- Embedded high frequency noise elimination circuit
- Low current consumption
- RoHS compliant 16QFN, 14SOP package

1.2 Application

- Mobile application (mobile phone / PDA / PMP / MP3 etc)
- Membrane switch replacement
- Sealed control panels, keypads
- Door key-lock matrix application

1.3 Package (16 QFN / 14SOP)



Drawings not to scale

2 Pin Description

2.1 16 QFN package

PIN No.	Name	I/O	Description	Protection
1	N.C.	–	Not connect	–
2	RBIAS	Analog Input	Internal bias adjust input	VDD/GND
3	GND	–	Connect to GND	VDD/GND
4	CS1	Analog Input	CH1 capacitive sensor input	VDD/GND
5	CS2	Analog Input	CH2 capacitive sensor input	VDD/GND
6	CS3	Analog Input	CH3 capacitive sensor input	VDD/GND
7	Dummy	Analog Input	Internal noise monitoring input Do not connect to anywhere	VDD/GND
8	GND	Ground	Supply ground	VDD
9	CS4	Analog Input	CH4 capacitive sensor input	VDD/GND
10	OUT1	Digital Output	Output1 for CS1 (Open Drain structure)	VDD/GND
11	OUT2	Digital Output	Output2 for CS2 (Open Drain structure)	VDD/GND
12	GND	Ground	Supply ground	VDD
13	OUT3	Digital Output	Output3 for CS3 (Open Drain structure)	VDD/GND
14	OUT4	Digital Output	Output4 for CS4 (Open Drain structure)	VDD/GND
15	GND	–	Connect to GND	VDD/GND
16	VDD	Power	Power (2.5V~5.0V)	GND

2.2 14 SOP

PIN No.	Name	I/O	Description	Protection
1	GND	–	Connect to GND	VDD/GND
2	VDD	Power	Power (2.5V~5.0V)	GND
3	RBIAS	Analog Input	Internal bias adjust input	VDD/GND
4	CS1	Analog Input	CH1 capacitive sensor input	VDD/GND
5	CS2	Analog Input	CH2 capacitive sensor input	VDD/GND
6	CS3	Analog Input	CH3 capacitive sensor input	VDD/GND
7	Dummy	Analog Input	Internal noise monitoring input Do not connect to anywhere	VDD/GND
8	GND	Ground	Supply ground	VDD
9	CS4	Analog Input	CH4 capacitive sensor input	VDD/GND
10	OUT1	Digital Output	Output1 for CS1 (Open Drain structure)	VDD/GND
11	OUT2	Digital Output	Output2 for CS2 (Open Drain structure)	VDD/GND
12	GND	Ground	Supply ground	VDD
13	OUT3	Digital Output	Output3 for CS3 (Open Drain structure)	VDD/GND
14	OUT4	Digital Output	Output4 for CS4 (Open Drain structure)	VDD/GND

3 Absolute Maximum Rating

Battery supply voltage	5.0V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Minimum Level	Reference
H.B.M	Pos / Neg	2000V	VDD
		2000V	VSS
		2000V	P to P
M.M	Pos / Neg	200V	VDD
		200V	VSS
		200V	P to P
C.D.M	Pos / Neg	500V	DIRECT
		800V	

4.2 Latch-up Characteristics

Mode	Polarity	Minimum Level	Test Step
I Test	Positive	200mA	25mA
	Negative	−200mA	
V supply over 5.0V	Positive	8.0V	1.0V

5 Electrical Characteristics

▪ V_{DD}=3.3V, Rb=510k, Sync Mode (Rsync = 2MΩ) (Unless otherwise noted), T_A = 25℃

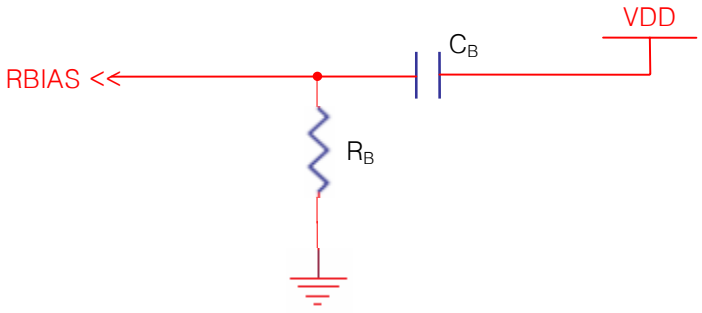
Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Operating supply voltage	V_{DD}		2.5	3.3	5.0	V
Current consumption	I_{DD}	V_{DD}= 3.3V R_B=510k R_{SB}=0	–	40	70	μA
		V_{DD}= 5.0V R_B=510k R_{SB} =0	–	80	140	
Digital output maximum sink current	I_{OUT}	T_A = 25℃ (Normal I2C Output)	–	–	4.0	mA
Internal reset criterion V_{DD} voltage	V_{DD_RST}	T_A = 25℃, R_B=510k	–	–	0.3·V_{DD}	V
Sense input capacitance range [Note1]	C_S		–	–	100	pF
Minimum detective capacitance difference	ΔC	Cs = 10pF	0.2	–	–	pF
Output impedance (open drain)	Z_O	ΔC > 0.2pF, Cs = 10pF	–	12	–	Ω
		ΔC < 0.2pF, Cs = 10pF	–	30M	–	
Self calibration time after system reset	T_{CAL}	V_{DD} = 3.3V R_B = 510k	–	100	–	ms
		V_{DD} = 5.0V R_B = 510k	–	80	–	
Sense input resistance range	R_S		–	200	1000	Ω
Recommended bias resistance range [Note2]	R_B	V_{DD} = 3.3V	200	510	820	kΩ
		V_{DD} = 5.0V	330	620	1200	
Maximum bias capacitance	C_{B_MAX}		–	820	1000	pF

Note 1 : The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern.

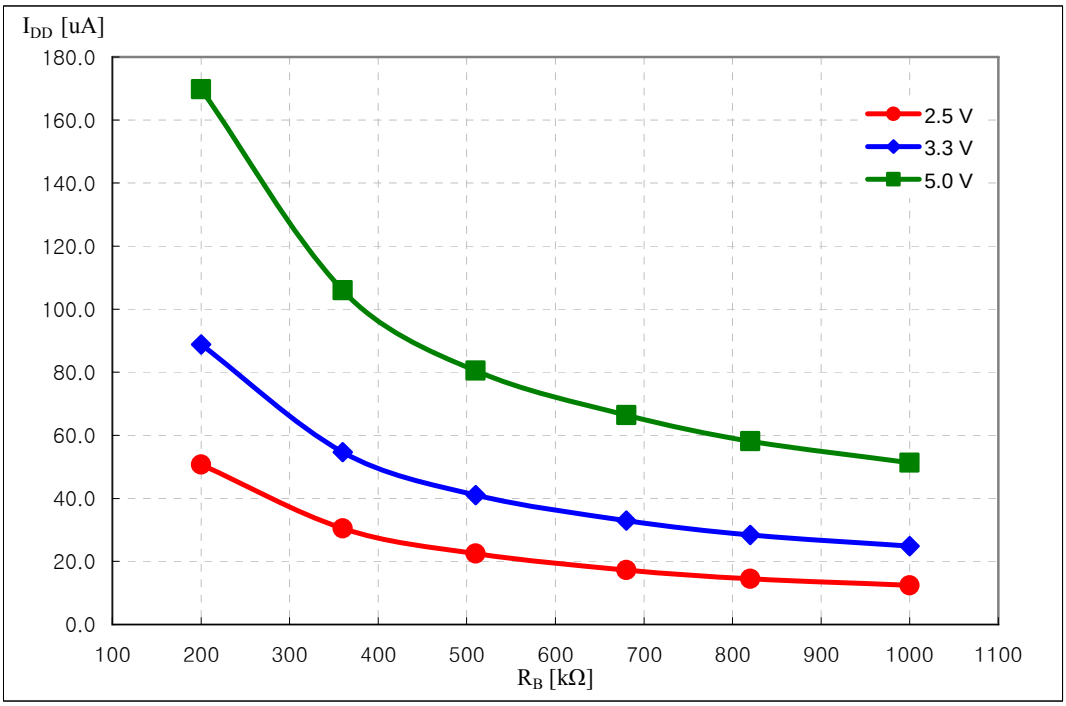
Note 2 : The lower R_B is recommended in noisy condition.

6 Implementation of TS04

6.1 RBIAS & SRBIAS implementation



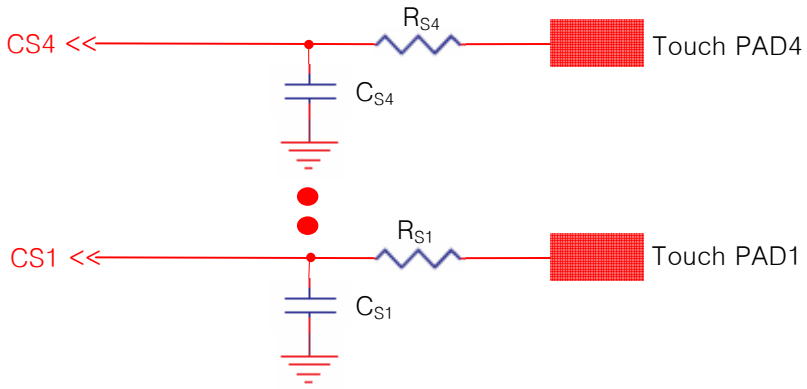
The RBIAS is connected the resistor to decide the oscillator and internal bias current. The sensing frequency, internal clock frequency and current consumption are therefore able to be adjusted with R_B. A voltage ripple on RBIAS can make critical internal error, so C_B is connected to the VDD (not GND) is recommended. (The typical value of C_B is 820pF and the maximum Value is 1nF.)



Normal operation current consumption curve

The current consumption curve of TS04 is represented in accordance with R_B value as above. The lower R_B requires more current consumption but it is recommended in noisy application. For example, refrigerator, air conditioner and so on.

6.2 CS implementation



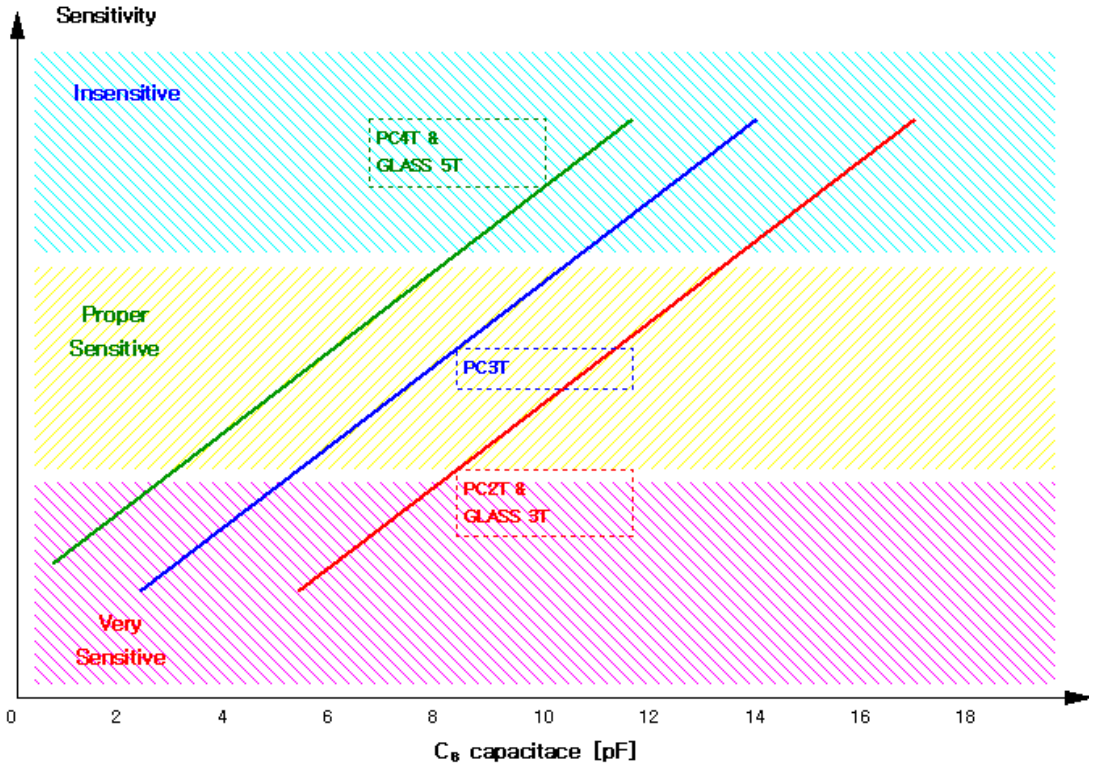
The TS04 has available sensing channel up to 4. The parallel capacitor C_{S1} is added to CS1 and C_{S4} to CS4 to adjust fine sensitivity. The sensitivity would increase when a smaller value of C_S is used. (Refer to the below Sensitivity Example Figure) It could be useful in case detail sensitivity mediation is required. The internal touch decision process of each channel is separated from each other. The four channel touch key board application can therefore be designed by using only one TS04 without coupling problem. The R_S is serial connection resistor to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS1 ~ CS4 to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line.

There are some sensitivity difference among CS1, CS2 and CS3, and CS4 caused by internal parasitic capacitance. That sensitivity difference could be compensated by using different C_S capacitor or sensitivity setting with internal register. To use different touch pattern area could be used for sensitivity compensation but not recommended. The sensitivity of each channel can be represented as below.

Sensitivity of CS1 ≥ Sensitivity of CS2, CS3 > Sensitivity of CS4
(In case of the external parasitic capacitance value is same on each channel.)

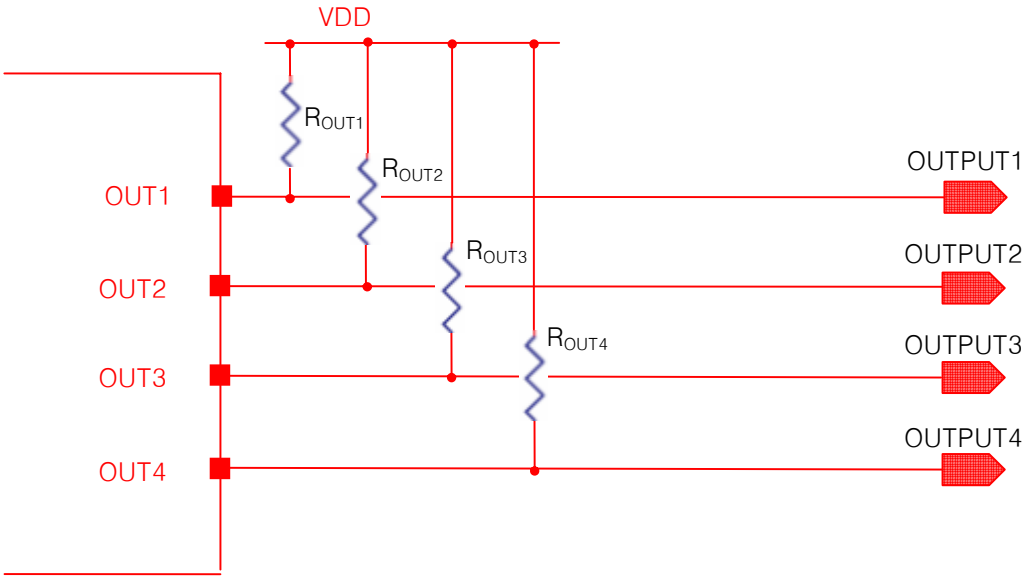
C_{CS1_PARA} + about 3.5pF = $C_{CS2,3_PARA}$ + about 3pF = C_{CS4_PARA}

* C_{CS1_PARA} : Parasitic capacitance of CS1
* $C_{CS2,3_PARA}$: Parasitic capacitance of CS2 and CS3
* C_{CS4_PARA} : Parasitic capacitance of CS4



Sensitivity example figure with default sensitivity selection

6.3 Output Circuit Implementation



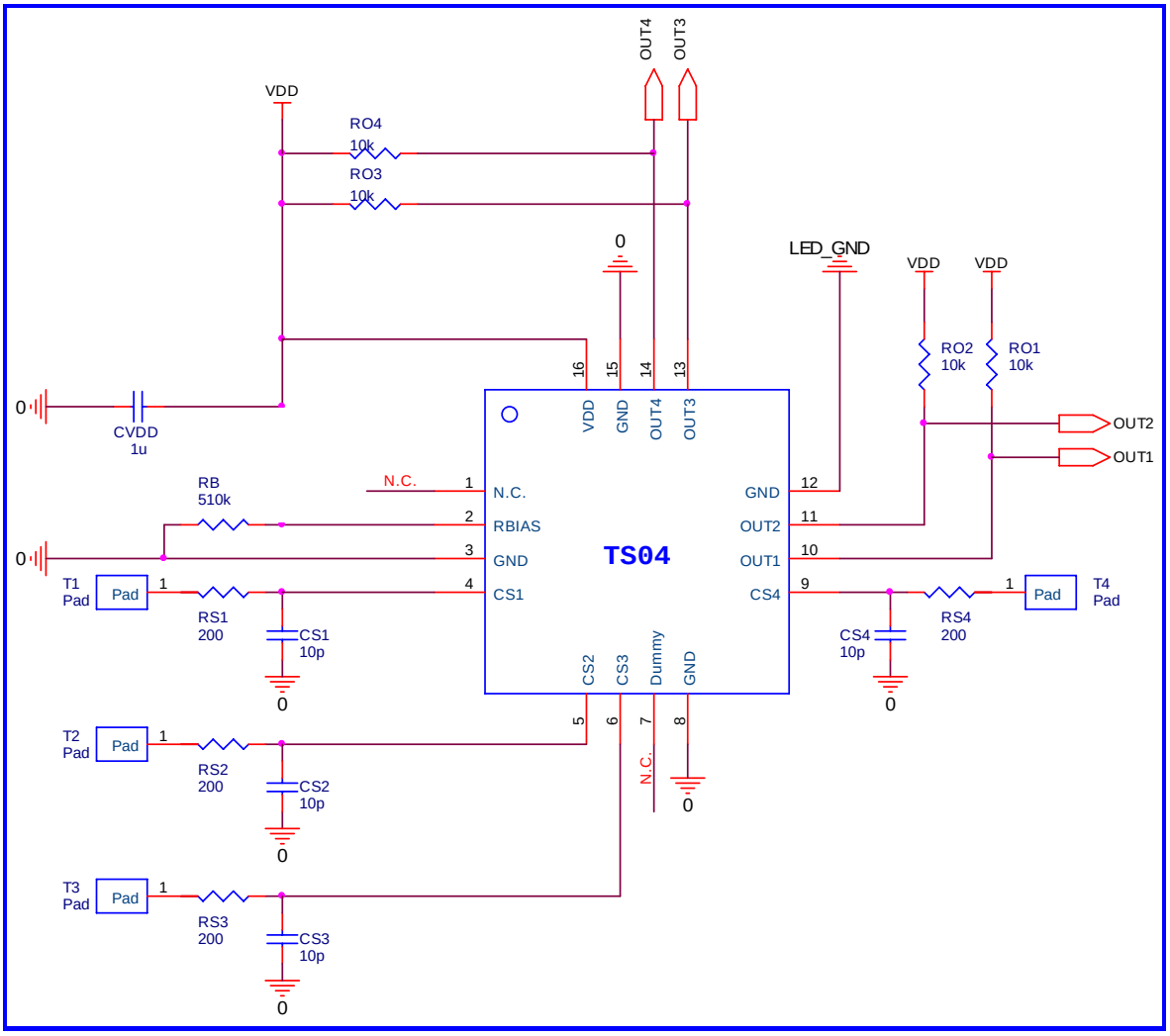
The OUTPUT pins have an open drain structure. For this reason, the connection of pull-up resistor R_{OUT} is required between OUTPUT and VDD. The maximum output sink current is 4mA, so over a few kΩ must be used as R_{OUT}. Normally 10kΩ is used as R_{OUT}.
The OUTPUT is high in normal situation, and the value is low when a touch is detected on the corresponding CS.

6.4 Internal reset operation

The TS04 has stable internal reset circuit to offer reset pulse to digital block. The supply voltage for a system start or restart should be under $0.3 \cdot V_{DD}$ of normal operation V_{DD}. No external components required for TS04 power reset, that helps simple circuit design and to realize the low cost application.

7 Recommended Circuit Diagram

7.1 Application Example (16QFN)

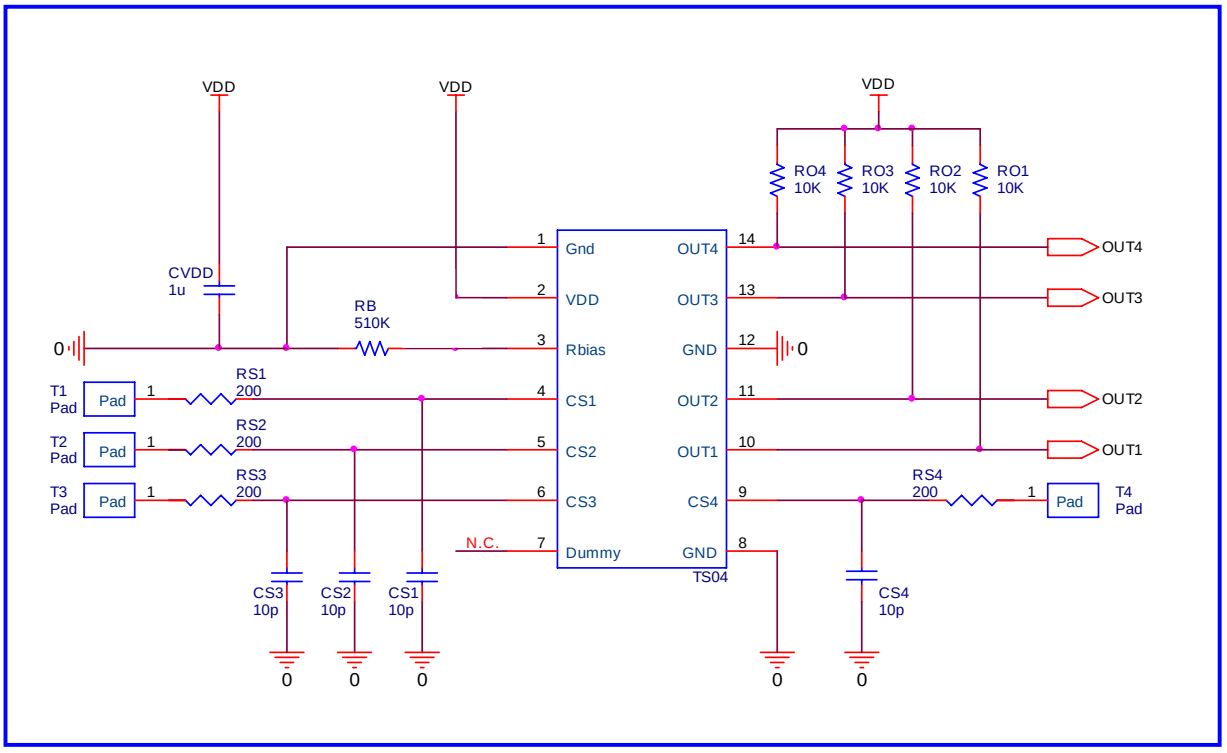


TS04(16QFN) Application Example Circuit

- In PCB layout, RB should not be placed on touch pattern. If not, CB has to be connected. The RB pattern should be routed as short as possible.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm (or narrower line).
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS04.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The TS04 is reset when power rise from 0V to proper VDD

- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The smaller R_B is recommended in noisy environments.
- About 200Ω Resistor (RS1~RS4) and parallel capacitor (CS1~CS4) is might be inserted to improve external noise immunity.
- Parallel capacitor value effects on touch sensitivity.
- The LED_GND and GND should be short in the system and the lines are recommended to be split from the most low impedance ground point to avoid ground bouncing problems.

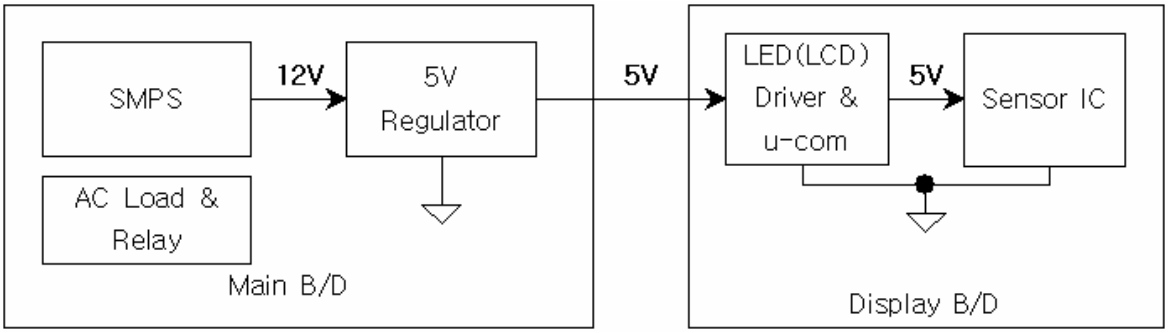
7.2 Application Example (14 SOP)



TS04(14 SOP) Application Example Circuit

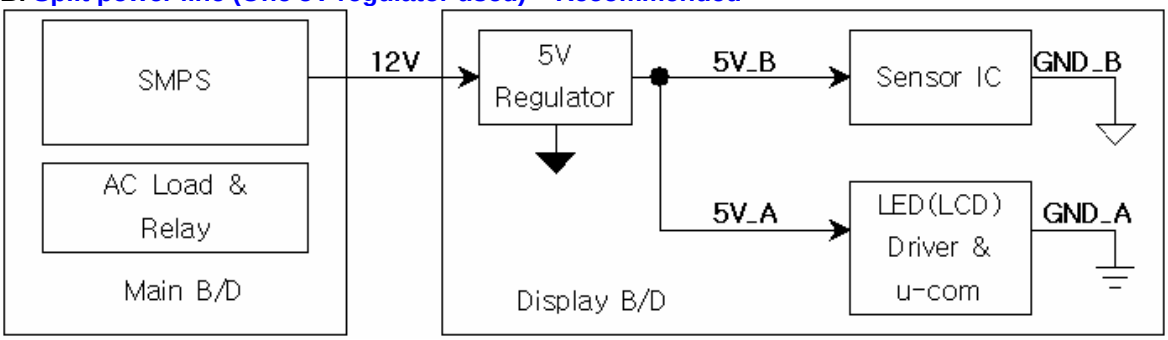
7.3 Example – Power Line Split Strategy PCB Layout

A. Not split power line (Bad power line design)

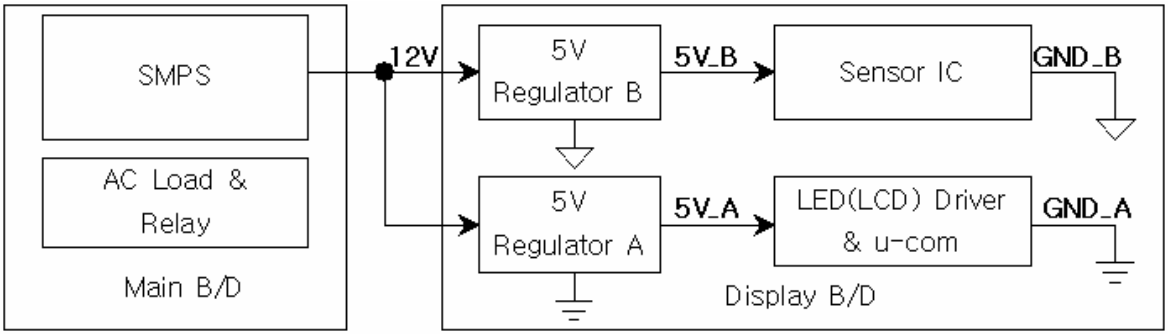


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power line (One 5V regulator used) – Recommended

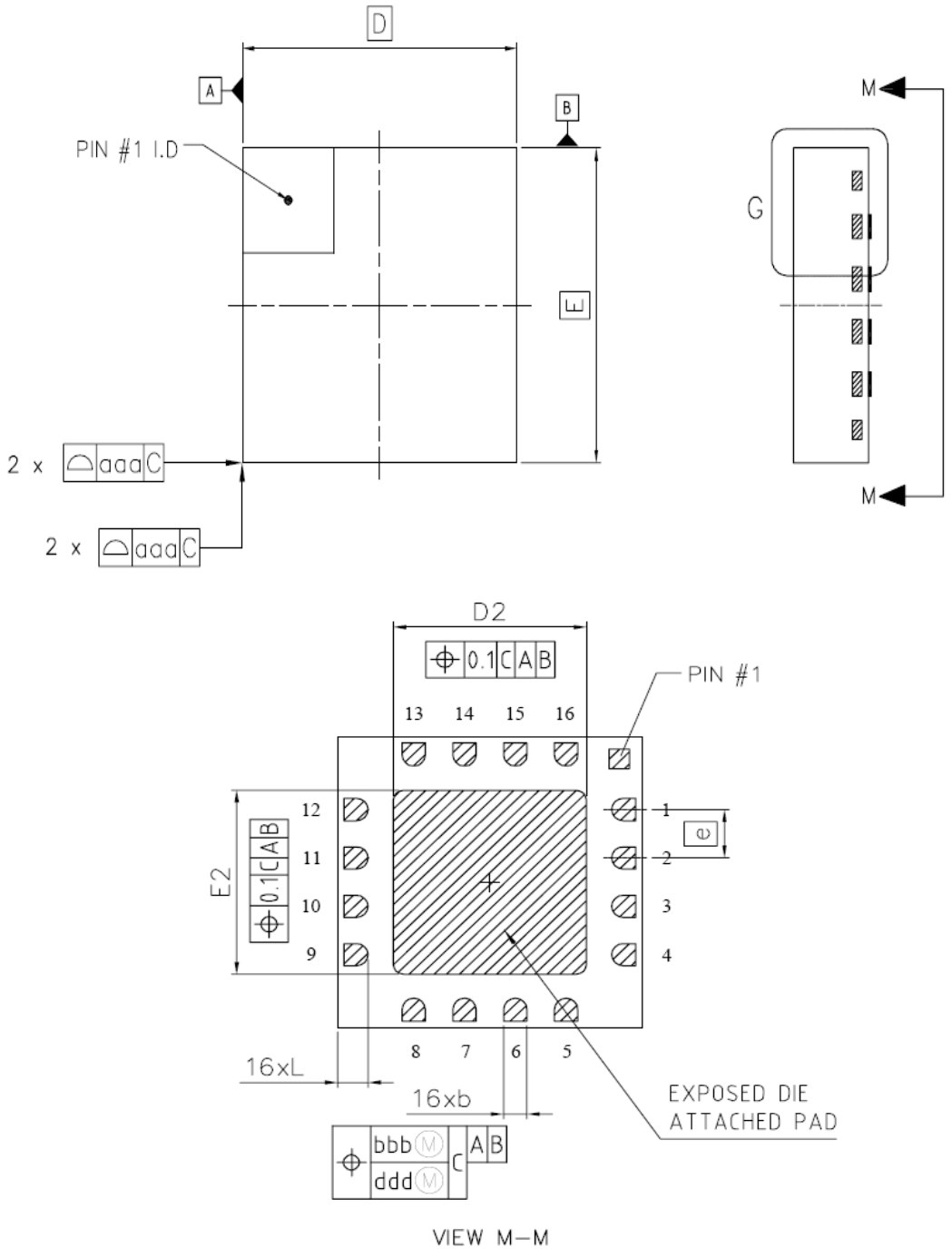


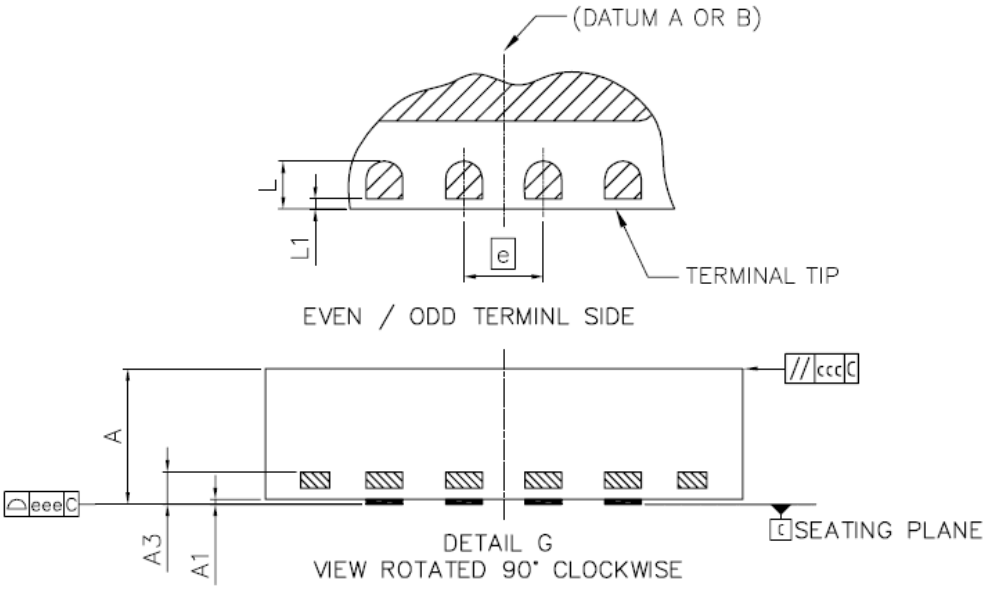
C. Split power line (Separated 5V regulator used) – Strongly recommended



8 MECHANICAL DRAWING

8.1 Mechanical drawing (16 QFN)





DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.18	0.23	0.28
D		3.00 BSC	
E		3.00 BSC	
D2	1.80	1.90	2.00
E2	1.80	1.90	2.00
e		0.50 BSC	
L	0.25	0.30	0.35
L1	0.00		0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

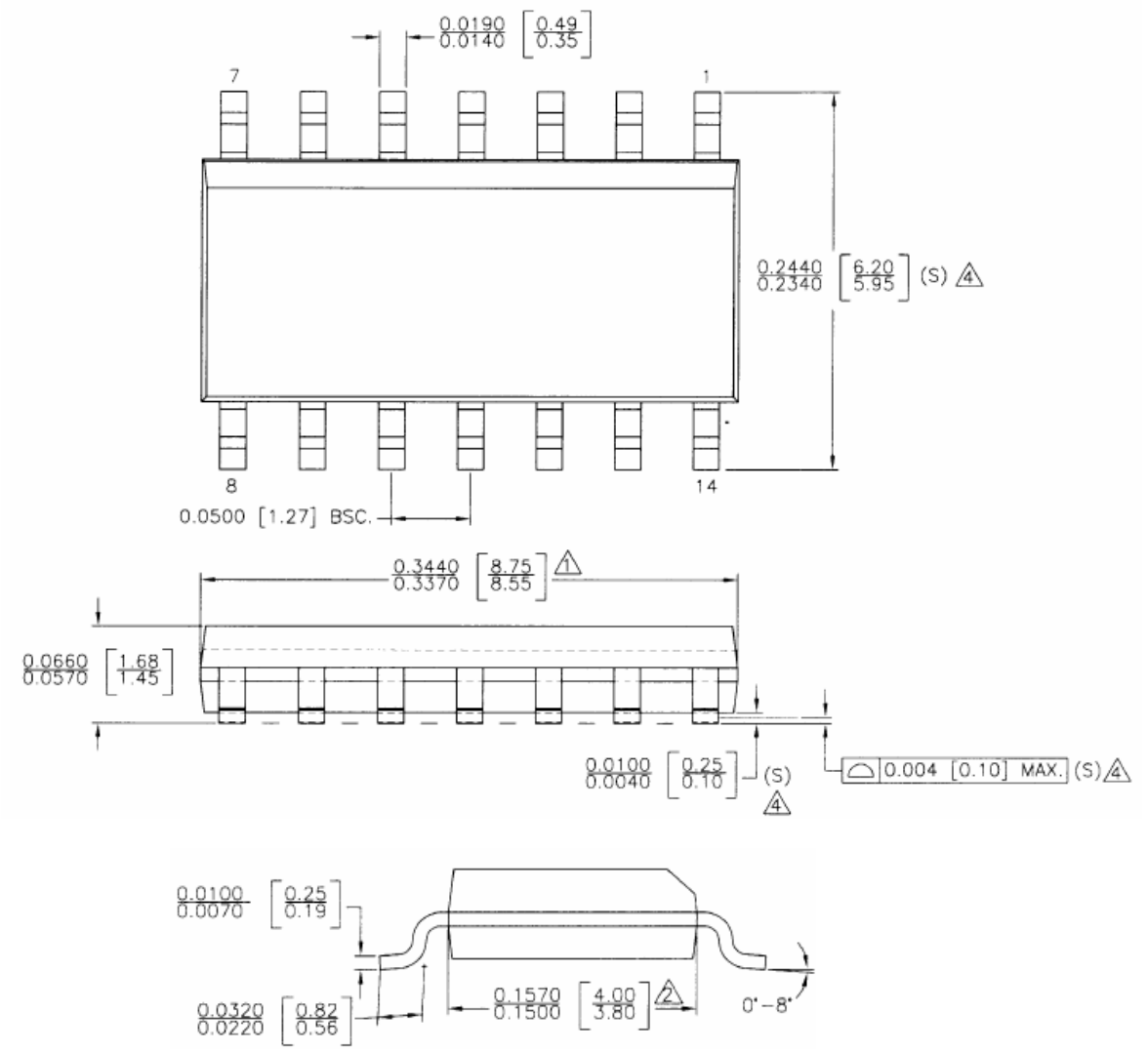
2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

8.2 Mechanical Drawing (14 SOP)

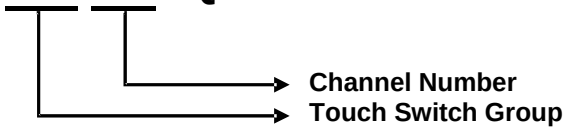


NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 INCH PER SIDE.
2. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS-012 AB.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. CONTROL DIMENSIONS IN INECHES.[mm]

9 MARKING DESCRIPTION

Device Code : **T S 0 4** **QFN or SOP**



Weekly Code : **YY WW**



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