HEF4017B

5-stage Johnson decade counter

Rev. 04 — 9 December 2008 Product data sheet

1. General description

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (Q0 to Q9), an active LOW carry output from the most significant flip-flop ($\overline{Q}$5-9), active HIGH and active LOW clock inputs (CP0, $\overline{CP}$1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP0 while $\overline{CP}$1 is LOW or a HIGH-to-LOW transition at $\overline{CP}$1 while CP0 is HIGH (see Table 3).

When cascading counters, the $\overline{Q}$5-9 output, which is LOW while the counter is in states 5, 6, 7, 8, and 9, can be used to drive the CP0 input of the next counter. A HIGH on MR resets the counter to zero (Q0 = $\overline{Q}$5-9 = HIGH; Q1 to Q9 = LOW) independent of the clock inputs (CP0, $\overline{CP}$1).

Automatic counter code correction is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

Schmitt trigger action makes the clock inputs highly tolerant of slower rise and fall times.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input. It is also suitable for use over both the industrial (−40 °C to +85 °C) and automotive (−40 °C to +125 °C) temperature ranges.

2. Features

- Automatic counter correction
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the automotive temperature range −40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Applications

- Industrial and automotive

NXP founded by Philips

4. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +125 °C

Type number	Package		
	Name	Description	Version
HEF4017BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF4017BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

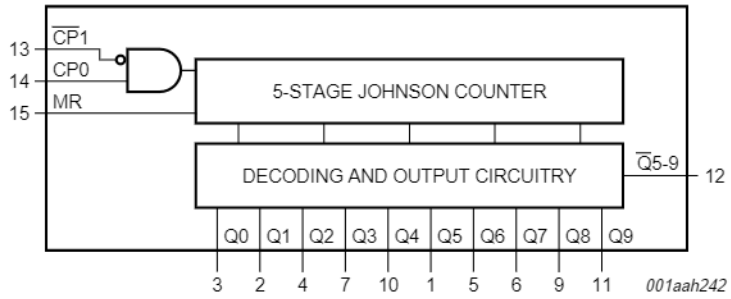


Fig 1. Functional diagram

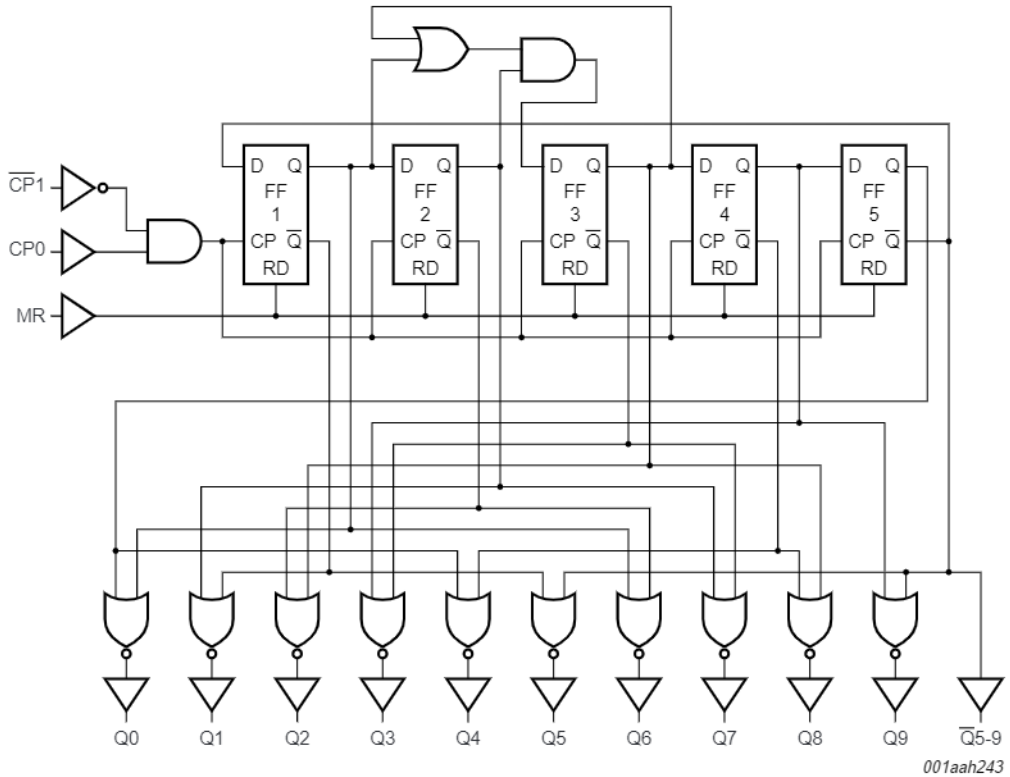


Fig 2. Logic diagram

© NXP B.V. 2008. All rights reserved.

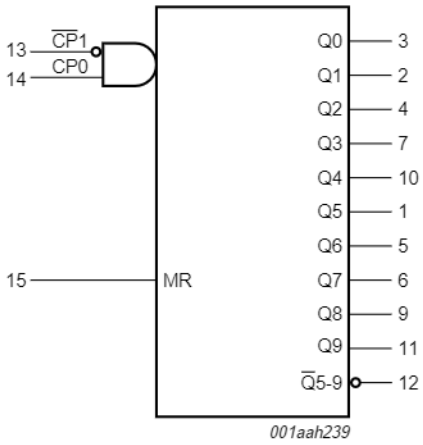


Fig 3. Logic symbol

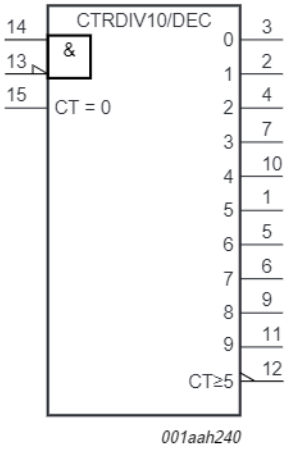


Fig 4. IEE logic symbol

6. Pinning information

6.1 Pinning

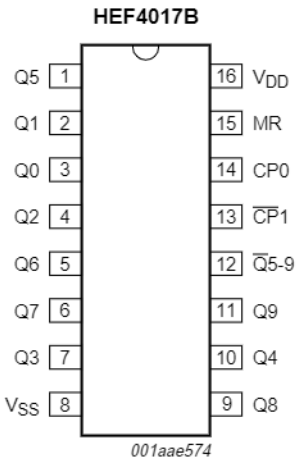


Fig 5. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0 to Q9	3, 2, 4, 7, 10, 1, 5, 6, 9, 11	decoded output
V_{SS}	8	ground supply voltage
$\overline{Q}5\text{-}9$	12	carry output (active LOW)
$\overline{CP}1$	13	clock input (HIGH-to-LOW edge-triggered)

© NXP B.V. 2008. All rights reserved.

Table 2. Pin description *...continued*

Symbol	Pin	Description
CP0	14	clock input (LOW-to-HIGH edge-triggered)
MR	15	master reset input
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table [1]

MR	CP0	$\overline{CP}$1	Operation
H	X	X	Q0 = $\overline{Q}$5-9 = H; Q1 to Q9 = L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = positive-going transition; ↓ = negative-going transition.

© NXP B.V. 2008. All rights reserved.

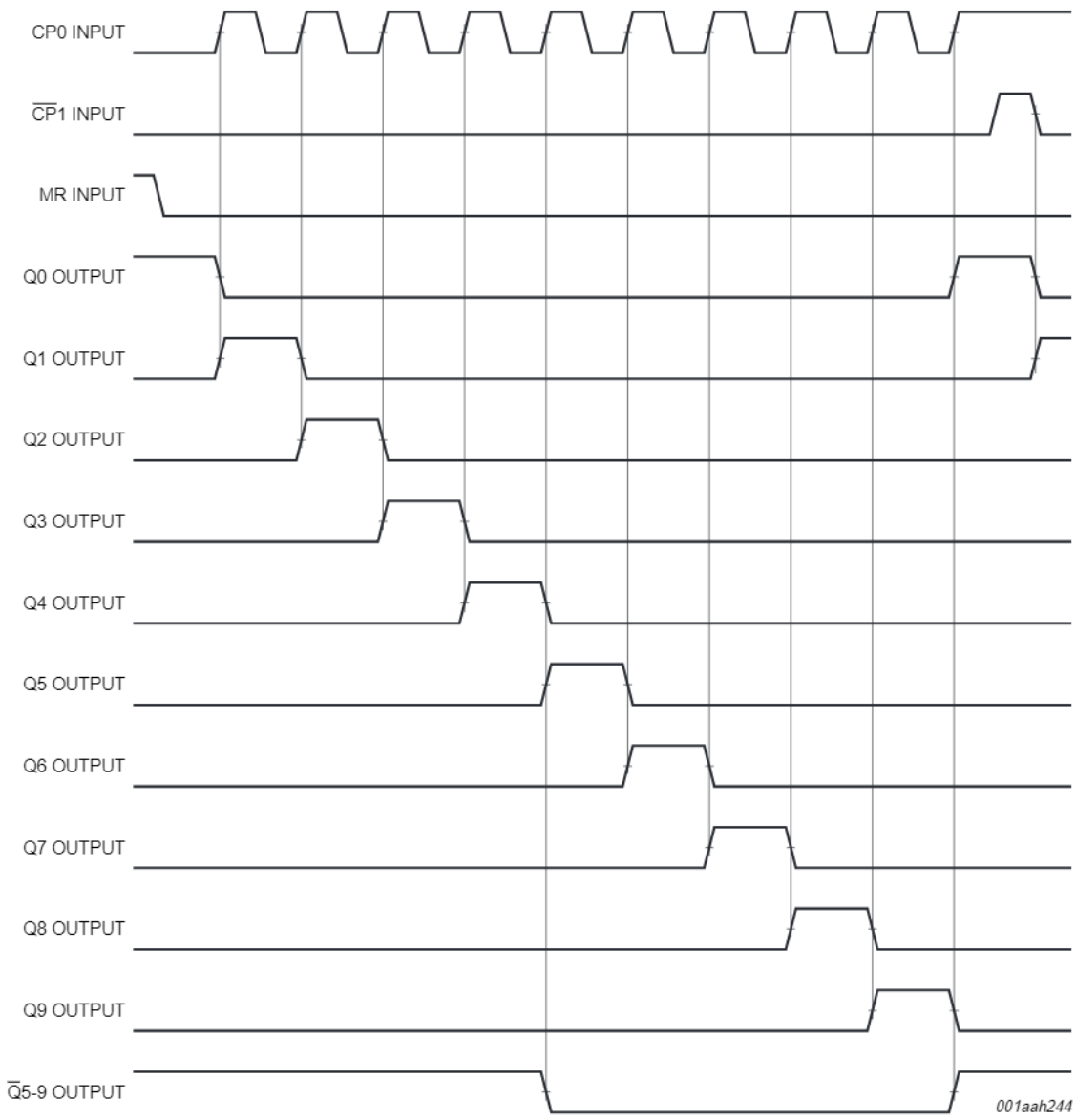


Fig 6. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+18	V
I_{IK}	input clamping current	$V_I < 0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
V_I	input voltage		−0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < 0.5$ V or $V_O > V_{DD} + 0.5$ V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA

© NXP B.V. 2008. All rights reserved.

Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+125	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	ns/V
		V_{DD} = 10 V	-	-	0.5	ns/V
		V_{DD} = 15 V	-	-	0.08	ns/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		T_{amb} = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 ∝A	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 ∝A	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 ∝A; V_I = V_{SS} or V_{DD}	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 ∝A; V_I = V_{SS} or V_{DD}	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V

© NXP B.V. 2008. All rights reserved.

Table 6. Static characteristics *...continued*

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		T_{amb} = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	−1.7	-	−1.4	-	−1.1	-	−1.1	-	mA
		V_O = 4.6 V	5 V	−0.64	-	−0.5	-	−0.36	-	−0.36	-	mA
		V_O = 9.5 V	10 V	−1.6	-	−1.3	-	−0.9	-	−0.9	-	mA
		V_O = 13.5 V	15 V	−4.2	-	−3.4	-	−2.4	-	−2.4	-	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.2	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	∝A
I_{DD}	supply current	I_O = 0 A; V_I = V_{SS} or V_{DD}	5 V	-	5	-	5	-	150	-	150	∝A
			10 V	-	10	-	10	-	300	-	300	∝A
			15 V	-	20	-	20	-	600	-	600	∝A
C_I	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C; V_{SS} = 0 V; for test circuit see Figure 10

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP0, $\overline{CP1}$ → Q0 to Q9; see Figure 7	5 V	113 ns + (0.55 ns/pF) C_L	-	140	280	ns
			10 V	44 ns + (0.23 ns/pF) C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns
		CP0, $\overline{CP1}$ → $\overline{Q}$5-9; see Figure 7	5 V	118 ns + (0.55 ns/pF) C_L	-	145	290	ns
			10 V	44 ns + (0.23 ns/pF) C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns
		MR → Q1 to Q9; see Figure 8	5 V	88 ns + (0.55 ns/pF) C_L	-	115	230	ns
			10 V	39 ns + (0.23 ns/pF) C_L	-	50	100	ns
			15 V	27 ns + (0.16 ns/pF) C_L	-	35	70	ns

© NXP B.V. 2008. All rights reserved.

Table 7. Dynamic characteristics *...continued*

T_{amb} = 25 °C; V_{SS} = 0 V; for test circuit see Figure 10

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	CP0, $\overline{CP}1 \rightarrow$ Q0 to Q9; see Figure 7	5 V	98 ns + (0.55 ns/pF) C_L	-	125	250	ns
			10 V	39 ns + (0.23 ns/pF) C_L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns
		CP0, $\overline{CP}1 \rightarrow \overline{Q}5$-9; see Figure 7	5 V	98 ns + (0.55 ns/pF) C_L	-	125	250	ns
			10 V	39 ns + (0.23 ns/pF) C_L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns
		MR $\rightarrow \overline{Q}5$-9; see Figure 8	5 V	83 ns + (0.55 ns/pF) C_L	-	110	220	ns
			10 V	34 ns + (0.23 ns/pF) C_L	-	45	90	ns
			15 V	27 ns + (0.16 ns/pF) C_L	-	35	70	ns
		MR $\rightarrow$ Q0; see Figure 8	5 V	103 ns + (0.55 ns/pF) C_L	-	130	260	ns
			10 V	44 ns + (0.23 ns/pF) C_L	-	55	105	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	75	ns
t_t	transition time	see Figure 7	5 V	[2] 10 ns + (1.00 ns/pF) C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF) C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF) C_L	-	20	40	ns
t_h	hold time	CP0 $\rightarrow \overline{CP}1$; see Figure 9	5 V		90	45	-	ns
			10 V		40	20	-	ns
			15 V		20	10	-	ns
		$\overline{CP}1 \rightarrow$ CP0; see Figure 9	5 V		80	40	-	ns
			10 V		40	20	-	ns
			15 V		30	10	-	ns
t_W	pulse width	CP0 input LOW; minimum width; see Figure 8	5 V		80	40	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
		$\overline{CP}1$ input HIGH; minimum width; see Figure 8	5 V		80	40	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
		MR input HIGH; minimum width; see Figure 8	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t_{rec}	recovery time	MR input; see Figure 8	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
f_{max}	maximum frequency	see Figure 8	5 V		6	12	-	MHz
			10 V		12	30	-	MHz
			15 V		15	30	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2] t_t is the same as t_{THL} and t_{TLH}.

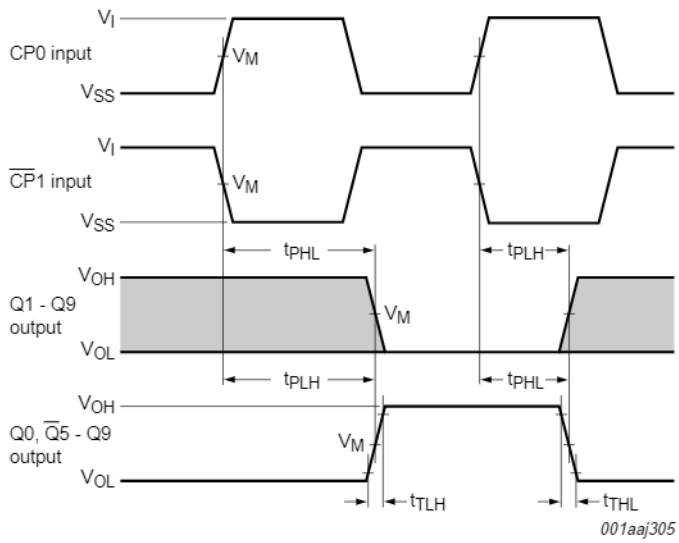
© NXP B.V. 2008. All rights reserved.

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (∝W)	where:
P_D	dynamic power dissipation	5 V	$P_D = 500 \cdot f_i + \Sigma(f_o \cdot C_L) \cdot V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 2200 \cdot f_i + \Sigma(f_o \cdot C_L) \cdot V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 6000 \cdot f_i + \Sigma(f_o \cdot C_L) \cdot V_{DD}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(C_L \cdot f_o)$ = sum of the outputs.

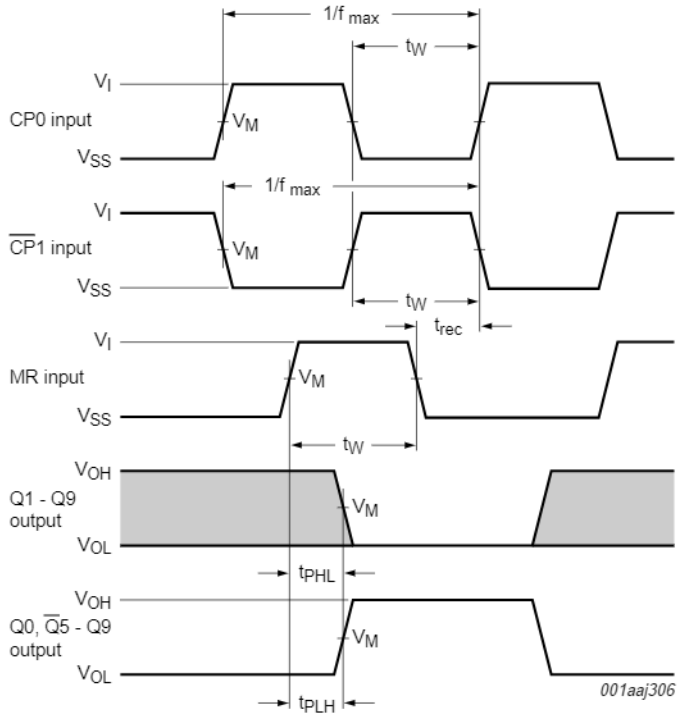
12. Waveforms



Conditions: $\overline{CP}1$ = LOW, while CP0 triggers on a LOW-to-HIGH transition. $\overline{CP}1$ triggers on a HIGH-to-LOW transition;
The shaded areas indicate where the output state is set by the input count.
Measurement points given in Table 9.

Fig 7. Waveforms showing the propagation delays for CP0, $\overline{CP}1$ to Qn, $\overline{Q}5$-9 outputs and the output transition times

© NXP B.V. 2008. All rights reserved.

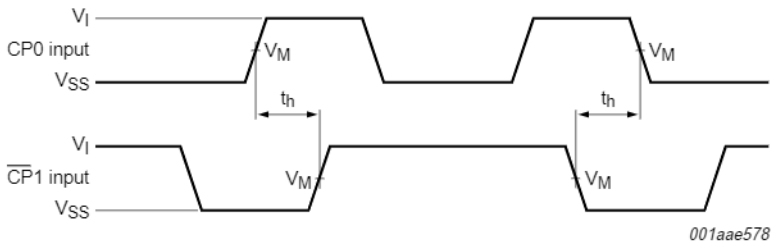


Conditions: $\overline{CP1}$ = LOW, while CP0 triggers on a LOW-to-HIGH transition. t_W and t_{rec} are measured when CP0 = HIGH and $\overline{CP1}$ triggers on a HIGH-to-LOW transition;

The shaded areas indicate where the output state is set by the input count.

Measurement points given in Table 9.

Fig 8. Waveforms showing the minimum pulse width for CP0, $\overline{CP1}$ and MR input; the maximum frequency for CP0 and $\overline{CP1}$ input; the recovery time for MR and the MR input to Qn and $\overline{Q}$5-9 output propagation delays



Hold times are shown as positive values, but may be specified as negative values;

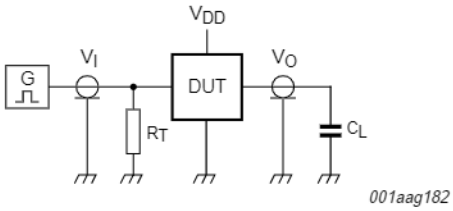
Measurement points given in Table 9.

Fig 9. Waveforms showing hold times for CP0 to $\overline{CP1}$ and $\overline{CP1}$ to CP0

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$

© NXP B.V. 2008. All rights reserved.



Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test;

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 10. Test circuit

Table 10. Test data

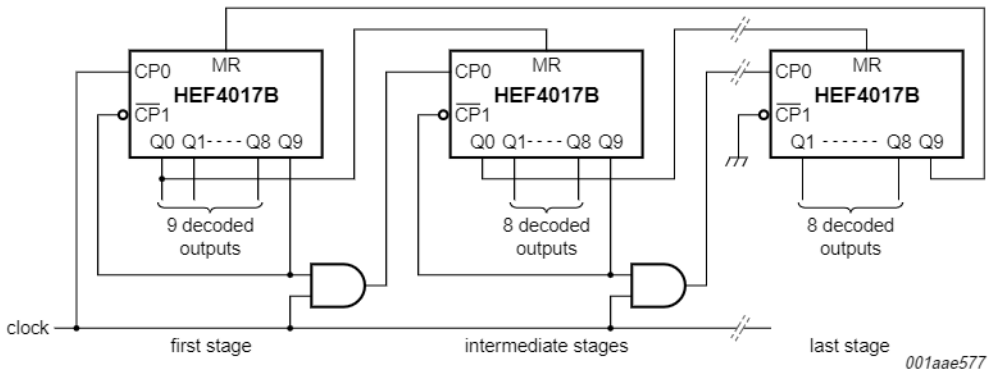
Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

13. Application information

Some examples of applications for the HEF4017B are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 11 shows a technique for extending the number of decoded output states for the HEF4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



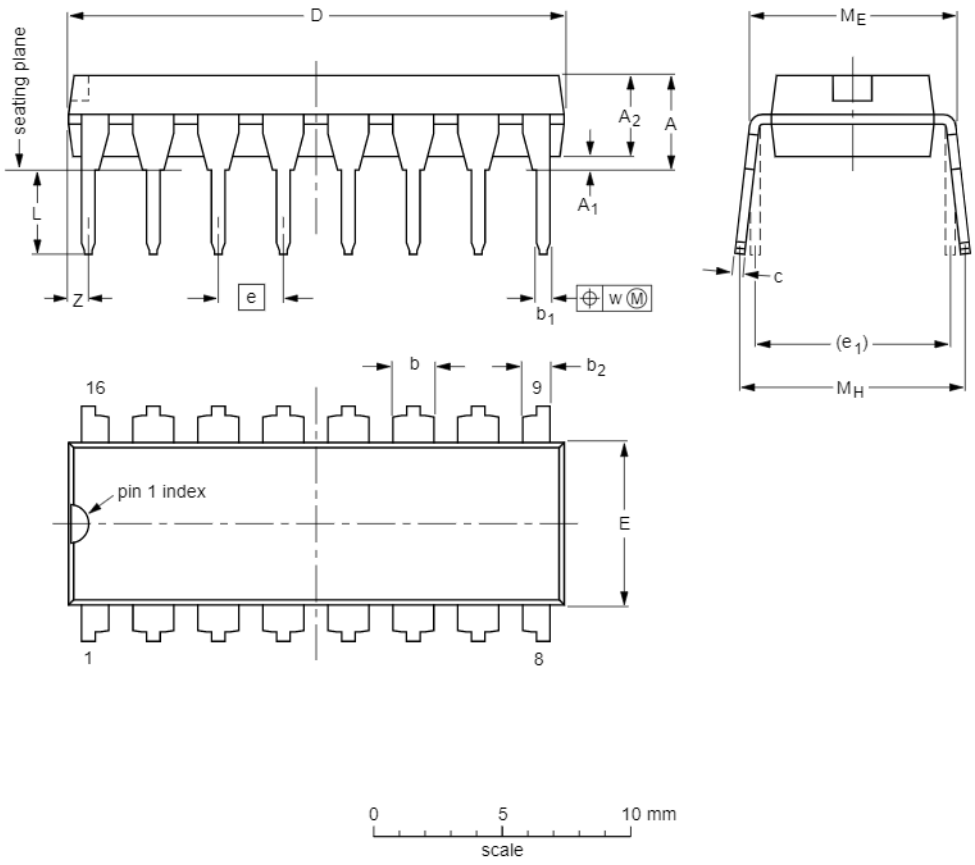
Enabling the counter on $\overline{CP1}$ when CP0 is HIGH, or on CP0 when $\overline{CP1}$ is LOW, causes an extra count.

Fig 11. Counter expansion

© NXP B.V. 2008. All rights reserved.

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

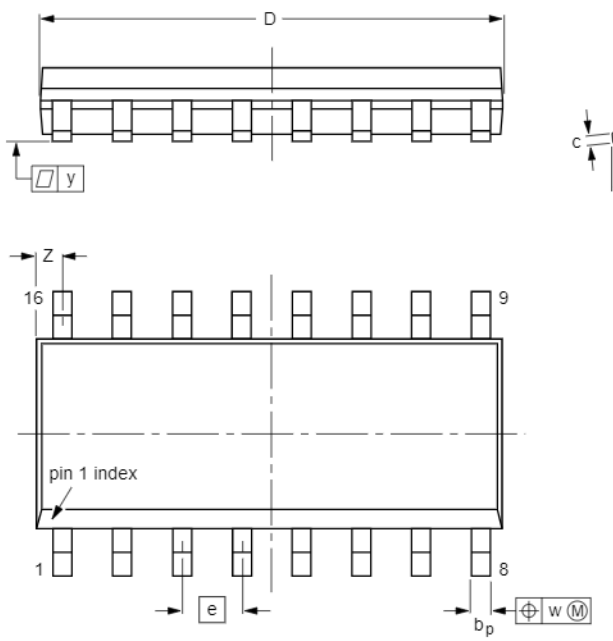
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 12. Package outline SOT38-4 (DIP16)

© NXP B.V. 2008. All rights reserved.

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

© NXP B.V. 2008. All rights reserved.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4017B_4	20081209	Product data sheet	-	HEF4017B_CNV_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Rename the pins throughout to be consistent with rest of HEF family. • Increased the maximum ambient temperature to 125 °C throughout. • Section 2 “Features” added. • Package version SOT38-1 changed to SOT38-4 in Section 4, and Figure 12. Package SOT74 removed from Section 4. • Table 1 “Ordering information” and Table 2 “Pin description” restructured. • Figure 3 “Logic symbol” and Figure 4 “IEE logic symbol” added. • Section 8 “Limiting values” and Section 10 “Static characteristics” added, taken from the HE4000B Family Specifications data sheet. • Section 9 “Recommended operating conditions” added. • Table 6 “Static characteristics” restructured. • Values for I_{DD}, I_{OL} and I_{OH} updated in Table 6 “Static characteristics”. • t_{hold} and t_{RMR} renamed to t_h hold time and t_{rec} recovery time in Table 7 “Dynamic characteristics”. and Section 12 “Waveforms”. • t_{WCPL}, t_{WCPH} and t_{WMRH} renamed to t_W minimum pulse width in Table 7 “Dynamic characteristics”. and Section 12 “Waveforms”. • Figure 7 “Waveforms showing the propagation delays for CP0, CP1 to Qn, Q5-9 outputs and the output transition times” and Figure 10 “Test circuit” added. • Maximum frequency and propagation added to Figure 8 “Waveforms showing the minimum pulse width for CP0, CP1 and MR input; the maximum frequency for CP0 and CP1 input; the recovery time for MR and the MR input to Qn and Q5-9 output propagation delays”. • Section 14 “Package outline” added.			
HEF4017B_CNV_3	19950101	Product specification	-	HEF4017B_CNV_2
HEF4017B_CNV_2	19950101	Product specification	-	-

© NXP B.V. 2008. All rights reserved.

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2008. All rights reserved.

19. Contents

1 General description 1
2 Features 1
3 Applications 1
4 Ordering information 2
5 Functional diagram 2
6 Pinning information 3
6.1 Pinning 3
6.2 Pin description 3
7 Functional description 4
8 Limiting values 5
9 Recommended operating conditions 6
10 Static characteristics 6
11 Dynamic characteristics 7
12 Waveforms 9
13 Application information 11
14 Package outline 12
15 Abbreviations 14
16 Revision history 14
17 Legal information 15
17.1 Data sheet status 15
17.2 Definitions 15
17.3 Disclaimers 15
17.4 Trademarks 15
18 Contact information 15
19 Contents 16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 December 2008
Document identifier: HEF4017B_4

founded by

PHILIPS