M51996AP/AFP

Switching Regulator Control

REJ03D0836-0201
Rev.2.01
Nov 14, 2007

Description

M51996A is the primary switching regulator controller which is especially designed to get the regulated DC voltage from AC power supply.

This IC can directly drive the MOS FET with fast rise and fast fall output pulse and with a large-drive totempole output.

Type M51996A has the functions of not only high frequency OSC and fast output drive but also current limit with fast response and high sensibility so the true "fast switching regulator" can be realized.

The M51996A is equivalent to the M51978 with externally re-settable OVP (over voltage protection) circuit.

Features

- 500kHz operation to MOS FET
- Output current : ±1 A
- Output rise time 60 ns, fall time 40 ns
- Modified totempole output method with small through current
- Compact and light-weight power supply
  - Small start-up current : 100 ∝A typ.
  - Big difference between "start-up voltage" and "stop voltage" makes the smoothing capacitor of the power input section small.
  - Start-up threshold 16 V , stop voltage 10 V
  - Packages with high power dissipation are used to with-stand the heat generated by the gate-drive current of MOS FET.
  - 14-pin DIP, 16-pin SOP 1.5W (at 25°C)
- Simplified peripheral circuit with protection circuit and built-in large-capacity totempole output
  - High-speed current limiting circuit using pulse-by-pulse method (CLM+pin)
  - Over-voltage protection circuit with an externally re-settable latch (OVP)
  - Protection circuit for output miss action at low supply voltage (UVLO)
- High-performance and highly functional power supply
  - Triangular wave oscillator for easy dead time setting
  - SOFT start function by expanding period

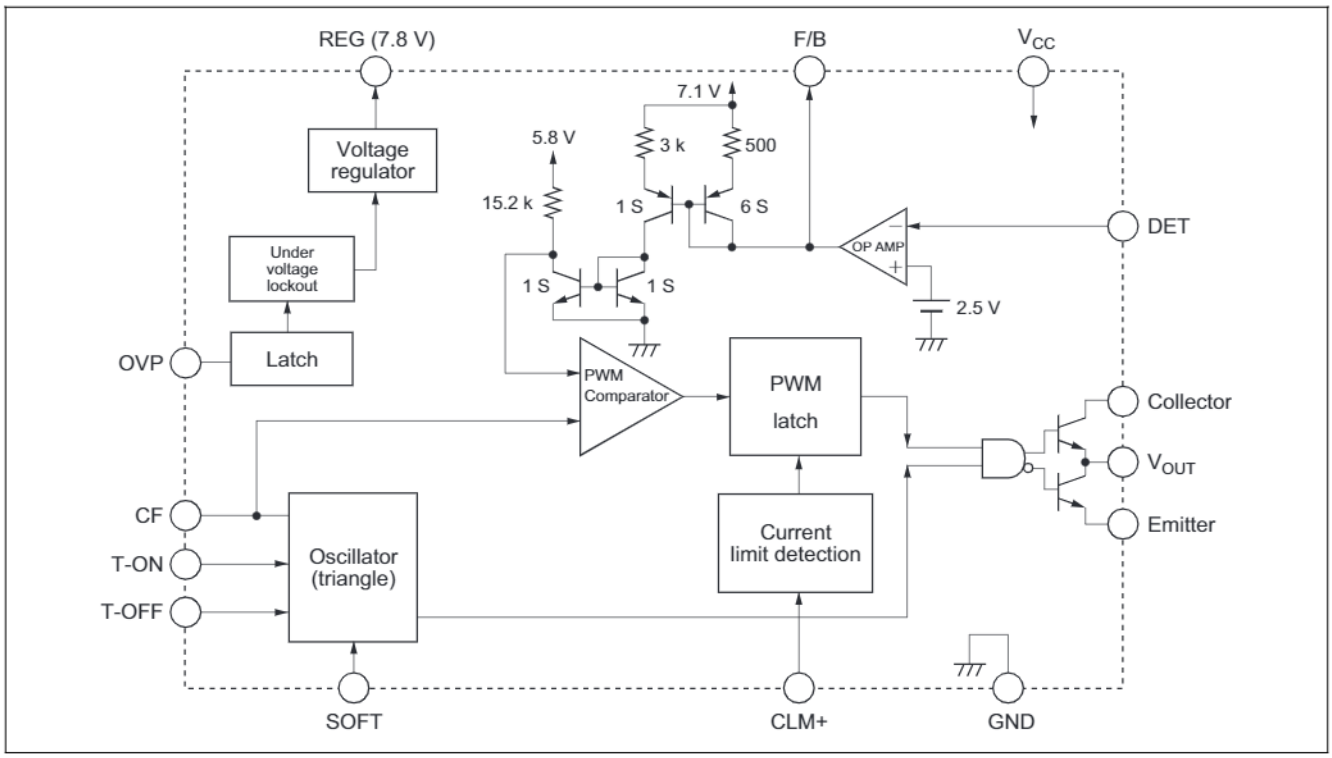
Application

Feed forward regulator, fly-back regulator

Recommended Operating Conditions

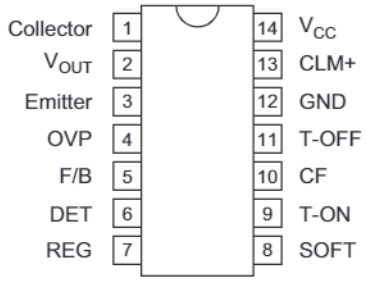
- Supply voltage range: 12 to 30 V
- Operating frequency: less than 500 kHz
- Oscillator frequency setting resistance
- T-ON pin resistance
  - R_{ON}: 10 k to 75 kΩ
- T-OFF pin resistance
  - R_{OFF}: 2 k to30 kΩ

Block Diagram



Pin Arrangement

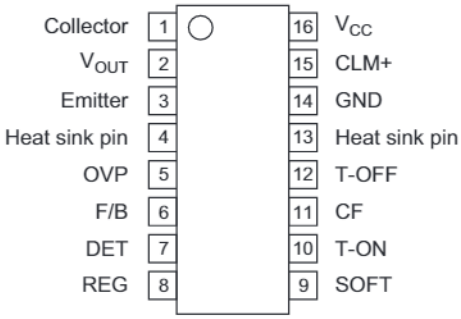
M51996AP



(Top view)

Outline: PRDP0014AA-A (14P4)

M51996AFP



(Top view)

Outline: PRSP0016DE-A (16P2N-A)

Note: Connect the heat sink pin to GND.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	31	V	
Collector voltage	V_C	31	V	
Output current	I_O	±1	A	Peak
		±0.15		Continuous
V_{REG} terminal output current	I_{VREG}	−6	mA	
SOFT terminal voltage	V_{SOFT}	V_{REG} + 0.2	V	
CLM+ terminal voltage	V_{CLM+}	−0.3 to +3	V	
DET terminal voltage	V_{DET}	6	V	
OVP terminal current	I_{OVP}	10	mA	
F/B terminal current	I_{FB}	−10	mA	
T-ON terminal input current	I_{TON}	−1	mA	
T-OFF terminal input current	I_{TOFF}	−2	mA	
Power dissipation	Pd	1.5	W	Ta = 25°C
Thermal derating	Kθ	12	mW/°C	Ta > 25°C
Operating temperature	Topr	−30 to +85	°C	
Storage temperature	Tstg	−40 to +125	°C	

Notes: 1. "+" sign shows the direction of current flowing into the IC and "−" sign shows the current flowing out from the IC.
2. The low impedance voltage supply should not be applied to the OVP terminal.

Electrical Characteristics

(V_{CC} = 18 V, Ta = 25°C, unless otherwise noted)

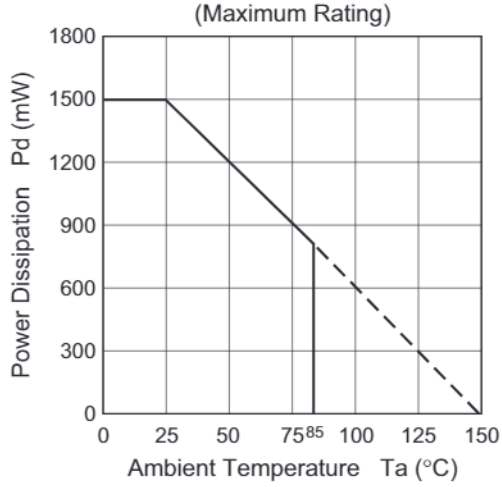
Block	Item	Symbol	Limits			Unit	Test Conditions
			Min.	Typ.	Max.		
Supply voltage/ circuit current	Operating supply voltage range	V_{CC}	$V_{CC(STOP)}$	—	30	V	
	Operation start up voltage	$V_{CC(START)}$	15.2	16.2	17.2	V	
	Operation stop voltage	$V_{CC(STOP)}$	9.0	9.9	10.9	V	
	$V_{CC(START)}$, $V_{CC(STOP)}$ difference	ΔV_{CC}	5.0	6.3	7.6	V	$\Delta V_{CC} = V_{CC(START)} - V_{CC(STOP)}$
	Stand-by current	I_{CCL}	65	100	150	∝A	V_{CC} = 14.5 V, Ta = 25°C
			50	100	200		V_{CC} = 14.5 V, –30 ≤ Ta ≤ 85°C
	Operating circuit current	I_{CCO}	7.3	11	17	mA	V_{CC} = 15 V, f = 188 kHz
			8	12	19		V_{CC} = 30 V, f = 188 kHz
	Circuit current in OVP state	I_{CCOVP}	1.3	2.0	3.0	mA	V_{CC} = 25 V
			140	210	320	∝A	V_{CC} = 9.5 V
F/B	Current at 0% duty	I_{FBMIND}	–2.1	–1.5	–1.0	mA	F/B terminal input current
	Current at maximum duty	I_{FBMAXD}	–0.9	–0.6	–0.4	mA	F/B terminal input current
	Current difference between max and 0% duty	ΔI_{FB}	–1.35	–0.99	–0.70	mA	$\Delta I_{FB} = I_{FBMIND} - I_{FBMAXD}$
	F/B terminal voltage	V_{FB}	4.9	5.9	7.1	V	F/B terminal input current = 0.95 mA
	OVP terminal resistance	R_{FB}	420	600	780	Ω	
OVP	OVP terminal H threshold voltage	V_{THOVPH}	540	750	960	mV	
	OVP terminal hysteresis voltage	ΔV_{THOVP}	—	30	—	mV	$\Delta V_{THOVP} = V_{THOVPH} - V_{THOVPL}$
	OVP terminal threshold current	I_{THOVP}	80	150	250	∝A	
	OVP terminal input current	I_{INOVP}	80	150	250	∝A	V_{OVP} = 400 mV
	OVP reset supply voltage	V_{CCOVPC}	7.5	9.0	10.0	V	OVP terminal is open. (high impedance)
	Difference supply voltage between operation stop and OVP reset	$V_{CC(STOP)} - V_{CCOVPC}$	0.55	1.20	—	V	
	Current from OVP terminal for OVP reset	I_{THOVPC}	–480	–320	–213	∝A	V_{CC} = 30 V
			–210	–140	–93		V_{CC} = 18 V
CLM+	CLM+ terminal threshold voltage	V_{THCLM+}	180	200	220	mV	
	CLM+ terminal current	I_{INCLM+}	–280	–200	–140	∝A	V_{CLM+} = 0 V
	Delay time from CLM+ to V_{OUT}	T_{PDCLM+}	—	150	—	ns	

(V_{CC} = 18 V, Ta = 25°C, unless otherwise noted)

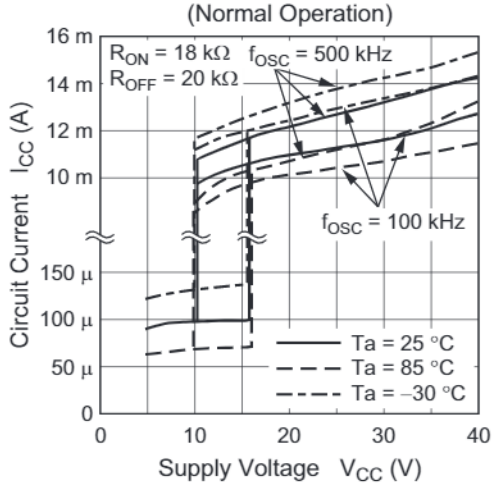
Block	Item	Symbol	Limits			Unit	Test Conditions
			Min.	Typ.	Max.		
Oscillator	Oscillating frequency	f_{OSC}	170	188	207	kHz	R_{ON} = 20 kΩ, R_{OFF} = 17 kΩ
	Maximum ON duty	T_{DUTY}	47	50	53	%	C_F = 220 pF, –5 ≤ Ta ≤ 85°C
	Upper limit voltage of oscillation waveform	V_{OSCH}	3.97	4.37	4.77	V	R_{ON} = 20 kΩ, R_{OFF} = 17 kΩ C_F = 220 pF
	Lower limit voltage of oscillation waveform	V_{OSCL}	1.76	1.96	2.16	V	
	Voltage difference between upper limit and lower limit of OSC waveform	ΔV_{OSC}	2.11	2.41	2.71	V	
	T-ON terminal voltage	$V_{T\text{-}ON}$	3.8	4.5	5.4	V	R_{ON} = 20 kΩ
	T-OFF terminal voltage	$V_{T\text{-}OFF}$	2.9	3.5	4.2	V	R_{OFF} = 17 kΩ
SOFT	Oscillating frequency during SOFT operation (V_{SOFT} = 5.5 V)	$f_{OSCSOFT}$	170	188	207	kHz	R_{ON} = 20 kΩ, R_{OFF} = 17 kΩ C_F = 220 pF
	Oscillating frequency during SOFT operation (V_{SOFT} = 2.5 V)		111	131	151		
	Oscillating frequency during SOFT operation (V_{SOFT} = 0.2 V)		19.0	23.3	27.0		
	SOFT terminal input current	I_{SOFTIN}	–0.5	–0.1	—	∝A	V_{SOFT} = 1 V
	SOFT terminal discharging current	I_{SOFDIS}	1	3.3	—	mA	Discharge current of SOFT terminal at V_{CC} less than $V_{CC(STOP)}$
REG	Regulator output voltage	V_{REG}	6.8	7.8	8.8	V	
Output	Output low voltage	$V_{OL}1$	—	0.04	0.4	V	V_{CC} = 18 V, I_O = 10 mA
		$V_{OL}2$	—	0.7	1.4	V	V_{CC} = 18 V, I_O = 100 mA
		$V_{OL}3$	—	0.85	1.0	V	V_{CC} = 5 V, I_O = 1 mA
		$V_{OL}4$	—	1.3	2.0	V	V_{CC} = 5 V, I_O = 100 mA
	Output high voltage	$V_{OH}1$	16.0	16.7	—	V	V_{CC} = 18 V, I_O = –10 mA
		$V_{OH}2$	15.5	16.5	—	V	V_{CC} = 18 V, I_O = –100 mA
	Output voltage rise time	T_{RISE}	—	60	—	ns	
	Output voltage fall time	T_{FALL}	—	40	—	ns	
Detection	Detection voltage	V_{DET}	2.4	2.5	2.6	V	
	DET terminal input current	I_{INDET}	—	1.0	3.0	∝A	V_{DET} = 2.5 V
	Voltage gain of detection amp	G_{AVDET}	30	40	—	dB	

Main Characteristics

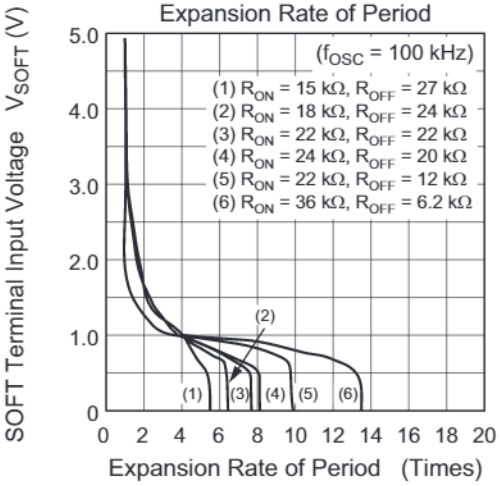
Thermal Derating
(Maximum Rating)



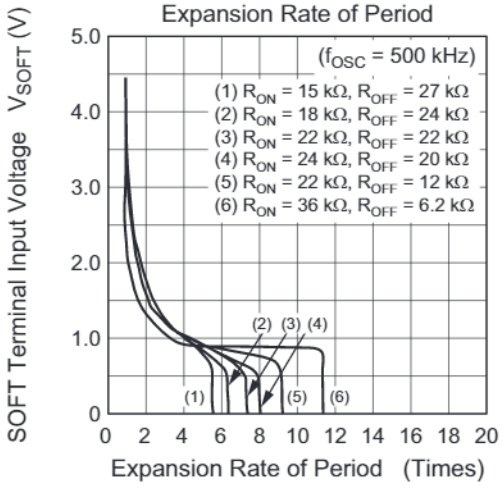
Circuit Current vs. Supply Voltage
(Normal Operation)



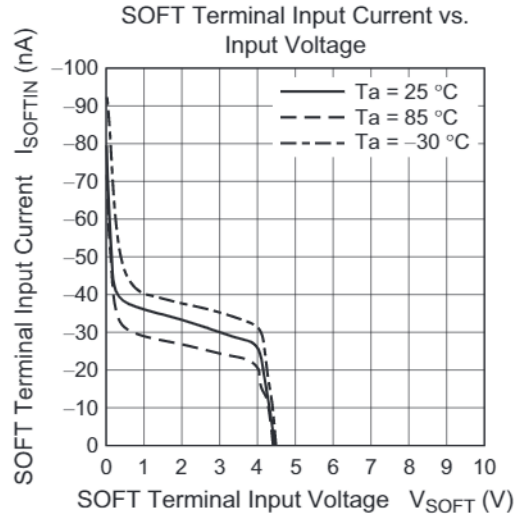
SOFT Terminal Input Voltage vs.
Expansion Rate of Period



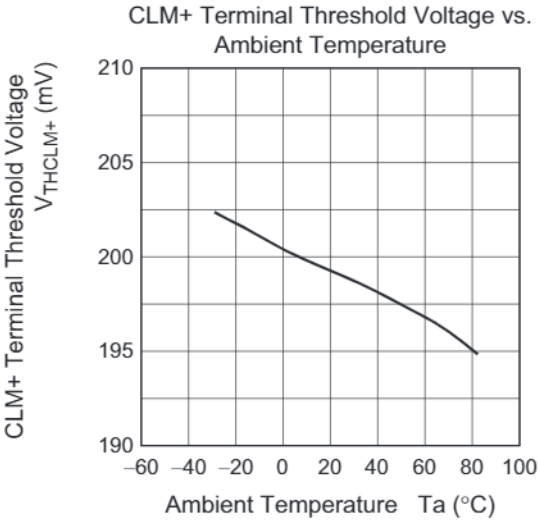
SOFT Terminal Input Voltage vs.
Expansion Rate of Period



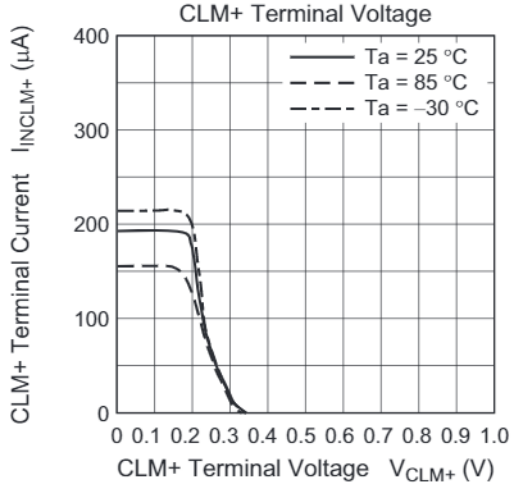
SOFT Terminal Input Current vs.
Input Voltage



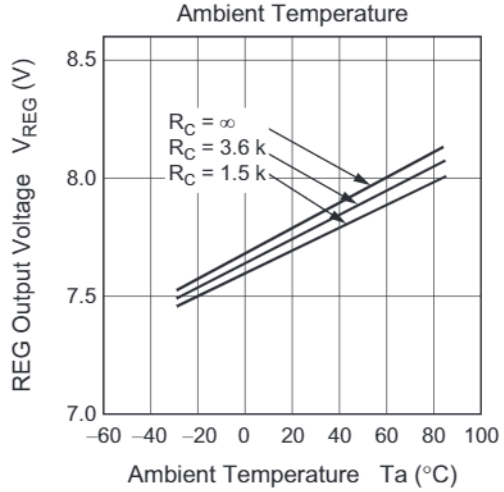
CLM+ Terminal Threshold Voltage vs.
Ambient Temperature



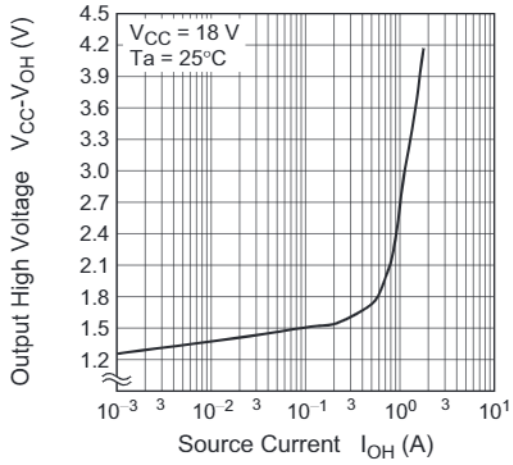
CLM+ Terminal Current vs.
CLM+ Terminal Voltage



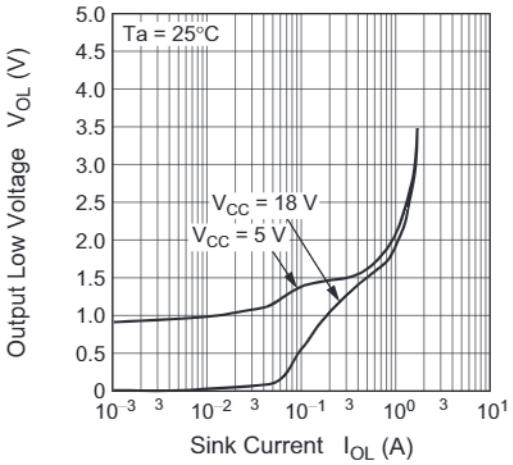
REG Output Voltage vs.
Ambient Temperature



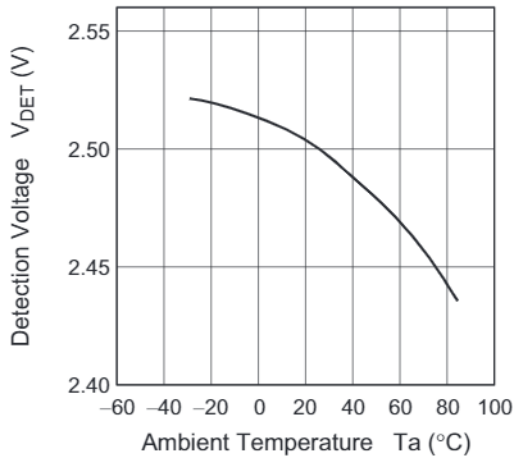
Output High Voltage vs.
Source Current



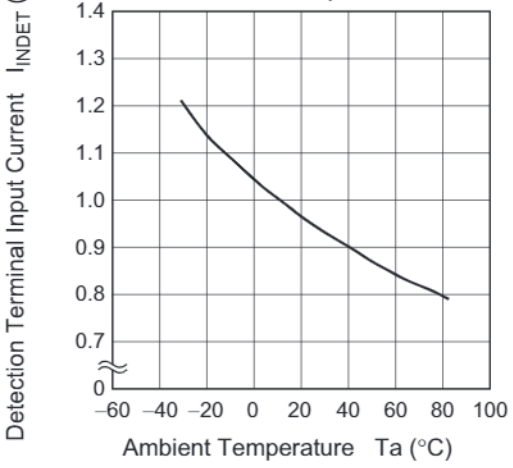
Output Low Voltage vs.
Sink Current



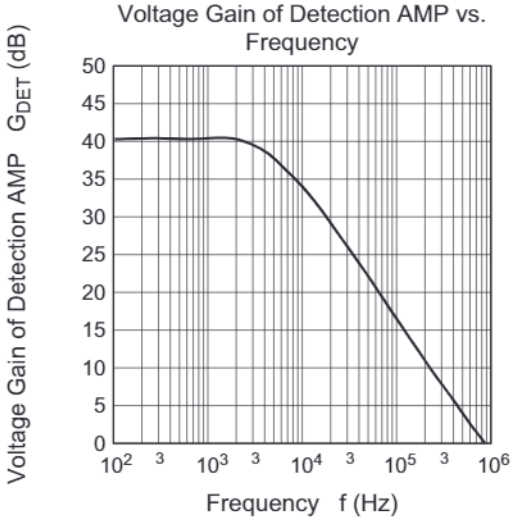
Detection Voltage vs.
Ambient Temperature



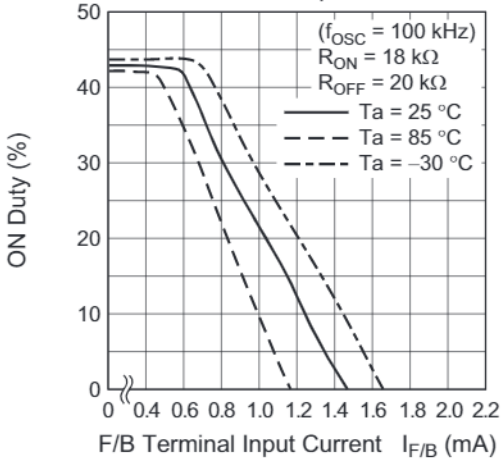
Detection Terminal Input Current vs.
Ambient Temperature



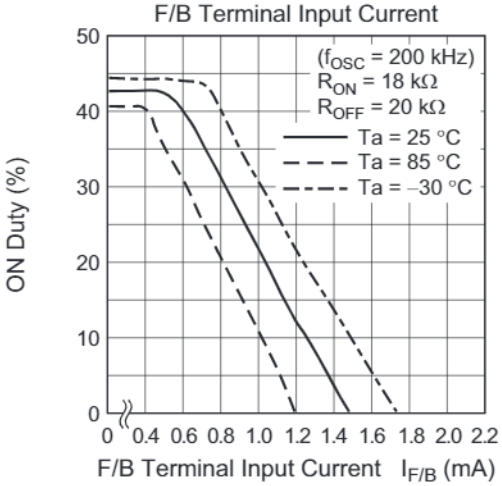
Voltage Gain of Detection AMP vs. Frequency



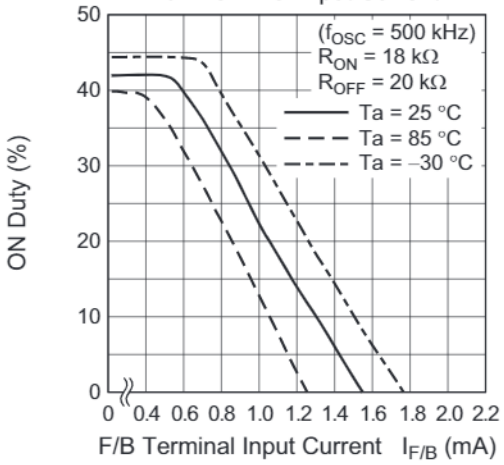
ON Duty vs. F/B Terminal Input Current



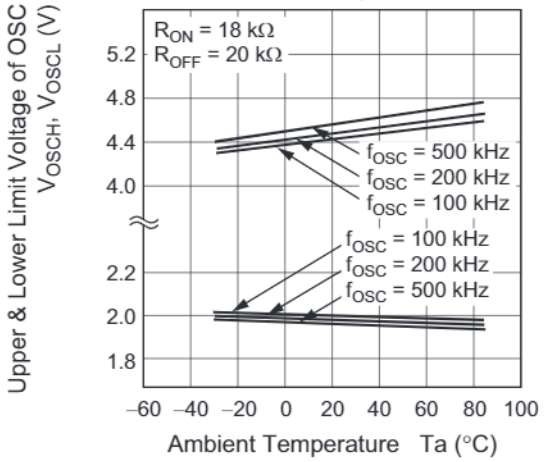
ON Duty vs. F/B Terminal Input Current



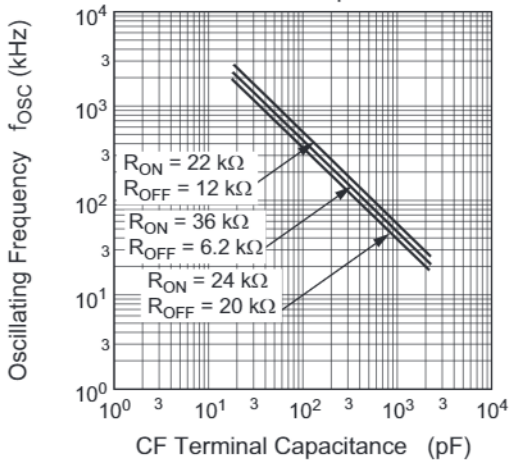
ON Duty vs. F/B Terminal Input Current



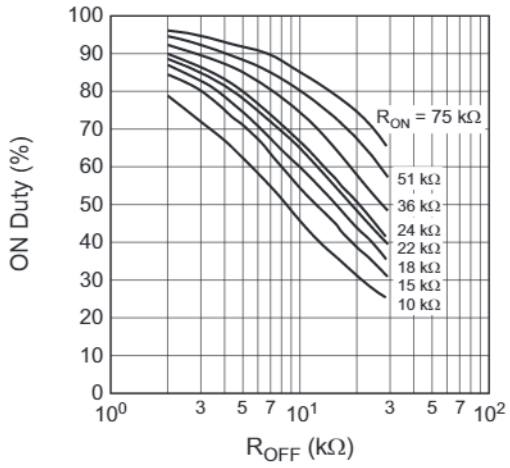
Upper & Lower Limit Voltage of OSC vs. Ambient Temperature



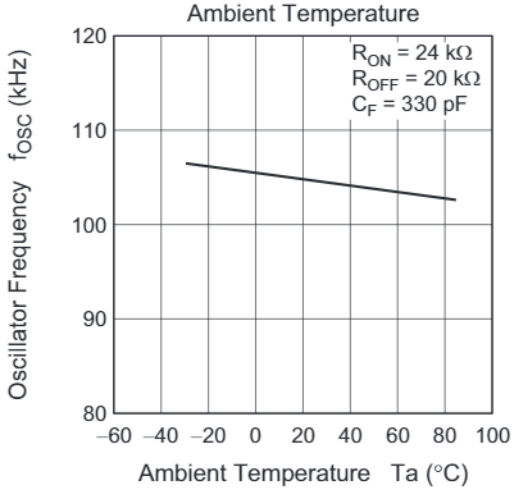
Oscillating Frequency vs. CF Terminal Capacitance



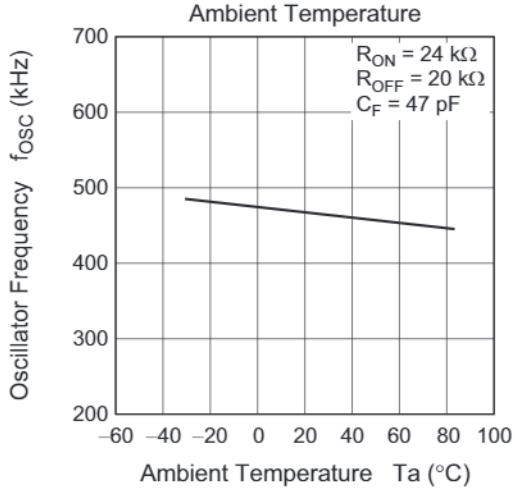
ON Duty vs. R_{OFF}



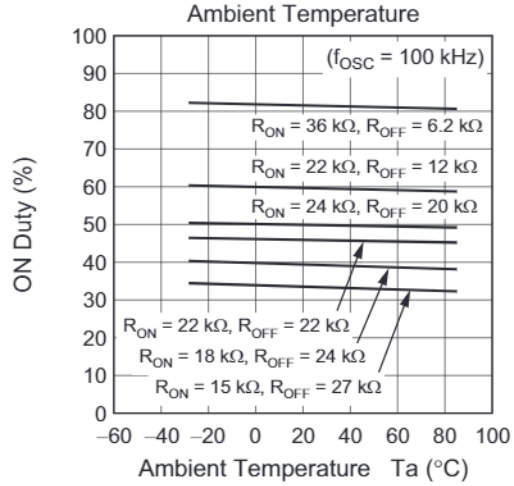
Oscillator Frequency vs. Ambient Temperature



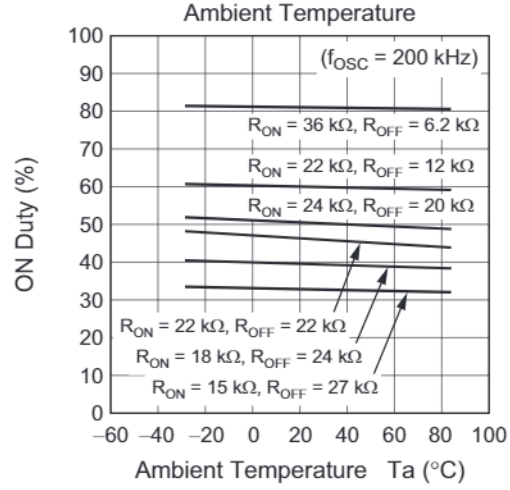
Oscillator Frequency vs. Ambient Temperature



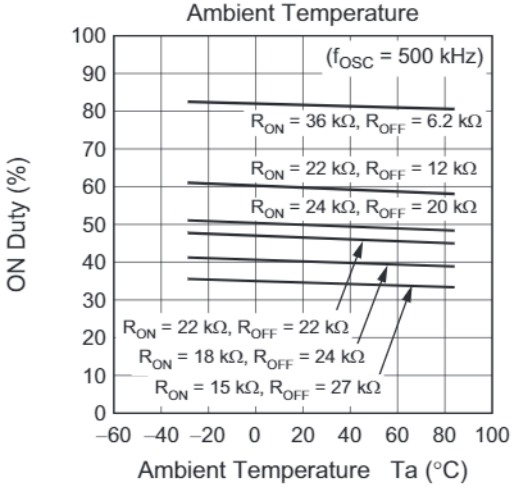
ON Duty vs. Ambient Temperature



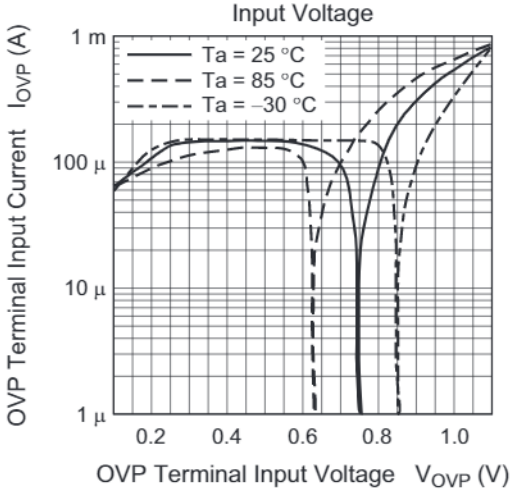
ON Duty vs. Ambient Temperature



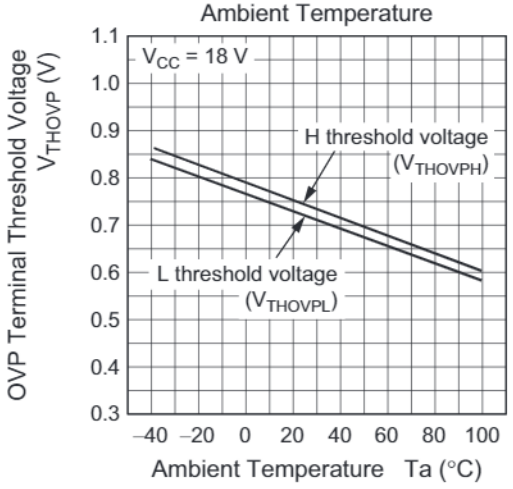
ON Duty vs. Ambient Temperature



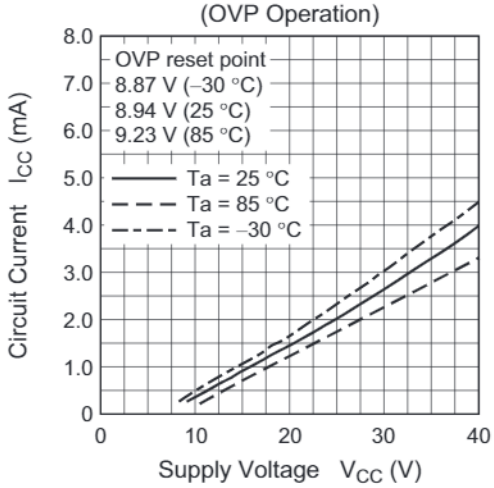
OVP Terminal Input Current vs. Input Voltage



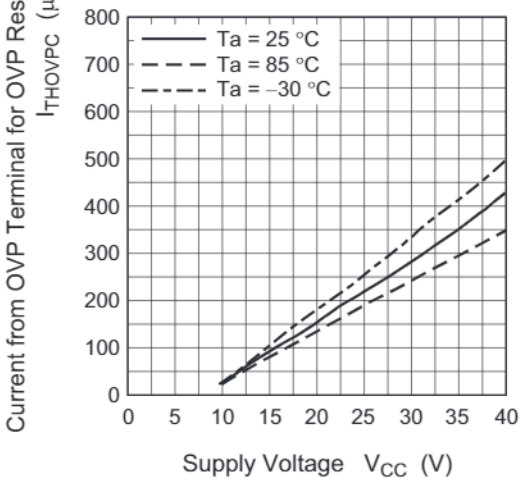
OVP Terminal Threshold Voltage vs. Ambient Temperature



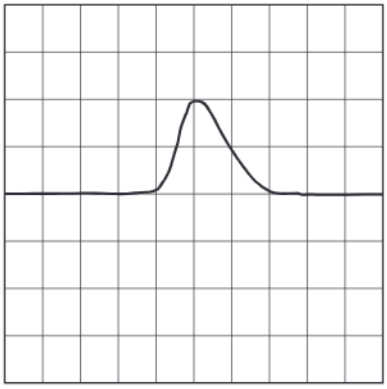
Circuit Current vs. Supply Voltage (OVP Operation)



Current from OVP Terminal for OVP Reset vs. Supply Voltage

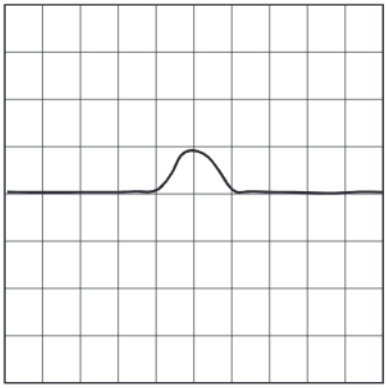


Output Through Current Waveform at Rising Edge of Output Pulse



Horizontal-axis: 20 ns/div
Vertical-axis: 50 mA/div

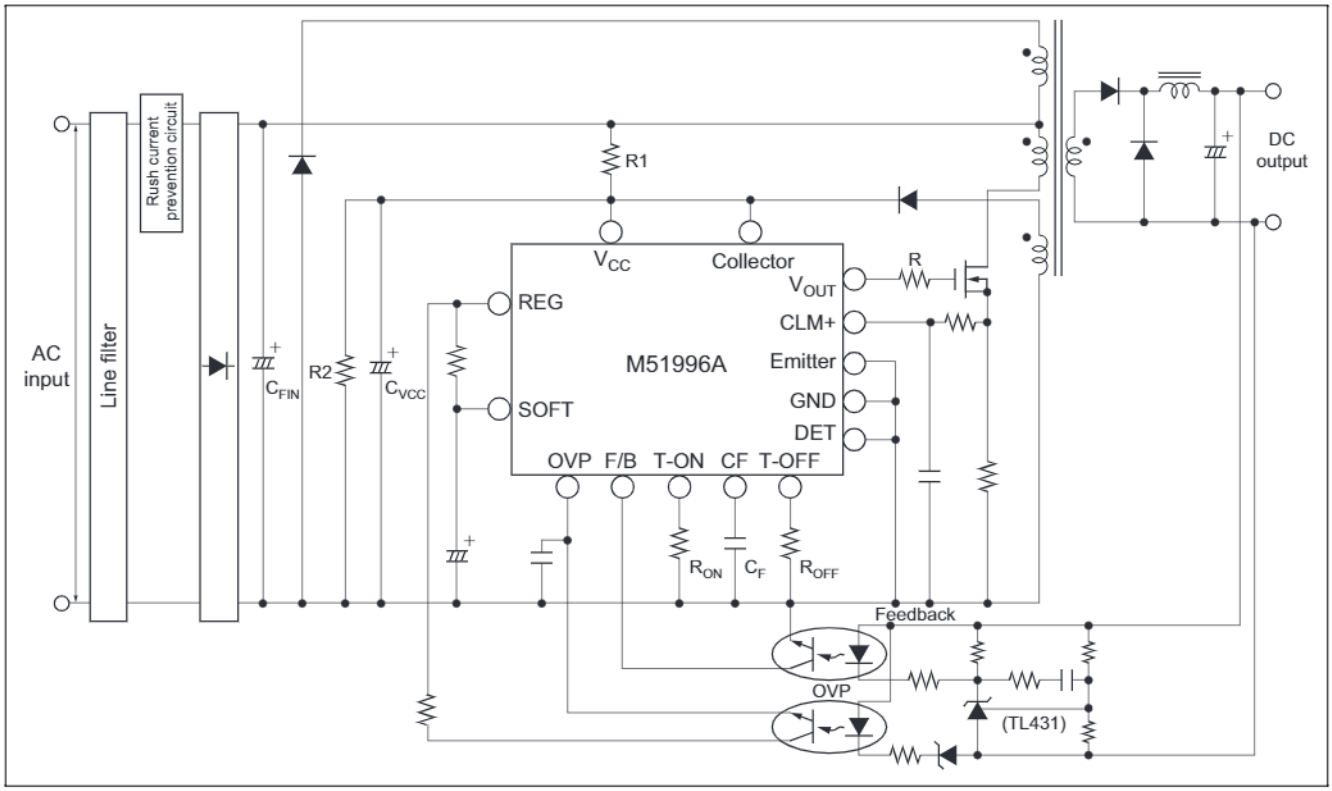
Output Through Current Waveform at Falling Edge of Output Pulse



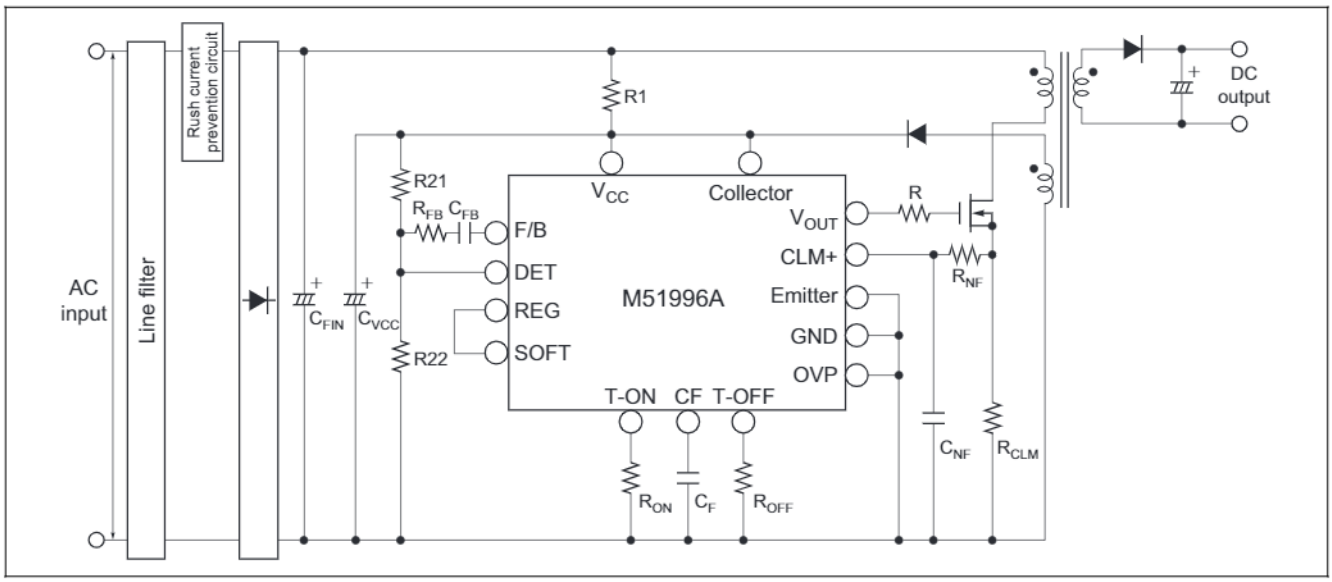
Horizontal-axis: 20 ns/div
Vertical-axis: 5 mA/div

Application Example

(1) Application Example for Feed Forward Regulator



(2) Application Example for Fly-back Regulator



Function Description

Type M51996AP and M51996AFP are especially designed for off-line primary PWM control IC of switching mode power supply to get DC voltage from AC power supply.

Using this IC, smart SMPS can be realized with reasonable cost and compact size as the number of external electric parts can be reduced and also parts can be replaced by reasonable one.

In the following circuit diagram, MOS FET is used for output transistor, however bipolar transistor can be replaced with no problem.

Start-up Circuit Section

The start-up current is such low current level as typical 100 ∝A, as shown in figure 1, when the V_{CC} voltage is increased from low level to start-up voltage $V_{CC(START)}$.

In this voltage range, only a few parts in this IC, which has the function to make the output voltage low level, is alive and I_{CC} current is used to keep output low level. The large voltage difference between $V_{CC(START)}$ and $V_{CC(STOP)}$ makes start-up easy, because it takes rather long duration from $V_{CC(START)}$ to $V_{CC(STOP)}$.

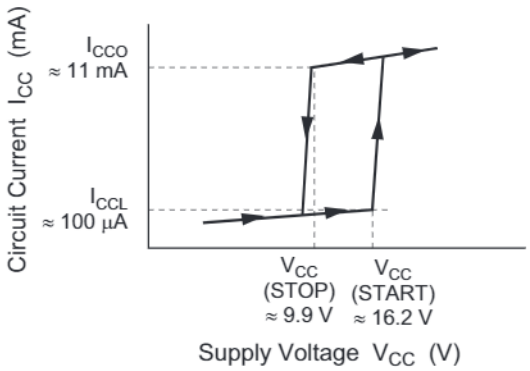


Figure 1 Circuit Current vs. Supply Voltage

Oscillator Section

The oscillation waveform is the triangle one. The ON-duration of output pulse depends on the rising duration of the triangle waveform and dead-time is decided by the falling duration.

The rising duration is determined by the product of external resistor R_{ON} and capacitor C_F and the falling duration is mainly determined by the product of resistor R_{OFF} and capacitor C_F.

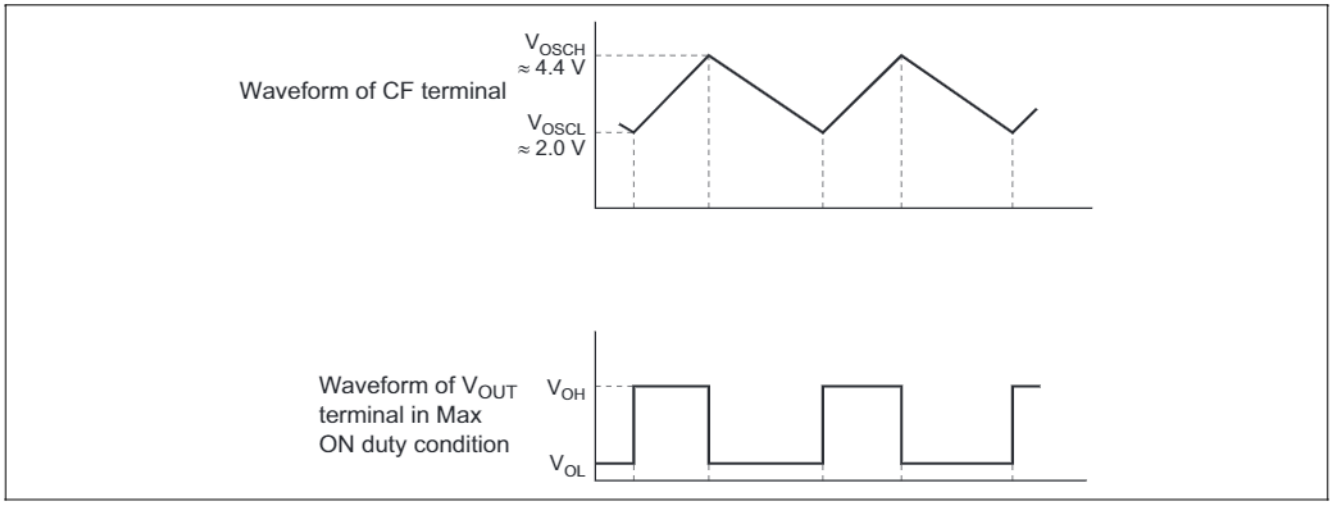


Figure 2 OSC. Waveform at Normal Condition
(no-operation of intermittent action and OSC control circuit)

1. Oscillator operation when SOFT circuit does not operate

   Figure 3 shows the equivalent charging and discharging circuit diagram of oscillator.
   The current flows through R_{ON} from the constant voltage source of 5.8 V. C_F is charged up by the same amplitude as R_{ON} current, when internal switch SW1, SW2 is switched to "charging side". The rise rate of C_F terminal is given as

$$\approx \frac{V_{T\text{-}ON}}{R_{ON} \times C_F} \text{ (V/s)} \quad \ldots\ldots (1)$$

   where $V_{T\text{-}ON} \approx 4.5$ V

   The maximum on duration is approximately given as

$$\approx \frac{(V_{OSCH} - V_{OSCL}) \times R_{ON} \times C_F}{V_{T\text{-}ON}} \text{ (s)} \quad \ldots\ldots (2)$$

   where $V_{OSCH} \approx 4.4$ V

   $V_{OSCL} \approx 2.0$ V

   C_F is discharged by the summed-up of R_{OFF} current and one sixteenth (1/16) of R_{ON} current by the function of Q2, Q3 and Q4 when SW1, SW2 are switched to "discharge side".
   So fall rate of CF terminal is given as

$$\approx \frac{V_{T\text{-}OFF}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F} \text{ (V/s)} \quad \ldots\ldots (3)$$

   The minimum off duration approximately is given as

$$\approx \frac{(V_{OSCH} - V_{OSCL}) \times C_F}{\frac{V_{T\text{-}OFF}}{R_{OFF}} + \frac{V_{T\text{-}ON}}{16 \times R_{ON}}} \text{ (s)} \quad \ldots\ldots (4)$$

   The cycle time of oscillation is given by the summation of equations 2 and 4.
   The frequency including the dead-time is not influenced by the temperature because of the built-in temperature compensating circuit.

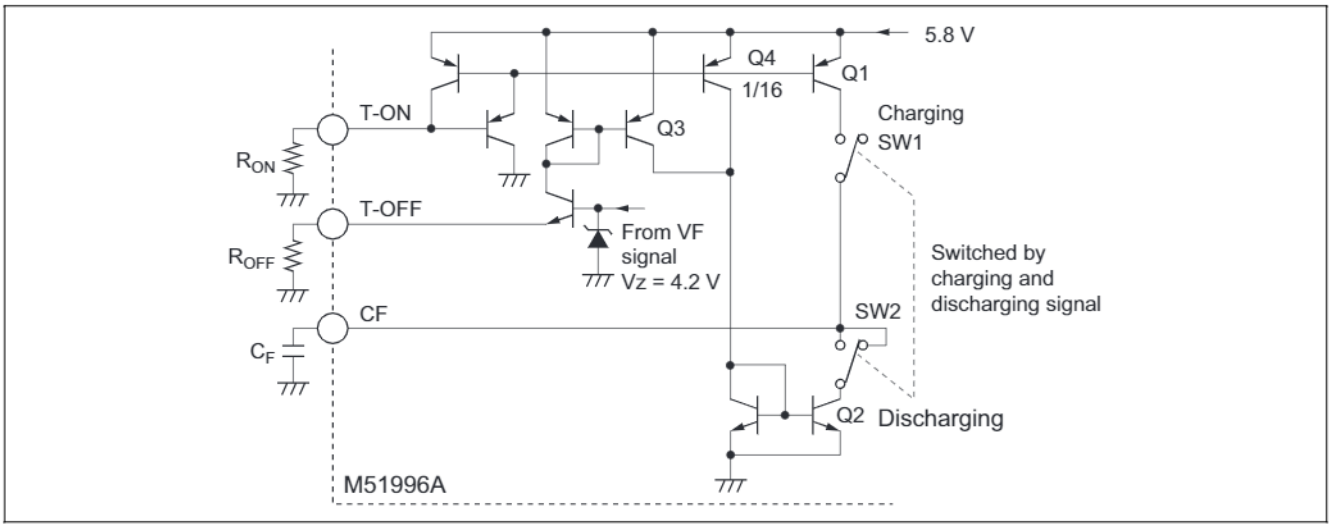


Figure 3 Schematic Diagram of Charging and Discharging Control Circuit for OSC Capacitor C_F

2. Oscillator operation when the SOFT (soft start) circuit is operating.
Output transistor is protected from rush current by CLM function at the start time of power on. SOFT terminal is used to improve the rising response of the output voltage of power supply (prevention of overshooting).
The ON duration of output is kept constant, and the OFF duration is extended as the SOFT terminal voltage becomes lower by the soft start circuit of this IC.
The maximum value of extension is set internally at approximately sixteen times of the maximum ON duration.
The features of this method are as follows :
(1) It is ideal for primary control as IC driving current is supplied from the third winding of the main transformer at the start-up because constant ON duration is obtained from start-up.
(2) It is possible to get a wide dynamic range for ON/OFF ratio by pulse-by-pulse current limit circuit.
(3) The response characteristics at power-on is not affected by input voltage as the pulse-by-pulse limit current value is not affected by the input voltage.
Figure 4 shows the circuit diagram of the soft start. If SOFT terminal voltage is low, T-OFF terminal voltage becomes low and $V_{T\text{-}OFF}$ in equations (3) and (4) become low.

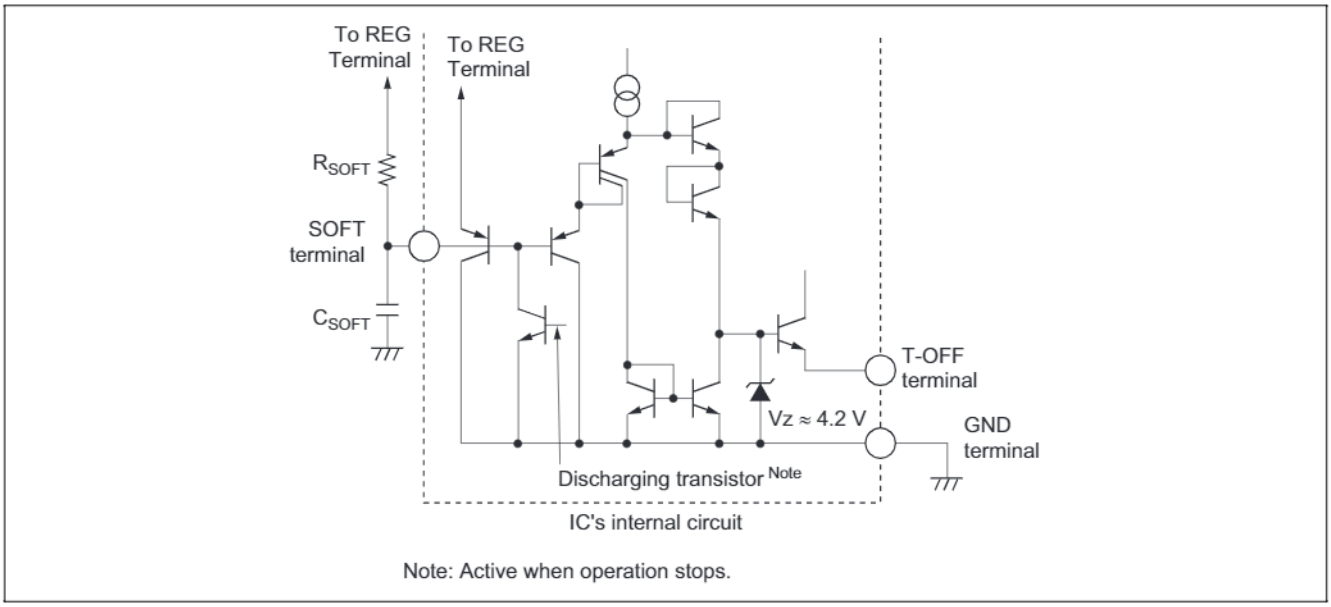


Figure 4 Circuit Diagram of SOFT Terminal Section and T-OFF Terminal Section

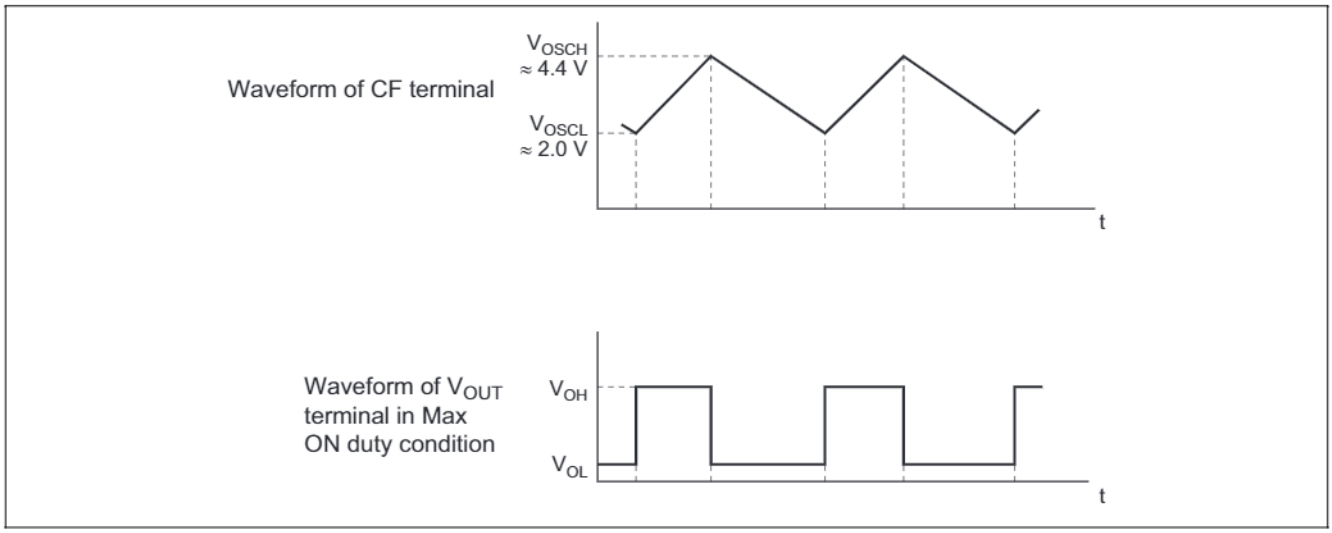


Figure 5 Oscillator Waveform When the SOFT Circuit is Operating

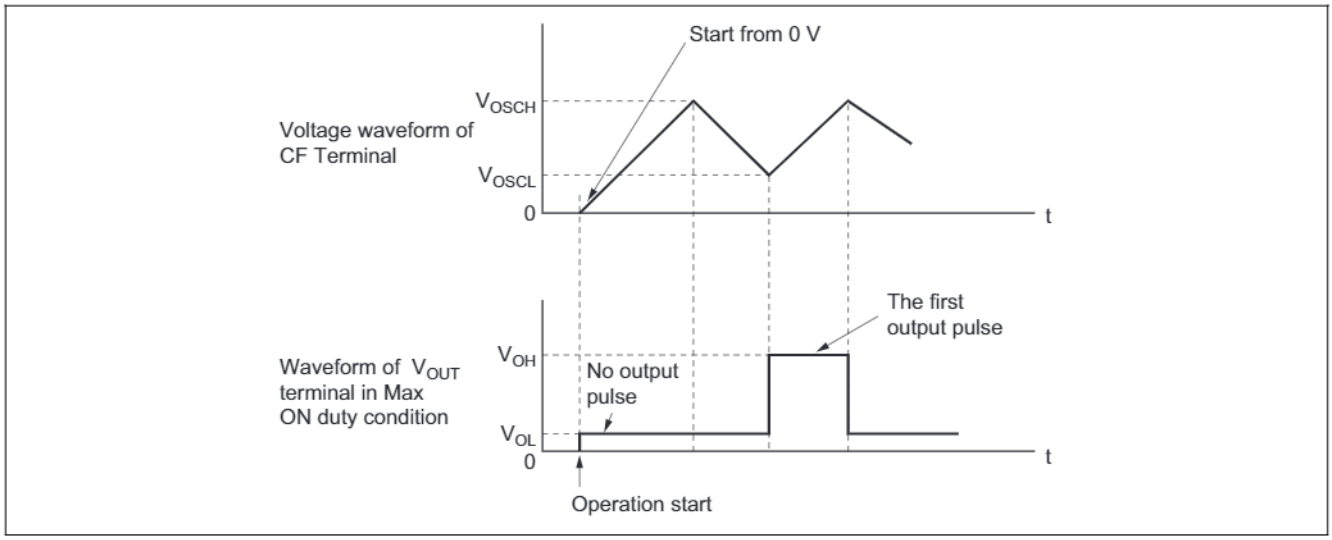


Figure 6 Relationship Between Oscillator Waveform and Output Waveform at Start-up

Figure 5 shows the relationship between oscillator waveform and output pulse.
If the SOFT terminal voltage is V_{SOFT}, the rise rate of CF terminal given as

$$\approx \frac{V_{T\text{-}ON}}{R_{ON} \times C_F} \text{ (V/s)} \quad \ldots\ldots (5)$$

The fall rate of oscillation waveform is given as

$$\approx \frac{V_{SOFT} - V_{BE}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F} \text{ (V/s)} \quad \ldots\ldots (6)$$

Where

V_{SOFT} ; SOFT terminal applied voltage

$V_{BE} \approx 0.65$ V

If $V_{SOFT} - V_{BE} < 0$, $V_{SOFT} - V_{BE} = 0$

If $V_{SOFT} - V_{BE} > V_{T\text{-}OFF}$ (≈ 3.5 V), $V_{SOFT} - V_{BE} = V_{T\text{-}OFF}$

PWM Comparator, PWM Latch and Current Limit Latch Section

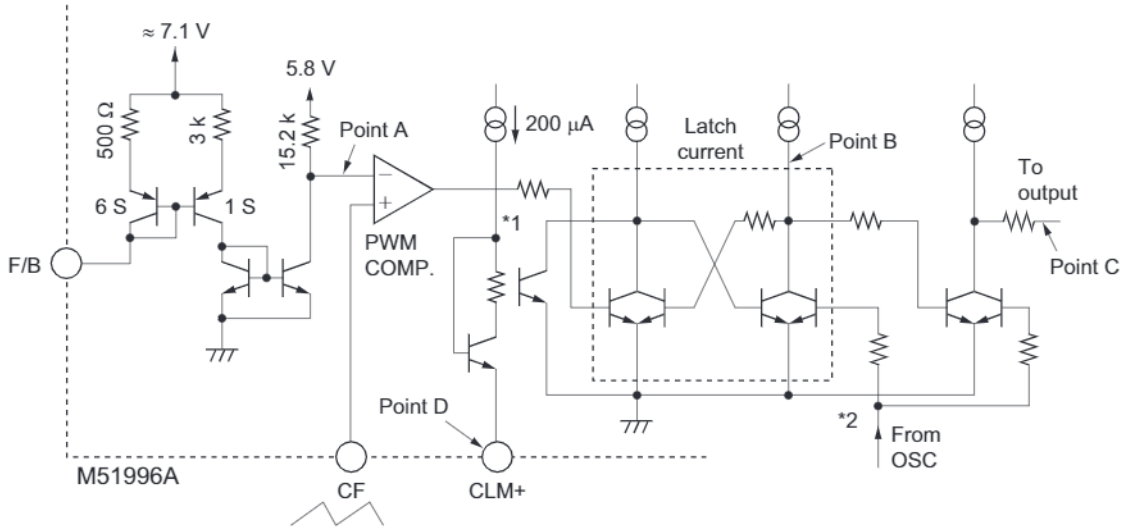
Figure 7 shows the schematic diagram of PWM comparator and PWM latch section. The on-duration of output waveform coincides with the rising duration of CF terminal waveform, when the no output current flows from F/B terminal.

When the F/B terminal has finite impedance and current flows out from F/B terminal, "A" point potential shown in figure 7 depends on this current. So the "A" point potential is close to GND level when the flow-out current becomes large.

"A" point potential is compared with the CF terminal oscillator waveform and PWM comparator, and the latch circuit is set when the potential of oscillator waveform is higher than "A" point potential.

The latch circuit is reset during the dead-time of oscillation (falling duration of oscillation current). So the "B" point potential or output waveform of latch circuit is the one shown in figure 8.

The final output waveform or "C" point potential is got by combining the "B" point signal and dead-time signal logically. (please refer to figure 8)



Notes: 1. Resistor to determine current limit sensitivety
2. High level during dead time

Figure 7 PWM Comparator PWM Latch and Current Limit Latch Section

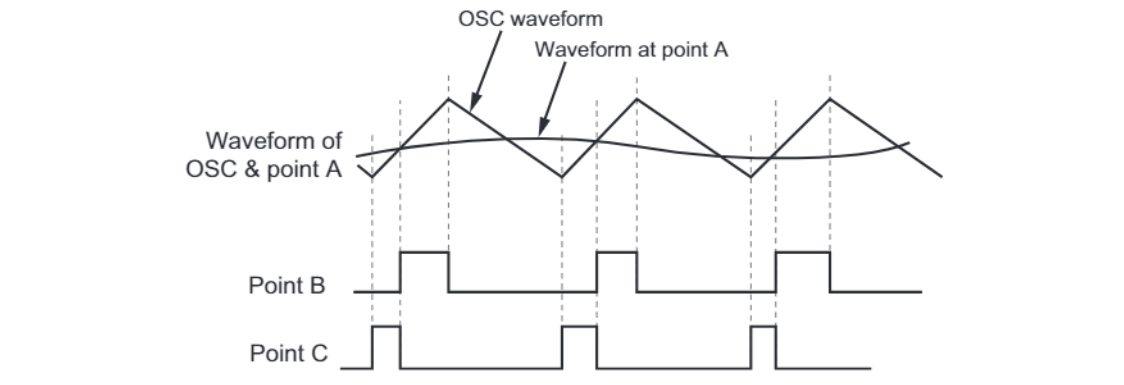


Figure 8 Waveforms of PWM Comparator Input Point A, Latch Circuit Points B and C

When the current-limit signal is applied before the crossing instant of "A" pint potential and CF terminal voltage shown in figure 7, this signal makes the output "off" and the off state will continue until next cycle. Figure 9 shows the timing relation among them.

If the current limiting circuit is set, no waveform is generated at output terminal, however this state is reset during the succeeding dead-time.

So this current limiting circuit is able to have the function in every cycle, and is named "pulse-by-pulse current limit".

There happen some noise voltage on R_{CLM} during the switching of power transistor due to the snubber circuit and stray capacitor of the transformer windings.

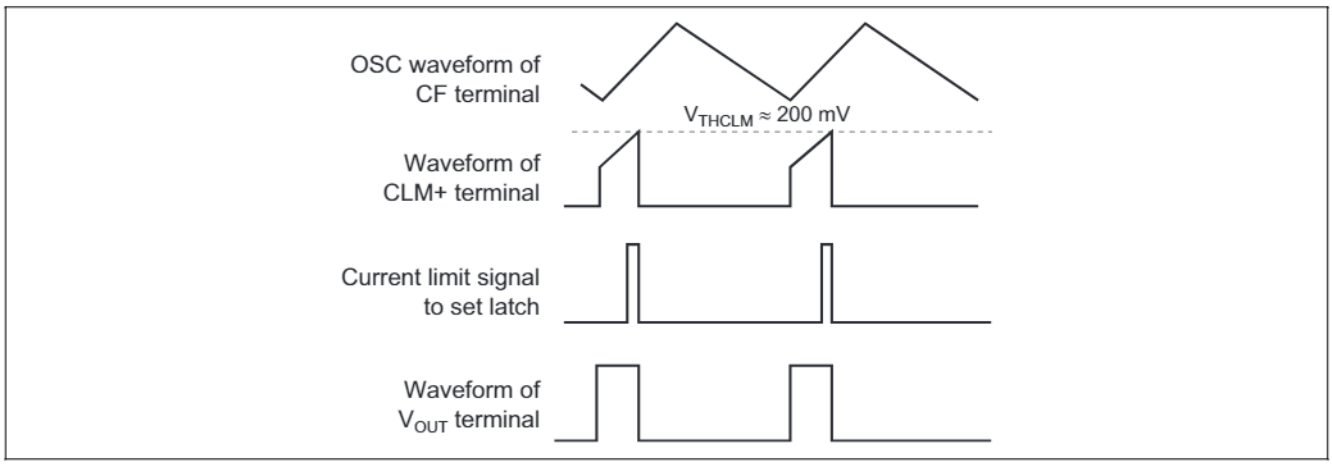


Figure 9 Operating Waveform of Current Limiting Circuit

To eliminate the abnormal operation by the noise voltage, the low pass filter, which consists of R_{NF} and C_{NF} is used as shown in figure 10.

It is recommended to use 10 to 100 Ω for R_{NF} because such range of R_{NF} is not influenced by the flow-out current of some 200 ∝A from CLM+ terminal and C_{NF} is designed to have the enough value to absorb the noise voltage.

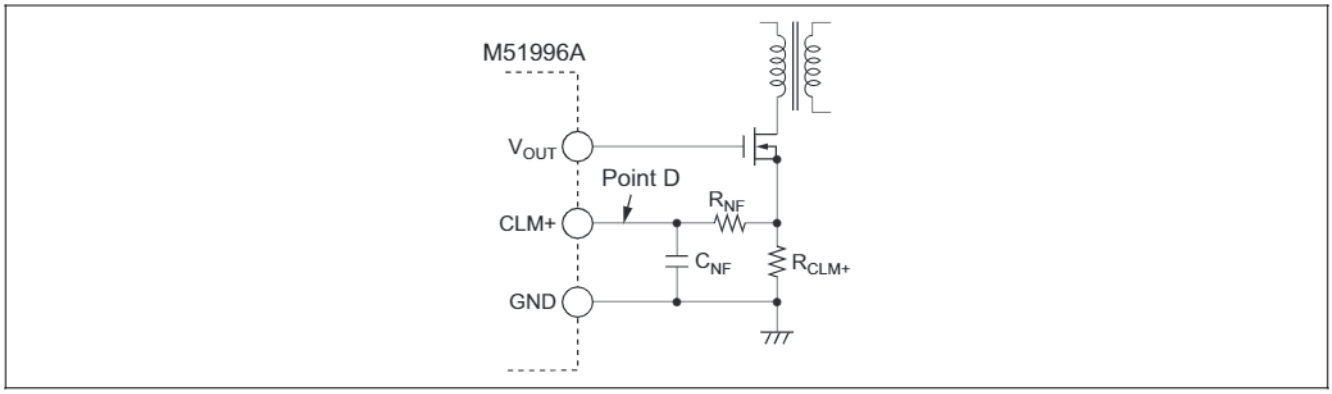


Figure 10 Connection Diagram of Current Limit Circuit

Voltage Detector Circuit (DET) Section

The DET terminal can be used to control the output voltage which is determined by the winding ratio of fly back transformer in fly-back system or in case of common ground circuit of primary and secondary in feed forward system.

The circuit diagram is quite similar to that of shunt regulator type 431 as shown in figure 11. As well known from figure 11 and figure 12, the output of OP AMP has the current-sink ability, when the DET terminal voltage is higher than 2.5 V.

But it becomes high impedance state when lower than 2.5 V DET terminal and F/B terminal have inverting phase characteristics each other, so it is recommended to connect the resistor and capacitor in series between them for phase compensation. It is very important one can not connect by resistor directly as there is the voltage difference between them and the capacitor has the DC stopper function.

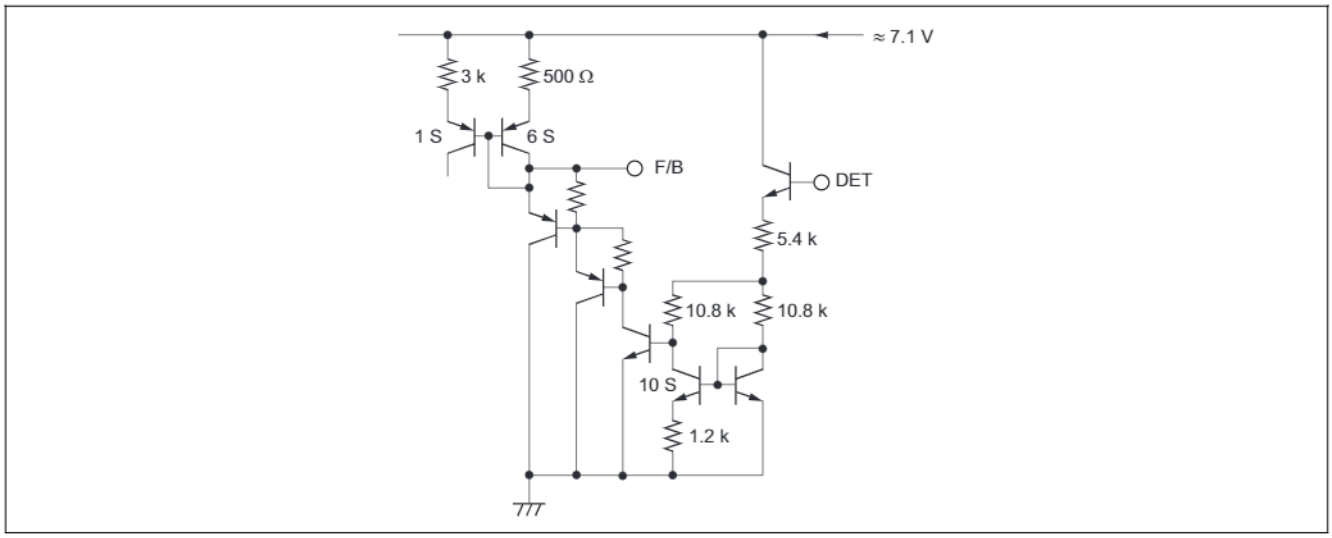


Figure 11 Voltage Detector Circuit Section (DET)

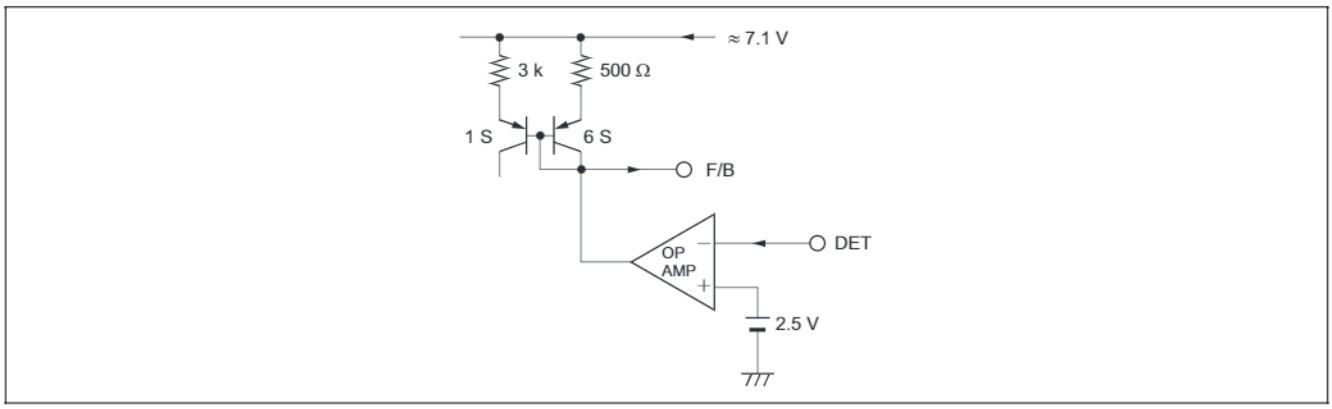


Figure 12 Schematic Diagram of Voltage Detector Circuit Section (DET)

OVP Circuit (Over Voltage Protection Circuit) Section

OVP circuit is basically positive feedback circuit constructed by Q2, Q3 as shown in figure 13.

Q2, Q3 turn on and the circuit operation of IC stops, when the input signal is applied to OVP terminal. (threshold voltage ≈ 750 mV)

The current value of I2 is about 150∝A when the OVP does not operates but it decreases to about 2 ∝A when OVP operates.

It is necessary to input the sufficient larger current (800 ∝A to 8 mA) than I2 for triggering the OVP operation.

The reason to decrease I2 is that it is necessary that I_{CC} at the OVP rest supply voltage is small.

It is necessary that OVP state holds by circuit current from R1 in the application example, so this IC has the characteristic of small I_{CC} at the OVP reset supply voltage (≈ stand-by current + 20 ∝A)

On the other hand, the circuit current is large in the higher supply voltage, so the supply voltage of this IC doesn't become so high by the voltage drop across R1.

This characteristic is shown in figure 14.

The OVP terminal input current in the voltage lower than the OVP threshold voltage is based on I2 and the input current in the voltage higher than the OVP threshold voltage is the sum of the current flowing to the base of Q3 and the current flowing from the collector of Q2 to the base.

For holding in the latch state, it is necessary that the OVP terminal voltage is kept in the voltage higher than V_{BE} of Q3.

So if the capacitor is connected between the OVP terminal and GND, even though Q2 turns on in a moment by the surge voltage, etc, this latch action does not hold if the OVP terminal voltage does not become higher than V_{BE} of Q3 by charging this capacitor.

For resetting OVP state, it is necessary to make the OVP terminal voltage lower than the OVP L threshold voltage or make V_{CC} lower than the OVP reset supply voltage.

As the OVP reset voltage is settled on the rather high voltage of 9.0 V, SMPS can be reset in rather short time from the switch-off of the AC power source if the smoothing capacitor is not so large value.

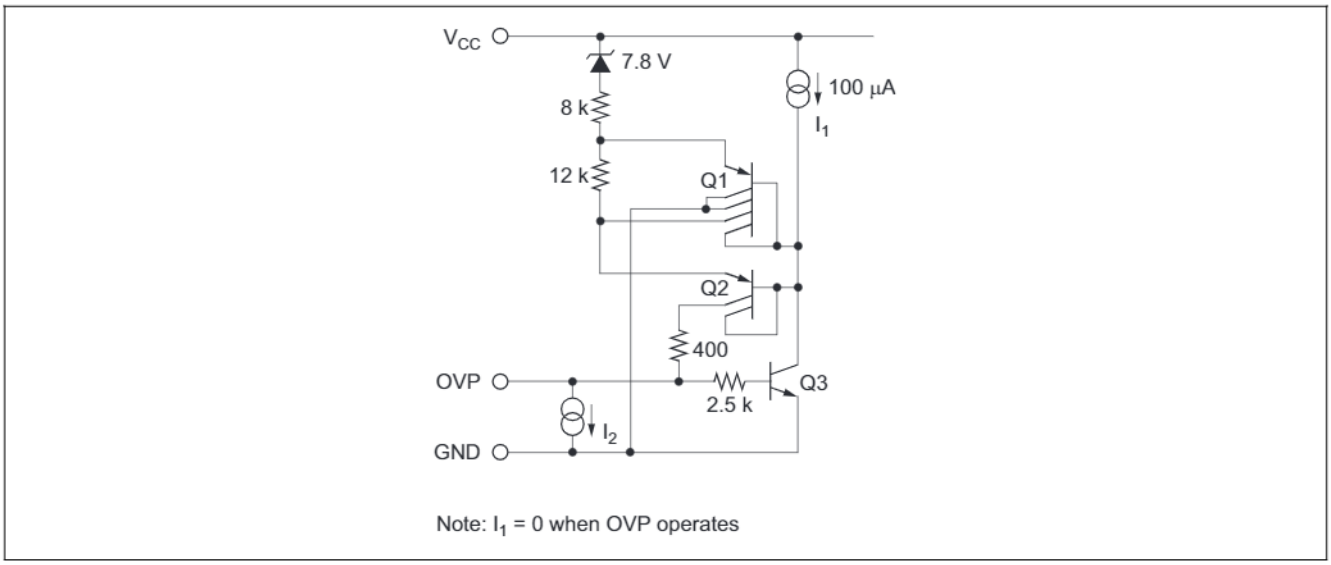


Figure 13 Detail Diagram of OVP Circuit

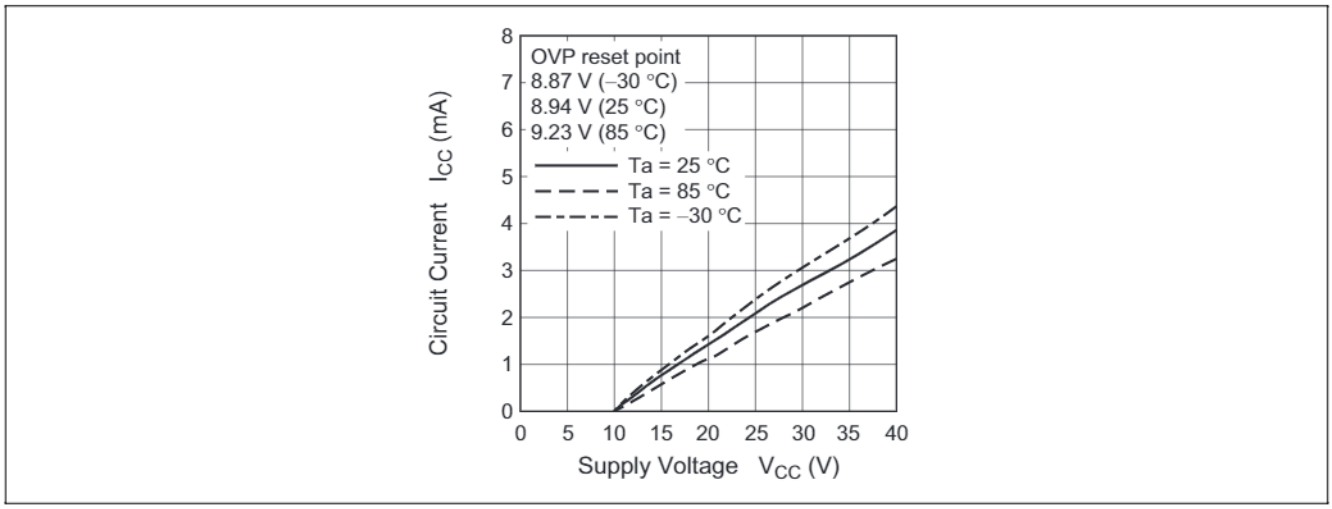


Figure 14 Circuit Current vs. Supply Voltage (OVP Operation)

Output Section

It is required that the output circuit have the high sink and source abilities for MOS FET drive. It is well known that the "totempole circuit has high sink and source ability. However, it has the demerit of high through current.

For example, the through current may reach such the high current level of 1 A, if type M51996A has the "conventional" totempole circuit. For the high frequency application such as higher than 100 kHz, this through current is very important factor and will cause not only the large I_{CC} current and the inevitable heat-up of IC but also the noise voltage.

This IC uses the improved totempole circuit, so without deteriorating the characteristic of operating speed, its through current is approximately 100 mA.

Application Note of Type M51996AP/AFP

Design of Start-up Circuit and The Power Supply of IC

1. The start-up circuit when it is not necessary to set the start and stop input voltage

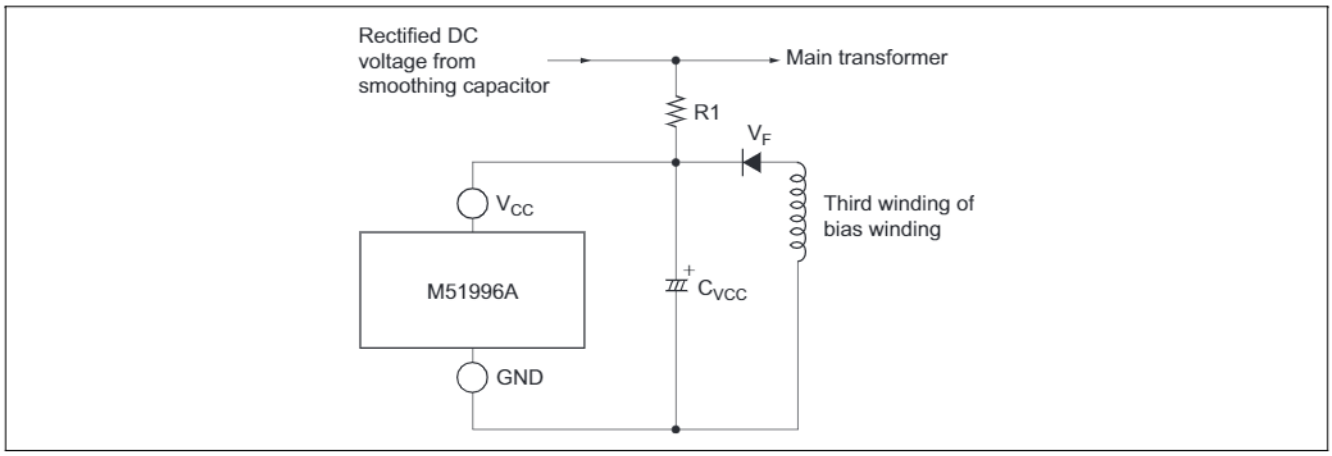


Figure 15 Start-up Circuit Diagram When it is Not Necessary to Set The Start and Stop Input Voltage

Figure 15 shows one of the example circuit diagram of the start-up circuit which is used when it is not necessary to set the start and stop voltage.

It is recommended that the current more than 300 ∝A flows through R1 in order to overcome the operation start-up current $I_{CC(START)}$ and C_{VCC} is in the range of 10 to 47 ∝F. The product of R1 by C_{VCC} causes the time delay of operation, so the response time will be long if the product is too much large.

Just after the start-up, the I_{CC} current is supplied from C_{VCC}, however, under the steady state condition, IC will be supplied from the third winding or bias winding of transformer, the winding ratio of the third winding must be designed so that the induced voltage may be higher than the operation-stop voltage $V_{CC(STOP)}$.

The V_{CC} voltage is recommended to be 12 V to 17 V as the normal and optimum gate voltage is 10 to 15 V and the output voltage (V_{OH}) of type M51996AP/AFP is about (V_{CC} − 2 V).

It is not necessary that the induced voltage is settled higher than the operation start-up voltage $V_{CC(START)}$, and the high gate drive voltage causes high gate dissipation, on the other hand, too low gate drive voltage does not make the MOS FET fully on-state or the saturation state.

2. The start-up circuit when it is not necessary to set the start and stop input voltage

It is recommend to use the third winding of "forward winding" or "positive polarity" as shown in figure 16, when the DC source voltages at both the IC operation start and stop must be settled at the specified values.

The input voltage ($V_{IN(START)}$), at which the IC operation starts, is decided by R1 and R2 utilizing the low start-up current characteristics of type M51996AP/AFP.

The input voltage ($V_{IN(STOP)}$), at which the IC operation stops, is decided by the ratio of third winding of transformer.

The $V_{IN(START)}$ and $V_{IN(STOP)}$ are given by following equations.

$$V_{IN\ (START)} \approx R1 \times I_{CCL} + \left(\frac{R1}{R2} + 1\right) \times V_{CC\ (START)} \quad \cdots\cdots\cdots \quad (7)$$

$$V_{IN\ (STOP)} \approx (V_{CC\ (STOP)} - V_F) \times \frac{N_P}{N_B} + \frac{1}{2} V'_{IN\ RIP\ (P\text{-}P)} \quad \cdots\cdots \quad (8)$$

Where

I_{CCL} is the operation start-up current of IC
$V_{CC(START)}$ is the operation start-up voltage of IC
$V_{CC(STOP)}$ is the operation stop voltage of IC
V_F is the forward voltage of rectifier diode
$V'_{IN(P\text{-}P)}$ is the peak to peak ripple voltage of

$$V_{CC}\ \text{terminal} \approx \frac{N_B}{N_P} V'_{IN\ RIP\ (P\text{-}P)}$$

It is required that the $V_{IN(START)}$ must be higher than $V_{IN(STOP)}$.

When the third winding is the "fly back winding" or "reverse polarity", the $V_{IN(START)}$ can be fixed, however, $V_{IN(STOP)}$ can not be settled by this system, so the auxiliary circuit is required.

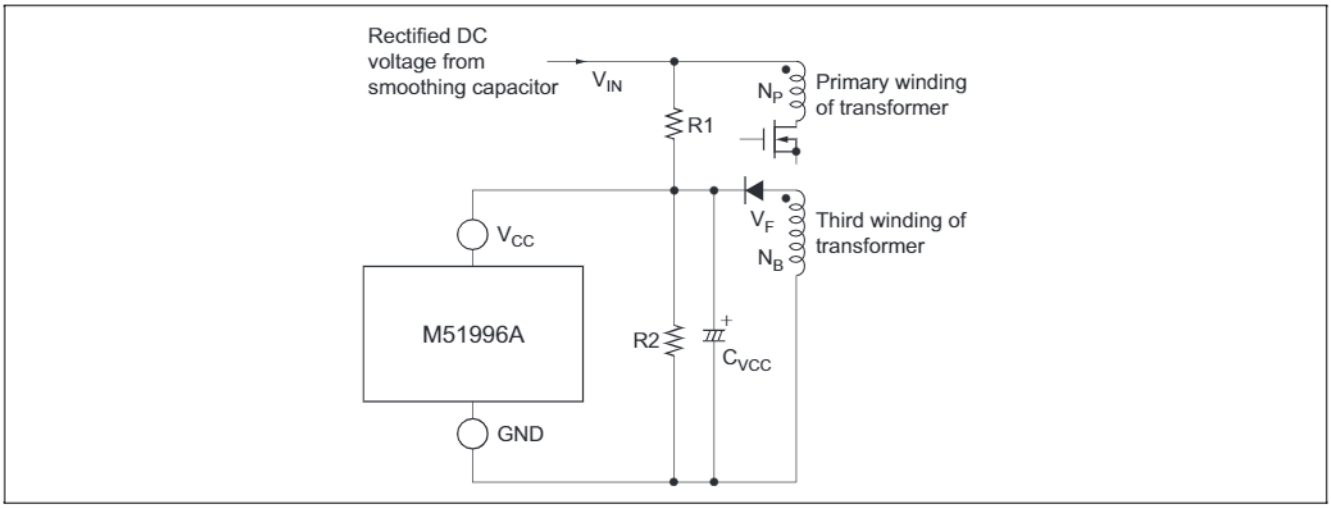


Figure 16 Start-up Circuit Diagram When It is Not Necessary to Set The Start and Stop Input Voltage

3. Notice to the V_{CC}, V_{CC} line and GND line

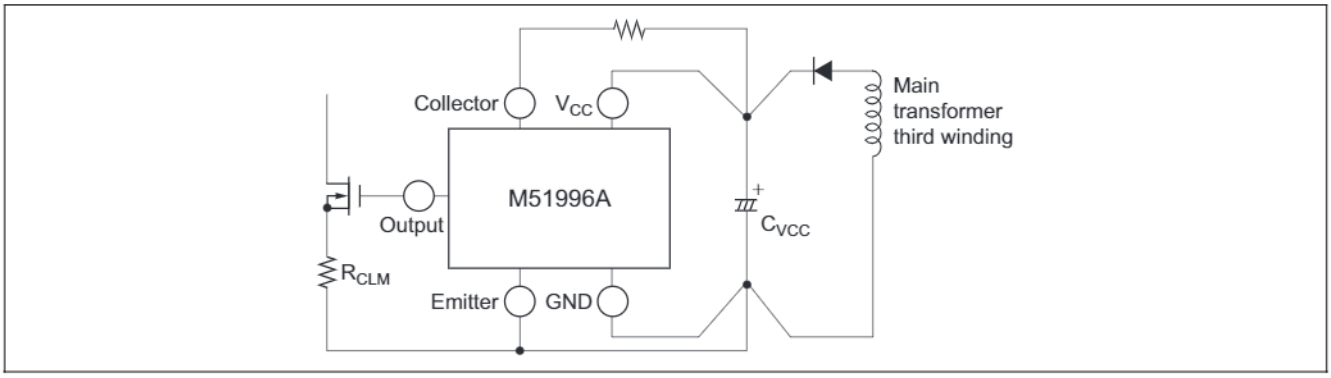


Figure 17 How to Design The Conductor-pattern of Type M51996A on PC Board (schematic example)

To avoid the abnormal IC operation, it is recommended to design the V_{CC} is not vary abruptly and has few spike voltage, which is induced from the stray capacity between the winding of main transformer.
To reduce the spike voltage, the C_{VCC}, which is connected between V_{CC} and ground, must have the good high frequency characteristics.
To design the conductor-pattern on PC board, following cautions must be considered as shown in figure 17.
(1) To separate the emitter line of type M51996A from the GND line of the IC
(2) The locate the C_{VCC} as near as possible to type M51996A and connect directly
(3) To separate the collector line of type M51996A from the V_{CC} line of the IC
(4) To connect the ground terminals of peripheral parts of ICs to GND of type M51996A as short as possible

4. Power supply circuit for easy start-up

When IC start to operate, the voltage of the C_{VCC} begins to decrease till the C_{VCC} becomes to be charged from the third winding of main-transformer as the I_{CC} of the IC increases abruptly. In case shown in figure 15 and 16, some "unstable start-up" or "fall to start-up" may happen, as the charging interval of C_{VCC} is very short duration; that is the charging does occur only the duration while the induced winding voltage is higher than the C_{VCC} voltage, if the induced winding voltage is nearly equal to the "operation-stop voltage" of type M51996A.

It is recommended to use the 10 to 47 ∝F for C_{VCC1}, and about 5 times capacity bigger than C_{VCC1} for C_{VCC2}.

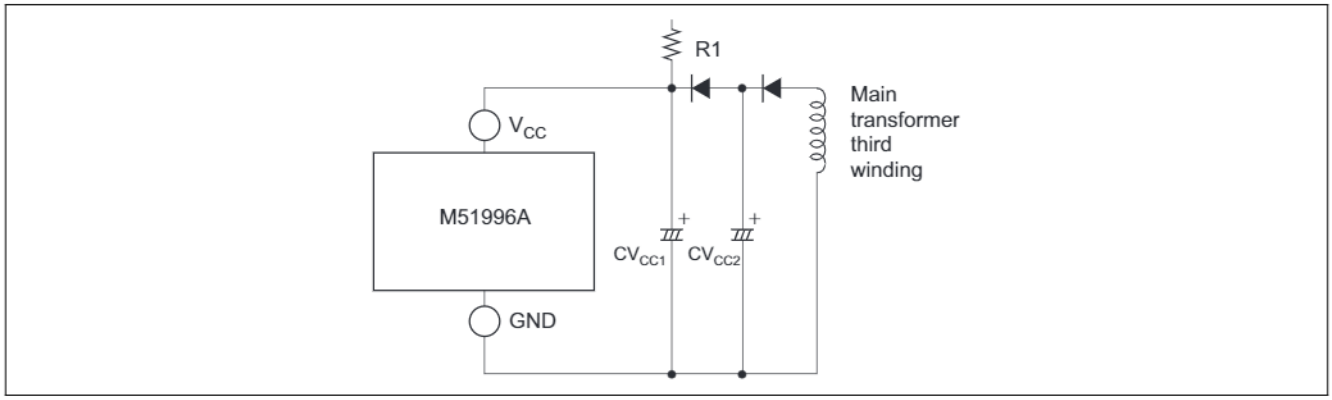


Figure 18 DC Source Circuit for Stable Start-up

OVP Circuit

1. To avoid the miss operation of OVP
   It is recommended to connect the capacitor between OVP terminal and GND for avoiding the miss operation by the spike noise.
   The OVP terminal is connected with the sink current source (≈ 150 ∝A) in IC when OVP does not operate, for absorbing the leak current of the photo coupler in the application.
   So the resistance between the OVP terminal and GND for leak-cut is not necessary.
   If the resistance is connected, the supply current at the OVP reset supply voltage becomes large.
   As the result, the OVP reset supply voltage may become higher than the operation stop voltage.
   In that case, the OVP action is reset when the OVP is triggered at the supply voltage a little high than the operation stop voltage.
   So it should be avoided absolutely to connect the resistance between the OVP terminal and GND.

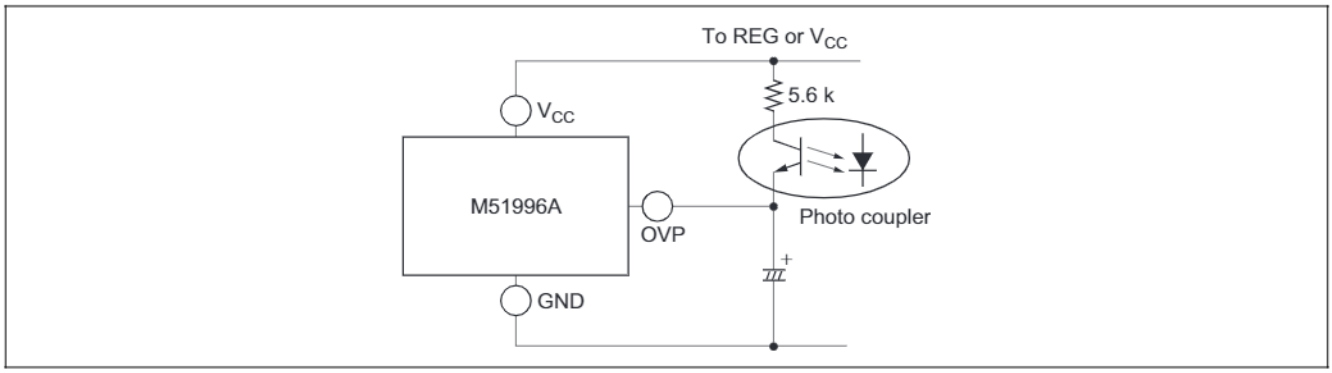


Figure 19 Peripheral Circuit of OVP Terminal

2. Application circuit to make the OVP-reset time fast
   The reset time may becomes problem when the discharge time constant of C_{FIN} • (R1 + R2) is long. Under such the circuit condition, it is recommend to discharge the C_{VCC} forcedly and to make the V_{CC} low value; This makes the OVP-reset time fast.

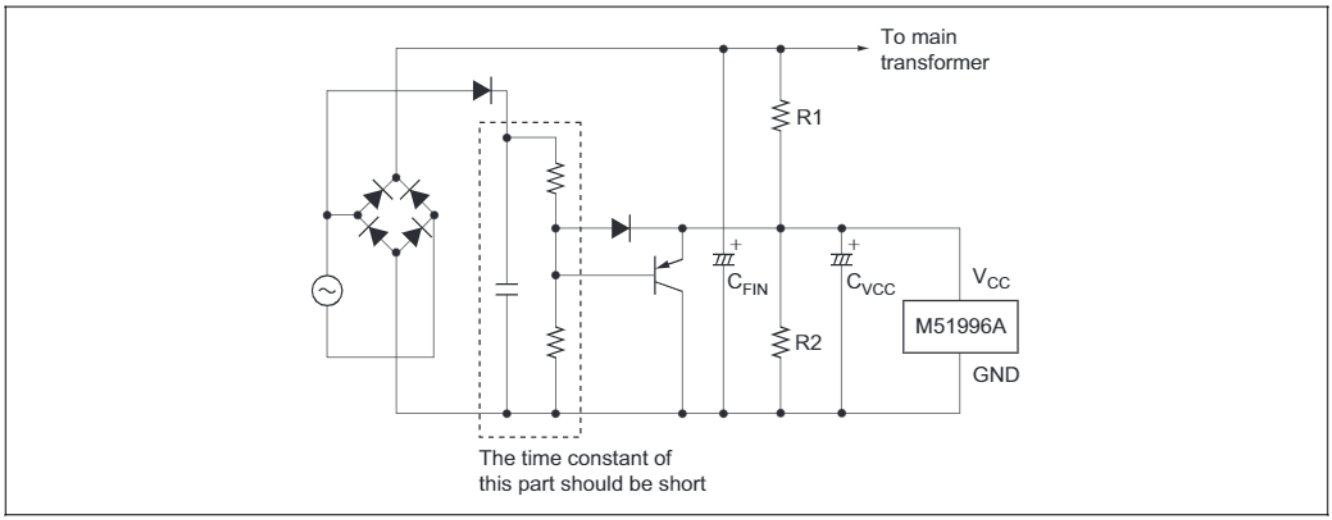


Figure 20 Example Circuit Diagram to Make The OVP-reset-time Fast

3. OVP setting method using the induced third winding voltage on fly back system
   For the over voltage protection (OVP), the induced fly back type third winding voltage can be utilized, as the induced third winding voltage depends on the output voltage. Figure 21 shows one of the example circuit diagram.

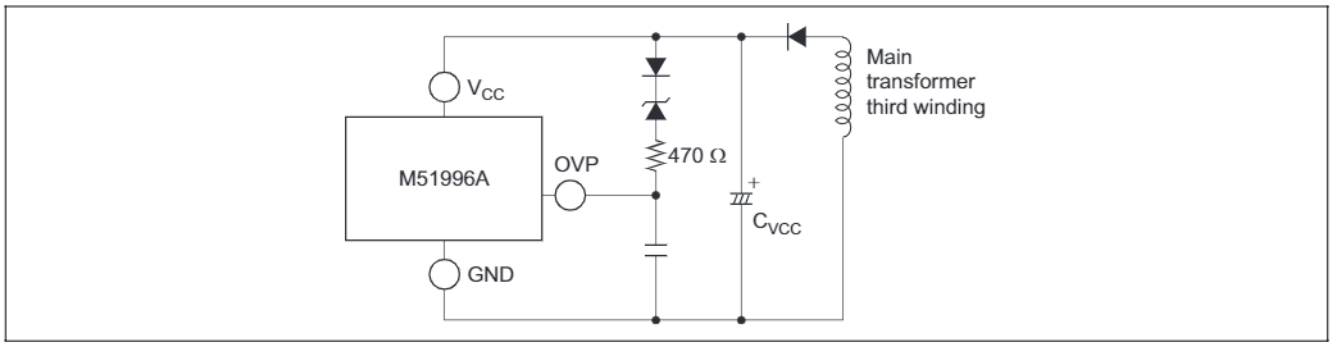


Figure 21 OVP Setting Method Using The Induced Third Winding Voltage on Fly Back System

4. Method to control for ON/OFF using the OVP terminal
   You can reset OVP to lower the OVP terminal voltage lower than V_{THOVPL}.
   So you can control for ON/OFF using this nature.
   The application is shown in figure 22.
   The circuit turns off by SW OFF and turns on by SW ON in this application.
   Of course you can make use of the transistor or photo-transistor instead of SW.

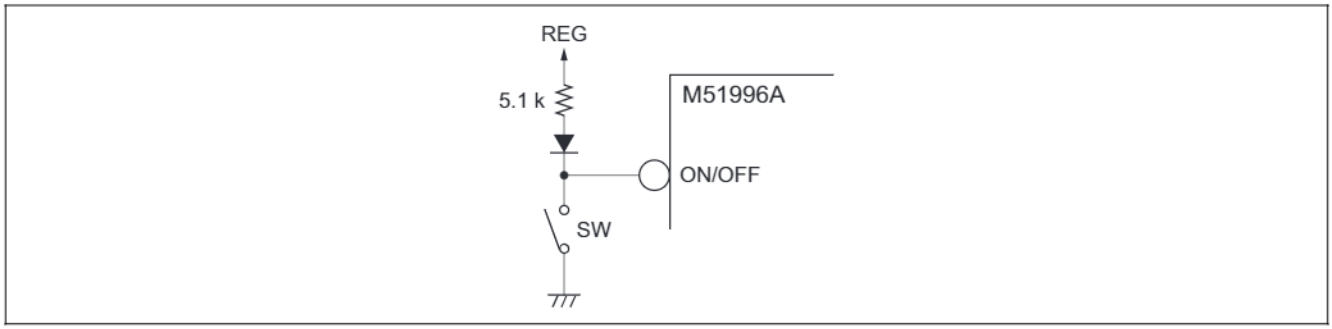


Figure 22 Method to Control for ON/OFF Using The OVP Terminal

Current Limiting Circuit

1. Peripheral circuit of CLM+ terminal

   Figure 23 shows the example circuit diagrams around the CLM+ terminal. It is required to connect the low pass filter, in order to reduce the spike current component, as the main current or drain current contains the spike current especially during the turn-on duration of MOS FET.

   1,000 pF to 22,000 pF is recommended for C_{NF} and the R_{NF1} and R_{NF2} have the function both to adjust the "current-detecting-sensitivity" and to consist the low pass filter.

   To design the R_{NF1} and R_{NF2}, it is required to consider the influence of CLM+ terminal source current (I_{INCLM+}), which value is in the range of 90 to 270 ∝A.

   In order to be not influenced from these resistor paralleled value of R_{NF1} and R_{NF2}, (R_{NF1}//R_{NF2}) is recommended to be less than 100 Ω.

   The R_{CLM} should be the non-inductive resistor.

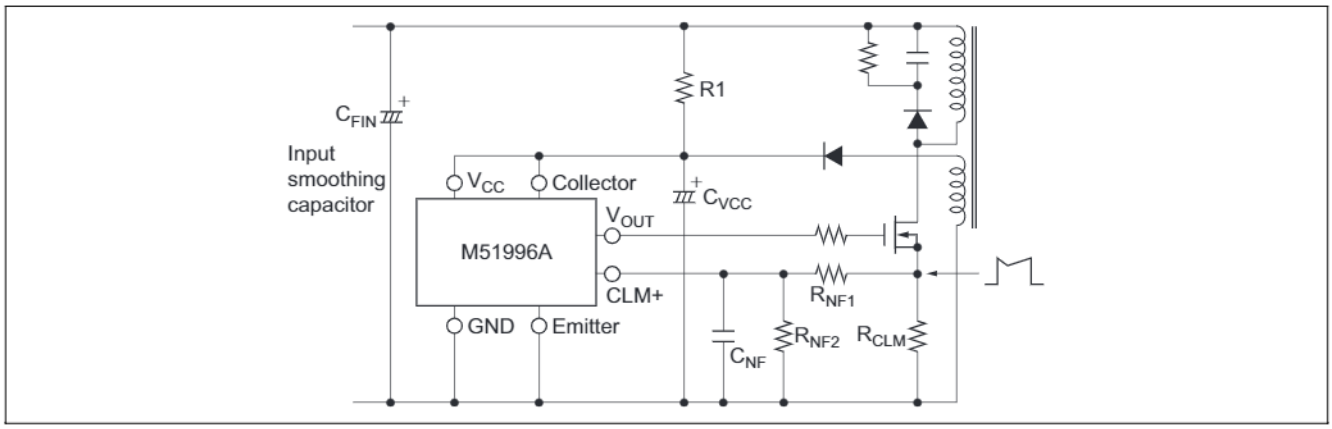


Figure 23 Peripheral Circuit Diagram of CLM+ Terminal

2. Over current limiting curve

   (1) In case of feed forward system

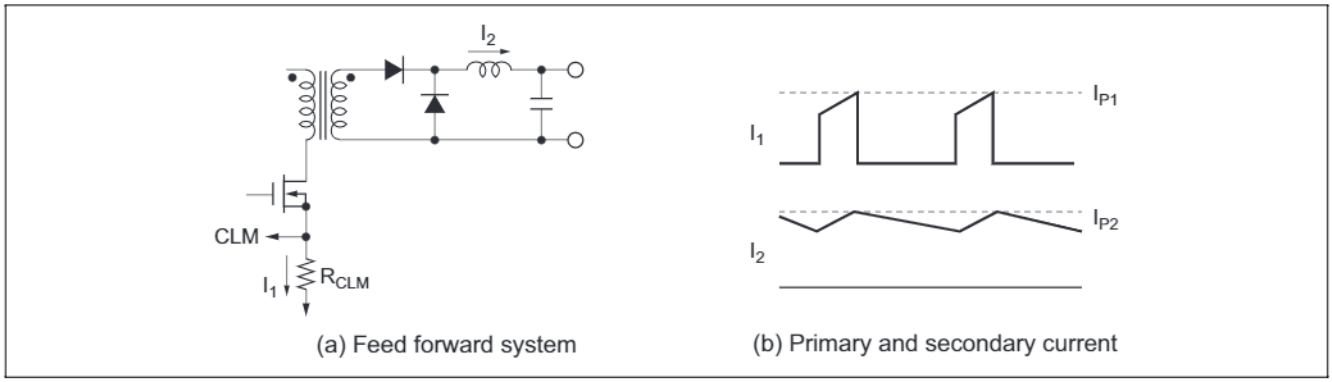


Figure 24 Primary and Secondary Current Waveforms Under The Current Limiting Operation Condition on Feed Forward System

Figure 24 shows the primary and secondary current wave-forms under the current limiting operation.

At the typical application of pulse by pulse primary current detecting circuit, the secondary current depends on the primary current. As the peak value of secondary current is limited to specified value, the characteristics curve of output voltage versus output current become to the one as shown in figure 25.

The demerit of the pulse by pulse current limiting system is that the output pulse width can not reduce to less than some value because of the delay time of low pass filter connected to the CLM+ terminal and propagation delay time T_{PDCLM} from CLM+ terminal to output terminal of type M51996A. The typical T_{PDCLM+} is 100 ns.

As the frequency becomes higher, the delay time must be shorter. And as the secondary output voltage becomes higher, the dynamic range of on-duty must be wider; it means that it is required to make the on-duration much more narrower.

So this system has the demerit at the higher oscillating frequency and higher output voltage applications.

To prevent that the SOFT terminal is used to lower the frequency when the curve starts to become vertical.

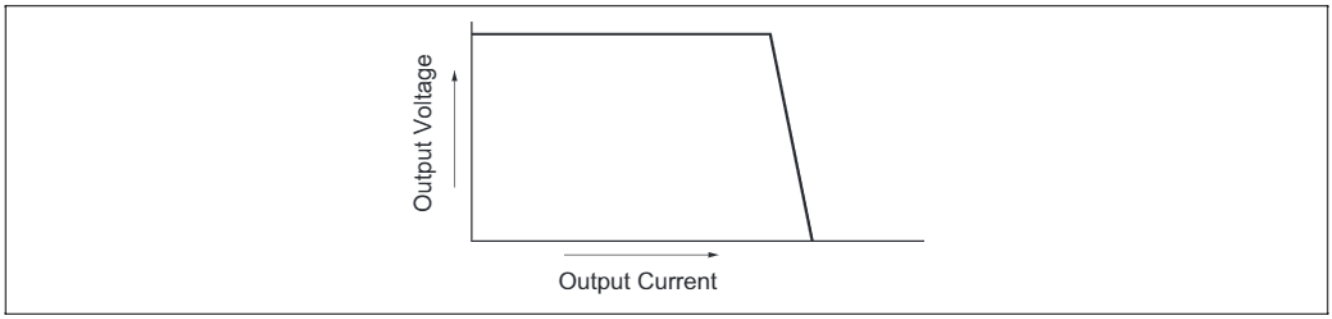


Figure 25 Over Current Limiting Curve on Feed Forward System

If the curve becomes vertical because of an excess current, the output voltage is lowered and no feedback current flows from feedback photo-coupler; the PWM comparator operates to enlarge the duty sufficiently, but the signal from the CLM+ section operates to make the pulse width narrower.

Under the condition in which I2 in figure 24 does not become 0, the output voltage is proportional to the product of the input voltage V_{IN} (primary side voltage of the main transformer) and on duty. If the bias winding is positive, V_{CC} is approximately proportional to V_{IN}. The existence of feed back current of the photo-coupler is known by measuring the F/B terminal voltage which becomes less than $2V_{BE}$ in the internal circuit of REG terminal and F/B terminal if the output current flows from the F/B terminal.

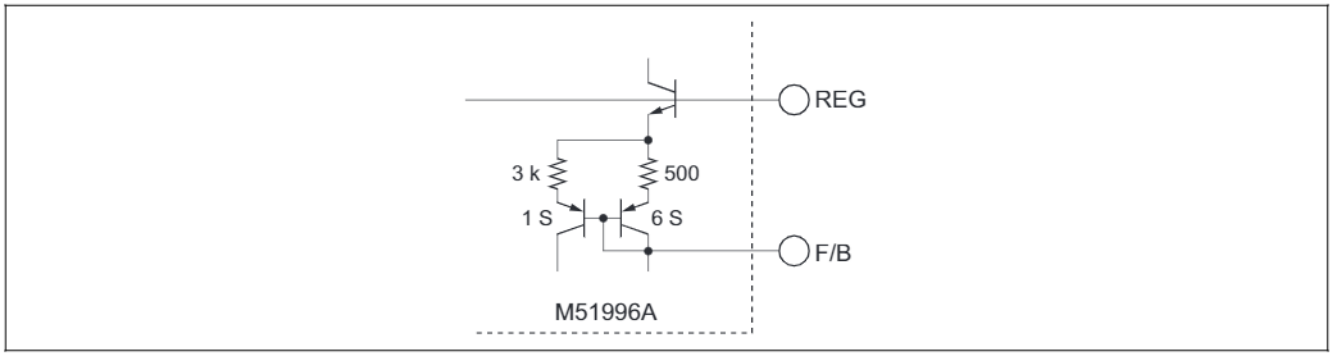


Figure 26 Relationship Between REG Terminal and F/B Terminal

Figure 27 shows an application example.

Q1 is turned on when normal output voltage is controlled at a certain value. The SOFT terminal is clamped to a high-level voltage. If the output voltage decreases and the curve starts to drop, no feed back current flows, Q1 is turned off and the SOFT terminal responds to the smoothed output voltage.

It is recommended to use an R1 and R2 of 10 kΩ to 30 kΩ. An R3 of 20 to 100 kΩ and C of 1000 pF to 8200 pF should be used.

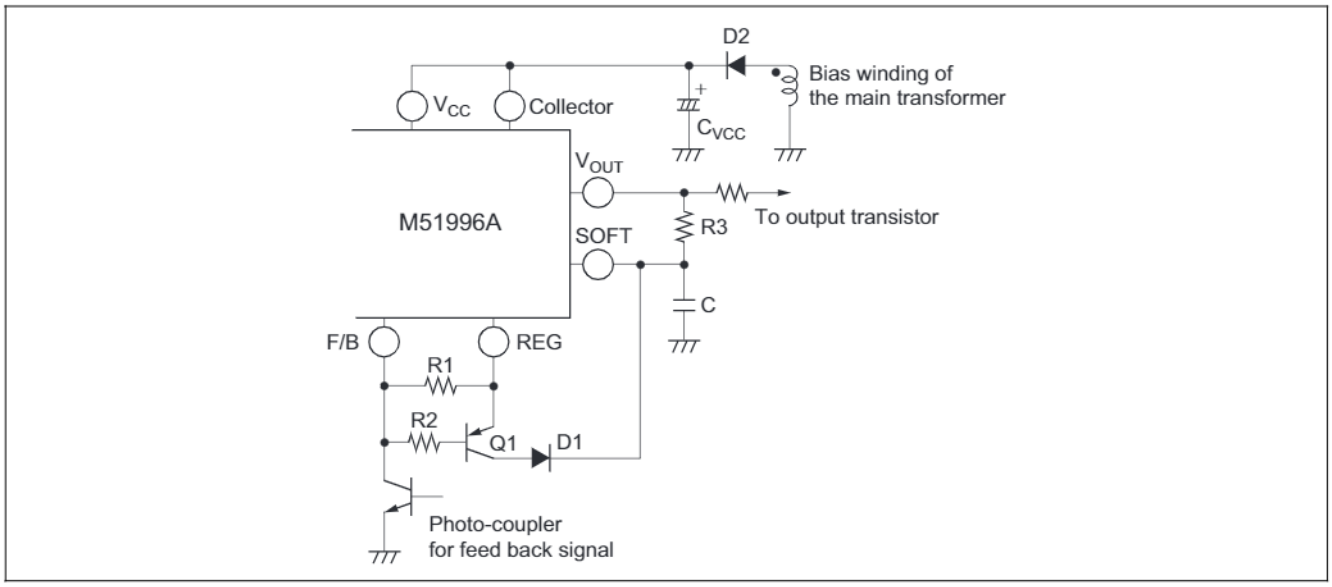


Figure 27 Current to Lower Frequency During Over Current

To change the knee point of frequency drop, use the circuit in figure 28.

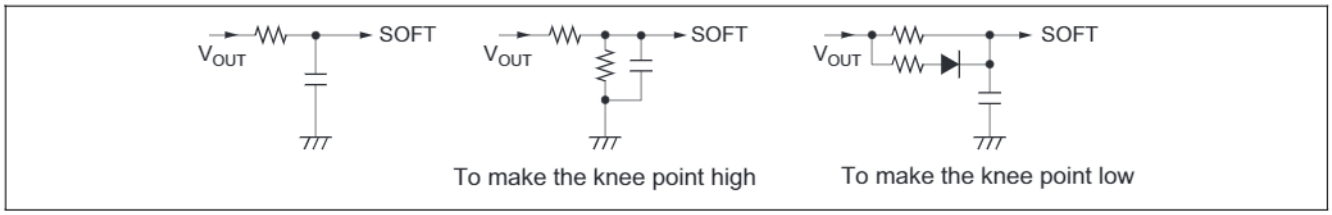


Figure 28 Method to Control The Knee Point of Frequency Drop

To have a normal SOFT start function in the circuit in figure 27, use the circuit in figure 29. It is recommended to use an R4 of 10 kΩ.

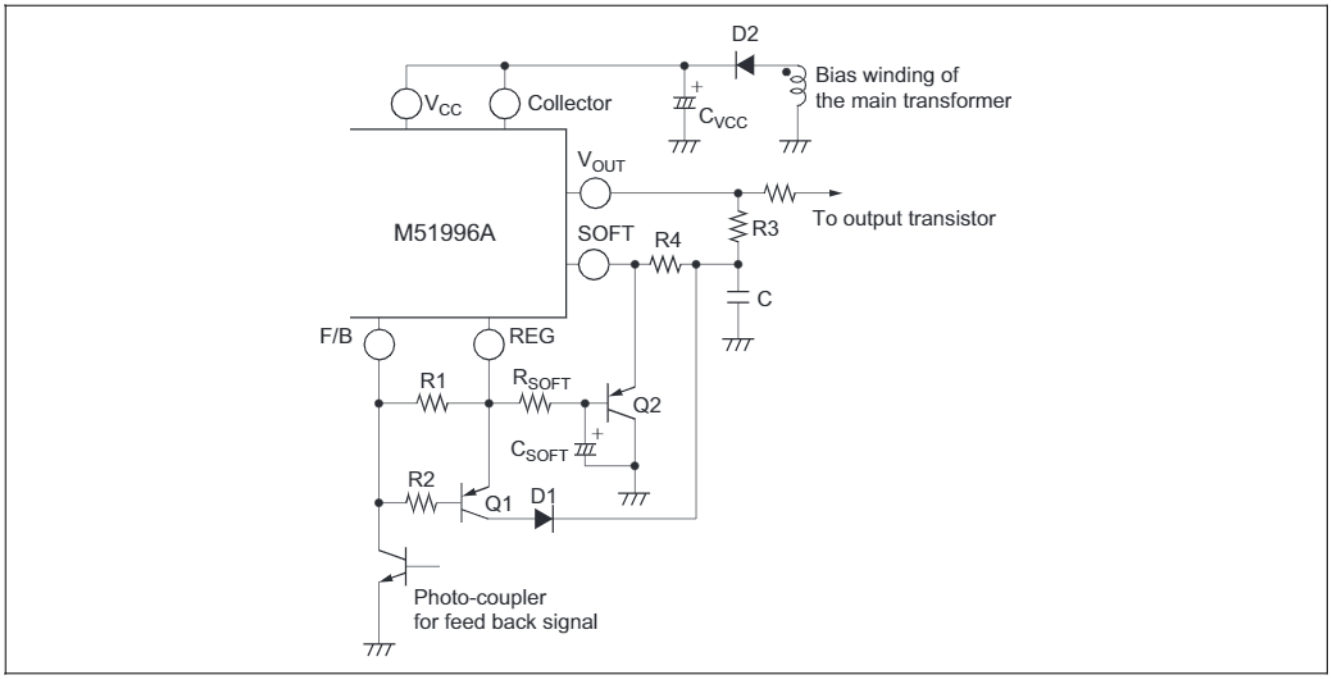


Figure 29 Circuit to Use Frequency Drop During The Over Current and Normal Soft Start

(2) In case of fly back system

The DC output voltage of SMPS depends on the V_{CC} voltage of type M51996A when the polarity of the third winding is negative and the system is fly back. So the operation of type M51996A will stop when the V_{CC} becomes lower than "Operation-stop voltage" of M51996A when the DC output voltage of SMPS decreases under specified value at over load condition.

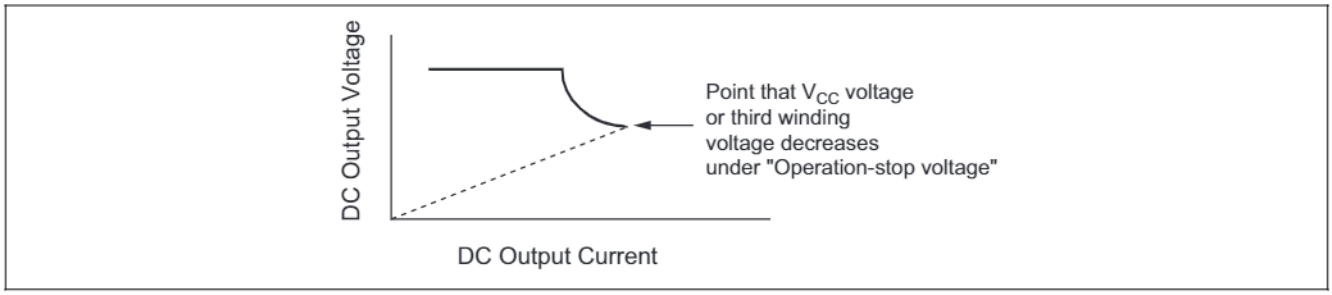


Figure 30 Over Current Limiting Curve on Fly Back System

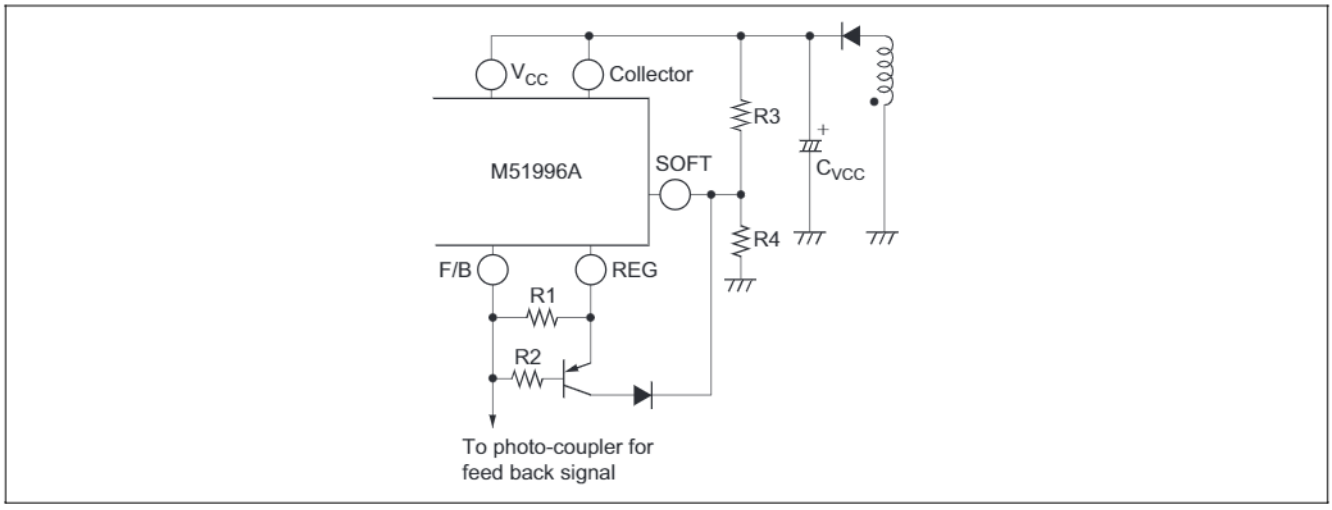


Figure 31 Current to Lower The Frequency During The Over Current in The Fly Back System

However, the M51996A will non-operate and operate intermittently, as the V_{CC} voltage rises in accordance with the decrease of I_{CC} current.

The fly back system has the constant output power characteristics as shown in figure 30 when the peak primary current and the operating frequency are constant.

To avoid an increases of the output current, the frequency is lowered when the DC output voltage of SMPS starts to drop using the SOFT terminal. V_{CC} is divided and is input to the SOFT terminal as shown in figure 31, because the voltage in proportional to the output voltage is obtained from the bias winding. In this application example, the current flowing to R3 added to the start-up current. So please use high resistance or 100 kΩ to 200 kΩ for R3.

The start-up current is not affected by R3 if R3 is connected to $C_{VCC}2$ in the circuit shown in figure 18.

Output Circuit

1. The output terminal characteristics at the V_{CC} voltage lower than the "Operation-stop" voltage
   The output terminal has the current sink ability even though the V_{CC} voltage lower than the "Operation-stop" voltage or $V_{CC(STOP)}$ (It means that the terminal is "Output low state" and please refer characteristics of output low voltage versus sink current.)
   This characteristics has the merit not to damage the MOS FET at the stop of operation when the V_{CC} voltage decreases lower than the voltage of $V_{CC(STOP)}$, as the gate charge of MOS FET, which shows the capacitive load characteristics to the output terminal, is drawn out rapidly.
   The output terminal has the draw-out ability above the V_{CC} voltage of 2 V, however, lower than the 2V, it loses the ability and the output terminal potential may rise due to the leakage current.
   In this case, it is recommended to connect the resistor of 100 kΩ between gate and source of MOS FET as shown in figure 32.

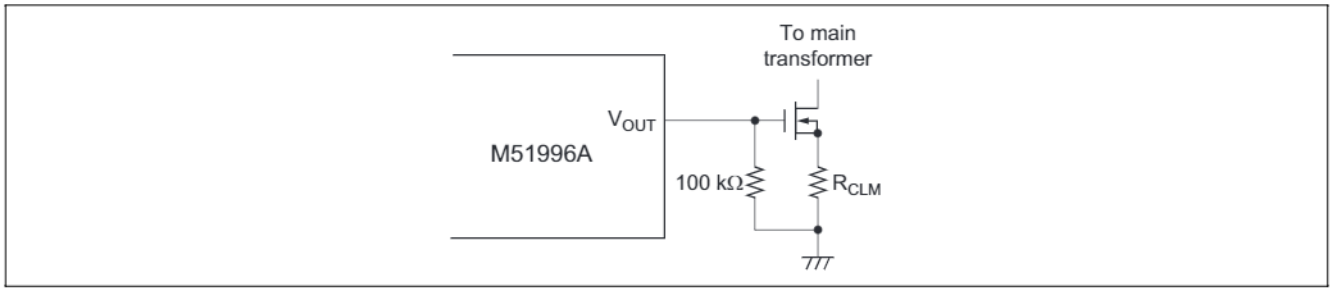


Figure 32 Circuit Diagram to Prevent The MOS-FET Gate potential Rising

2. MOS FET gate drive power dissipation
   Figure 33 shows the relation between the applied gate voltage and the stored gate charge.
   In the region 1, the charge is mainly stored at C_{GS} as the depletion is spread and C_{GD} is small owing to the off-state of MOS FET and the high drain voltage.
   In the region 2, the C_{GD} is multiplied by the "mirror effect" as the characteristics of MOS FET transfers from off-state to on-state.
   In the region 3, both the C_{GD} and C_{GS} affect to the characteristics as the MOS FET is on-state and the drain voltage is low.

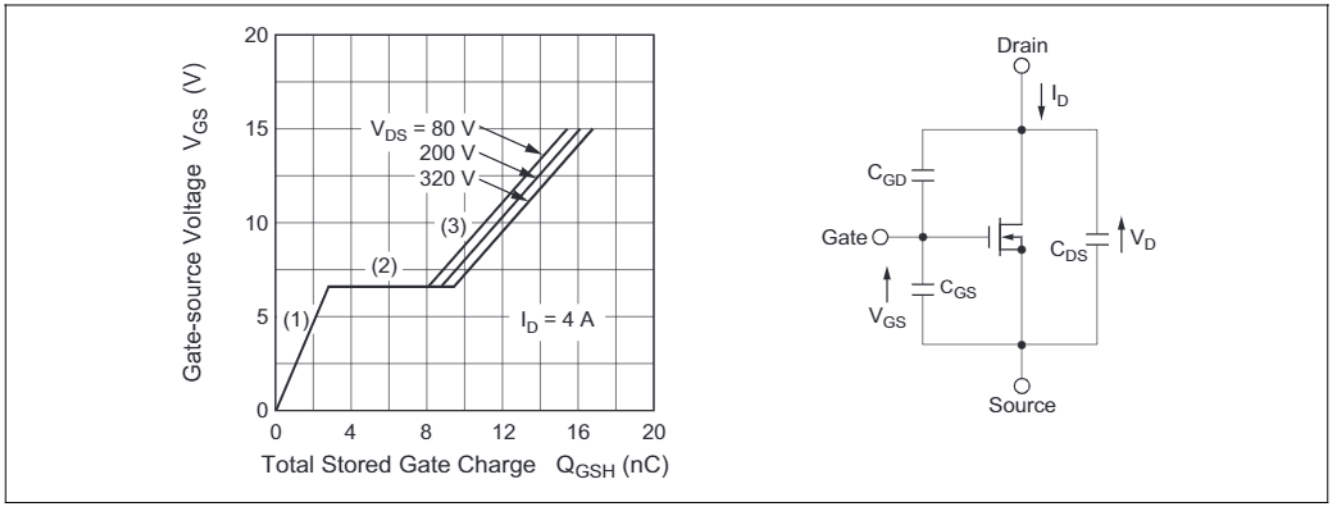


Figure 33 The Relation Between Applied Gate-source Voltage and Stored Gate Charge

The charging and discharging current caused by this gate charge makes the gate power dissipation. The relation between gate drive current I_D and total gate charge Q_{GSH} is shown by following equation;

$$I_D = Q_{GSH} \bullet f_{OSC} \quad \cdots\cdots (9)$$

Where

f_{OSC} is switching frequency

As the gate drive current may reach up to several tenths milliamperes at 500 kHz operation, depending on the size of MOS FET, the power dissipation caused by the gate current can not be neglected.
In this case, following action will be considered to avoid heat up of type M51996A.
(1) To attach the heat sink to type M51996A
(2) To use the printed circuit board with the good thermal conductivity
(3) To use the buffer circuit shown next section

3. Output buffer circuit
It is recommended to use the output buffer circuit as shown in figure 34, when type M51996A drives the large capacitive load or bipolar transistor.

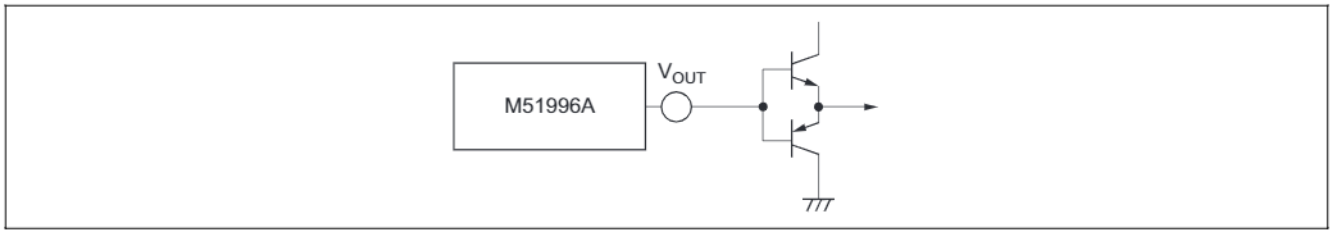


Figure 34 Output Buffer Circuit Diagram

DET Circuit

Figure 35 shows how to use the DET circuit for the voltage detector and error amplifier.

For the phase shift compensation, it is recommended to connected the CR network between DET terminal and F/B terminal.

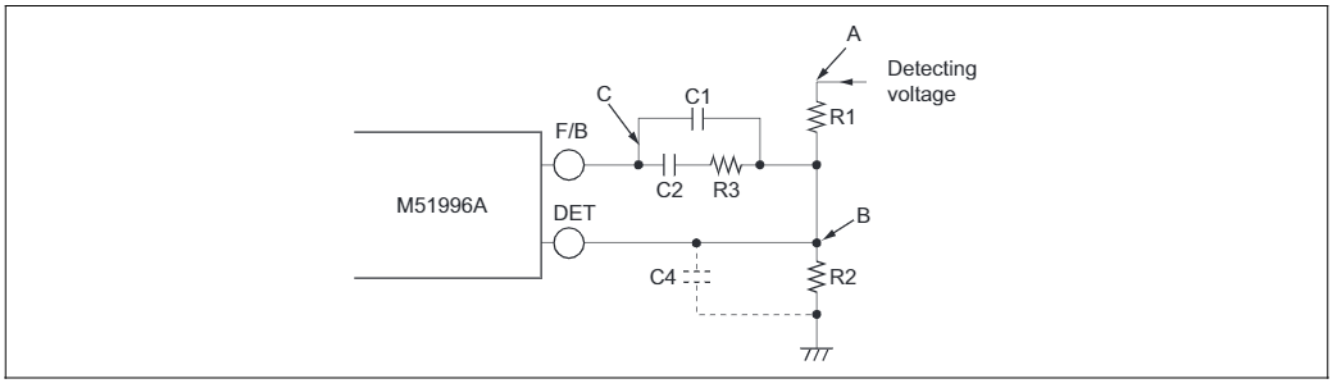


Figure 35 How to Use The DET Circuit for The Voltage Detector

Figure 36 shows the gain-frequency characteristics between point B and point C shown in figure 35.

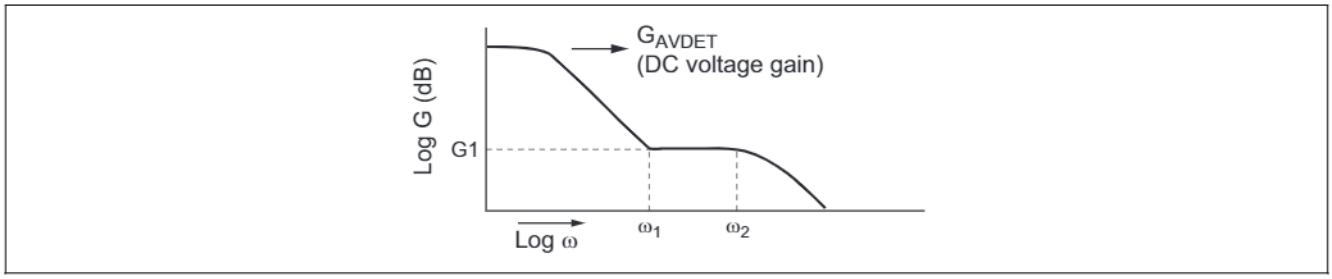


Figure 36 Gain-frequency Characteristics Between Point B and C Shown in Figure 35

The G1, ω1 and ω2 are given by following equations;

$$G1 = \frac{R3}{R1 / R2} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (10)$$

$$\omega_1 = \frac{1}{C2 \bullet R3} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (11)$$

$$\omega_2 = \frac{C1 + C2}{C1 \bullet C2 \bullet R3} \quad \cdots\cdots\cdots\cdots\cdots \quad (12)$$

At the start of the operation, there happen to be no output pulse due to F/B terminal current through C1 and C2, as the potential of F/B terminal rises sharply just after the start of the operation.

Not to lack the output pulse, is recommended to connect the capacitor C4 as shown by broken line.

Please take notice that the current flows through the R1 and R2 are superposed to $I_{CC(START)}$. Not to superpose, R1 is connected to C_{VCC2} as shown in figure 18.

How to Get The Narrow Pulse Width During The Start of Operation

Figure 37 shows how to get the narrow pulse width during the start of the operation. If the pulse train of forcedly narrowed pulse-width continues too long, the misstart of operation may happen, so it is recommended to make the output pulse width narrow only for a few pulse at the start of operation. 0.1 ∝F is recommended for the C.

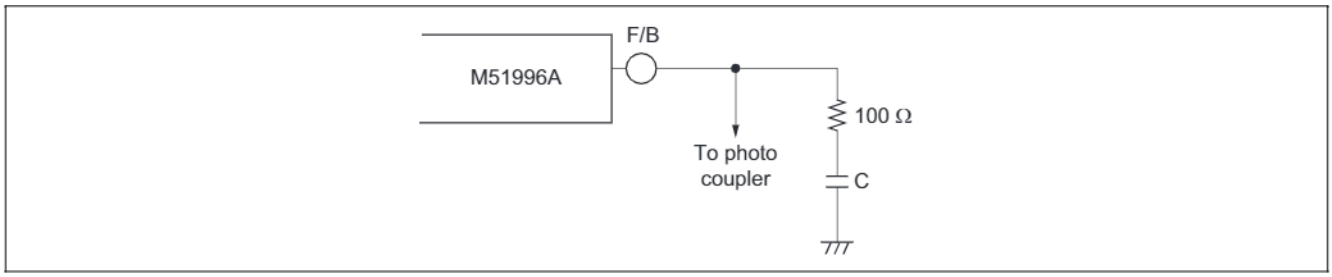


Figure 37 How to Get The Narrow Pulse Width During The Start of Operation

How to Synchronize with External Circuit

Type M51996A has no function to synchronize with external circuit, however, there is some application circuit for synchronization as shown in figure 38.

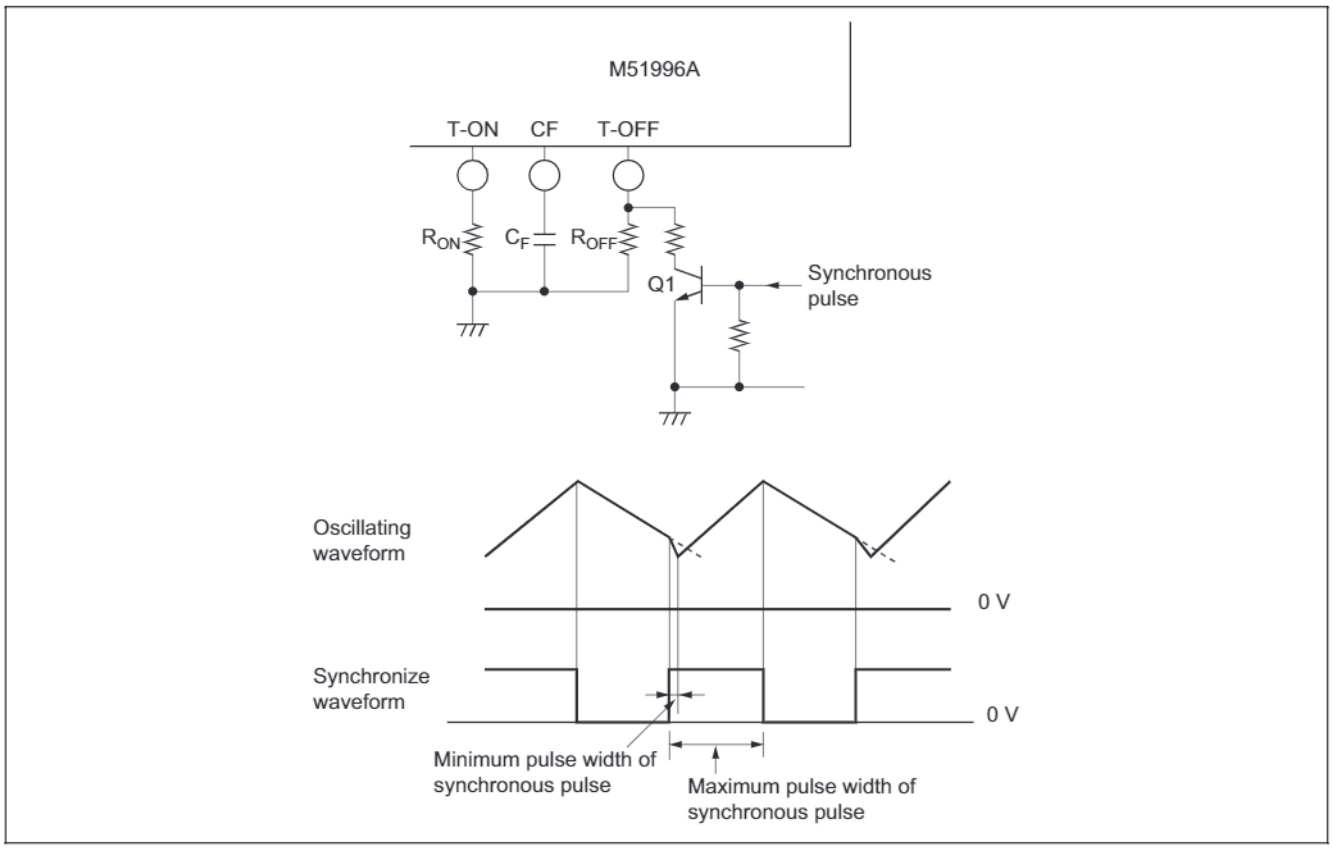


Figure 38 How to Synchronize With External Circuit

Driver Circuit for Bipolar Transistor

When the bipolar transistor is used instead of MOS FET, the base current of bipolar transistor must be sinked by the negative base voltage source for the switching-off duration, in order to make the switching speed of bipolar transistor fast one.

In this case, over current can not be detected by detecting resistor in series to bipolar transistor, so it is recommended to use the CT (current transformer).

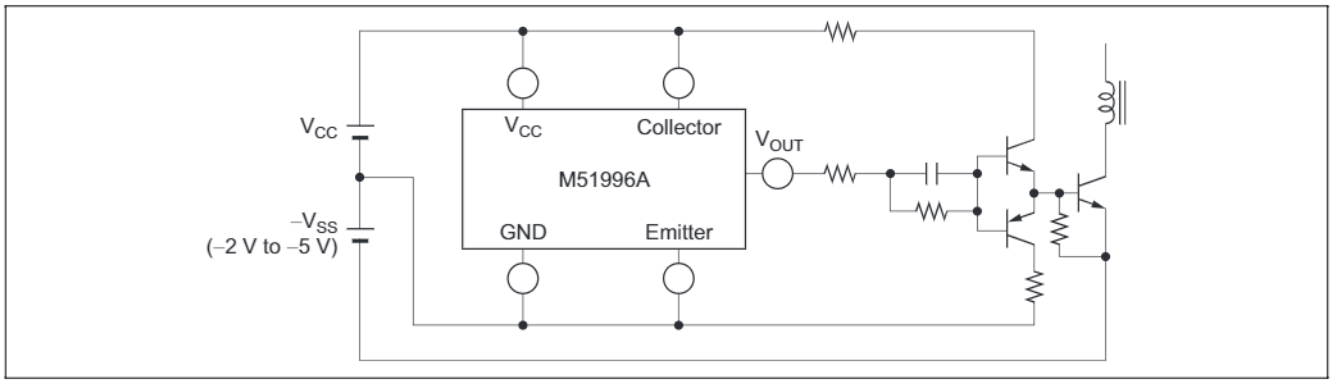


Figure 39 Driver Circuit Diagram (1) for Bipolar Transistor

For the low current rating transistor, type M51996A can drive it directly as shown in figure 40.

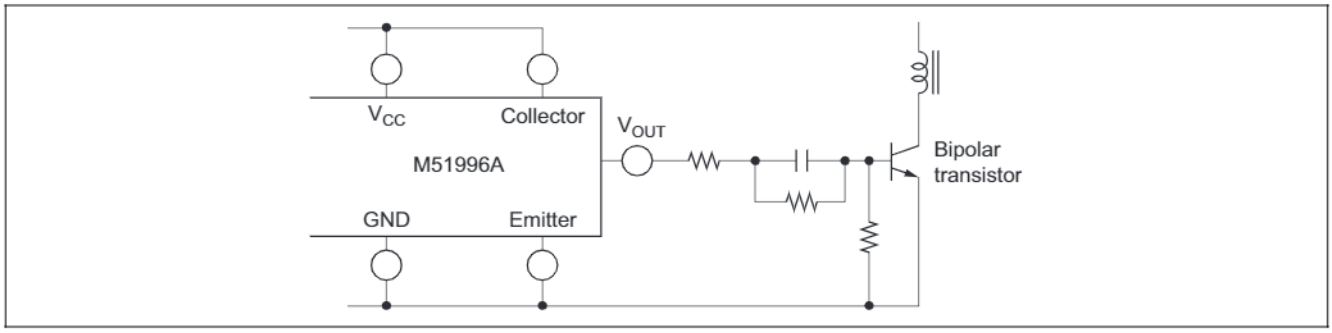


Figure 40 Driver Circuit Diagram (2) for Bipolar Transistor

Attention for Heat Generation

The maximum ambient temperature of type M51996A is +85°C, however the ambient temperature in vicinity of the IC is not uniform and varies place by place, as the amount of power dissipation is fearfully large and the power dissipation is generated locally in the switching regulator.

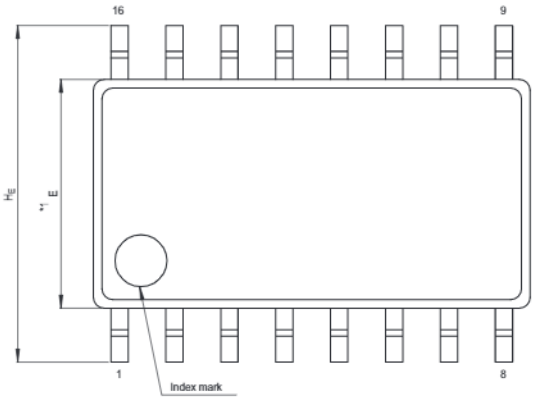
So it is one of the good idea to check the IC package temperature.

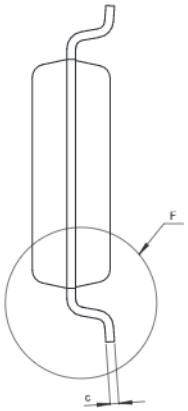
The temperature difference between IC junction and the surface of IC package is 15°C or less, when the IC junction temperature is measured by temperature dependency of forward voltage of pin junction, and IC package temperature is measured by "thermo-viewer", and also the IC is mounted on the “phenol-base” PC board in normal atmosphere.

So it is concluded that the maximum case temperature (surface temperature of IC) rating is 120°C with adequate margin.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.3x10.1-1.27	PRSP0016DE-A	16P2N-A	0.2g



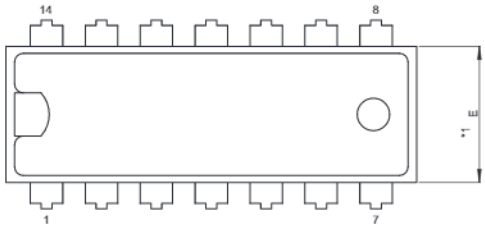


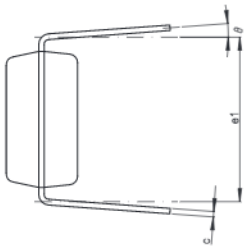


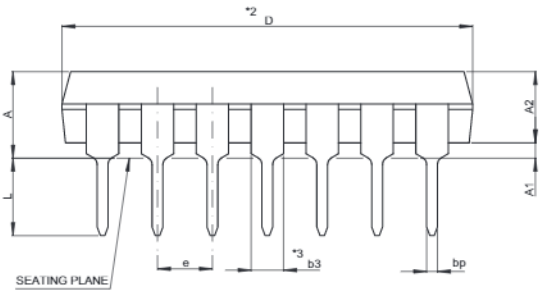
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19-2.54	PRDP0014AA-A	14P4	1.0g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

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