

ENC28J60
Data Sheet

Stand-Alone Ethernet Controller with SPI Interface

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ENC28J60

Stand-Alone Ethernet Controller with SPI Interface

Ethernet Controller Features

- IEEE 802.3 compatible Ethernet controller
- Integrated MAC and 10BASE-T PHY
- Supports one 10BASE-T port with automatic polarity detection and correction
- Supports Full and Half-Duplex modes
- Programmable automatic retransmit on collision
- Programmable padding and CRC generation
- Programmable automatic rejection of erroneous packets
- SPI Interface with clock speeds up to 20 MHz

Buffer

- 8-Kbyte transmit/receive packet dual port SRAM
- Configurable transmit/receive buffer size
- Hardware-managed circular receive FIFO
- Byte-wide random and sequential access with auto-increment
- Internal DMA for fast data movement
- Hardware assisted checksum calculation for various network protocols

Medium Access Controller (MAC) Features

- Supports Unicast, Multicast and Broadcast packets
- Programmable receive packet filtering and wake-up host on logical AND or OR of the following:
  - Unicast destination address
  - Multicast address
  - Broadcast address
  - Magic Packet™
  - Group destination addresses as defined by 64-bit hash table
  - Programmable pattern matching of up to 64 bytes at user-defined offset

Physical Layer (PHY) Features

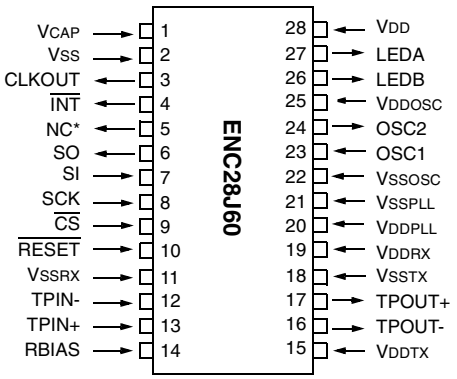
- Loopback mode
- Two programmable LED outputs for LINK, TX, RX, collision and full/half-duplex status

Operational

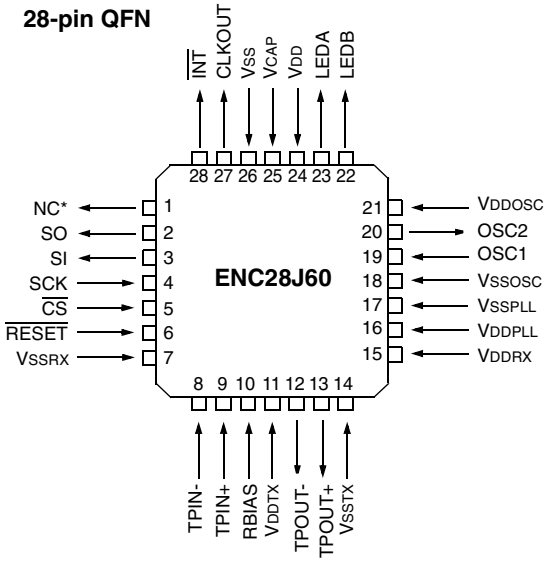
- Six interrupt sources and one interrupt output pin
- 25 MHz clock input requirement
- Clock out pin with programmable prescaler
- Operating voltage of 3.1V to 3.6V (3.3V typical)
- 5V tolerant inputs
- Temperature range: -40°C to +85°C Industrial, 0°C to +70°C Commercial (SSOP only)
- 28-pin SPDIP, SSOP, SOIC, QFN packages

Package Types

28-Pin SPDIP, SSOP, SOIC



28-pin QFN



* Reserved pin; always leave disconnected.

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1.0 OVERVIEW

The ENC28J60 is a stand-alone Ethernet controller with an industry standard Serial Peripheral Interface (SPI). It is designed to serve as an Ethernet network interface for any controller equipped with SPI.

The ENC28J60 meets all of the IEEE 802.3 specifications. It incorporates a number of packet filtering schemes to limit incoming packets. It also provides an internal DMA module for fast data throughput and hardware assisted checksum calculation, which is used in various network protocols. Communication with the host controller is implemented via an interrupt pin and the SPI, with clock rates of up to 20 MHz. Two dedicated pins are used for LED link and network activity indication.

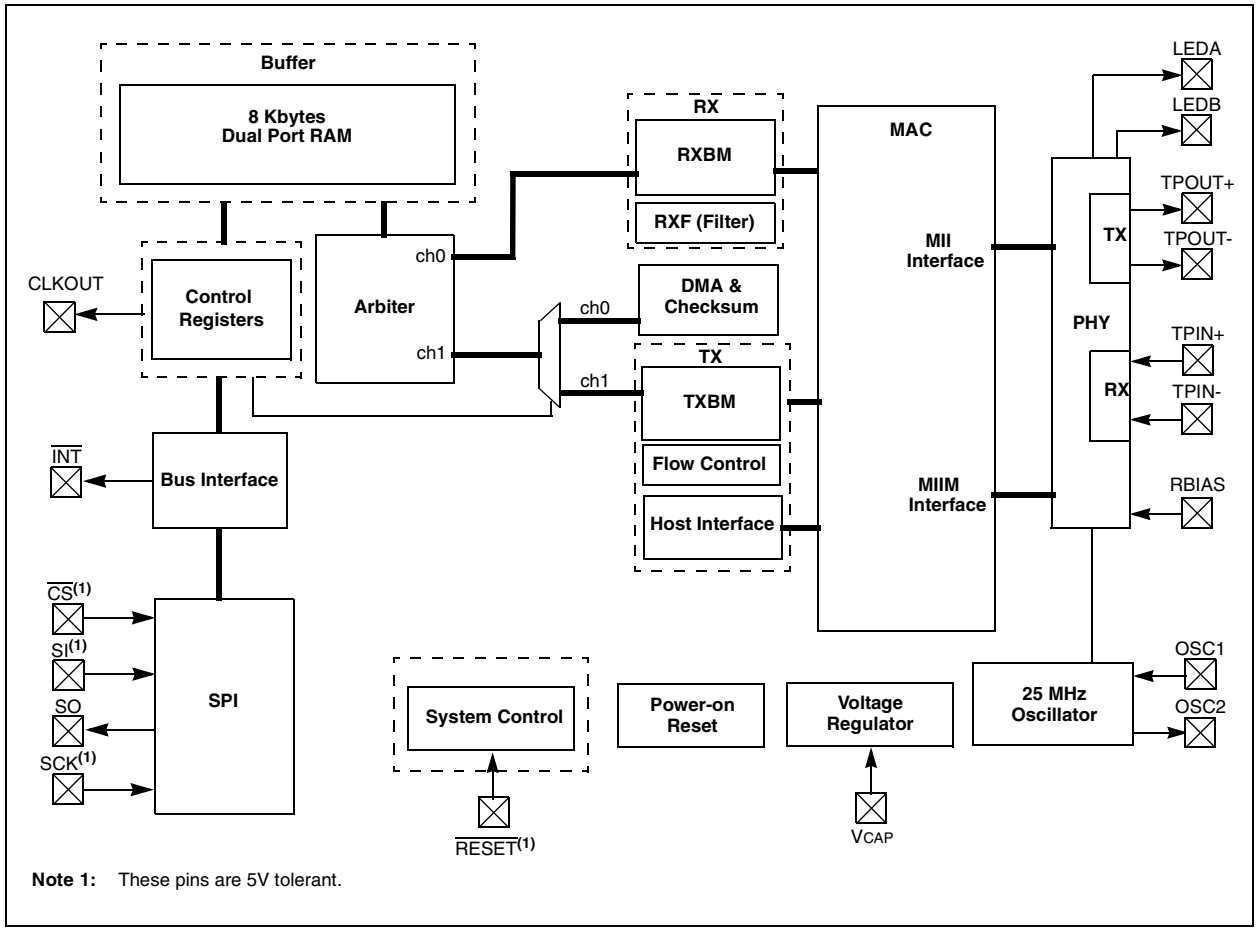
A simple block diagram of the ENC28J60 is shown in Figure 1-1. A typical application circuit using the device is shown in Figure 1-2. With the ENC28J60, two pulse transformers and a few passive components are all that is required to connect a microcontroller to an Ethernet network.

The ENC28J60 consists of seven major functional blocks:

1. An SPI interface that serves as a communication channel between the host controller and the ENC28J60.
2. Control Registers which are used to control and monitor the ENC28J60.
3. A dual port RAM buffer for received and transmitted data packets.
4. An arbiter to control the access to the RAM buffer when requests are made from DMA, transmit and receive blocks.
5. The bus interface that interprets data and commands received via the SPI interface.
6. The MAC (Medium Access Control) module that implements IEEE 802.3 compliant MAC logic.
7. The PHY (Physical Layer) module that encodes and decodes the analog data that is present on the twisted pair interface.

The device also contains other support blocks, such as the oscillator, on-chip voltage regulator, level translators to provide 5V tolerant I/Os and system control logic.

FIGURE 1-1: ENC28J60 BLOCK DIAGRAM



Note 1: These pins are 5V tolerant.

FIGURE 1-2: TYPICAL ENC28J60-BASED INTERFACE

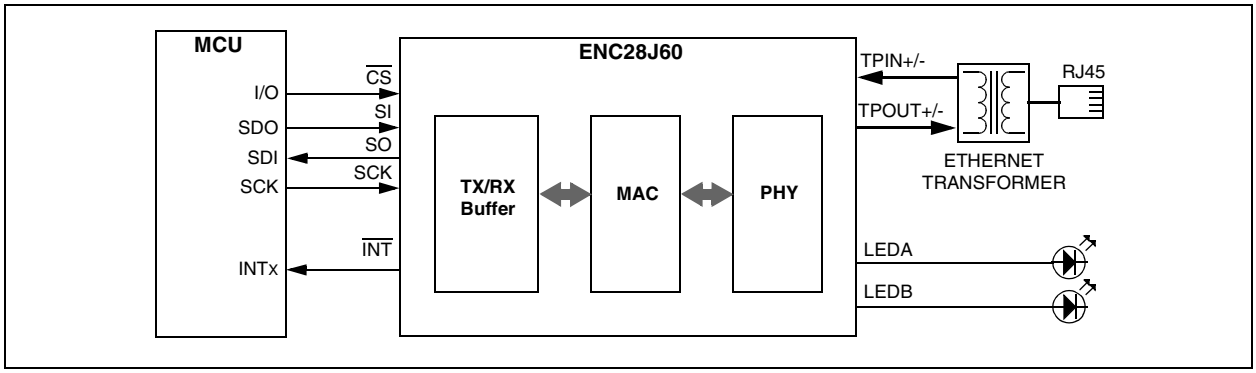


TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	SPDIP, SOIC, SSOP	QFN			
VCAP	1	25	P	—	2.5V output from internal regulator. A low Equivalent Series Resistance (ESR) capacitor, with a typical value of 10 µF and a minimum value of 1 µF to ground, must be placed on this pin.
VSS	2	26	P	—	Ground reference.
CLKOUT	3	27	O	—	Programmable clock output pin.(1)
$\overline{INT}$	4	28	O	—	$\overline{INT}$ interrupt output pin.(2)
NC	5	1	O	—	Reserved function; always leave unconnected.
SO	6	2	O	—	Data out pin for SPI interface.(2)
SI	7	3	I	ST	Data in pin for SPI interface.(3)
SCK	8	4	I	ST	Clock in pin for SPI interface.(3)
$\overline{CS}$	9	5	I	ST	Chip select input pin for SPI interface.(3,4)
$\overline{RESET}$	10	6	I	ST	Active-low device Reset input.(3, 4)
VSSRX	11	7	P	—	Ground reference for PHY RX.
TPIN-	12	8	I	ANA	Differential signal input.
TPIN+	13	9	I	ANA	Differential signal input.
RBIAS	14	10	I	ANA	Bias current pin for PHY. Must be tied to ground via a resistor (refer to **Section 2.4 "Magnetics, Termination and Other External Components"** for details).
VDDTX	15	11	P	—	Positive supply for PHY TX.
TPOUT-	16	12	O	—	Differential signal output.
TPOUT+	17	13	O	—	Differential signal output.
VSSTX	18	14	P	—	Ground reference for PHY TX.
VDDRX	19	15	P	—	Positive 3.3V supply for PHY RX.
VDDPLL	20	16	P	—	Positive 3.3V supply for PHY PLL.
VSSPLL	21	17	P	—	Ground reference for PHY PLL.
VSSOSC	22	18	P	—	Ground reference for oscillator.
OSC1	23	19	I	ANA	Oscillator input.
OSC2	24	20	O	—	Oscillator output.
VDDOSC	25	21	P	—	Positive 3.3V supply for oscillator.
LEDB	26	22	O	—	LEDB driver pin.(5)
LEDA	27	23	O	—	LEDA driver pin.(5)
VDD	28	24	P	—	Positive 3.3V supply.

Legend: I = Input, O = Output, P = Power, DIG = Digital input, ANA = Analog signal input, ST = Schmitt Trigger

Note 1: Pins have a maximum current capacity of 8 mA.

2: Pins have a maximum current capacity of 4 mA.

3: Pins are 5V tolerant.

4: Pins have an internal weak pull-up to VDD.

5: Pins have a maximum current capacity of 12 mA.

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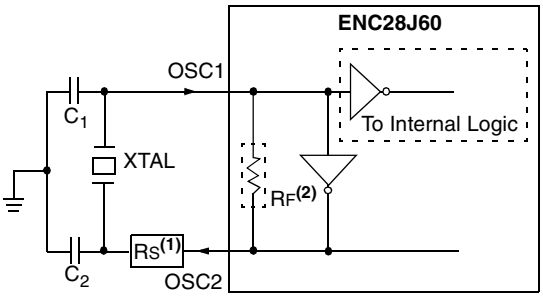
2.0 EXTERNAL CONNECTIONS

2.1 Oscillator

The ENC28J60 is designed to operate at 25 MHz with a crystal connected to the OSC1 and OSC2 pins. The ENC28J60 design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturer specifications. A typical oscillator circuit is shown in Figure 2-1.

The ENC28J60 may also be driven by an external clock source connected to the OSC1 pin as shown in Figure 2-2.

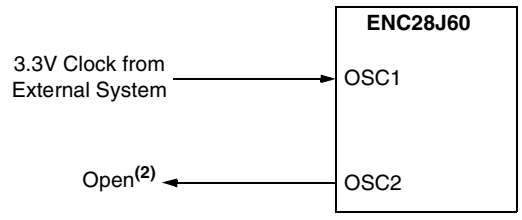
FIGURE 2-1: CRYSTAL OSCILLATOR OPERATION



Note 1: A series resistor, RS, may be required for AT strip cut crystals.

2: The feedback resistor, RF, is typically in the range of 2 to 10 MΩ.

FIGURE 2-2: EXTERNAL CLOCK SOURCE(1)



Note 1: Duty cycle restrictions must be observed.

2: A resistor to ground may be used to reduce system noise. This may increase system current.

2.2 Oscillator Start-up Timer

The ENC28J60 contains an Oscillator Start-up Timer (OST) to ensure that the oscillator and integrated PHY have stabilized before use. The OST does not expire until 7500 OSC1 clock cycles (300 μs) pass after Power-on Reset or wake-up from Power-Down mode occurs. During the delay, all Ethernet registers and buffer memory may still be read and written to through the SPI bus. However, software should not attempt to transmit any packets (set ECON1.TXRTS), enable reception of packets (set ECON1.RXEN) or access any MAC, MII or PHY registers during this period.

When the OST expires, the CLKRDY bit in the ESTAT register will be set. The application software should poll this bit as necessary to determine when normal device operation can begin.

Note: After a Power-on Reset, or the ENC28J60 is removed from Power-Down mode, the CLKRDY bit must be polled before transmitting packets, enabling packet reception or accessing any MAC, MII or PHY registers.

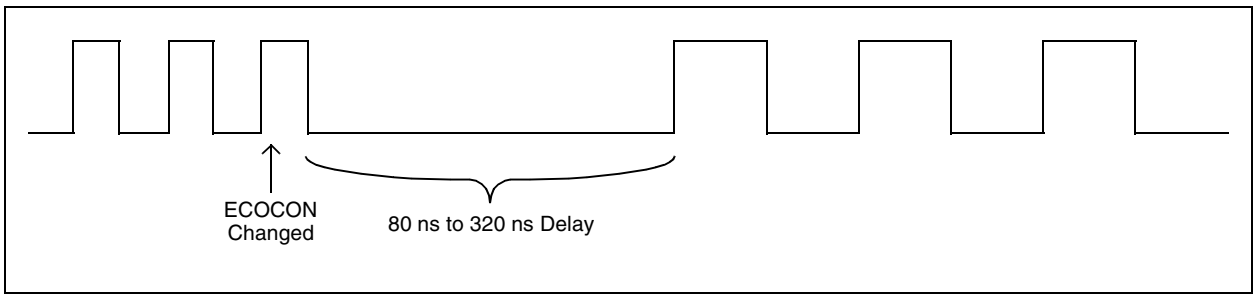
2.3 CLKOUT Pin

The clock out pin is provided to the system designer for use as the host controller clock or as a clock source for other devices in the system. The CLKOUT has an internal prescaler which can divide the output by 1, 2, 3, 4 or 8. The CLKOUT function is enabled and the prescaler is selected via the ECOCON register (Register 2-1).

To create a clean clock signal, the CLKOUT pin is held low for a period when power is first applied. After the Power-on Reset ends, the OST will begin counting. When the OST expires, the CLKOUT pin will begin outputting its default frequency of 6.25 MHz (main clock divided by 4). At any future time that the ENC28J60 is reset by software or the $\overline{\text{RESET}}$ pin, the CLKOUT function will not be altered (ECOCON will not change value). Additionally, Power-Down mode may be entered and the CLKOUT function will continue to operate. When Power-Down mode is cancelled, the OST will be reset but the CLKOUT function will continue. When the CLKOUT function is disabled (ECOCON = 0), the CLKOUT pin is driven low.

The CLKOUT function is designed to ensure that minimum timings are preserved when the CLKOUT pin function is enabled, disabled or the prescaler value is changed. No high or low pulses will be outputted which exceed the frequency specified by the ECOCON configuration. However, when switching frequencies, a delay between two and eight OSC1 clock periods will occur where no clock pulses will be produced (see Figure 2-3). During this period, CLKOUT will be held low.

FIGURE 2-3: CLKOUT TRANSITION



REGISTER 2-1: ECOCON: CLOCK OUTPUT CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	COCON2	COCON1	COCON0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **COCON2:COCON0**: Clock Output Configuration bits

11x = Reserved for factory test. Do not use. Glitch prevention not assured.
101 = CLKOUT outputs main clock divided by 8 (3.125 MHz)
100 = CLKOUT outputs main clock divided by 4 (6.25 MHz)
011 = CLKOUT outputs main clock divided by 3 (8.333333 MHz)
010 = CLKOUT outputs main clock divided by 2 (12.5 MHz)
001 = CLKOUT outputs main clock divided by 1 (25 MHz)
000 = CLKOUT is disabled. The pin is driven low.

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2.4 Magnetics, Termination and Other External Components

To complete the Ethernet interface, the ENC28J60 requires several standard components to be installed externally. These components should be connected as shown in Figure 2-4.

The internal analog circuitry in the PHY module requires that an external 2.32 kΩ, 1% resistor be attached from RBIAS to ground. The resistor influences the TPOUT+/- signal amplitude. The resistor should be placed as close as possible to the chip with no immediately adjacent signal traces to prevent noise capacitively coupling into the pin and affecting the transmit behavior. It is recommended that the resistor be a surface mount type.

Some of the device's digital logic operates at a nominal 2.5V. An on-chip voltage regulator is incorporated to generate this voltage. The only external component required is an external filter capacitor, connected from VCAP to ground. The capacitor must have low equivalent-series resistance (ESR), with a typical value of 10 μF, and a minimum value of 1 μF. The internal regulator is not designed to drive external loads.

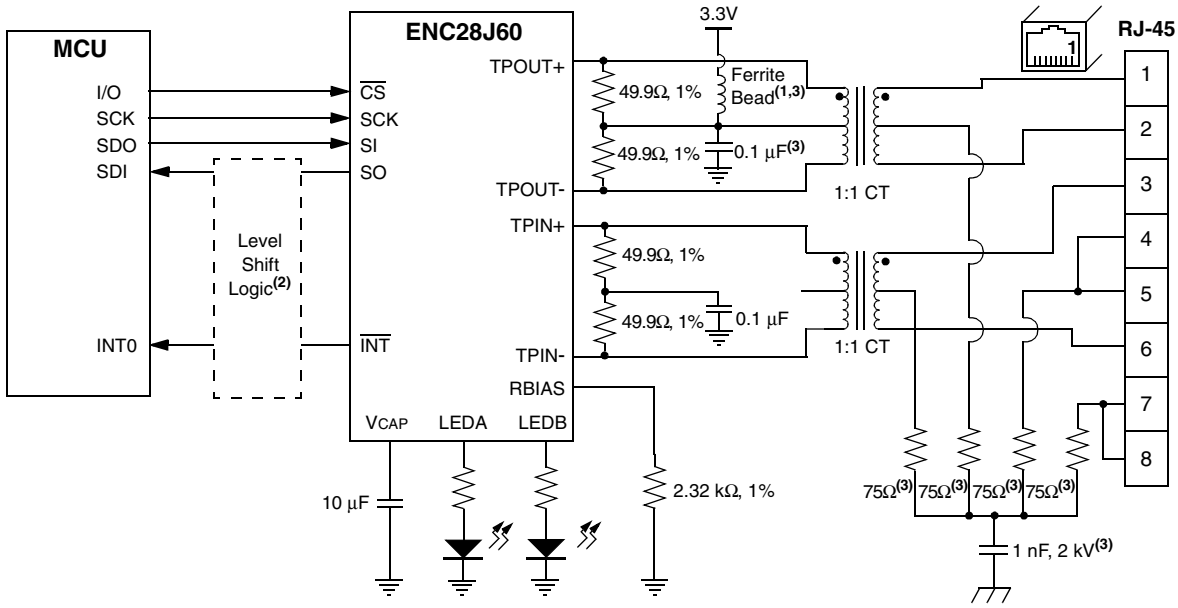
On the TPIN+/TPIN- and TPOUT+/TPOUT- pins, 1:1 center-taped pulse transformers rated for Ethernet operations are required. When the Ethernet module is enabled, current is continually sunk through both TPOUT pins. When the PHY is actively transmitting, a differential voltage is created on the Ethernet cable by varying the relative current sunk by TPOUT+ compared to TPOUT-.

A common-mode choke on the TPOUT interface, placed between the TPOUT pins and the Ethernet transformer (not shown), is not recommend. If a common-mode choke is used to reduce EMI emissions, it should be placed between the Ethernet transformer and pins 1 and 2 of the RJ-45 connector. Many Ethernet transformer modules include common-mode chokes inside the same device package. The transformers should have at least the isolation rating specified in Table 16-5 to protect against static voltages and meet IEEE 802.3 isolation requirements (see **Section 16.0 "Electrical Characteristics"** for specific transformer requirements). Both transmit and receive interfaces additionally require two resistors and a capacitor to properly terminate the transmission line, minimizing signal reflections.

All power supply pins must be externally connected to the same power source. Similarly, all ground references must be externally connected to the same ground node. Each VDD and VSS pin pair should have a 0.1 μF ceramic bypass capacitor (not shown in the schematic) placed as close to the pins as possible.

Since relatively high currents are necessary to operate the twisted-pair interface, all wires should be kept as short as possible. Reasonable wire widths should be used on power wires to reduce resistive loss. If the differential data lines cannot be kept short, they should be routed in such a way as to have a 100Ω characteristic impedance.

FIGURE 2-4: ENC28J60 ETHERNET TERMINATION AND EXTERNAL CONNECTIONS



Note 1: Ferrite Bead should be rated for at least 80 mA.

2: Required only if the microcontroller is operating at 5V. See **Section 2.5 "I/O Levels"** for more information.

3: These components are installed for EMI reduction purposes.

2.5 I/O Levels

The ENC28J60 is a 3.3V part; however, it was designed to be easily integrated into 5V systems. The SPI $\overline{CS}$, SCK and SI inputs, as well as the $\overline{RESET}$ pin, are all 5V tolerant. On the other hand, if the host controller is operated at 5V, it quite likely will not be within specifications when its SPI and interrupt inputs are driven by the 3.3V CMOS outputs on the ENC28J60. A unidirectional level translator would be necessary.

An economical 74HCT08 (quad AND gate), 74ACT125 (quad 3-state buffer) or many other 5V CMOS chips with TTL level input buffers may be used to provide the necessary level shifting. The use of 3-state buffers permits easy integration into systems which share the SPI bus with other devices. Figure 2-5 and Figure 2-6 show example translation schemes.

FIGURE 2-5: LEVEL SHIFTING USING AND GATES

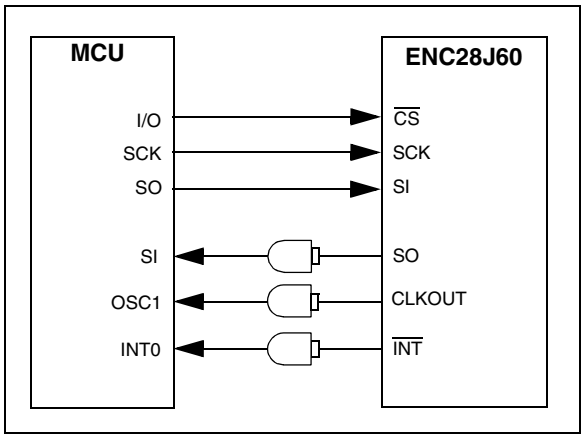
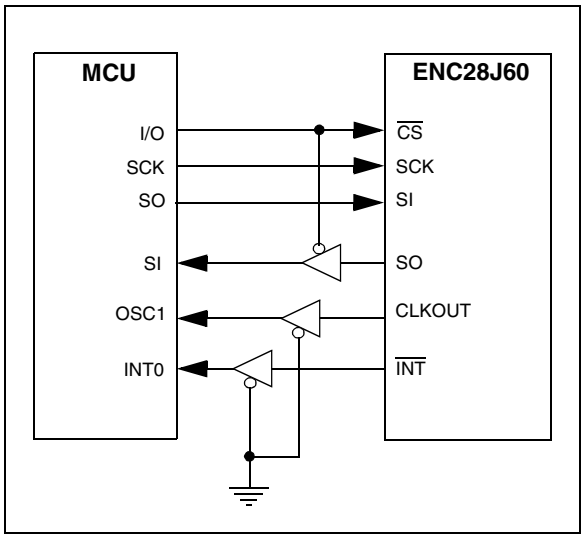


FIGURE 2-6: LEVEL SHIFTING USING 3-STATE BUFFERS

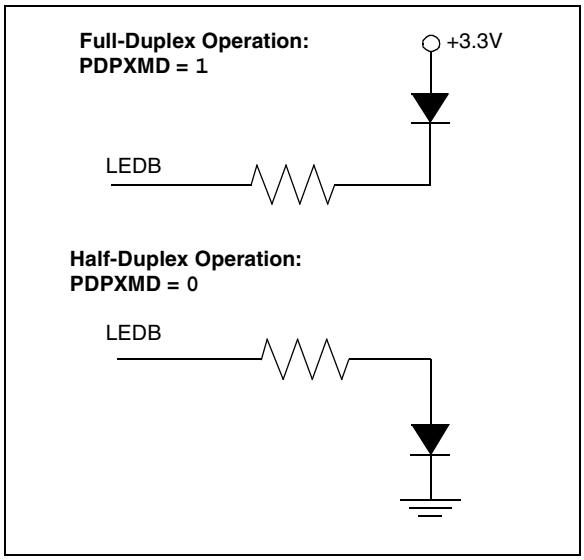


2.6 LED Configuration

The LEDA and LEDB pins support automatic polarity detection on Reset. The LEDs can be connected such that the pin must source current to turn the LED on, or alternately connected such that the pin must sink current to turn the LED on. Upon system Reset, the ENC28J60 will detect how the LED is connected and begin driving the LED to the default state configured by the PHLCON register. If the LED polarity is changed while the ENC28J60 is operating, the new polarity will not be detected until the next system Reset occurs.

LEDB is unique in that the connection of the LED is automatically read on Reset and determines how to initialize the PHCON1.PDPXMD bit. If the pin sources current to illuminate the LED, the bit is cleared on Reset and the PHY defaults to half-duplex operation. If the pin sinks current to illuminate the LED, the bit is set on Reset and the PHY defaults to full-duplex operation. Figure 2-7 shows the two available options. If no LED is attached to the LEDB pin, the PDPXMD bit will reset to an indeterminate value.

FIGURE 2-7: LEDB POLARITY AND RESET CONFIGURATION OPTIONS



The LEDs can also be configured separately to control their operating polarity (on or off when active), blink rate and blink stretch interval. The options are controlled by the LACFG3:LACFG0 and LBCFG3:LBCFG0 bits. Typical values for blink stretch are listed in Table 2-1.

TABLE 2-1: LED BLINK STRETCH LENGTH

Stretch Length	Typical Stretch (ms)
TNSTRCH (normal)	40
TMSTRCH (medium)	70
TLSTRCH (long)	140

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REGISTER 2-2: PHLCON: PHY MODULE LED CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
r	r	r	r	LACFG3	LACFG2	LACFG1	LACFG0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-x
LBCFG3	LBCFG2	LBCFG1	LBCFG0	LFRQ1	LFRQ0	STRCH	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Reserved:** Write as '0'

bit 13-12 **Reserved:** Write as '1'

bit 11-8 **LACFG3:LACFG0:** LEDA Configuration bits
1111 = Reserved
1110 = Display duplex status and collision activity (always stretched)
1101 = Display link status and transmit/receive activity (always stretched)
1100 = Display link status and receive activity (always stretched)
1011 = Blink slow
1010 = Blink fast
1001 = Off
1000 = On
0111 = Display transmit and receive activity (stretchable)
0110 = Reserved
0101 = Display duplex status
0100 = Display link status
0011 = Display collision activity (stretchable)
0010 = Display receive activity (stretchable)
0001 = Display transmit activity (stretchable)
0000 = Reserved

bit 7-4 **LBCFG3:LBCFG0:** LEDB Configuration bits
1110 = Display duplex status and collision activity (always stretched)
1101 = Display link status and transmit/receive activity (always stretched)
1100 = Display link status and receive activity (always stretched)
1011 = Blink slow
1010 = Blink fast
1001 = Off
1000 = On
0111 = Display transmit and receive activity (stretchable)
0110 = Reserved
0101 = Display duplex status
0100 = Display link status
0011 = Display collision activity (stretchable)
0010 = Display receive activity (stretchable)
0001 = Display transmit activity (stretchable)
0000 = Reserved

bit 3-2 **LFRQ1:LFRQ0:** LED Pulse Stretch Time Configuration bits (see Table 2-1)
11 = Reserved
10 = Stretch LED events by T_{LSTRCH}
01 = Stretch LED events by T_{MSTRCH}
00 = Stretch LED events by T_{NSTRCH}

bit 1 **STRCH:** LED Pulse Stretching Enable bit
1 = Stretchable LED events will cause lengthened LED pulses based on LFRQ1:LFRQ0 configuration
0 = Stretchable LED events will only be displayed while they are occurring

bit 0 **Reserved:** Write as '0'

NOTES:

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3.0 MEMORY ORGANIZATION

All memory in the ENC28J60 is implemented as static RAM. There are three types of memory in the ENC28J60:

- Control Registers
- Ethernet Buffer
- PHY Registers

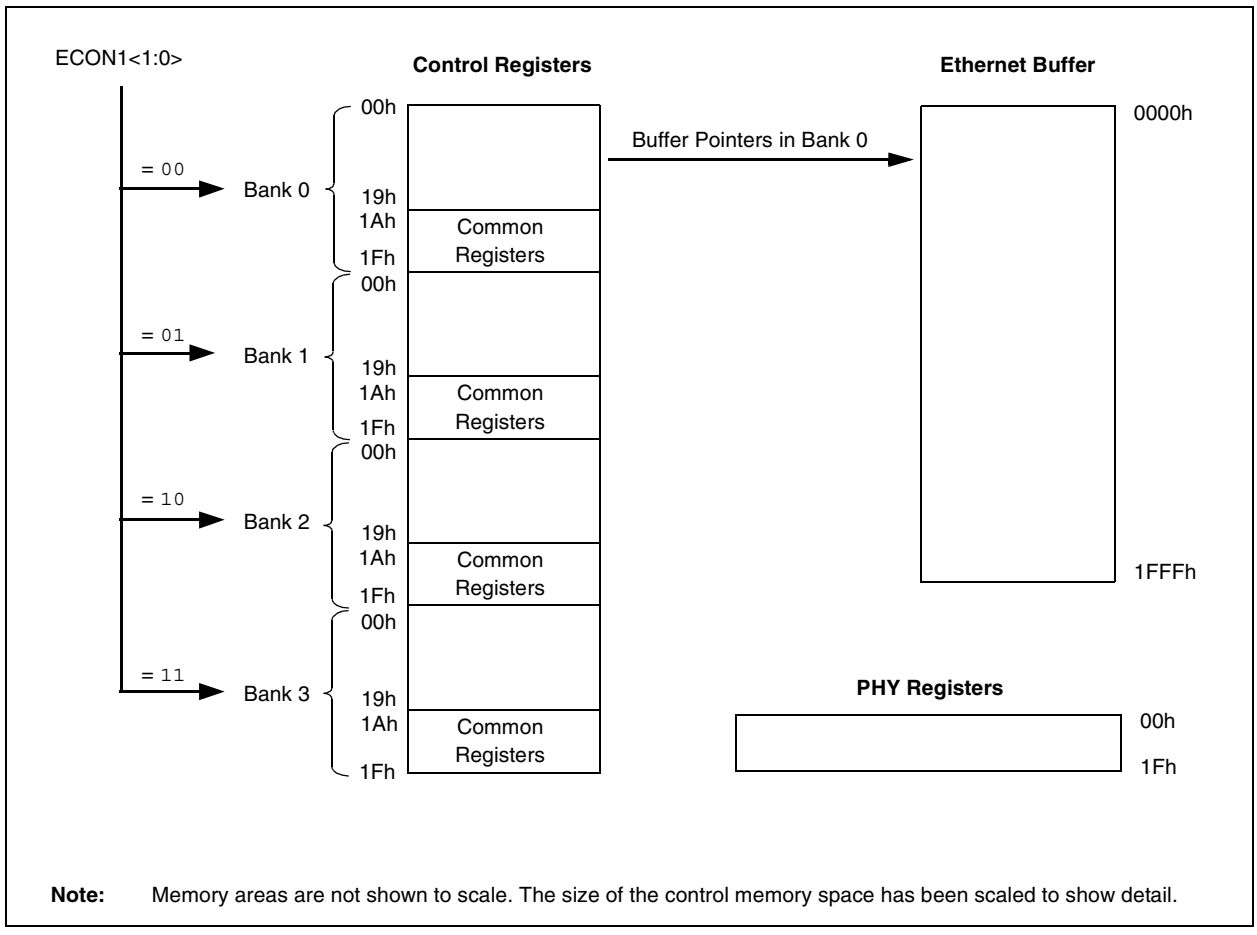
The Control registers' memory contains the registers that are used for configuration, control and status retrieval of the ENC28J60. The Control registers are directly read and written to by the SPI interface.

The Ethernet buffer contains transmit and receive memory used by the Ethernet controller in a single memory space. The sizes of the memory areas are programmable by the host controller using the SPI interface. The Ethernet buffer memory can only be accessed via the read buffer memory and write buffer memory SPI commands (see **Section 4.2.2 "Read Buffer Memory Command"** and **Section 4.2.4 "Write Buffer Memory Command"**).

The PHY registers are used for configuration, control and status retrieval of the PHY module. The registers are not directly accessible through the SPI interface; they can only be accessed through Media Independent Interface Management (MIIM) implemented in the MAC.

Figure 3-1 shows the data memory organization for the ENC28J60.

FIGURE 3-1: ENC28J60 MEMORY ORGANIZATION



Note: Memory areas are not shown to scale. The size of the control memory space has been scaled to show detail.

3.1 Control Registers

The Control Registers provide the main interface between the host controller and the on-chip Ethernet controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

The Control Register memory is partitioned into four banks, selectable by the bank select bits BSEL1:BSEL0 in the ECON1 register. Each bank is 32 bytes long and addressed by a 5-bit address value.

The last five locations (1Bh to 1Fh) of all banks point to a common set of registers: EIE, EIR, ESTAT, ECON2 and ECON1. These are key registers used in controlling and monitoring the operation of the device. Their common mapping allows easy access without switching the bank. The ECON1 and ECON2 registers are discussed later in this section.

Some of the available addresses are unimplemented. Any attempts to write to these locations are ignored while reads return '0's. The register at address 1Ah in each bank is reserved; read and write operations should not be performed on this register. All other reserved registers may be read, but their contents must not be changed. When reading and writing to registers which contain reserved bits, any rules stated in the register definition should be observed.

Control registers for the ENC28J60 are generically grouped as ETH, MAC and MII registers. Register names starting with "E" belong to the ETH group. Similarly, registers names starting with "MA" belong to the MAC group and registers prefixed with "MI" belong to the MII group.

TABLE 3-1: ENC28J60 CONTROL REGISTER MAP

Bank 0		Bank 1		Bank 2		Bank 3	
Address	Name	Address	Name	Address	Name	Address	Name
00h	ERDPTL	00h	EHT0	00h	MACON1	00h	MAADR5
01h	ERDPTH	01h	EHT1	01h	Reserved	01h	MAADR6
02h	EWRPTL	02h	EHT2	02h	MACON3	02h	MAADR3
03h	EWRPTH	03h	EHT3	03h	MACON4	03h	MAADR4
04h	ETXSTL	04h	EHT4	04h	MABBIPG	04h	MAADR1
05h	ETXSTH	05h	EHT5	05h	—	05h	MAADR2
06h	ETXNDL	06h	EHT6	06h	MAIPGL	06h	EBSTSD
07h	ETXNDH	07h	EHT7	07h	MAIPGH	07h	EBSTCON
08h	ERXSTL	08h	EPMM0	08h	MACLCON1	08h	EBSTCSL
09h	ERXSTH	09h	EPMM1	09h	MACLCON2	09h	EBSTCSH
0Ah	ERXNDL	0Ah	EPMM2	0Ah	MAMXFLL	0Ah	MISTAT
0Bh	ERXNDH	0Bh	EPMM3	0Bh	MAMXFLH	0Bh	—
0Ch	ERXRDPTL	0Ch	EPMM4	0Ch	Reserved	0Ch	—
0Dh	ERXRDPTH	0Dh	EPMM5	0Dh	Reserved	0Dh	—
0Eh	ERXWRPTL	0Eh	EPMM6	0Eh	Reserved	0Eh	—
0Fh	ERXWRPTH	0Fh	EPMM7	0Fh	—	0Fh	—
10h	EDMASTL	10h	EPMCSL	10h	Reserved	10h	—
11h	EDMASTH	11h	EPMCSH	11h	Reserved	11h	—
12h	EDMANDL	12h	—	12h	MICMD	12h	EREVID
13h	EDMANDH	13h	—	13h	—	13h	—
14h	EDMADSTL	14h	EPMOL	14h	MIREGADR	14h	—
15h	EDMADSTH	15h	EPMOH	15h	Reserved	15h	ECOCON
16h	EDMACSL	16h	Reserved	16h	MIWRL	16h	Reserved
17h	EDMACSH	17h	Reserved	17h	MIWRH	17h	EFLOCON
18h	—	18h	ERXFCON	18h	MIRDL	18h	EPAUSL
19h	—	19h	EPKTCNT	19h	MIRDH	19h	EPAUSH
1Ah	Reserved	1Ah	Reserved	1Ah	Reserved	1Ah	Reserved
1Bh	EIE	1Bh	EIE	1Bh	EIE	1Bh	EIE
1Ch	EIR	1Ch	EIR	1Ch	EIR	1Ch	EIR
1Dh	ESTAT	1Dh	ESTAT	1Dh	ESTAT	1Dh	ESTAT
1Eh	ECON2	1Eh	ECON2	1Eh	ECON2	1Eh	ECON2
1Fh	ECON1	1Fh	ECON1	1Fh	ECON1	1Fh	ECON1

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TABLE 3-2: ENC28J60 CONTROL REGISTER SUMMARY

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset	Details on Page
EIE	INTIE	PKTIE	DMAIE	LINKIE	TXIE	r	TXERIE	RXERIE	0000 0000	65
EIR	—	PKTIF	DMAIF	LINKIF	TXIF	r	TXERIF	RXERIF	-000 0000	66
ESTAT	INT	BUFER	r	LATECOL	—	RXBUSY	TXABRT	CLKRDY(1)	0000 -000	64
ECON2	AUTOINC	PKTDEC	PWRSV	r	VRPS	—	—	—	1000 0---	16
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	0000 0000	15
ERDPTL	Read Pointer Low Byte ERDPT<7:0>								1111 1010	17
ERDPTH	—	—	—	Read Pointer High Byte (ERDPT<12:8>)					---0 0101	17
EWRPTL	Write Pointer Low Byte (EWRPT<7:0>)								0000 0000	17
EWRPTH	—	—	—	Write Pointer High Byte (EWRPT<12:8>)					---0 0000	17
ETXSTL	TX Start Low Byte (ETXST<7:0>)								0000 0000	17
ETXSTH	—	—	—	TX Start High Byte (ETXST<12:8>)					---0 0000	17
ETXNDL	TX End Low Byte (ETXND<7:0>)								0000 0000	17
ETXNDH	—	—	—	TX End High Byte (ETXND<12:8>)					---0 0000	17
ERXSTL	RX Start Low Byte (ERXST<7:0>)								1111 1010	17
ERXSTH	—	—	—	RX Start High Byte (ERXST<12:8>)					---0 0101	17
ERXNDL	RX End Low Byte (ERXND<7:0>)								1111 1111	17
ERXNDH	—	—	—	RX End High Byte (ERXND<12:8>)					---1 1111	17
ERXRDPTL	RX RD Pointer Low Byte (ERXRDPT<7:0>)								1111 1010	17
ERXRDPTH	—	—	—	RX RD Pointer High Byte (ERXRDPT<12:8>)					---0 0101	17
ERXWRPTL	RX WR Pointer Low Byte (ERXWRPT<7:0>)								0000 0000	17
ERXWRPTH	—	—	—	RX WR Pointer High Byte (ERXWRPT<12:8>)					---0 0000	17
EDMASTL	DMA Start Low Byte (EDMAST<7:0>)								0000 0000	71
EDMASTH	—	—	—	DMA Start High Byte (EDMAST<12:8>)					---0 0000	71
EDMANDL	DMA End Low Byte (EDMAND<7:0>)								0000 0000	71
EDMANDH	—	—	—	DMA End High Byte (EDMAND<12:8>)					---0 0000	71
EDMADSTL	DMA Destination Low Byte (EDMADST<7:0>)								0000 0000	71
EDMADSTH	—	—	—	DMA Destination High Byte (EDMADST<12:8>)					---0 0000	71
EDMACSL	DMA Checksum Low Byte (EDMACS<7:0>)								0000 0000	72
EDMACSH	DMA Checksum High Byte (EDMACS<15:8>)								0000 0000	72
EHT0	Hash Table Byte 0 (EHT<7:0>)								0000 0000	52
EHT1	Hash Table Byte 1 (EHT<15:8>)								0000 0000	52
EHT2	Hash Table Byte 2 (EHT<23:16>)								0000 0000	52
EHT3	Hash Table Byte 3 (EHT<31:24>)								0000 0000	52
EHT4	Hash Table Byte 4 (EHT<39:32>)								0000 0000	52
EHT5	Hash Table Byte 5 (EHT<47:40>)								0000 0000	52
EHT6	Hash Table Byte 6 (EHT<55:48>)								0000 0000	52
EHT7	Hash Table Byte 7 (EHT<63:56>)								0000 0000	52
EPMM0	Pattern Match Mask Byte 0 (EPMM<7:0>)								0000 0000	51
EPMM1	Pattern Match Mask Byte 1 (EPMM<15:8>)								0000 0000	51
EPMM2	Pattern Match Mask Byte 2 (EPMM<23:16>)								0000 0000	51
EPMM3	Pattern Match Mask Byte 3 (EPMM<31:24>)								0000 0000	51
EPMM4	Pattern Match Mask Byte 4 (EPMM<39:32>)								0000 0000	51
EPMM5	Pattern Match Mask Byte 5 (EPMM<47:40>)								0000 0000	51
EPMM6	Pattern Match Mask Byte 6 (EPMM<55:48>)								0000 0000	51
EPMM7	Pattern Match Mask Byte 7 (EPMM<63:56>)								0000 0000	51

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved, do not modify.

Note 1: CLKRDY resets to '0' on Power-on Reset but is unaffected on all other Resets.

2: EREVID is a read-only register.

3: ECOCON resets to '---- -100' on Power-on Reset and '---- -uuu' on all other Resets.

TABLE 3-2: ENC28J60 CONTROL REGISTER SUMMARY (CONTINUED)

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset	Details on Page
EPMCSL	Pattern Match Checksum Low Byte (EPMCS<7:0>)								0000 0000	51
EPMCSH	Pattern Match Checksum High Byte (EPMCS<15:0>)								0000 0000	51
EPMOL	Pattern Match Offset Low Byte (EPMO<7:0>)								0000 0000	51
EPMOH	—	—	—	Pattern Match Offset High Byte (EPMO<12:8>)					---0 0000	51
ERXFCON	UCEN	ANDOR	CRCEN	PMEN	MPEN	HTEN	MCEN	BCEN	1010 0001	48
EPKTCNT	Ethernet Packet Count								0000 0000	43
MACON1	—	—	—	r	TXPAUS	RXPAUS	PASSALL	MARXEN	---0 0000	34
MACON3	PADCFG2	PADCFG1	PADCFG0	TXCRCEN	PHDREN	HFRMEN	FRMLNEN	FULDPX	0000 0000	35
MACON4	—	DEFER	BPEN	NOBKOFF	—	—	r	r	-000 --00	36
MABBIPG	—	Back-to-Back Inter-Packet Gap (BBIPG<6:0>)							-000 0000	36
MAIPGL	—	Non-Back-to-Back Inter-Packet Gap Low Byte (MAIPGL<6:0>)							-000 0000	34
MAIPGH	—	Non-Back-to-Back Inter-Packet Gap High Byte (MAIPGH<6:0>)							-000 0000	34
MACLCON1	—	—	—	—	Retransmission Maximum (RETMAX<3:0>)				---- 1111	34
MACLCON2	—	—	Collision Window (COLWIN<5:0>)						--11 0111	34
MAMXFLL	Maximum Frame Length Low Byte (MAMXFL<7:0>)								0000 0000	34
MAMXFLH	Maximum Frame Length High Byte (MAMXFL<15:8>)								0000 0110	34
MICMD	—	—	—	—	—	—	MIISCAN	MIIRD	---- --00	21
MIREGADR	—	—	—	MII Register Address (MIREGADR<4:0>)					---0 0000	19
MIWRL	MII Write Data Low Byte (MIWR<7:0>)								0000 0000	19
MIWRH	MII Write Data High Byte (MIWR<15:8>)								0000 0000	19
MIRDL	MII Read Data Low Byte (MIRD<7:0>)								0000 0000	19
MIRDH	MII Read Data High Byte(MIRD<15:8>)								0000 0000	19
MAADR5	MAC Address Byte 5 (MAADR<15:8>)								0000 0000	34
MAADR6	MAC Address Byte 6 (MAADR<7:0>)								0000 0000	34
MAADR3	MAC Address Byte 3 (MAADR<31:24>), OUI Byte 3								0000 0000	34
MAADR4	MAC Address Byte 4 (MAADR<23:16>)								0000 0000	34
MAADR1	MAC Address Byte 1 (MAADR<47:40>), OUI Byte 1								0000 0000	34
MAADR2	MAC Address Byte 2 (MAADR<39:32>), OUI Byte 2								0000 0000	34
EBSTSD	Built-in Self-Test Fill Seed (EBSTSD<7:0>)								0000 0000	76
EBSTCON	PSV2	PSV1	PSV0	PSEL	TMSEL1	TMSEL0	TME	BISTST	0000 0000	75
EBSTCSL	Built-in Self-Test Checksum Low Byte (EBSTCS<7:0>)								0000 0000	76
EBSTCSH	Built-in Self-Test Checksum High Byte (EBSTCS<15:8>)								0000 0000	76
MISTAT	—	—	—	—	r	NVALID	SCAN	BUSY	---- 0000	21
EREVID(2)	—	—	—	Ethernet Revision ID (EREVID<4:0>)					---q qqqq	22
ECOCON(3)	—	—	—	—	—	COCON2	COCON1	COCON0	---- -100	6
EFLOCON	—	—	—	—	—	FULDPXS	FCEN1	FCEN0	---- -000	56
EPAUSL	Pause Timer Value Low Byte (EPAUS<7:0>)								0000 0000	57
EPAUSH	Pause Timer Value High Byte (EPAUS<15:8>)								0001 0000	57

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved, do not modify.

Note 1: CLKRDY resets to '0' on Power-on Reset but is unaffected on all other Resets.

2: EREVID is a read-only register.

3: ECOCON resets to '---- -100' on Power-on Reset and '---- -uuu' on all other Resets.

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3.1.1 ECON1 REGISTER

The ECON1 register, shown in Register 3-1, is used to control the main functions of the ENC28J60. Receive enable, transmit request, DMA control and bank select bits can all be found in ECON1.

REGISTER 3-1: ECON1: ETHERNET CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TXRST:** Transmit Logic Reset bit
1 = Transmit logic is held in Reset
0 = Normal operation

bit 6 **RXRST:** Receive Logic Reset bit
1 = Receive logic is held in Reset
0 = Normal operations

bit 5 **DMAST:** DMA Start and Busy Status bit
1 = DMA copy or checksum operation is in progress
0 = DMA hardware is Idle

bit 4 **CSUMEN:** DMA Checksum Enable bit
1 = DMA hardware calculates checksums
0 = DMA hardware copies buffer memory

bit 3 **TXRTS:** Transmit Request to Send bit
1 = The transmit logic is attempting to transmit a packet
0 = The transmit logic is Idle

bit 2 **RXEN:** Receive Enable bit
1 = Packets which pass the current filter configuration will be written into the receive buffer
0 = All packets received will be ignored

bit 1-0 **BSEL1:BSEL0:** Bank Select bits
11 = SPI accesses registers in Bank 3
10 = SPI accesses registers in Bank 2
01 = SPI accesses registers in Bank 1
00 = SPI accesses registers in Bank 0

3.1.2 ECON2 REGISTER

The ECON2 register, shown in Register 3-2, is used to control other main functions of the ENC28J60.

REGISTER 3-2: ECON2: ETHERNET CONTROL REGISTER 2

R/W-1	R/W-0(1)	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
AUTOINC	PKTDEC	PWRSV	r	VRPS	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **AUTOINC:** Automatic Buffer Pointer Increment Enable bit
1 = Automatically increment ERDPT or EWRPT on reading from or writing to EDATA
0 = Do not automatically change ERDPT and EWRPT after the buffer is accessed

bit 6 **PKTDEC:** Packet Decrement bit
1 = Decrement the EPKTCNT register by one
0 = Leave EPKTCNT unchanged

bit 5 **PWRSV:** Power Save Enable bit
1 = MAC, PHY and control logic are in Low-Power Sleep mode
0 = Normal operation

bit 4 **Reserved:** Maintain as '0'

bit 3 **VRPS:** Voltage Regulator Power Save Enable bit
When PWRSV = 1:
1 = Internal voltage regulator is in Low-Current mode
0 = Internal voltage regulator is in Normal Current mode
When PWRSV = 0:
The bit is ignored; the regulator always outputs as much current as the device requires.

bit 2-0 **Unimplemented:** Read as '0'

Note 1: This bit is automatically cleared once it is set.

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3.2 Ethernet Buffer

The Ethernet buffer contains transmit and receive memory used by the Ethernet controller. The entire buffer is 8 Kbytes, divided into separate receive and transmit buffer spaces. The sizes and locations of transmit and receive memory are fully programmable by the host controller using the SPI interface.

The relationship of the buffer spaces is shown in Figure 3-2.

3.2.1 RECEIVE BUFFER

The receive buffer constitutes a circular FIFO buffer managed by hardware. The register pairs ERXSTH:ERXSTL and ERXNDH:ERXNDL serve as Pointers to define the buffer's size and location within the memory. The byte pointed to by ERXST and the byte pointed to by ERXND are both included in the FIFO buffer.

As bytes of data are received from the Ethernet interface, they are written into the receive buffer sequentially. However, after the memory pointed to by ERXND is written to, the hardware will automatically write the next byte of received data to the memory pointed to by ERXST. As a result, the receive hardware will never write outside the boundaries of the FIFO.

The host controller may program the ERXST and ERXND Pointers when the receive logic is not enabled. The Pointers must not be modified while the receive logic is enabled (ECON1.RXEN is set). If desired, the Pointers may span the 1FFFh to 0000h memory boundary; the hardware will still operate as a FIFO.

The ERXWRPTH:ERXWRPTL registers define a location within the FIFO where the hardware will write bytes that it receives. The Pointer is read-only and is automatically updated by the hardware whenever a new packet is successfully received. The Pointer is useful for determining how much free space is available within the FIFO.

The ERXRDPT registers define a location within the FIFO where the receive hardware is forbidden to write to. In normal operation, the receive hardware will write data up to, but not including, the memory pointed to by ERXRDPT. If the FIFO fills up with data and new data continues to arrive, the hardware will not overwrite the previously received data. Instead, the new data will be thrown away and the old data will be preserved. In order to continuously receive new data, the host controller must periodically advance this Pointer whenever it finishes processing some, or all, of the old received data.

3.2.2 TRANSMIT BUFFER

Any space within the 8-Kbyte memory, which is not programmed as part of the receive FIFO buffer, is considered to be the transmit buffer. The responsibility of managing where packets are located in the transmit buffer belongs to the host controller. Whenever the host controller decides to transmit a packet, the ETXST and ETXND Pointers are programmed with addresses specifying where, within the transmit buffer, the particular packet to transmit is located. The hardware does not check that the start and end addresses do not overlap with the receive buffer. To prevent buffer corruption, the host controller must make sure to not transmit a packet while the ETXST and ETXND Pointers are overlapping the receive buffer, or while the ETXND Pointer is too close to the receive buffer. See **Section 7.1 "Transmitting Packets"** for more information.

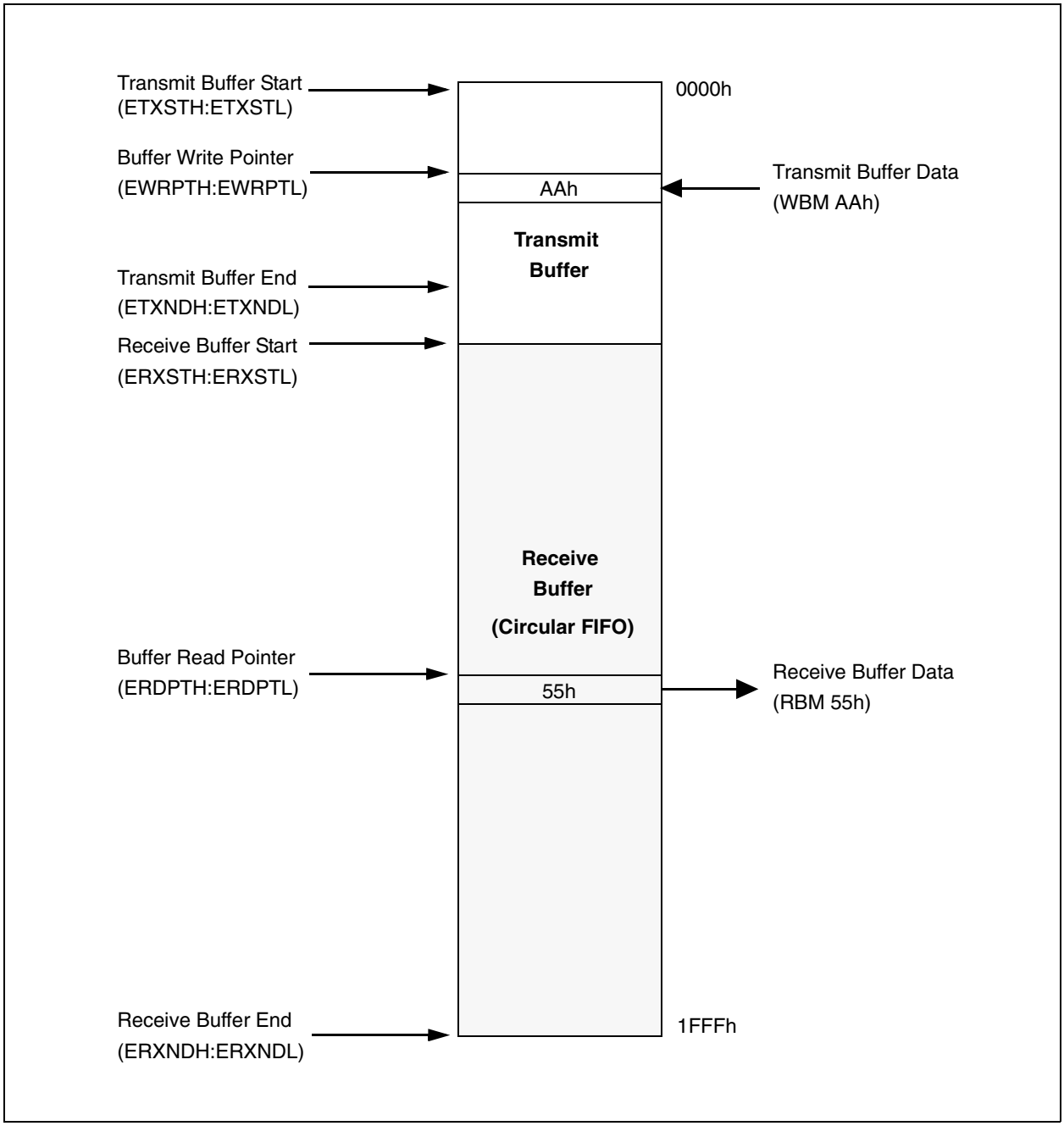
3.2.3 READING AND WRITING TO THE BUFFER

The Ethernet buffer contents are accessed from the host controller though separate Read and Write Pointers (ERDPT and EWRPT) combined with the read buffer memory and write buffer memory SPI commands. While sequentially reading from the receive buffer, a wrapping condition will occur at the end of the receive buffer. While sequentially writing to the buffer, no wrapping conditions will occur. See **Section 4.2.2 "Read Buffer Memory Command"** and **Section 4.2.4 "Write Buffer Memory Command"** for more information.

3.2.4 DMA ACCESS TO THE BUFFER

The integrated DMA controller must read from the buffer when calculating a checksum and it must read and write to the buffer when copying memory. The DMA follows the same wrapping rules that SPI accesses do. While it sequentially reads, it will be subject to a wrapping condition at the end of the receive buffer. All writes it does will not be subject to any wrapping conditions. See **Section 13.0 "Direct Memory Access Controller"** for more information.

FIGURE 3-2: ETHERNET BUFFER ORGANIZATION



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3.3 PHY Registers

The PHY registers provide configuration and control of the PHY module, as well as status information about its operation. All PHY registers are 16 bits in width. There are a total of 32 PHY addresses; however, only 9 locations are implemented. Writes to unimplemented locations are ignored and any attempts to read these locations will return '0'. All reserved locations should be written as '0'; their contents should be ignored when read.

Unlike the ETH, MAC and MII control registers, or the buffer memory, the PHY registers are not directly accessible through the SPI control interface. Instead, access is accomplished through a special set of MAC control registers that implement Media Independent Interface Management (MIIM). These control registers are referred to as the MII registers. The registers that control access to the PHY registers are shown in Register 3-3 and Register 3-4.

3.3.1 READING PHY REGISTERS

When a PHY register is read, the entire 16 bits are obtained.

To read from a PHY register:

1. Write the address of the PHY register to read from into the MIREGADR register.
2. Set the MICMD.MIIRD bit. The read operation begins and the MISTAT.BUSY bit is set.
3. Wait 10.24 μs. Poll the MISTAT.BUSY bit to be certain that the operation is complete. While busy, the host controller should not start any MIISCAN operations or write to the MIWRH register.
   When the MAC has obtained the register contents, the BUSY bit will clear itself.
4. Clear the MICMD.MIIRD bit.
5. Read the desired data from the MIRDL and MIRDH registers. The order that these bytes are accessed is unimportant.

3.3.2 WRITING PHY REGISTERS

When a PHY register is written to, the entire 16 bits is written at once; selective bit writes are not implemented. If it is necessary to reprogram only select bits in the register, the controller must first read the PHY register, modify the resulting data and then write the data back to the PHY register.

To write to a PHY register:

1. Write the address of the PHY register to write to into the MIREGADR register.
2. Write the lower 8 bits of data to write into the MIWRL register.
3. Write the upper 8 bits of data to write into the MIWRH register. Writing to this register automatically begins the MIIM transaction, so it must be written to after MIWRL. The MISTAT.BUSY bit becomes set.

The PHY register will be written after the MIIM operation completes, which takes 10.24 μs. When the write operation has completed, the BUSY bit will clear itself. The host controller should not start any MIISCAN or MIIRD operations while busy.

3.3.3 SCANNING A PHY REGISTER

The MAC can be configured to perform automatic back-to-back read operations on a PHY register. This can significantly reduce the host controller complexity when periodic status information updates are desired. To perform the scan operation:

1. Write the address of the PHY register to read from into the MIREGADR register.
2. Set the MICMD.MIISCAN bit. The scan operation begins and the MISTAT.BUSY bit is set. The first read operation will complete after 10.24 μs. Subsequent reads will be done at the same interval until the operation is cancelled. The MISTAT.NVALID bit may be polled to determine when the first read operation is complete.

After setting the MIISCAN bit, the MIRDL and MIRDH registers will automatically be updated every 10.24 μs. There is no status information which can be used to determine when the MIRD registers are updated. Since the host controller can only read one MII register at a time through the SPI, it must not be assumed that the values of MIRDL and MIRDH were read from the PHY at exactly the same time.

When the MIISCAN operation is in progress, the host controller must not attempt to write to MIWRH or start an MIIRD operation. The MIISCAN operation can be cancelled by clearing the MICMD.MIISCAN bit and then polling the MISTAT.BUSY bit. New operations may be started after the BUSY bit is cleared.

TABLE 3-3: ENC28J60 PHY REGISTER SUMMARY

Addr	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
00h	PHCON1	PRST	PLOOPBK	—	—	PPWRSV	r	—	PDPXMD(1)	r	—	—	—	—	—	—	—	00-- 00-q 0--- ----
01h	PHSTAT1	—	—	—	PFDPX	PHDPX	—	—	—	—	—	—	—	—	LLSTAT	JBSTAT	—	---1 1--- ---- -00-
02h	PHID1	PHY Identifier (OUI3:OUI18) = 0083h																0000 0000 1000 0011
03h	PHID2	PHY Identifier (OUI19:OUI24) = 000101						PHY P/N (PPN5:PPN0) = 00h						PHY Revision (PREV3:PREV0) = 00h				0001 0100 0000 0000
10h	PHCON2	—	FRCLNK	TXDIS	r	r	JABBER	r	HDLDIS	r	r	r	r	r	r	r	r	-000 0000 0000 0000
11h	PHSTAT2	—	—	TXSTAT	RXSTAT	COLSTAT	LSTAT	DPXSTAT(1)	—	—	—	PLRITY	—	—	—	—	—	--00 00q- --0- ----
12h	PHIE	r	r	r	r	r	r	r	r	r	r	r	PLNKIE	r	r	PGEIE	r	0000 0000 0000 0000
13h	PHIR	r	r	r	r	r	r	r	r	r	r	r	PLNKIF	r	PGIF	r	r	xxxx xxxx xx00 00x0
14h	PHLCON	r	r	r	r	LACFG3:LACFG0				LBCFG3:LBCFG0				LFRQ1:LFRQ0		STRCH	r	0011 0100 0010 001x

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved, do not modify.

Note 1: Reset values of the Duplex mode/status bits depend on the connection of the LED to the LEDB pin (see **Section 2.6 “LED Configuration”** for additional details).

Preliminary

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REGISTER 3-3: MICMD: MII COMMAND REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	MIISCAN	MIIRD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **MIISCAN:** MII Scan Enable bit
1 = PHY register at MIREGADR is continuously read and the data is placed in MIRD
0 = No MII Management scan operation is in progress

bit 0 **MIIRD:** MII Read Enable bit
1 = PHY register at MIREGADR is read once and the data is placed in MIRD
0 = No MII Management read operation is in progress

REGISTER 3-4: MISTAT: MII STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	r	NVALID	SCAN	BUSY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **Reserved:** Maintain as '0'

bit 2 **NVALID:** MII Management Read Data Not Valid bit
1 = The contents of MIRD are not valid yet
0 = The MII Management read cycle has completed and MIRD has been updated

bit 1 **SCAN:** MII Management Scan Operation bit
1 = MII Management scan operation is in progress
0 = No MII Management scan operation is in progress

bit 0 **BUSY:** MII Management Busy bit
1 = A PHY register is currently being read or written to
0 = The MII Management interface is Idle

3.3.4 PHSTAT REGISTERS

The PHSTAT1 and PHSTAT2 registers contain read-only bits that show the current status of the PHY module's operations, particularly the conditions of the communications link to the rest of the network.

The PHSTAT1 register (Register 3-5) contains the LLSTAT bit; it clears and latches low if the physical layer link has gone down since the last read of the register. Periodic polling by the host controller can be used to determine exactly when the link fails. It may be particularly useful if the link change interrupt is not used.

The PHSTAT1 register also contains a jabber status bit. An Ethernet controller is said to be "jabbering" if it continuously transmits data without stopping and allowing other nodes to share the medium. Generally, the jabber condition indicates that the local controller may be grossly violating the maximum packet size defined by the IEEE specification. This bit latches high to indicate that a jabber condition has occurred since the last read of the register.

The PHSTAT2 register (Register 3-6) contains status bits which report if the PHY module is linked to the network and whether or not it is transmitting or receiving.

3.3.5 PHID1 AND PHID2 REGISTERS

The PHID1 and PHID2 registers are read-only registers. They hold constant data that help identify the Ethernet controller and may be useful for debugging purposes. This includes:

- The part number of the PHY module (PPN5:PPN0)
- The revision level of the PHY module (PREV3:PREV0); and
- The PHY Identifier, as part of Microchip's corporate Organizationally Unique Identifier (OUI) (OUI3:OUI24)

The PHY part number and revision are part of PHID2. The upper two bytes of the PHY identifier are located in PHID1, with the remainder in PHID2. The exact locations within registers are shown in Table 3-3.

The 22 bits of the OUI contained in the PHY Identifier (OUI3:OUI24, corresponding to PHID1<15:0> and PHID2<15:10>) are concatenated with '00' as the first two digits (OUI1 and OUI2) to generate the entire OUI. For convenience, this 24-bit string is usually interpreted in hexadecimal; the resulting OUI for Microchip Technology is 0004A3h.

Revision information is also stored in EREVID. This is a read-only control register which contains a 5-bit identifier for the specific silicon revision level of the device. Details of this register are shown in Table 3-2.

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REGISTER 3-5: PHSTAT1: PHYSICAL LAYER STATUS REGISTER 1

U-0	U-0	U-0	R-1	R-1	U-0	U-0	U-0
—	—	—	PFDPX	PHDPX	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/LL-0	R/LH-0	U-0
—	—	—	—	—	LLSTAT	JBSTAT	—
bit 7							bit 0

Legend:	'1' = Bit is set		
R = Read-only bit	'0' = Bit is cleared	U = Unimplemented bit, read as '0'	
-n = Value at POR	R/L = Read-only latch bit	LL = Bit latches low	LH = Bit latches high

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **PFDPX:** PHY Full-Duplex Capable bit
1 = PHY is capable of operating at 10 Mbps in Full-Duplex mode (this bit is always set)

bit 11 **PHDPX:** PHY Half-Duplex Capable bit
1 = PHY is capable of operating at 10 Mbps in Half-Duplex mode (this bit is always set)

bit 10-3 **Unimplemented:** Read as '0'

bit 2 **LLSTAT:** PHY Latching Link Status bit
1 = Link is up and has been up continously since PHSTAT1 was last read
0 = Link is down or was down for a period since PHSTAT1 was last read

bit 1 **JBSTAT:** PHY Latching Jabber Status bit
1 = PHY has detected a transmission meeting the jabber criteria since PHSTAT1 was last read
0 = PHY has not detected any jabbering transmissions since PHSTAT1 was last read

bit 0 **Unimplemented:** Read as '0'

REGISTER 3-6: PHSTAT2: PHYSICAL LAYER STATUS REGISTER 2

U-0	U-0	R-0	R-0	R-0	R-0	R-x	U-0
—	—	TXSTAT	RXSTAT	COLSTAT	LSTAT	DPXSTAT(1)	—
bit 15							bit 8

U-0	U-0	R-0	U-0	U-0	U-0	U-0	U-0
—	—	PLRITY	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **TXSTAT:** PHY Transmit Status bit
1 = PHY is transmitting data
0 = PHY is not transmitting data

bit 12 **RXSTAT:** PHY Receive Status bit
1 = PHY is receiving data
0 = PHY is not receiving data

bit 11 **COLSTAT:** PHY Collision Status bit
1 = A collision is occuring
0 = A collision is not occuring

bit 10 **LSTAT:** PHY Link Status bit (non-latching)
1 = Link is up
0 = Link is down

bit 9 **DPXSTAT:** PHY Duplex Status bit(1)
1 = PHY is configured for full-duplex operation (PHCON1<8> is set)
0 = PHY is configured for half-duplex operation (PHCON1<8> is clear)

bit 8-6 **Unimplemented:** Read as '0'

bit 5 **PLRITY:** Polarity Status bit
1 = The polarity of the signal on TPIN+/TPIN- is reversed
0 = The polarity of the signal on TPIN+/TPIN- is correct

bit 4-0 **Unimplemented:** Read as '0'

Note 1: Reset values of the Duplex mode/status bit depends on the connection of the LED to the LEDB pin (see **Section 2.6 "LED Configuration"** for additional details).

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4.0 SERIAL PERIPHERAL INTERFACE (SPI)

4.1 Overview

The ENC28J60 is designed to interface directly with the Serial Peripheral Interface (SPI) port available on many microcontrollers. The implementation used on this device supports SPI mode 0,0 only. In addition, the SPI port requires that SCK be at Idle in a low state; selectable clock polarity is not supported.

Commands and data are sent to the device via the SI pin, with data being clocked in on the rising edge of SCK. Data is driven out by the ENC28J60 on the SO line, on the falling edge of SCK. The $\overline{CS}$ pin must be held low while any operation is performed and returned high when finished.

FIGURE 4-1: SPI INPUT TIMING

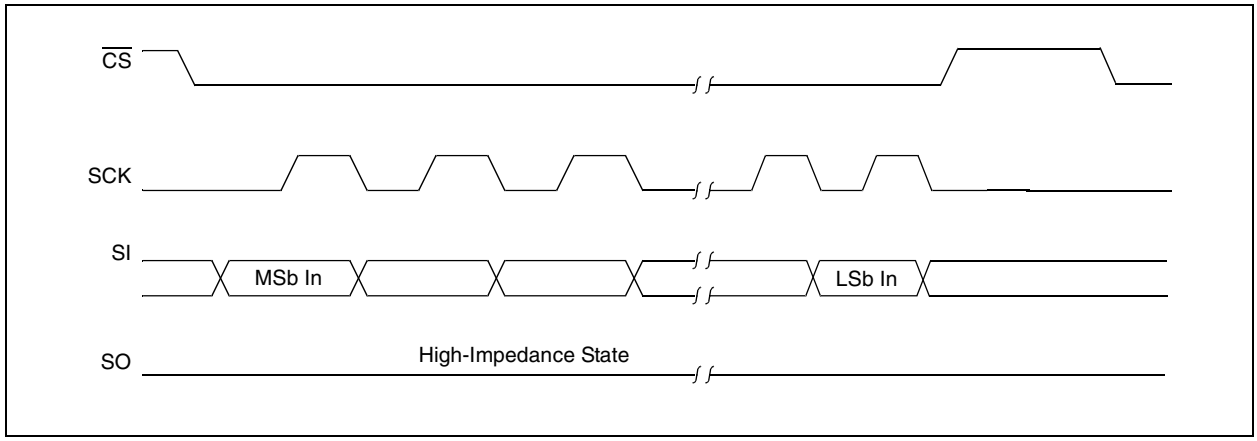
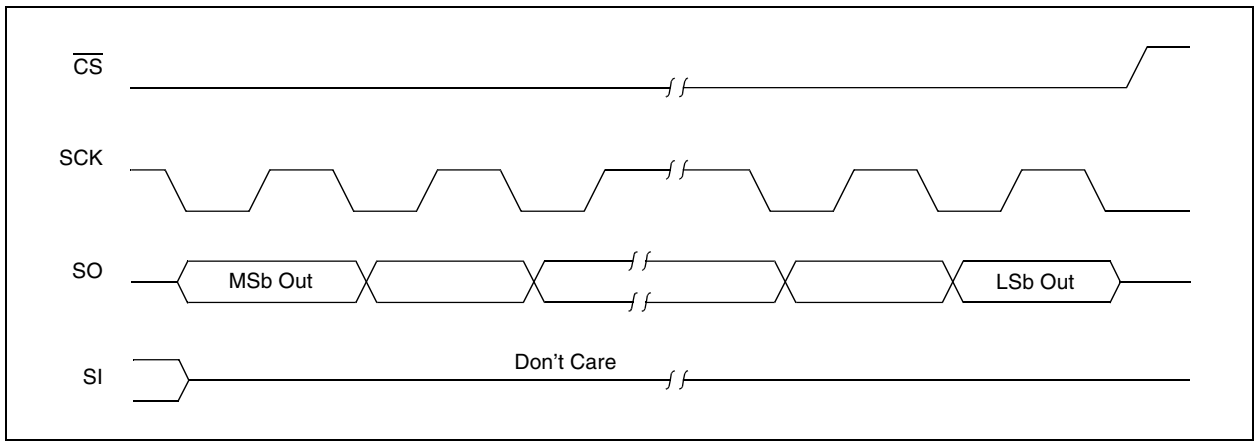


FIGURE 4-2: SPI OUTPUT TIMING



4.2 SPI Instruction Set

The operation of the ENC28J60 depends entirely on commands given by an external host controller over the SPI interface. These commands take the form of instructions, of one or more bytes, which are used to access the control memory and Ethernet buffer spaces. At the least, instructions consist of a 3-bit opcode, followed by a 5-bit argument that specifies either a register address or a data constant. Write and bit field instructions are also followed by one or more bytes of data.

A total of seven instructions are implemented on the ENC28J60. Table 4-1 shows the command codes for all operations.

TABLE 4-1: SPI INSTRUCTION SET FOR THE ENC28J60

Instruction Name and Mnemonic	Byte 0								Byte 1 and Following							
	Opcode			Argument					Data							
Read Control Register (RCR)	0	0	0	a	a	a	a	a	N/A							
Read Buffer Memory (RBM)	0	0	1	1	1	0	1	0	N/A							
Write Control Register (WCR)	0	1	0	a	a	a	a	a	d	d	d	d	d	d	d	d
Write Buffer Memory (WBM)	0	1	1	1	1	0	1	0	d	d	d	d	d	d	d	d
Bit Field Set (BFS)	1	0	0	a	a	a	a	a	d	d	d	d	d	d	d	d
Bit Field Clear (BFC)	1	0	1	a	a	a	a	a	d	d	d	d	d	d	d	d
System Reset Command (Soft Reset) (SRC)	1	1	1	1	1	1	1	1	N/A							

Legend: a = control register address, d = data payload.

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4.2.1 READ CONTROL REGISTER COMMAND

The Read Control Register (RCR) command allows the host controller to read any of the ETH, MAC and MII registers in any order. The contents of the PHY registers are read via a special MII register interface (see **Section 3.3.1 "Reading PHY Registers"** for more information).

The RCR command is started by pulling the $\overline{CS}$ pin low. The RCR opcode is then sent to the ENC28J60, followed by a 5-bit register address (A4 through A0). The 5-bit address identifies any of the 32 control registers in the current bank. If the 5-bit address is an ETH register, then data in the selected register will immediately start shifting out MSb first on the SO pin. Figure 4-3 shows the read sequence for these registers.

If the address specifies one of the MAC or MII registers, a dummy byte will first be shifted out the SO pin. After the dummy byte, the data will be shifted out MSb first on the SO pin. The RCR operation is terminated by raising the $\overline{CS}$ pin. Figure 4-4 shows the read sequence for MAC and MII registers.

FIGURE 4-3: READ CONTROL REGISTER COMMAND SEQUENCE (ETH REGISTERS)

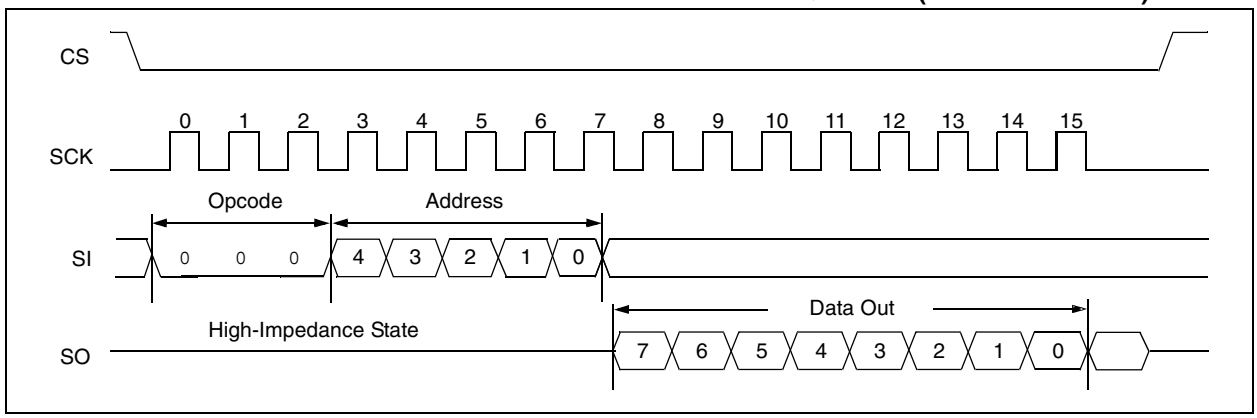
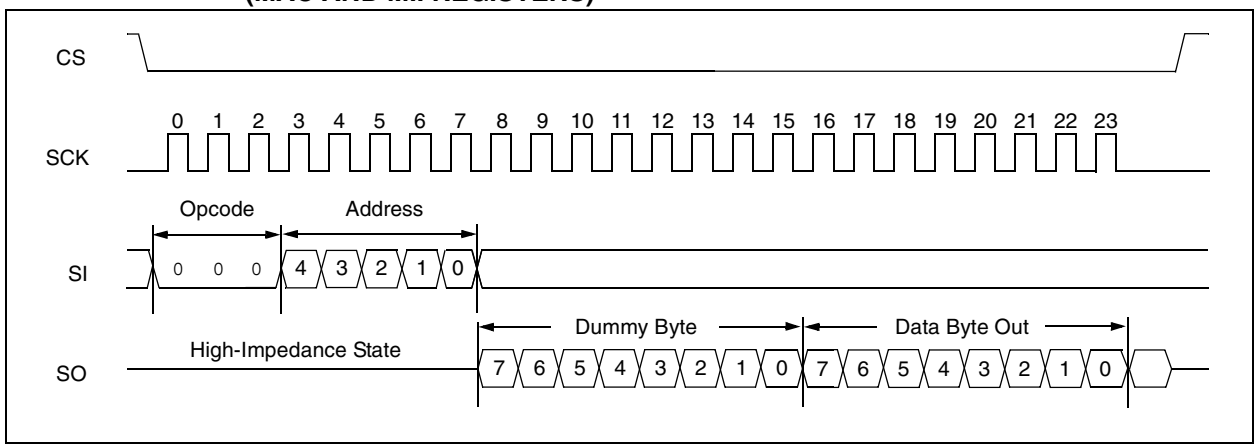


FIGURE 4-4: READ CONTROL REGISTER COMMAND SEQUENCE (MAC AND MII REGISTERS)



4.2.2 READ BUFFER MEMORY COMMAND

The Read Buffer Memory (RBM) command allows the host controller to read bytes from the integrated 8-Kbyte transmit and receive buffer memory.

If the AUTOINC bit in the ECON2 register is set, the ERDPT Pointer will automatically increment to point to the next address after the last bit of each byte is read. The next address will normally be the current address incremented by one. However, if the last byte in the receive buffer is read (ERDPT = ERXND), the ERDPT Pointer will change to the beginning of the receive buffer (ERXST). This allows the host controller to read packets from the receive buffer in a continuous stream without keeping track of when a wraparound is needed. If AUTOINC is set when address 1FFFh is read and ERXND does not point to this address, the Read Pointer will increment and wrap around to 0000h.

The RBM command is started by pulling the $\overline{CS}$ pin low. The RBM opcode is then sent to the ENC28J60, followed by the 5-bit constant 1Ah. After the RBM command and constant are sent, the data stored in the memory pointed to by ERDPT will be shifted out MSb first on the SO pin. If the host controller continues to provide clocks on the SCK pin, without raising $\overline{CS}$, the byte pointed to by ERDPT will again be shifted out MSb first on the SO pin. In this manner, with AUTOINC enabled, it is possible to continuously read sequential bytes from the buffer memory without any extra SPI command overhead. The RBM command is terminated by raising the $\overline{CS}$ pin.

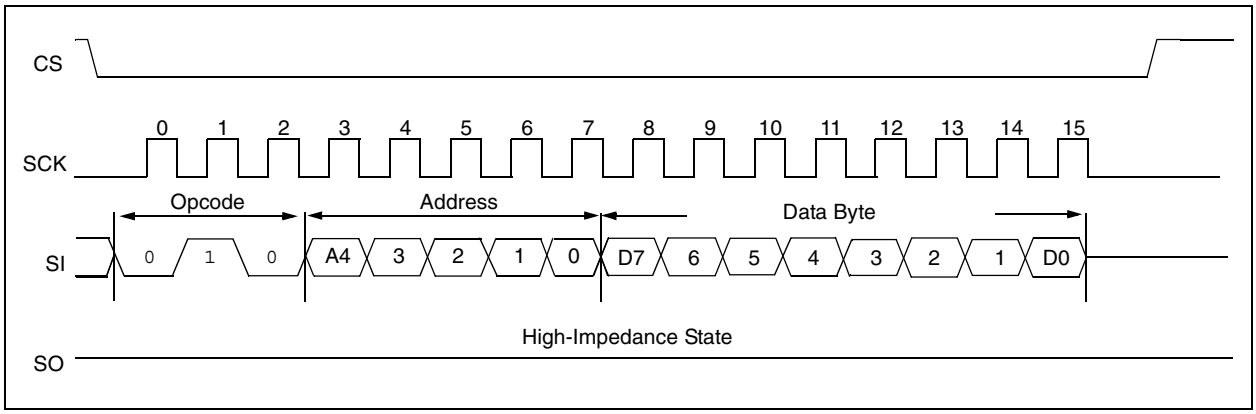
4.2.3 WRITE CONTROL REGISTER COMMAND

The Write Control Register (WCR) command allows the host controller to write to any of the ETH, MAC and MII Control registers in any order. The PHY registers are written to via a special MII register interface (see **Section 3.3.2 "Writing PHY Registers"** for more information).

The WCR command is started by pulling the $\overline{CS}$ pin low. The WCR opcode is then sent to the ENC28J60, followed by a 5-bit address (A4 through A0). The 5-bit address identifies any of the 32 control registers in the current bank. After the WCR command and address are sent, actual data that is to be written is sent, MSb first. The data will be written to the addressed register on the rising edge of the SCK line.

The WCR operation is terminated by raising the $\overline{CS}$ pin. If the $\overline{CS}$ line is allowed to go high before eight bits are loaded, the write will be aborted for that data byte. Refer to the timing diagram in Figure 4-5 for a more detailed illustration of the byte write sequence.

FIGURE 4-5: WRITE CONTROL REGISTER COMMAND SEQUENCE



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4.2.4 WRITE BUFFER MEMORY COMMAND

The Write Buffer Memory (WBM) command allows the host controller to write bytes to the integrated 8-Kbyte transmit and receive buffer memory.

If the AUTOINC bit in the ECON2 register is set, after the last bit of each byte is written, the EWRPT Pointer will automatically be incremented to point to the next sequential address (current address + 1). If address 1FFFh is written with AUTOINC set, the Write Pointer will increment to 0000h.

The WBM command is started by lowering the $\overline{CS}$ pin. The WBM opcode should then be sent to the ENC28J60, followed by the 5-bit constant 1Ah. After the WBM command and constant are sent, the data to be stored in the memory pointed to by EWRPT should be shifted out MSb first to the ENC28J60. After 8 data bits are received, the Write Pointer will automatically increment if AUTOINC is set. The host controller can continue to provide clocks on the SCK pin and send data on the SI pin, without raising $\overline{CS}$, to keep writing to the memory. In this manner, with AUTOINC enabled, it is possible to continuously write sequential bytes to the buffer memory without any extra SPI command overhead.

The WBM command is terminated by bringing up the $\overline{CS}$ pin. Refer to Figure 4-6 for a detailed illustration of the write sequence.

4.2.5 BIT FIELD SET COMMAND

The Bit Field Set (BFS) command is used to set up to 8 bits in any of the ETH Control registers. Note that this command cannot be used on the MAC registers, MII registers, PHY registers or buffer memory. The BFS command uses the provided data byte to perform a bit-wise OR operation on the addressed register contents.

The BFS command is started by pulling the $\overline{CS}$ pin low. The BFS opcode is then sent, followed by a 5-bit address (A4 through A0). The 5-bit address identifies any of the ETH registers in the current bank. After the BFS command and address are sent, the data byte containing the bit field set information should be sent, MSb first. The supplied data will be logically ORed to the content of the addressed register on the rising edge of the SCK line for the D0 bit.

If the $\overline{CS}$ line is brought high before eight bits are loaded, the operation will be aborted for that data byte. The BFS operation is terminated by raising the $\overline{CS}$ pin.

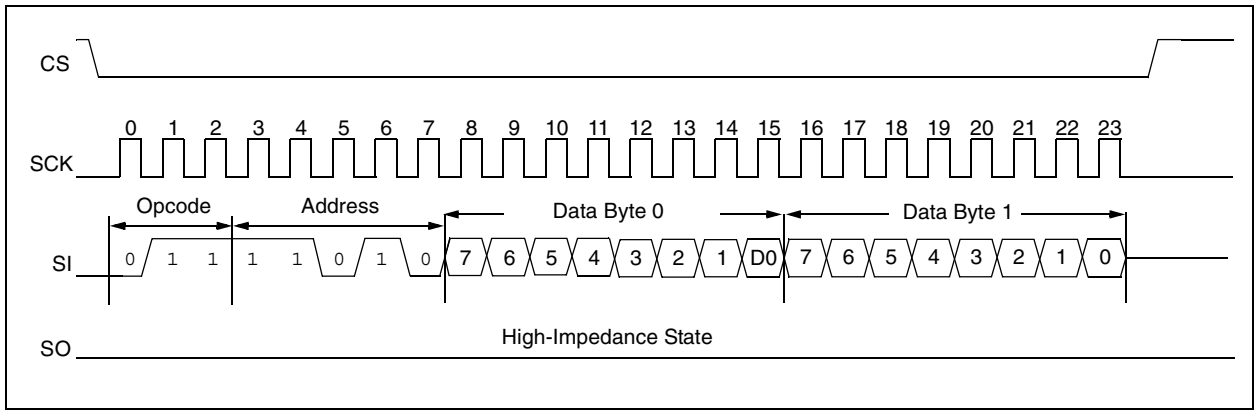
4.2.6 BIT FIELD CLEAR COMMAND

The Bit Field Clear (BFC) command is used to clear up to 8 bits in any of the ETH Control registers. Note that this command cannot be used on the MAC registers, MII registers, PHY registers or buffer memory. The BFC command uses the provided data byte to perform a bit-wise NOTAND operation on the addressed register contents. As an example, if a register had the contents of F1h and the BFC command was executed with an operand of 17h, then the register would be changed to have the contents of E0h.

The BFC command is started by lowering the $\overline{CS}$ pin. The BFC opcode should then be sent, followed by a 5-bit address (A4 through A0). The 5-bit address identifies any of the ETH registers in the current bank. After the BFC command and address are sent, a data byte containing the bit field clear information should be sent, MSb first. The supplied data will be logically inverted and subsequently ANDed to the contents of the addressed register on the rising edge of the SCK line for the D0 bit.

The BFC operation is terminated by bringing the $\overline{CS}$ pin high. If $\overline{CS}$ is brought high before eight bits are loaded, the operation will be aborted for that data byte.

FIGURE 4-6: WRITE BUFFER MEMORY COMMAND SEQUENCE



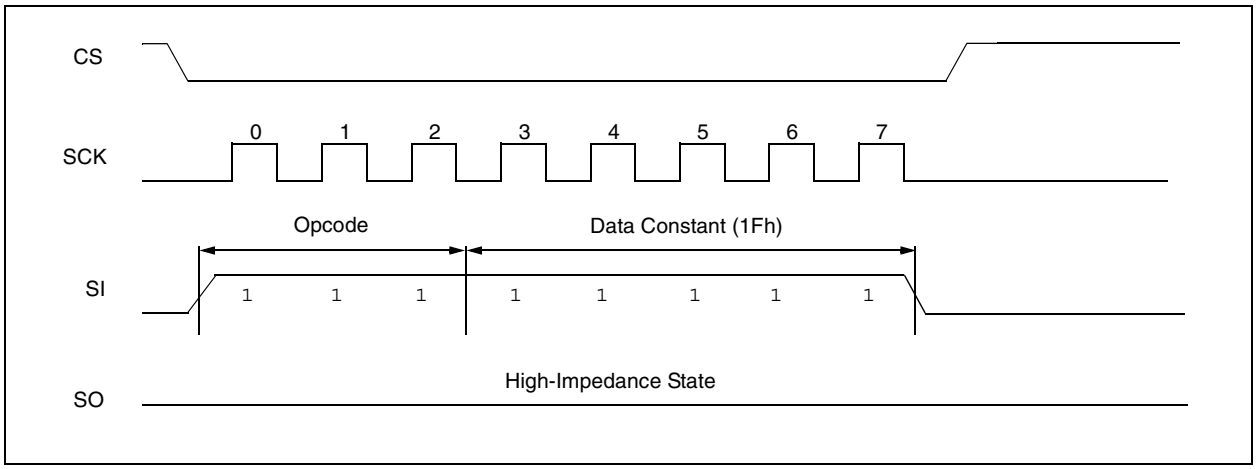
4.2.7 SYSTEM RESET COMMAND

The System Reset Command (SRC) allows the host controller to issue a System Soft Reset command. Unlike other SPI commands, the SRC is only a single-byte command and does not operate on any register.

The command is started by pulling the $\overline{CS}$ pin low. The SRC opcode is the sent, followed by a 5-bit Soft Reset command constant of 1Fh. The SRC operation is terminated by raising the $\overline{CS}$ pin.

Figure 4-7 shows a detailed illustration of the System Reset Command sequence. For more information on SRC's Soft Reset, refer to **Section 11.2 "System Reset"**.

FIGURE 4-7: SYSTEM RESET COMMAND SEQUENCE



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5.0 ETHERNET OVERVIEW

Before discussing the use of the ENC28J60 as an Ethernet interface, it may be helpful to review the structure of a typical data frame. Users requiring more information should refer to IEEE Standard 802.3 which is the basis for the Ethernet protocol.

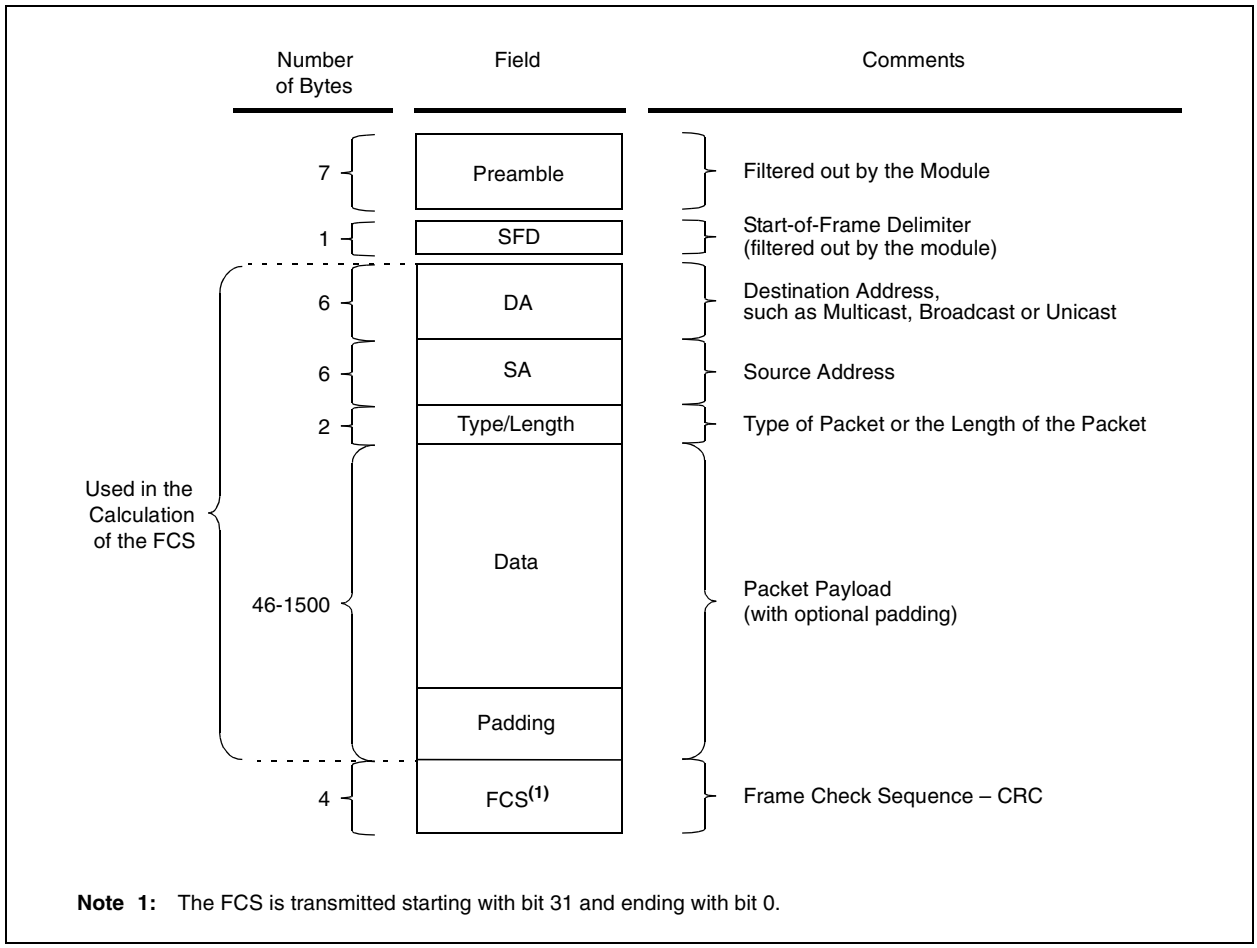
5.1 Packet Format

Normal IEEE 802.3 compliant Ethernet frames are between 64 and 1518 bytes long. They are made up of five or six different fields: a destination MAC address, a source MAC address, a type/length field, data payload, an optional padding field and a Cyclic Redundancy Check (CRC). Additionally, when transmitted on the Ethernet medium, a 7-byte preamble field and start-of-frame delimiter byte are appended to the beginning of the Ethernet packet. Thus, traffic seen on the twisted pair cabling will appear as shown in Figure 5-1.

5.1.1 PREAMBLE/START-OF-FRAME DELIMITER

When transmitting and receiving data with the ENC28J60, the preamble and start of frame delimiter bytes will automatically be generated or stripped from the packets when they are transmitted or received. The host controller does not need to concern itself with them. Normally, the host controller will also not need to concern itself with padding and the CRC which the ENC28J60 will also be able to automatically generate when transmitting and verify when receiving. The padding and CRC fields will, however, be written into the receive buffer when packets arrive, so they may be evaluated by the host controller if needed.

FIGURE 5-1: ETHERNET PACKET FORMAT



Note 1: The FCS is transmitted starting with bit 31 and ending with bit 0.

5.1.2 DESTINATION ADDRESS

The destination address field is a 6-byte field filled with the MAC address of the device that the packet is directed to. If the Least Significant bit in the first byte of the MAC address is set, the address is a multicast destination. For example, 01-00-00-00-F0-00 and 33-45-67-89-AB-CD are multicast addresses, while 00-00-00-00-F0-00 and 32-45-67-89-AB-CD are not.

Packets with multicast destination addresses are designed to arrive and be important to a selected group of Ethernet nodes. If the destination address field is the reserved multicast address, FF-FF-FF-FF-FF-FF, the packet is a broadcast packet and it will be directed to everyone sharing the network. If the Least Significant bit in the first byte of the MAC address is clear, the address is a unicast address and will be designed for usage by only the addressed node.

The ENC28J60 incorporates receive filters which can be used to discard or accept packets with multicast, broadcast and/or unicast destination addresses. When transmitting packets, the host controller is responsible for writing the desired destination address into the transmit buffer.

5.1.3 SOURCE ADDRESS

The source address field is a 6-byte field filled with the MAC address of the node which created the Ethernet packet. Users of the ENC28J60 must generate a unique MAC address for each controller used.

MAC addresses consist of two portions. The first three bytes are known as the Organizationally Unique Identifier (OUI). OUIs are distributed by the IEEE. The last three bytes are address bytes at the discretion of the company that purchased the OUI.

When transmitting packets, the assigned source MAC address must be written into the transmit buffer by the host controller. The ENC28J60 will not automatically transmit the contents of the MAADR registers which are used for the unicast receive filter.

5.1.4 TYPE/LENGTH

The type/length field is a 2-byte field which defines which protocol the following packet data belongs to. Alternately, if the field is filled with the contents of 05DCh (1500) or any smaller number, the field is considered a length field and it specifies the amount of non-padding data which follows in the data field. Users implementing proprietary networks may choose to treat this field as a length field, while applications implementing protocols such as the Internet Protocol (IP) or Address Resolution Protocol (ARP), should program this field with the appropriate type defined by the protocol's specification when transmitting packets.

5.1.5 DATA

The data field is a variable length field anywhere from 0 to 1500 bytes. Larger data packets will violate Ethernet standards and will be dropped by most Ethernet nodes. The ENC28J60, however, is capable of transmitting and receiving larger packets when the Huge Frame Enable bit is set (MACON3.HFRMEN = 1).

5.1.6 PADDING

The padding field is a variable length field added to meet IEEE 802.3 specification requirements when small data payloads are used. The destination, source, type, data and padding of an Ethernet packet must be no smaller than 60 bytes. Adding the required 4-byte CRC field, packets must be no smaller than 64 bytes. If the data field is less than 46 bytes long, a padding field is required.

When transmitting packets, the ENC28J60 automatically generates zero padding if the MACON3.PADCFG<2:0> bits are configured to do so. Otherwise, the host controller should manually add padding to the packet before transmitting it. The ENC28J60 will not prevent the transmission of undersize packets should the host controller command such an action.

When receiving packets, the ENC28J60 automatically rejects packets which are less than 18 bytes; it is assumed that a packet this small does not contain even the minimum of source and destination addresses, type information and FCS checksum required for all packets. All packets 18 bytes and larger will be subject to the standard receive filtering criteria and may be accepted as normal traffic. To conform with IEEE 802.3 requirements, the application itself will need to inspect all received packets and reject those smaller than 64 bytes.

5.1.7 CRC

The CRC field is a 4-byte field which contains an industry standard 32-bit CRC calculated with the data from the destination, source, type, data and padding fields.

When receiving packets, the ENC28J60 will check the CRC of each incoming packet. If ERXFCON.CRCEN is set, packets with invalid CRCs will automatically be discarded. If CRCEN is clear and the packet meets all other receive filtering criteria, the packet will be written into the receive buffer and the host controller will be able to determine if the CRC was valid by reading the receive status vector (see **Section 7.2 "Receiving Packets"**).

When transmitting packets, the ENC28J60 will automatically generate a valid CRC and transmit it if the MACON3.PADCFG<2:0> bits are configured to cause this. Otherwise, the host controller must generate the CRC and place it in the transmit buffer. Given the complexity of calculating a CRC, it is highly recommended that the PADCFG bits be configured such that the ENC28J60 will automatically generate the CRC field.

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6.0 INITIALIZATION

Before the ENC28J60 can be used to transmit and receive packets, certain device settings must be initialized. Depending on the application, some configuration options may need to be changed. Normally, these tasks may be accomplished once after Reset and do not need to be changed thereafter.

6.1 Receive Buffer

Before receiving any packets, the receive buffer must be initialized by programming the ERXST and ERXND Pointers. All memory between and including the ERXST and ERXND addresses will be dedicated to the receive hardware. It is recommended that the ERXST Pointer be programmed with an even address.

Applications expecting large amounts of data and frequent packet delivery may wish to allocate most of the memory as the receive buffer. Applications that may need to save older packets or have several packets ready for transmission should allocate less memory.

When programming the ERXST or ERXND Pointer, the internal hardware copy of the ERXWRPT registers will automatically be updated with the value of ERXST. This value will be used as the starting location when the receive hardware begins writing received data. The ERXWRPT registers are updated by the hardware only when a new packet is successfully received.

Note:	After writing to ERXST or ERXND, the ERXWRPT registers are not updated immediately; only the internal hardware copy of the ERXWRPT registers is updated. Therefore, comparing if (ERXWRPT = = ERXST) is not practical in a firmware initialization routine.

For tracking purposes, the ERXRDPT registers should additionally be programmed with the same value. To program ERXRDPT, the host controller must write to ERXRDPTL first, followed by ERXRDPTH. See **Section 7.2.4 "Freeing Receive Buffer Space"** for more information.

6.2 Transmission Buffer

All memory which is not used by the receive buffer is considered the transmission buffer. Data which is to be transmitted should be written into any unused space. After a packet is transmitted, however, the hardware will write a seven-byte status vector into memory after the last byte in the packet. Therefore, the host controller should leave at least seven bytes between each packet and the beginning of the receive buffer. No explicit action is required to initialize the transmission buffer.

6.3 Receive Filters

The appropriate receive filters should be enabled or disabled by writing to the ERXFCON register. See **Section 8.0 "Receive Filters"** for information on how to configure it.

6.4 Waiting For OST

If the initialization procedure is being executed immediately following a Power-on Reset, the ESTAT.CLKRDY bit should be polled to make certain that enough time has elapsed before proceeding to modify the MAC and PHY registers. For more information on the OST, see **Section 2.2 "Oscillator Start-up Timer"**.

6.5 MAC Initialization Settings

Several of the MAC registers require configuration during initialization. This only needs to be done once; the order of programming is unimportant.

1. Set the MARXEN bit in MACON1 to enable the MAC to receive frames. If using full duplex, most applications should also set TXPAUS and RXPAUS to allow IEEE defined flow control to function.
2. Configure the PADCFG, TXCRCEN and FULDPX bits of MACON3. Most applications should enable automatic padding to at least 60 bytes and always append a valid CRC. For convenience, many applications may wish to set the FRMLNEN bit as well to enable frame length status reporting. The FULDPX bit should be set if the application will be connected to a full-duplex configured remote node; otherwise, it should be left clear.
3. Configure the bits in MACON4. For conformance to the IEEE 802.3 standard, set the DEFER bit.
4. Program the MAMXFL registers with the maximum frame length to be permitted to be received or transmitted. Normal network nodes are designed to handle packets that are 1518 bytes or less.
5. Configure the Back-to-Back Inter-Packet Gap register, MABBIPG. Most applications will program this register with 15h when Full-Duplex mode is used and 12h when Half-Duplex mode is used.
6. Configure the Non-Back-to-Back Inter-Packet Gap register low byte, MAIPGL. Most applications will program this register with 12h.
7. If half duplex is used, the Non-Back-to-Back Inter-Packet Gap register high byte, MAIPGH, should be programmed. Most applications will program this register to 0Ch.
8. If Half-Duplex mode is used, program the Retransmission and Collision Window registers, MACLCON1 and MACLCON2. Most applications will not need to change the default Reset values. If the network is spread over exceptionally long cables, the default value of MACLCON2 may need to be increased.
9. Program the local MAC address into the MAADR1:MAADR6 registers.

REGISTER 6-1: MACON1: MAC CONTROL REGISTER 1

U-0	U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	r	TXPAUS	RXPAUS	PASSALL	MARXEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **Reserved:** Maintain as '0'

bit 3 **TXPAUS:** Pause Control Frame Transmission Enable bit
- 1 = Allow the MAC to transmit pause control frames (needed for flow control in full duplex)
- 0 = Disallow pause frame transmissions

bit 2 **RXPAUS:** Pause Control Frame Reception Enable bit
- 1 = Inhibit transmissions when pause control frames are received (normal operation)
- 0 = Ignore pause control frames which are received

bit 1 **PASSALL:** Pass All Received Frames Enable bit
- 1 = Control frames received by the MAC will be written into the receive buffer if not filtered out
- 0 = Control frames will be discarded after being processed by the MAC (normal operation)

bit 0 **MARXEN:** MAC Receive Enable bit
- 1 = Enable packets to be received by the MAC
- 0 = Disable packet reception

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REGISTER 6-2: MACON3: MAC CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PADCFG2	PADCFG1	PADCFG0	TXCRCEN	PHDREN	HFRMEN	FRMLNEN	FULDPX
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **PADCFG2:PADCFG0:** Automatic Pad and CRC Configuration bits

111 = All short frames will be zero padded to 64 bytes and a valid CRC will then be appended
110 = No automatic padding of short frames
101 = MAC will automatically detect VLAN Protocol frames which have a 8100h type field and automatically pad to 64 bytes. If the frame is not a VLAN frame, it will be padded to 60 bytes. After padding, a valid CRC will be appended.
100 = No automatic padding of short frames
011 = All short frames will be zero padded to 64 bytes and a valid CRC will then be appended
010 = No automatic padding of short frames
001 = All short frames will be zero padded to 60 bytes and a valid CRC will then be appended
000 = No automatic padding of short frames

bit 4 **TXCRCEN:** Transmit CRC Enable bit

1 = MAC will apend a valid CRC to all frames transmitted regardless of PADCFG. TXCRCEN must be set if PADCFG specifies that a valid CRC will be appended.
0 = MAC will not append a CRC. The last 4 bytes will be checked and if it is an invalid CRC, it will be reported in the transmit status vector.

bit 3 **PHDREN:** Proprietary Header Enable bit

1 = Frames presented to the MAC contain a 4-byte proprietary header which will not be used when calculating the CRC
0 = No proprietary header is present. The CRC will cover all data (normal operation).

bit 2 **HFRMEN:** Huge Frame Enable bit

1 = Frames of any size will be allowed to be transmitted and receieved
0 = Frames bigger than MAMXFL will be aborted when transmitted or received

bit 1 **FRMLNEN:** Frame Length Checking Enable bit

1 = The type/length field of transmitted and received frames will be checked. If it represents a length, the frame size will be compared and mismatches will be reported in the transmit/receive status vector.
0 = Frame lengths will not be compared with the type/length field

bit 0 **FULDPX:** MAC Full-Duplex Enable bit

1 = MAC will operate in Full-Duplex mode. PDPXMD bit must also be set.
0 = MAC will operate in Half-Duplex mode. PDPXMD bit must also be clear.

REGISTER 6-3: MACON4: MAC CONTROL REGISTER 4

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R-0	R-0
—	DEFER	BPEN	NOBKOFF	—	—	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **DEFER:** Defer Transmission Enable bit (applies to half duplex only)
- 1 = When the medium is occupied, the MAC will wait indefinitely for it to become free when attempting to transmit (use this setting for 802.3 compliance)
- 0 = When the medium is occupied, the MAC will abort the transmission after the excessive deferral limit is reached

bit 5 **BPEN:** No Backoff During Backpressure Enable bit (applies to half duplex only)
- 1 = After incidentally causing a collision during backpressure, the MAC will immediately begin retransmitting
- 0 = After incidentally causing a collision during backpressure, the MAC will delay using the Binary Exponential Backoff algorithm before attempting to retransmit (normal operation)

bit 4 **NOBKOFF:** No Backoff Enable bit (applies to half duplex only)
- 1 = After any collision, the MAC will immediately begin retransmitting
- 0 = After any collision, the MAC will delay using the Binary Exponential Backoff algorithm before attempting to retransmit (normal operation)

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Maintain as '0'

REGISTER 6-4: MABBIPG: MAC BACK-TO-BACK INTER-PACKET GAP REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	BBIPG6	BBIPG5	BBIPG4	BBIPG3	BBIPG2	BBIPG1	BBIPG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **BBIPG6:BBIPG0:** Back-to-Back Inter-Packet Gap Delay Time bits

When FULDPX (MACON3<0>) = 1:

Nibble time offset delay between the end of one transmission and the beginning of the next in a back-to-back sequence. The register value should be programmed to the desired period in nibble times minus 3. The recommended setting is 15h which represents the minimum IEEE specified Inter-Packet Gap (IPG) of 9.6 µs.

When FULDPX (MACON3<0>) = 0:

Nibble time offset delay between the end of one transmission and the beginning of the next in a back-to-back sequence. The register value should be programmed to the desired period in nibble times minus 6. The recommended setting is 12h which represents the minimum IEEE specified Inter-Packet Gap (IPG) of 9.6 µs.

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6.6 PHY Initialization Settings

Depending on the application, bits in three of the PHY module's registers may also require configuration.

The PHCON1.PDPXMD bit partially controls the device's half/full-duplex configuration. Normally, this bit is initialized correctly by the external circuitry (see **Section 2.6 "LED Configuration"**). If the external circuitry is not present or incorrect, however, the host controller must program the bit properly. Alternatively, for an externally configurable system, the PDPXMD bit may be read and the FULDPX bit be programmed to match.

For proper duplex operation, the PHCON1.PDPXMD bit must also match the value of the MACON3.FULDPX bit.

If using half duplex, the host controller may wish to set the PHCON2.HDLDIS bit to prevent automatic loopback of the data which is transmitted.

The PHY register, PHLCON, controls the outputs of LEDA and LEDB. If an application requires a LED configuration other than the default, PHLCON must be altered to match the new requirements. The settings for LED operation are discussed in **Section 2.6 "LED Configuration"**. The PHLCON register is shown in Register 2-2 (page 9).

REGISTER 6-5: PHCON2: PHY CONTROL REGISTER 2

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FRCLNK	TXDIS	r	r	JABBER	r	HDLDIS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	r	r	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **FRCLNK:** PHY Force Linkup bit
1 = Force linkup even when no link partner is detected
0 = Normal operation

bit 13 **TXDIS:** Twisted-Pair Transmitter Disable bit
1 = Disable twisted-pair transmitter
0 = Normal operation

bit 12-11 **Reserved:** Write as '0'

bit 10 **JABBER:** Jabber Correction Disable bit
1 = Disable jabber correction
0 = Normal operation

bit 9 **Reserved:** Write as '0'

bit 8 **HDLDIS:** PHY Half-Duplex Loopback Disable bit
When PHCON1<8> = 1 or PHCON1<14> = 1:
This bit is ignored.
When PHCON1<8> = 0 and PHCON1<14> = 0:
1 = Transmitted data will only be sent out on the twisted-pair interface
0 = Transmitted data will be looped back to the MAC and sent out on the twisted-pair interface

bit 7-0 **Reserved:** Write as '0'

NOTES:

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7.0 TRANSMITTING AND RECEIVING PACKETS

7.1 Transmitting Packets

The MAC inside the ENC28J60 will automatically generate the preamble and start-of-frame delimiter fields when transmitting. Additionally, the MAC can generate any padding (if needed) and the CRC if configured to do so. The host controller must generate and write all other frame fields into the buffer memory for transmission.

Additionally, the ENC28J60 requires a single per packet control byte to precede the packet for transmission. The per packet control byte is organized as shown in Figure 7-1. Before transmitting packets, the MAC registers which alter the transmission characteristics should be initialized as documented in **Section 6.0 "Initialization"**.

For an example of how the entire transmit packet and results will look in memory, see Figure 7-2.

FIGURE 7-1: FORMAT FOR PER PACKET CONTROL BYTES

—	—	—	—	PHUGEEN	PPADEN	PCRCEN	POVERRIDE
bit 7							bit 0

bit 7-4 **Unused**

bit 3 **PHUGEEN:** Per Packet Huge Frame Enable bit

When POVERRIDE = 1:

1 = The packet will be transmitted in whole

0 = The MAC will transmit up to the number of bytes specified by MAMXFL. If the packet is larger than MAMXFL, it will be aborted after MAMXFL is reached.

When POVERRIDE = 0:

This bit is ignored.

bit 2 **PPADEN:** Per Packet Padding Enable bit

When POVERRIDE = 1:

1 = The packet will be zero padded to 60 bytes if it is less than 60 bytes

0 = The packet will be trasmitted without adding any padding bytes

When POVERRIDE = 0:

This bit is ignored.

bit 1 **PCRCEN:** Per Packet CRC Enable bit

When POVERRIDE = 1:

1 = A valid CRC will be calculated and attached to the frame

0 = No CRC will be appended. The last 4 bytes of the frame will be checked for validity as a CRC.

When POVERRIDE = 0:

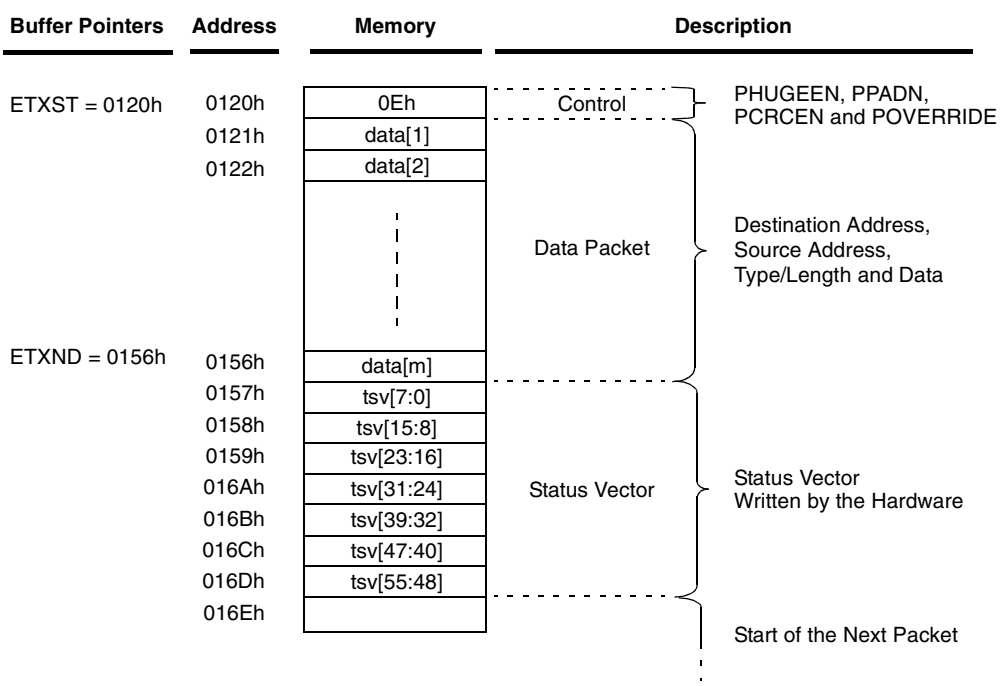
This bit is ignored.

bit 0 **POVERRIDE:** Per Packet Override bit

1 = The values of PCRCEN, PPADEN and PHUGEEN will override the configuration defined by MACON3

0 = The values in MACON3 will be used to determine how the packet will be transmitted

FIGURE 7-2: SAMPLE TRANSMIT PACKET LAYOUT



To achieve the example layout shown in Figure 7-2 and to transmit a packet, the host controller should:

1. Appropriately program the ETXST Pointer to point to an unused location in memory. It will point to the per packet control byte. In the example, it would be programmed to 0120h. It is recommended that an even address be used for ETXST.
2. Use the WBM SPI command to write the per packet control byte, the destination address, the source MAC address, the type/length and the data payload.
3. Appropriately program the ETXND Pointer. It should point to the last byte in the data payload. In the example, it would be programmed to 0156h.
4. Clear EIR.TXIF, set EIE.TXIE and set EIE.INTIE to enable an interrupt when done (if desired).
5. Start the transmission process by setting ECON1.TXRTS.

If a DMA operation was in progress while the TXRTS bit was set, the ENC28J60 will wait until the DMA operation is complete before attempting to transmit the packet. This possible delay is required because the DMA and transmission engine share the same memory access port. Similarly, if the DMAST bit in ECON1 is set after TXRTS is already set, the DMA will wait until the TXRTS bit becomes clear before doing anything. While the transmission is in progress, none of the unshaded bits (except for the EECON1 register's bits) in Table 7-2 should be changed. Additionally, none of the bytes to be transmitted should be read or written to through the SPI. If the host controller wishes to cancel the transmission, it can clear the TXRTS bit.

When the packet is finished transmitting or was aborted due to an error/cancellation, the ECON1.TXRTS bit will be cleared, a seven-byte transmit status vector will be written to the location pointed to by ETXND + 1, the EIR.TXIF will be set and an interrupt will be generated (if enabled). The ETXST and ETXND Pointers will not be modified. To check if the packet was successfully transmitted, the ESTAT.TXABRT bit should be read. If it was set, the host controller may interrogate the ESTAT.LATECOL bit in addition to the various fields in the transmit status vector to determine the cause. The transmit status vector is organized as shown in Table 7-1. Multi-byte fields are written in little-endian format.

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TABLE 7-1: TRANSMIT STATUS VECTORS

Bit	Field	Description
55-52	Zero	0
51	Transmit VLAN Tagged Frame	Frame's length/type field contained 8100h which is the VLAN protocol identifier.
50	Backpressure Applied	Carrier sense method backpressure was previously applied.
49	Transmit Pause Control Frame	The frame transmitted was a control frame with a valid pause opcode.
48	Transmit Control Frame	The frame transmitted was a control frame.
47-32	Total Bytes Transmitted on Wire	Total bytes transmitted on the wire for the current packet, including all bytes from collided attempts.
31	Transmit Underrun	Reserved. This bit will always be '0'.
30	Transmit Giant	Byte count for frame was greater than MAMXFL.
29	Transmit Late Collision	Collision occurred beyond the collision window (MACLCON2).
28	Transmit Excessive Collision	Packet was aborted after the number of collisions exceeded the retransmission maximum (MACLCON1).
27	Transmit Excessive Defer	Packet was deferred in excess of 24,287 bit times (2.4287ms).
26	Transmit Packet Defer	Packet was deferred for at least one attempt but less than an excessive defer.
25	Transmit Broadcast	Packet's destination address was a broadcast address.
24	Transmit Multicast	Packet's destination address was a multicast address.
23	Transmit Done	Transmission of the packet was completed.
22	Transmit Length Out of Range	Indicates that frame type/length field was larger than 1500 bytes (type field).
21	Transmit Length Check Error	Indicates that frame length field value in the packet does not match the actual data byte length and is not a type field. MACON3.FRMLNEN must be set to get this error.
20	Transmit CRC Error	The attached CRC in the packet did not match the internally generated CRC.
19-16	Transmit Collision Count	Number of collisions the current packet incurred during transmission attempts. It applies to successfully transmitted packets and as such, will not show the possible maximum count of 16 collisions.
15-0	Transmit Byte Count	Total bytes in frame not counting collided bytes.

TABLE 7-2: SUMMARY OF REGISTERS USED FOR PACKET TRANSMISSION

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
EIE	INTIE	PKTIE	DMAIE	LINKIE	TXIE	r	TXERIE	RXERIE	13
EIR	—	PKTIF	DMAIF	LINKIF	TXIF	r	TXERIF	RXERIF	13
ESTAT	INT	BUFER	r	LATECOL	—	RXBUSY	TXABRT	CLKRDY	13
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	13
ETXSTL	TX Start Low Byte (ETXST<7:0>)								13
ETXSTH	—	—	—	TX Start High Byte (ETXST<12:8>)					13
ETXNDL	TX End Low Byte (ETXND<7:0>)								13
ETXNDH	—	—	—	TX End High Byte (ETXND<12:8>)					13
MACON1	—	—	—	r	TXPAUS	RXPAUS	PASSALL	MARXEN	14
MACON3	PADCFG2	PADCFG1	PADCFG0	TXCRCEN	PHDREN	HFRMEN	FRMLNEN	FULDPX	14
MACON4	—	DEFER	BPEN	NOBKOFF	—	—	r	r	14
MABBIPG	—	Back-to-Back Inter-Packet Gap (BBIPG<6:0>)							14
MAIPGL	—	Non-Back-to-Back Inter-Packet Gap Low Byte (MAIPGL<6:0>)							14
MAIPGH	—	Non-Back-to-Back Inter-Packet Gap High Byte (MAIPGH<6:0>)							14
MACLCON1	—	—	—	—	Retransmission Maximum (RETMAX<3:0>)				14
MACLCON2	—	—	Collision Window (COLWIN<5:0>)						14
MAMXFLL	Maximum Frame Length Low Byte (MAMXFL<7:0>)								14
MAMXFLH	Maximum Frame Length High Byte (MAMXFL<15:8>)								14

Legend: — = unimplemented, r = reserved bit. Shaded cells are not used.

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7.2 Receiving Packets

7.2.1 ENABLING RECEPTION

Assuming that the receive buffer has been initialized, the MAC has been properly configured and the receive filters have been configured to receive Ethernet packets, the host controller should:

1. If an interrupt is desired whenever a packet is received, set EIE.PKTIE and EIE.INTIE.
2. If an interrupt is desired whenever a packet is dropped due to insufficient buffer space, clear EIR.RXERIF and set both EIE.RXERIE and EIE.INTIE
3. Enable reception by setting ECON1.RXEN.

After setting RXEN, the Duplex mode and the Receive Buffer Start and End Pointers should not be modified. Additionally, to prevent unexpected packets from arriving, it is recommended that RXEN be cleared before altering the receive filter configuration (ERXFCON) and MAC address.

After reception is enabled, packets which are not filtered out will be written into the circular receive buffer. Any packet which does not meet the necessary filter criteria will be discarded and the host controller will not have any means of identifying that a packet was thrown away. When a packet is accepted and completely written into the buffer, the EPKTCNT register will increment, the EIR.PKTIF bit will be set, an interrupt will be generated (if enabled) and the Hardware Write Pointer, ERXWRPT, will automatically advance.

7.2.2 RECEIVE PACKET LAYOUT

Figure 7-3 shows the layout of a received packet. The packets are preceded by a six-byte header which contains a Next Packet Pointer, in addition to a receive status vector which contains receive statistics, including the packet's size. This receive status vector is shown in Table 7-3.

If the last byte in the packet ends on an odd value address, the hardware will automatically add a padding byte when advancing the Hardware Write Pointer. As such, all packets will start on an even boundary.

FIGURE 7-3: SAMPLE RECEIVE PACKET LAYOUT

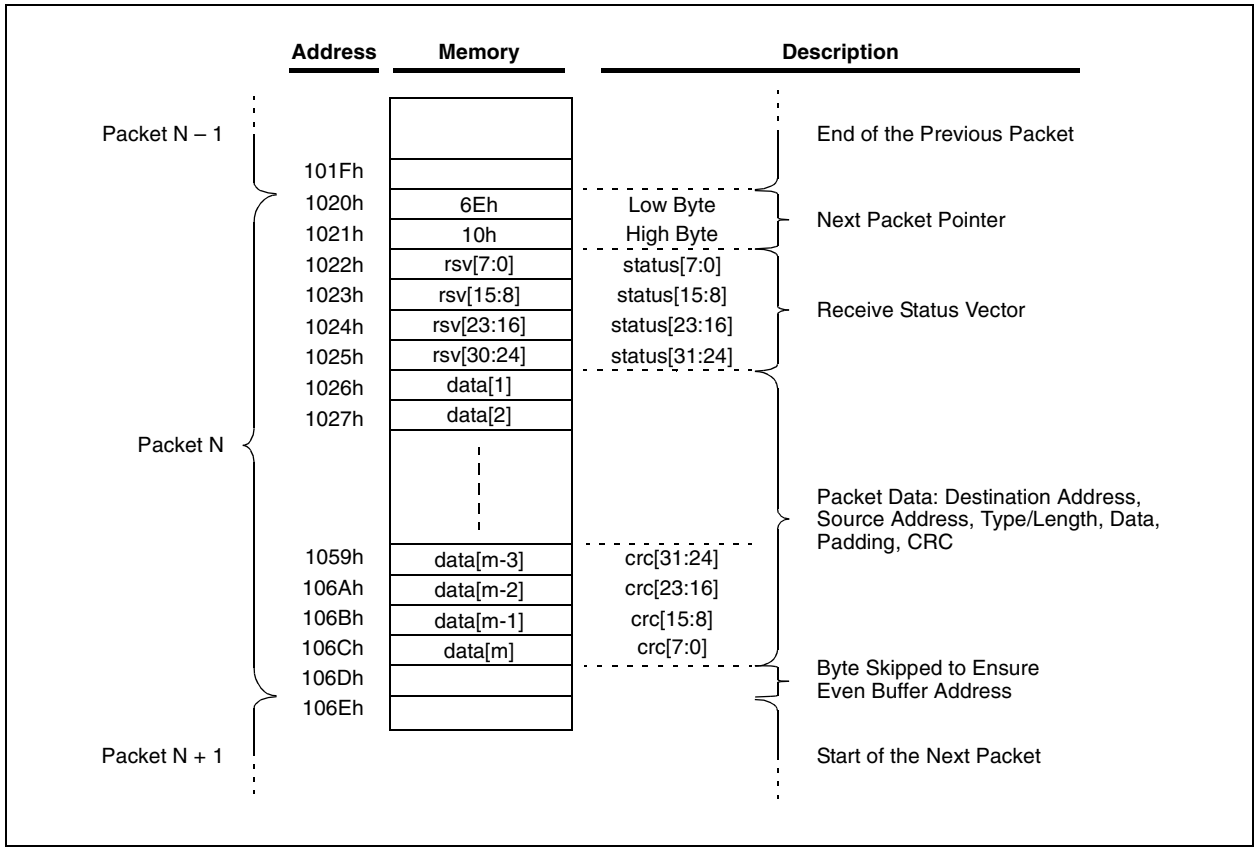


TABLE 7-3: RECEIVE STATUS VECTORS

Bit	Field	Description
31	Zero	0
30	Receive VLAN Type Detected	Current frame was recognized as a VLAN tagged frame.
29	Receive Unknown Opcode	Current frame was recognized as a control frame but it contained an unknown opcode.
28	Receive Pause Control Frame	Current frame was recognized as a control frame containing a valid pause frame opcode and a valid destination address.
27	Receive Control Frame	Current frame was recognized as a control frame for having a valid type/length designating it as a control frame.
26	Dribble Nibble	Indicates that after the end of this packet, an additional 1 to 7 bits were received. The extra bits were thrown away.
25	Receive Broadcast Packet	Indicates packet received had a valid broadcast address.
24	Receive Multicast Packet	Indicates packet received had a valid multicast address.
23	Received Ok	Indicates that at the packet had a valid CRC and no symbol errors.
22	Length Out of Range	Indicates that frame type/length field was larger than 1500 bytes (type field).
21	Length Check Error	Indicates that frame length field value in the packet does not match the actual data byte length and specifies a valid length.
20	CRC Error	Indicates that frame CRC field value does not match the CRC calculated by the MAC.
19	Reserved	
18	Carrier Event Previously Seen	Indicates that at some time since the last receive, a carrier event was detected. The carrier event is not associated with this packet. A carrier event is activity on the receive channel that does not result in a packet receive attempt being made.
17	Reserved	
16	Long Event/Drop Event	Indicates a packet over 50,000 bit times occurred or that a packet was dropped since the last receive.
15-0	Received Byte Count	Indicates length of the received frame. This includes the destination address, source address, type/length, data, padding and CRC fields. This field is stored in little-endian format.

7.2.3 READING RECEIVED PACKETS

To process the packet, the host controller will normally use the RBM SPI command and start reading from the beginning of the next Packet Pointer. The host controller will save the next Packet Pointer, any necessary bytes from the receive status vector and then proceed to read the actual packet contents. If ECON2.AUTOINC is set, it will be able to sequentially read the entire packet without ever modifying the ERDPT registers. The Read Pointer would automatically wrap at the end of the circular receive buffer to the beginning.

In the event that the application needed to do random access to the packet, it would be necessary to manually calculate the proper ERDPT, taking care to not exceed the end of the receive buffer if the packet spans the ERXND-to-ERXST buffer boundary. In other words, given the packet start address and a desired offset, the application should follow the logic shown in Example 7-1.

EXAMPLE 7-1: RANDOM ACCESS ADDRESS CALCULATION

```
if Packet Start Address + Offset > ERXND, then
        ERDPT = Packet Start Address + Offset – (ERXND – ERXST + 1)
else
        ERDPT = Packet Start Address + Offset
```

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7.2.4 FREEING RECEIVE BUFFER SPACE

After the host controller has processed a packet (or part of the packet) and wishes to free the buffer space used by the processed data, the host controller must advance the Receive Buffer Read Pointer, ERXRDPT. The ENC28J60 will always write up to, but not including, the memory pointed to by the Receive Buffer Read Pointer. If the ENC28J60 ever attempts to overwrite the Receive Buffer Read Pointer location, the packet in progress will be aborted, the EIR.RXERIF will be set and an interrupt will be generated (if enabled). In this manner, the hardware will never overwrite unprocessed packets. Normally, the ERXRDPT will be advanced to the value pointed to by the next Packet Pointer which precedes the receive status vector for the current packet. Following such a procedure will not require any Pointer calculations to account for wrapping at the end of the circular receive buffer.

The Receive Buffer Read Pointer Low Byte (ERXRDPTL register) is internally buffered to prevent the Pointer from moving when only one byte is updated through the SPI. To move ERXRDPT, the host controller must write to ERXRDPTL first. The write will update the internal buffer but will not affect the register. When the host controller writes to ERXRDPTH, the internally buffered low byte will be loaded into the ERXRDPTL register at the same time. The ERXRDPT bytes can be read in any order. When they are read, the actual value of the registers will be returned. As a result, the buffered low byte is not readable.

In addition to advancing the Receive Buffer Read Pointer, after each packet is fully processed, the host controller must write a '1' to the ECON2.PKTDEC bit. Doing so will cause the EPKTCNT register to decrement by 1. After decrementing, if EPKTCNT is '0', the EIR.PKTIF flag will automatically be cleared. Otherwise, it will remain set, indicating that additional packets are in the receive buffer and are waiting to be processed. Attempts to decrement EPKTCNT below 0 are ignored. Additionally, if the EPKTCNT register ever maximizes at 255, all new packets which are received will be aborted, even if buffer space is available. To indicate the error, the EIR.RXERIF will be set and an interrupt will be generated (if enabled). To prevent this condition, the host controller must properly decrement the counter whenever a packet is processed.

Because only one Pointer is available to control buffer area ownership, the host controller must process packets in the order they are received. If the host controller wishes to save a packet to be processed later, it should copy the packet to an unused location in memory. It may accomplish this efficiently using the integrated DMA controller (see **Section 13.0 "Direct Memory Access Controller"**).

7.2.5 RECEIVE BUFFER FREE SPACE

At any time the host controller wishes to know how much receive buffer space is remaining, it should read the Hardware Write Pointer (ERXWRPT registers) and compare it with the ERXRDPT registers. Combined with the known size of the receive buffer, the free space can be derived.

Note:	The ERXWRPT registers only update when a packet has been successfully received. If the host controller reads it just before another packet is to be successfully completed, the value returned could be stale and off by the maximum frame length permitted (MAMXFLN) plus 7. Furthermore, as the host controller reads one byte of ERXWRPT, a new packet may arrive and update the Pointer before the host controller has an opportunity to read the other byte of ERXWRPT.

When reading the ERXWRPT register with the receive hardware enabled, special care must be taken to ensure the low and high bytes are read as a matching set.

To be assured that a matching set is obtained:

1. Read the EPKTCNT register and save its contents.
2. Read ERXWRPTL and ERXWRPTH.
3. Read the EPKTCNT register again.
4. Compare the two packet counts. If they are not the same, go back to step 2.

With the Hardware Write Pointer obtained, the free space can be calculated as shown in Example 7-2. The hardware prohibits moving the Write Pointer to the same value occupied by ERXRDPT (except when the Buffer Pointers are being configured), so at least one byte will always go unused in the buffer. The example calculation reflects the lost byte.

EXAMPLE 7-2: RECEIVE BUFFER FREE SPACE CALCULATION

```
if ERXWRPT > ERXRDPT, then
        Free Space = (ERXND – ERXST) – (ERXWRPT – ERXRDPT)
else if ERXWRPT = ERXRDPT, then
        Free Space = (ERXND – ERXST)
else
        Free Space = ERXRDPT – ERXWRPT – 1
```

TABLE 7-4: SUMMARY OF REGISTERS USED FOR PACKET RECEPTION

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
EIE	INTIE	PKTIE	DMAIE	LINKIE	TXIE	r	TXERIE	RXERIE	13
EIR	—	PKTIF	DMAIF	LINKIF	TXIF	r	TXERIF	RXERIF	13
ESTAT	INT	BUFER	r	LATECOL	—	RXBUSY	TXABRT	CLKRDY	13
ECON2	AUTOINC	PKTDEC	PWRSV	r	VRPS	—	—	—	13
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	13
ERXSTL	RX Start Low Byte (ERXST<7:0>)								13
ERXSTH	—	—	—	RX Start High Byte (ERXST<12:8>)					13
ERXNDL	RX End Low Byte (ERXND<7:0>)								13
ERXNDH	—	—	—	RX End High Byte (ERXND<12:8>)					13
ERXRDPTL	RX RD Pointer Low Byte (ERXRDPT<7:0>)								13
ERXRDPTH	—	—	—	RX RD Pointer High Byte (ERXRDPT<12:8>)					13
ERXFCON	UCEN	ANDOR	CRCEN	PMEN	MPEN	HTEN	MCEN	BCEN	14
EPKTCNT	Ethernet Packet Count								14
MACON1	—	—	—	r	TXPAUS	RXPAUS	PASSALL	MARXEN	14
MACON3	PADCFG2	PADCFG1	PADCFG0	TXCRCEN	PHDREN	HFRMEN	FRMLNEN	FULDPX	14
MAMXFLL	Maximum Frame Length Low Byte (MAMXFL<7:0>)								14
MAMXFLH	Maximum Frame Length High Byte (MAMXFL<15:8>)								14

Legend: — = unimplemented, r = reserved bit. Shaded cells are not used.

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8.0 RECEIVE FILTERS

To minimize the processing requirements of the host controller, the ENC28J60 incorporates several different receive filters which can automatically reject packets which are not needed. Six different types of packet filters are implemented:

- Unicast
- Pattern Match
- Magic Packet™
- Hash Table
- Multicast
- Broadcast

The individual filters are all configured by the ERXFCON register (Register 8-1). More than one filter can be active at any given time. Additionally, the filters can be configured by the ANDOR bit to either logically AND, or logically OR, the tests of several filters. In other words, the filters may be set so that only packets accepted by all active filters are accepted, or a packet accepted by any one filter is accepted. The flowcharts in Figure 8-1 and Figure 8-2 show the effect that each of the filters will have depending on the setting of ANDOR.

The device can enter Promiscuous mode and receive all packets by clearing the ERXFCON register. The proper setting of the register will depend on the application requirements.

REGISTER 8-1: ERXFCON: ETHERNET RECEIVE FILTER CONTROL REGISTER

R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
UCEN	ANDOR	CRCEN	PMEN	MPEN	HTEN	MCEN	BCEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **UCEN:** Unicast Filter Enable bit
When ANDOR = 1:
1 = Packets not having a destination address matching the local MAC address will be discarded
0 = Filter disabled
When ANDOR = 0:
1 = Packets with a destination address matching the local MAC address will be accepted
0 = Filter disabled

bit 6 **ANDOR:** AND/OR Filter Select bit
1 = AND: Packets will be rejected unless all enabled filters accept the packet
0 = OR: Packets will be accepted unless all enabled filters reject the packet

bit 5 **CRCEN:** Post-Filter CRC Check Enable bit
1 = All packets with an invalid CRC will be discarded
0 = The CRC validity will be ignored

bit 4 **PMEN:** Pattern Match Filter Enable bit
When ANDOR = 1:
1 = Packets must meet the Pattern Match criteria or they will be discarded
0 = Filter disabled
When ANDOR = 0:
1 = Packets which meet the Pattern Match criteria will be accepted
0 = Filter disabled

bit 3 **MPEN:** Magic Packet Filter Enable bit
When ANDOR = 1:
1 = Packets must be Magic Packets for the local MAC address or they will be discarded
0 = Filter disabled
When ANDOR = 0:
1 = Magic Packets for the local MAC address will be accepted
0 = Filter disabled

bit 2 **HTEN:** Hash Table Filter Enable bit
When ANDOR = 1:
1 = Packets must meet the Hash Table criteria or they will be discarded
0 = Filter disabled
When ANDOR = 0:
1 = Packets which meet the Hash Table criteria will be accepted
0 = Filter disabled

bit 1 **MCEN:** Multicast Filter Enable bit
When ANDOR = 1:
1 = Packets must have the Least Significant bit set in the destination address or they will be discarded
0 = Filter disabled
When ANDOR = 0:
1 = Packets which have the Least Significant bit set in the destination address will be accepted
0 = Filter disabled

bit 0 **BCEN:** Broadcast Filter Enable bit
When ANDOR = 1:
1 = Packets must have a destination address of FF-FF-FF-FF-FF-FF or they will be discarded
0 = Filter disabled
When ANDOR = 0:
1 = Packets which have a destination address of FF-FF-FF-FF-FF-FF will be accepted
0 = Filter disabled

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FIGURE 8-1: RECEIVE FILTERING USING OR LOGIC

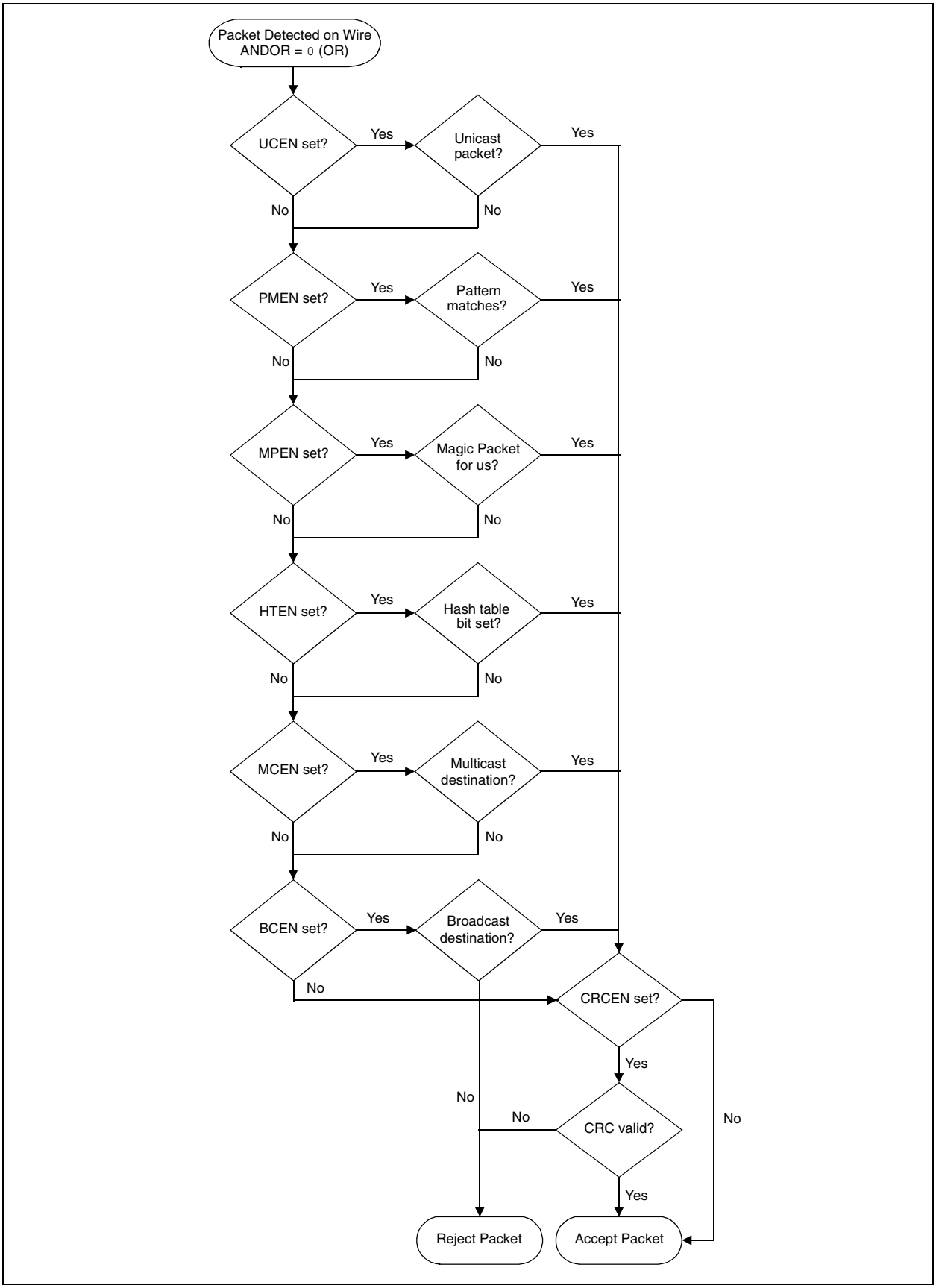
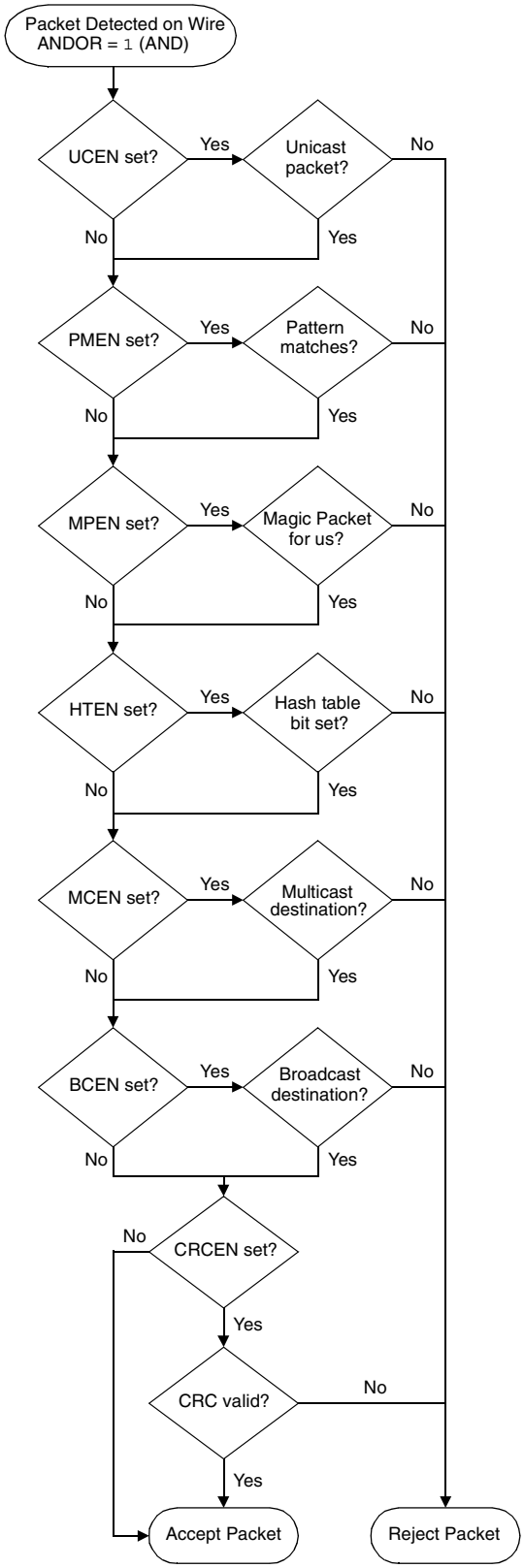


FIGURE 8-2: RECEIVE FILTERING USING AND LOGIC



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8.1 Unicast Filter

The unicast receive filter checks the destination address of all incoming packets. If the destination address exactly matches the contents of the MAADR registers, the packet will meet the unicast filter criteria.

8.2 Pattern Match Filter

The pattern match filter selects up to 64 bytes from the incoming packet and calculates an IP checksum of the bytes. The checksum is then compared to the EPMCS registers. The packet meets the pattern match filter criteria if the calculated checksum matches the EPMCS registers. The pattern match filter may be useful for filtering packets which have expected data inside them.

To use the pattern match filter, the host controller must program the pattern match offset (EPMOH:EPMOL), all of the pattern match mask bytes (EPMM7:EPMM0) and the pattern match checksum register pair (EPMCSH:EPMCSL). The pattern match offset should be loaded with the offset from the beginning of the destination address field to the 64-byte window which will be used for the checksum computation. Within the 64-byte window, each individual byte can be selectively included or excluded from the checksum computation by setting or clearing the respective bit in the pattern match mask. If a packet is received which would cause the 64 byte window to extend past the end of the CRC, the filter criteria will immediately not be met, even if the corresponding mask bits are all '0'. The pattern match checksum registers should be programmed to the checksum which is expected for the selected bytes. The checksum is calculated in the same manner that the DMA module calculates checksums (see **Section 13.2 "Checksum Calculations"**). Data bytes which have corresponding mask bits programmed to '0' are completely removed for purposes of calculating the checksum, as opposed to treating the data bytes as zero.

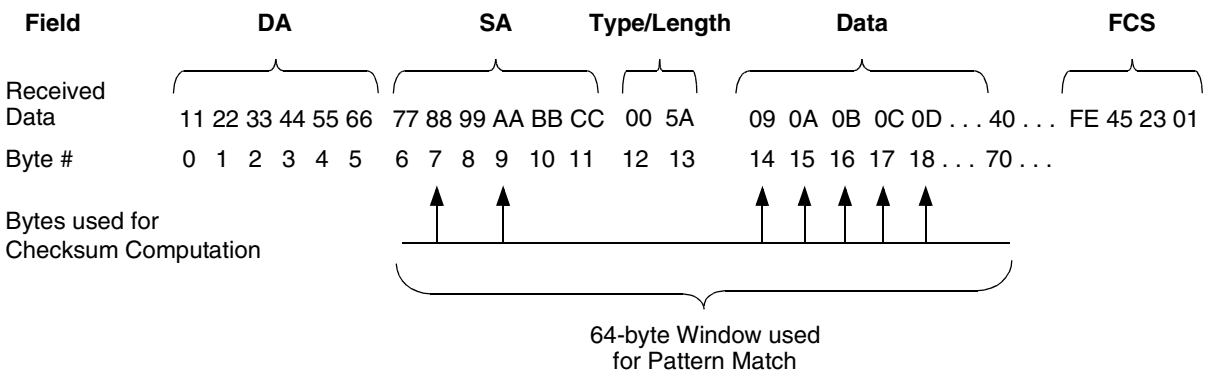
As an example, if the application wished to filter all packets having a particular source MAC address of 00-04-A3-FF-FF-FF, it could program the pattern match offset to 0000h and then set bits 6 and 7 of EPMM0 and bits 0, 1, 2 and 3 of EPMM1 (assuming all other mask bits are '0'). The proper checksum to program into the EPMCS registers would be 0x5BFC. As an alternative configuration, it could program the offset to 0006h and set bits 0, 1, 2, 3, 4 and 5 of EPMM0. The checksum would still be 5BFCh. However, the second case would be less desirable as packets less than 70 bytes long could never meet the pattern match criteria, even if they would generate the proper checksum given the mask configuration.

Another example of a pattern matching filter is illustrated in Figure 8-3.

FIGURE 8-3: SAMPLE PATTERN MATCH FORMAT

Input Configuration:

EMPOH:EPMOL = 0006h
EPMM7:EPMM0 = 0000000000001F0Ah
EPMCSH:EPMCSL = 563Fh



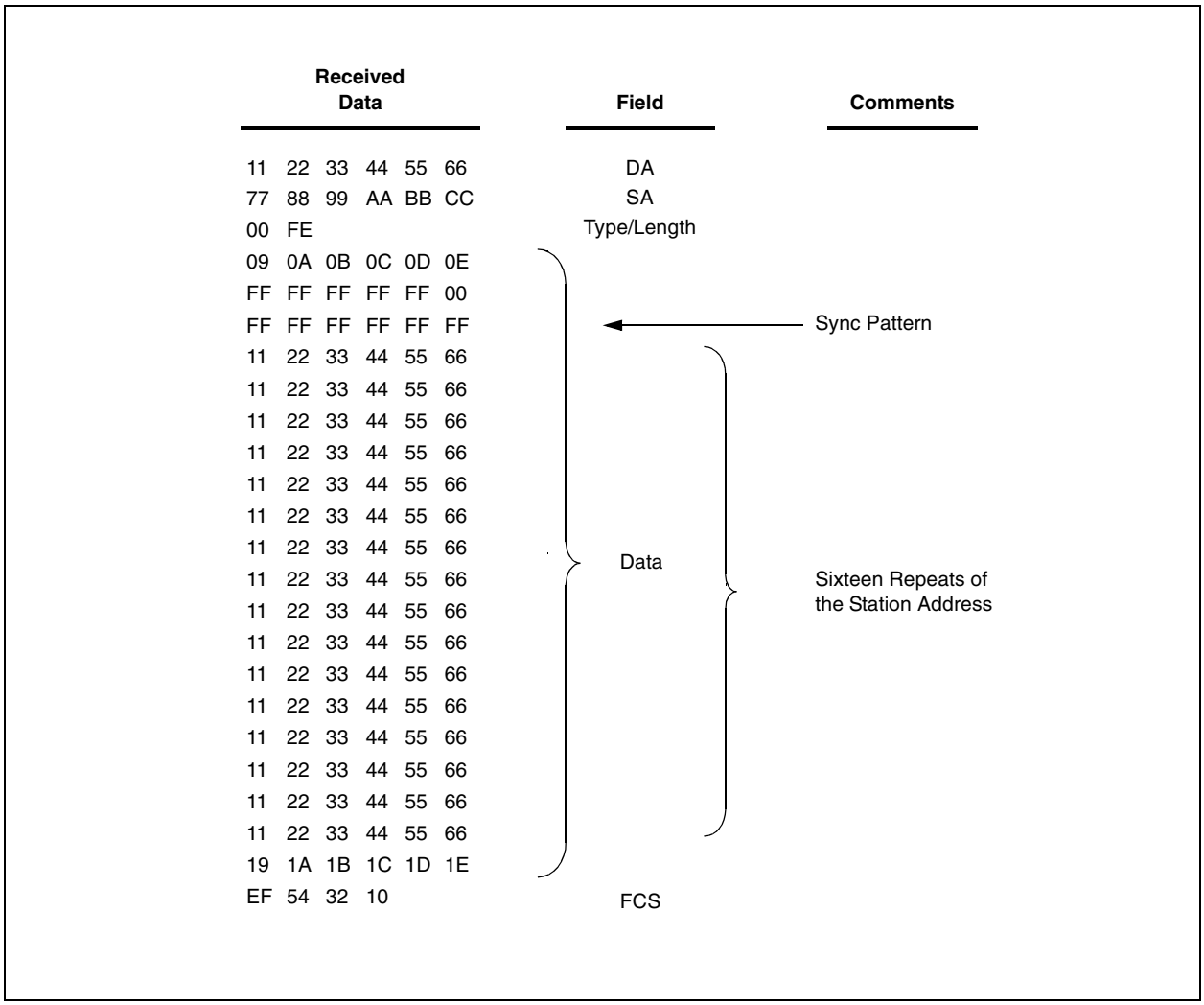
Values used for Checksum Computation = {88h, AAh, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 00h}
(00h padding byte added by hardware)

Note: Received data is shown in hexadecimal. Byte numbers are shown in decimal format.

8.3 Magic Packet™ Filter

The Magic Packet filter checks the destination address and data fields of all incoming packets. If the destination address matches the MAADR registers and the data field holds a valid Magic Packet pattern someplace within it, then the packet will meet the Magic Packet filter criteria. The Magic Packet pattern consists of a sync pattern of six 0xFF bytes, followed by 16 repeats of the destination address. See Figure 8-4 for a sample Magic Packet.

FIGURE 8-4: SAMPLE MAGIC PACKET™ FORMAT



8.4 Hash Table Filter

The hash table receive filter performs a CRC over the six destination address bytes in the packet. The CRC is then used as a Pointer into the bits of the EHT registers. If the Pointer points to a bit which is set, the packet meets the hash table filter criteria. For example, if the CRC is calculated to be 0x5, bit 5 in the hash table will be checked. If it is set, the hash table filter criteria will be met. If every bit is clear in the hash table, the filter criteria will never be met. Similarly, if every bit is set in the hash table, the filter criteria will always be met.

8.5 Multicast Filter

The multicast receive filter checks the destination address of all incoming packets. If the Least Significant bit of the first byte of the destination address is set, the packet will meet the multicast filter criteria.

8.6 Broadcast Filter

The broadcast receive filter checks the destination address of all incoming packets. If the destination address is FF-FF-FF-FF-FF-FF, the packet will meet the broadcast filter criteria.

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9.0 DUPLEX MODE CONFIGURATION AND NEGOTIATION

The ENC28J60 does not support automatic duplex negotiation. If it is connected to an automatic duplex negotiation enabled network switch or Ethernet controller, the ENC28J60 will be detected as a half-duplex device. To communicate in Full-Duplex mode, the ENC28J60 and the remote node (switch, router or Ethernet controller) must be manually configured for full-duplex operation.

9.1 Half-Duplex Operation

The ENC28J60 operates in Half-Duplex mode when MACON3.FULDPX = 0 and PHCON1.PDPXMD = 0. If only one of these two bits is set, the ENC28J60 will be in an indeterminate state and not function correctly. Since switching between Full and Half-Duplex modes may result in this indeterminate state, the host controller should not transmit any packets (maintain ECON1.TXRTS clear) and packet reception should be disabled (ECON1.RXEN and ESTAT.RXBUSY should be clear) during this period.

In Half-Duplex mode, only one Ethernet controller may be transmitting on the physical medium at any time. If the host controller sets the ECON1.TXRTS bit, requesting that a packet be transmitted while another Ethernet controller is already transmitting, the ENC28J60 will delay, waiting for the remote transmitter to stop. After the transmission stops, the ENC28J60 will attempt to transmit its packet. If another Ethernet controller starts transmitting at approximately the same time that the ENC28J60 starts transmitting, the data on the wire will become corrupt and a collision will occur. The hardware will handle this condition in one of two ways:

1. If the collision occurs before the number of bytes specified by the “Collision Window” in MACLCON2 were transmitted, the ECON1.TXRTS bit will remain set, a random exponential back off delay will elapse as defined by the IEEE 802.3 specification and then a new attempt to transmit the packet from the beginning will occur. The host controller will not need to intervene. If the number of retransmission attempts already matches the “Retransmission Maximum” (RETMAX) defined in MACLCON1, the packet will be aborted and ECON1.TXRTS will be cleared. The host controller will then be responsible for taking appropriate action. The host controller will be able to determine that the packet was aborted instead of being successfully transmitted by reading the ESTAT.TXABRT flag. For more information, see **Section 7.1 “Transmitting Packets”**. A transmit abort will cause the transmit error interrupt.
2. If the collision occurs after the number of bytes specified by the “Collision Window” in MACLCON2 were transmitted, the packet will be immediately aborted without any retransmission attempts. Ordinarily, in 802.3 compliant networks which are properly configured, this late collision will not occur. User intervention may be required to correct the issue. This problem may occur as a result of a full-duplex node attempting to transmit on the half-duplex medium. Alternately, the ENC28J60 may be attempting to operate in Half-Duplex mode while it may be connected to a full-duplex network. Excessively long cabling and network size may also be a possible cause of late collisions.

When set in Half-Duplex mode, the Reset default configuration will loop transmitted packets back to itself. Unless the receive filter configuration filters these packets out, they will be written into the circular receive buffer, just as any other network traffic. To stop this behavior, the host controller should set the PHCON2.HDLDIS bit.

9.2 Full-Duplex Operation

The ENC28J60 operates in Full-Duplex mode when MACON3.FULDPX = 1 and PHCON1.PDPXMD = 1. If only one of these two bits is clear, the ENC28J60 will be in an indeterminate state and not function correctly. Since switching between Full and Half-Duplex modes may result in this indeterminate state, the host controller should not transmit any packets (maintain ECON1.TXRTS clear) and packet reception should be disabled (ECON1.RXEN and ESTAT.RXBUSY should be clear) during this period.

In Full-Duplex mode, packets will be transmitted simultaneously while packets may be received. Given this, it is impossible to cause any collisions when transmitting packets. Several configuration fields, such as “Retransmission Maximum” (RETMAX) in MACLCON1 and “Collision Window” (COLWIN) in MACLCON2, will not be used.

When set in Full-Duplex mode, the Reset default configuration will not loop transmitted packets back to itself. If loopback is desired for diagnostic purposes, the PHCON1.PLOOPBK bit should be set by the host controller. Enabling loopback in Full-Duplex mode will disable the twisted pair output driver and ignore all incoming data, thus dropping any link (if established). All packets received as a result of the loopback configuration will be subject to all enabled receive filters, just as ordinary network traffic would be.

NOTES:

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10.0 FLOW CONTROL

The ENC28J60 implements hardware flow control for both Full and Half-Duplex modes. The operation of this feature differs depending on which mode is being used.

10.1 Half-Duplex Mode

In Half-Duplex mode, setting the EFLOCON.FCEN0 bit causes flow control to be enabled. When FCEN0 is set, a continuous preamble pattern of alternating '1's and '0's (55h) will automatically be transmitted on the Ethernet medium. Any connected nodes will see the transmission and either not transmit anything, waiting for the ENC28J60's transmission to end, or will attempt to transmit and immediately cause a collision. Because a collision will always occur, no nodes on the network will be able to communicate with each other and no new packets will arrive.

When the host controller tells the ENC28J60 to transmit a packet by setting ECON1.TXRTS, the preamble pattern will stop being transmitted. An Inter-Packet Gap delay will pass as configured by register MABBIPG and then the ENC28J60 will attempt to transmit its packet. During the Inter-Packet Gap delay, other nodes may begin to transmit. Because all traffic was jammed previously, several nodes may begin transmitting and a series of collisions may occur. When the ENC28J60 successfully finishes transmitting its packet or aborts it, the transmission of the preamble pattern will automatically restart. When the host controller wishes to no longer jam the network, it should clear the FCEN0 bit. The preamble transmission will cease and normal network operation will resume.

Given the detrimental network effects that are possible and lack of effectiveness, it is not recommend that half-duplex flow control be used unless the application will be in a closed network environment with proper testing.

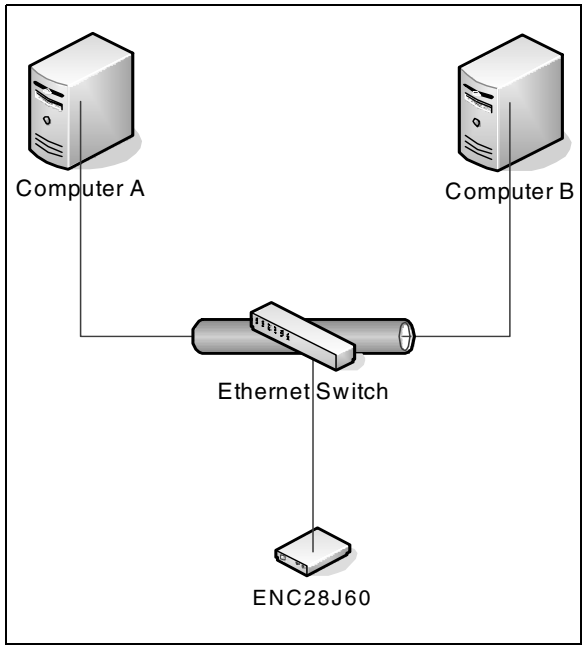
10.2 Full-Duplex Mode

In Full-Duplex mode (MACON3.FULDPX = 1), hardware flow control is implemented by means of transmitting pause control frames as defined by the IEEE 802.3 specification. Pause control frames are 64-byte frames consisting of the reserved multicast destination address of 01-80-C2-00-00-01, the source address of the sender, a special pause opcode, a two-byte pause timer value and padding/CRC.

Normally, when a pause control frame is received by a MAC, the MAC will finish the packet it is transmitting and then stop transmitting any new frames. The pause timer value will be extracted from the control frame and used to initialize an internal timer. The timer will automatically decrement every 512 bit times or 51.2 µs. While the timer is counting down, reception of packets is still enabled. If new pause frames arrive, the timer will be reinitialized with the new pause timer value. When the timer reaches zero or was sent a frame with a zero pause timer value, the MAC that received the pause frame will resume transmitting any pending packets. To prevent a pause frame from stopping all traffic on the entire network, Ethernet switches and routers do not propagate pause control frames in Full-Duplex mode. The pause operation only applies to the recipient.

A sample network is shown in Figure 10-1. If Computer A were to be transmitting too much data to the ENC28J60 in Full-Duplex mode, the ENC28J60 could transmit a pause control frame to stop the data which is being sent to it. The Ethernet switch would take the pause frame and stop sending data to the ENC28J60. If Computer A continues to send data, the Ethernet switch will buffer the data so it can be transmitted later when its pause timer expires. If the Ethernet switch begins to run out of buffer space, it will likely transmit a pause control frame of its own to Computer A. If, for some reason, the Ethernet switch does not generate a pause control frame of its own, or one of the nodes does not properly handle the pause frame it receives, then packets will inevitably be dropped. In any event, any communication between Computer A and Computer B will always be completely unaffected.

FIGURE 10-1: SAMPLE FULL-DUPLEX NETWORK



To enable flow control on the ENC28J60 in Full-Duplex mode, the host controller must set the TXPAUS and RXPAUS bits in the MACON1 register. Then, at any time that the receiver buffer is running out of space, the host controller should turn flow control on by writing the value 02h to the EFLOCON register. The hardware will periodically transmit pause frames loaded with the pause timer value specified in the EPAUS registers. The host controller can continue to transmit its own packets without interfering with the flow control hardware.

When space has been made available for more packets in the receive buffer, the host controller should turn flow control off by writing the value 03h to the EFLOCON register. The hardware will send one last pause frame loaded with a pause timer value of 0000h. When the pause frame is received by the remote node, it will resume normal network operations.

When RXPAUS is set in the MACON1 register and a valid pause frame arrives with a non-zero pause timer value, the ENC28J60 will automatically inhibit transmissions. If the host controller sets the ECON1.TXRTS bit to send a packet, the hardware will simply wait until the pause timer expires before attempting to send the packet and subsequently clearing the TXRTS bit. Normally, the host controller will never know that a pause frame has been received. However, if it is desirable to the host controller to know when the MAC is paused or not, it should set the PASSALL bit in MACON1 and then manually interpret the pause control frames which may arrive.

REGISTER 10-1: EFLOCON: ETHERNET FLOW CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R/W-0	R/W-0
—	—	—	—	—	FULDPXS	FCEN1	FCEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **FULDPXS:** Read-Only MAC Full-Duplex Shadow bit

1 = MAC is configured for Full-Duplex mode, FULDPX (MACON3<0>) is set
0 = MAC is configured for Half-Duplex mode, FULDPX (MACON3<0>) is clear

bit 1-0 **FCEN1:FCEN0:** Flow Control Enable bits

When FULDPXS = 1:
11 = Send one pause frame with a '0' timer value and then turn flow control off
10 = Send pause frames periodically
01 = Send one pause frame then turn flow control off
00 = Flow control off

When FULDPXS = 0:
11 = Flow control on
10 = Flow control off
01 = Flow control on
00 = Flow control off

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TABLE 10-1: SUMMARY OF REGISTERS USED WITH FLOW CONTROL

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	13
MACON1	—	—	—	r	TXPAUS	RXPAUS	PASSALL	MARXEN	14
MABBIPG	—	Back-to-Back Inter-Packet Gap (BBIPG<6:0>)							14
EFLOCON	—	—	—	—	—	FULDPXS	FCEN1	FCEN0	14
EPAUSL	Pause Timer Value Low Byte (EPAUS<7:0>)								14
EPAUSH	Pause Timer Value High Byte (EPAUS<15:8>)								14

Legend: — = unimplemented, read as '0'. Shaded cells are not used.

NOTES:

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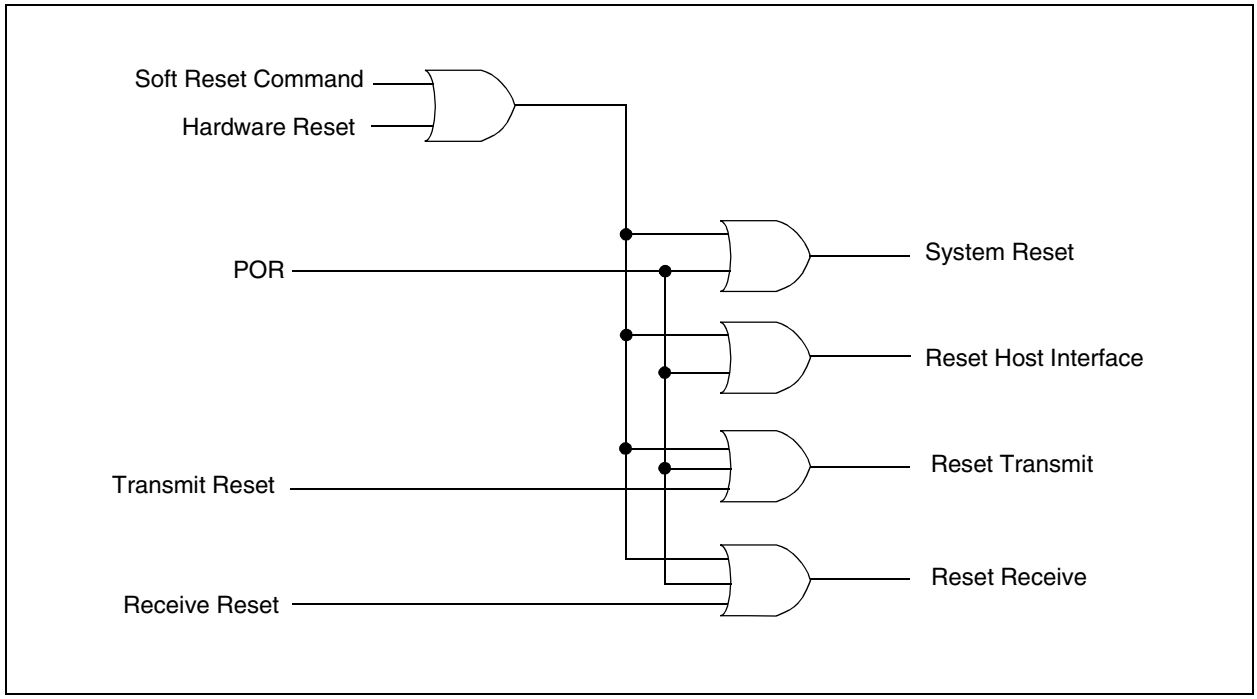
11.0 RESET

The ENC28J60 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- System Reset
- Transmit Only Reset
- Receive Only Reset
- Miscellaneous MAC and PHY Subsystem Resets

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 11-1.

FIGURE 11-1: ON-CHIP RESET CIRCUIT



11.1 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

The POR circuitry is always enabled. As a result, most applications do not need to attach any external circuitry to the $\overline{\text{RESET}}$ pin to ensure a proper Reset at power-up. The $\overline{\text{RESET}}$ pin's internal weak pull-up will maintain a logical high level on the pin during normal device operation.

To ensure proper POR operation, a minimum rise rate for VDD is specified (parameter D003). The application circuit must meet this requirement to allow the Oscillator Start-up Timer and CLKOUT functions to reset properly.

After a Power-on Reset, the contents of the dual port buffer memory will be unknown. However, all registers will be loaded with their specified Reset values. Certain portions of the ENC28J60 must not be accessed immediately after a POR. See **Section 2.2 "Oscillator Start-up Timer"** for more information.

11.2 System Reset

The System Reset of ENC28J60 can be accomplished by either the $\overline{\text{RESET}}$ pin, or through the SPI interface.

The $\overline{\text{RESET}}$ pin provides an asynchronous method for triggering an external Reset of the device. A Reset is generated by holding the $\overline{\text{RESET}}$ pin low. The ENC28J60 has a noise filter in the $\overline{\text{RESET}}$ path which detects and ignores small pulses of time tRSTLOW or less. When the $\overline{\text{RESET}}$ pin is held high, the ENC28J60 will operate normally.

The ENC28J60 can also be reset via the SPI using the System Reset Command. See **Section 4.0 "Serial Peripheral Interface (SPI)"**.

The $\overline{\text{RESET}}$ pin will not be driven low by any internal Resets, including a System Reset Command via the SPI interface.

After a System Reset, all PHY registers should not be read or written to until at least 50 µs have passed since the Reset has ended. All registers will revert to their Reset default values. The dual port buffer memory will maintain state throughout the System Reset.

11.3 Transmit Only Reset

The Transmit Only Reset is performed by writing a '1' to the TXRST bit in the ECON1 register using the SPI interface. If a packet was being transmitted when the TXRST bit was set, the hardware will automatically clear the TXRTS bit and abort the transmission. This action resets the transmit logic only. The System Reset automatically performs the Transmit Only Reset. Other register and control blocks, such as buffer management and host interface, are not affected by a Transmit Only Reset event. When the host controller wishes to return to normal operation, it should clear the TXRST bit.

11.4 Receive Only Reset

The Receive Only Reset is performed by writing a '1' to the RXRST bit in the ECON1 register using the SPI interface. If packet reception was enabled (the RXEN bit was set) when RXRST was set, the hardware will automatically clear the RXEN bit. If a packet was being received, it would be immediately aborted. This action resets receive logic only. The System Reset automatically performs Receive Only Reset. Other register and control blocks, such as the buffer management and host interface blocks, are not affected by a Receive Only Reset event. When the host controller wishes to return to normal operation, it should clear the RXRST bit.

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11.5 PHY Subsystem Reset

The PHY module may be reset by writing a '1' to the PRST bit in the PHCON1 register (Register 11-1). All the PHY register contents will revert to their Reset defaults.

Unlike other Resets, the PHY cannot be removed from Reset immediately after setting PRST. The PHY requires a delay, after which the hardware automatically clears the PRST bit. After a Reset is issued, the host controller should poll PRST and wait for it to become clear before using the PHY.

REGISTER 11-1: PHCON1: PHY CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0
PRST	PLOOPBK	—	—	PPWRSV	r	—	PDPXMD
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
r	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PRST:** PHY Software Reset bit
1 = PHY is processing a Software Reset (automatically resets to '0' when done)
0 = Normal operation

bit 14 **PLOOPBK:** PHY Loopback bit
1 = All data transmitted will be returned to the MAC. The twisted-pair interface will be disabled.
0 = Normal operation

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **PPWRSV:** PHY Power-Down bit
1 = PHY is shut down
0 = Normal operation

bit 10 **Reserved:** Maintain as '0'

bit 9 **Unimplemented:** Read as '0'

bit 8 **PDPXMD:** PHY Duplex Mode bit
1 = PHY operates in Full-Duplex mode
0 = PHY operates in Half-Duplex mode

bit 7 **Reserved:** Maintain as '0'

bit 6-0 **Unimplemented:** Read as '0'

NOTES:

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12.0 INTERRUPTS

The ENC28J60 has multiple interrupt sources and an interrupt output pin to signal the occurrence of events to the host controller. The interrupt pin is designed for use by a host controller that is capable of detecting falling edges.

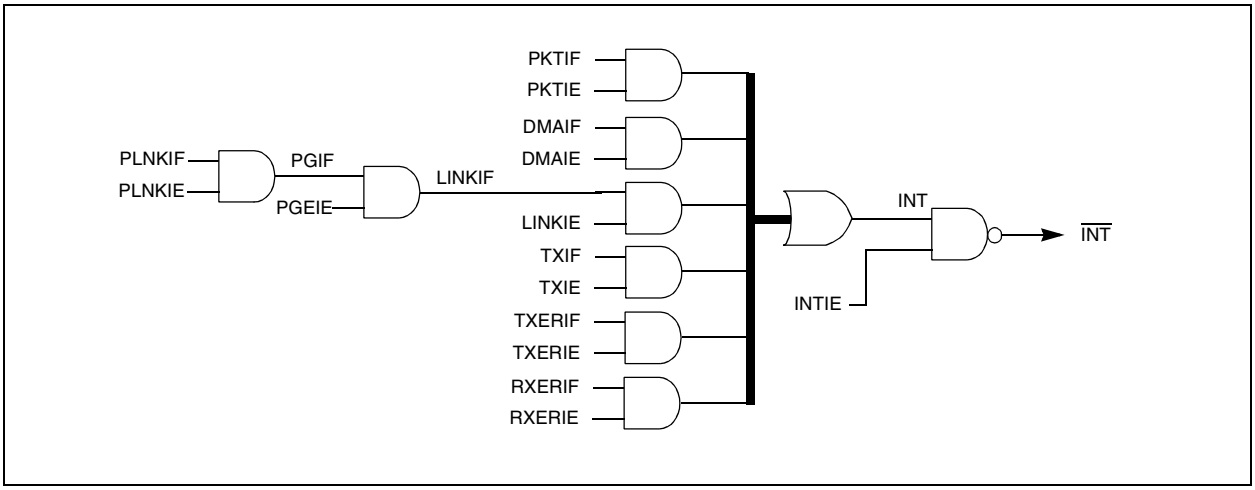
Interrupts are managed with two registers. The EIE register contains the individual interrupt enable bits for each interrupt source, while the EIR register contains the corresponding interrupt flag bits. When an interrupt occurs, the interrupt flag is set. If the interrupt is enabled in the EIE register and the INTIE global interrupt enable bit is set, the $\overline{INT}$ pin will be driven low (see Figure 12-1).

Note:	Except for the LINKIF interrupt flag, interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the associated global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

When an enabled interrupt occurs, the interrupt pin will remain low until all flags which are causing the interrupt are cleared or masked off (enable bit is cleared) by the host controller. If more than one interrupt source is enabled, the host controller must poll each flag in the EIR register to determine the source(s) of the interrupt. It is recommended that the Bit Field Clear (BFC) SPI command be used to reset the flag bits in the EIR register rather than the normal Write Control Register (WCR) command. This is necessary to prevent unintentionally altering a flag that changes during the write command. The BFC and WCR commands are discussed in detail in **Section 4.0 "Serial Peripheral Interface (SPI)"**.

After an interrupt occurs, the host controller should clear the global enable bit for the interrupt pin before servicing the interrupt. Clearing the enable bit will cause the interrupt pin to return to the non-asserted state (high). Doing so will prevent the host controller from missing a falling edge should another interrupt occur while the immediate interrupt is being serviced. After the interrupt has been serviced, the global enable bit may be restored. If an interrupt event occurred while the previous interrupt was being processed, the act of resetting the global enable bit will cause a new falling edge on the interrupt pin to occur.

FIGURE 12-1: ENC28J60 INTERRUPT LOGIC



12.1 INT Interrupt Enable (INTIE)

The INT Interrupt Enable bit (INTIE) is a global enable bit which allows the following interrupts to drive the INT pin:

- Receive Error Interrupt (RXERIF)
- Transmit Error Interrupt (TXERIF)
- Transmit Interrupt (TXIF)
- Link Change Interrupt (LINKIF)
- DMA Interrupt (DMAIF)
- Receive Packet Pending Interrupt (PKTIF)

When any of the above interrupts are enabled and generated, the virtual bit, INT in the ESTAT register (Register 12-1), will be set to '1'. If EIE.INTIE is '1', the INT pin will be driven low.

12.1.1 INT INTERRUPT REGISTERS

The registers associated with the INT interrupts are shown in Register 12-2, Register 12-3, Register 12-4 and Register 12-5.

REGISTER 12-1: ESTAT: ETHERNET STATUS REGISTER

R-0	R/C-0	R-0	R/C-0	U-0	R-0	R/C-0	R/W-0
INT	BUFER	r	LATECOL	—	RXBUSY	TXABRT	CLKRDY
bit 7							bit 0

Legend:			
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **INT:** INT Interrupt Flag bit
1 = INT interrupt is pending
0 = No INT interrupt is pending

bit 6 **BUFER:** Ethernet Buffer Error Status bit
1 = An Ethernet read or write has generated a buffer error (overrun or underrun)
0 = No buffer error has occurred

bit 5 **Reserved:** Read as '0'

bit 4 **LATECOL:** Late Collision Error bit
1 = A collision occurred after 64 bytes had been transmitted
0 = No collisions after 64 bytes have occurred

bit 3 **Unimplemented:** Read as '0'

bit 2 **RXBUSY:** Receive Busy bit
1 = Receive logic is receiving a data packet
0 = Receive logic is Idle

bit 1 **TXABRT:** Transmit Abort Error bit
1 = The transmit request was aborted
0 = No transmit abort error

bit 0 **CLKRDY:** Clock Ready bit
1 = OST has expired; PHY is ready
0 = OST is still counting; PHY is not ready

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REGISTER 12-2: EIE: ETHERNET INTERRUPT ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTIE	PKTIE	DMAIE	LINKIE	TXIE	r	TXERIE	RXERIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **INTIE:** Global INT Interrupt Enable bit
1 = Allow interrupt events to drive the $\overline{INT}$ pin
0 = Disable all $\overline{INT}$ pin activity (pin is continuously driven high)

bit 6 **PKTIE:** Receive Packet Pending Interrupt Enable bit
1 = Enable receive packet pending interrupt
0 = Disable receive packet pending interrupt

bit 5 **DMAIE:** DMA Interrupt Enable bit
1 = Enable DMA interrupt
0 = Disable DMA interrupt

bit 4 **LINKIE:** Link Status Change Interrupt Enable bit
1 = Enable link change interrupt from the PHY
0 = Disable link change interrupt

bit 3 **TXIE:** Transmit Enable bit
1 = Enable transmit interrupt
0 = Disable transmit interrupt

bit 2 **Reserved:** Maintain as '0'

bit 1 **TXERIE:** Transmit Error Interrupt Enable bit
1 = Enable transmit error interrupt
0 = Disable transmit error interrupt

bit 0 **RXERIE:** Receive Error Interrupt Enable bit
1 = Enable receive error interrupt
0 = Disable receive error interrupt

REGISTER 12-3: EIR: ETHERNET INTERRUPT REQUEST (FLAG) REGISTER

U-0	R-0	R/C-0	R-0	R/C-0	R-0	R/C-0	R/C-0
—	PKTIF	DMAIF	LINKIF	TXIF	r	TXERIF	RXERIF
bit 7							bit 0

Legend:			
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **PKTIF:** Receive Packet Pending Interrupt Flag bit
1 = Receive buffer contains one or more unprocessed packets; cleared when PKTDEC is set
0 = Receive buffer is empty

bit 5 **DMAIF:** DMA Interrupt Flag bit
1 = DMA copy or checksum calculation has completed
0 = No DMA interrupt is pending

bit 4 **LINKIF:** Link Change Interrupt Flag bit
1 = PHY reports that the link status has changed; read PHIR register to clear
0 = Link status has not changed

bit 3 **TXIF:** Transmit Interrupt Flag bit
1 = Transmit request has ended
0 = No transmit interrupt is pending

bit 2 **Reserved:** Maintain as ‘0’

bit 1 **TXERIF:** Transmit Error Interrupt Flag bit
1 = A transmit error has occurred
0 = No transmit error has occurred

bit 0 **RXERIF:** Receive Error Interrupt Flag bit
1 = A packet was aborted because there is insufficient buffer space or the packet count is 255
0 = No receive error interrupt is pending

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REGISTER 12-4: PHIE: PHY INTERRUPT ENABLE REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
r	r	r	r	r	r	r	r
bit 15							bit 8

R-0	R-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
r	r	r	PLNKIE	r	r	PGEIE	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Reserved:** Write as '0', ignore on read

bit 5 **Reserved:** Maintain as '0'

bit 4 **PLNKIE:** PHY Link Change Interrupt Enable bit
1 = PHY link change interrupt is enabled
0 = PHY link change interrupt is disabled

bit 3-2 **Reserved:** Write as '0', ignore on read

bit 1 **PGEIE:** PHY Global Interrupt Enable bit
1 = PHY interrupts are enabled
0 = PHY interrupts are disabled

bit 0 **Reserved:** Maintain as '0'

REGISTER 12-5: PHIR: PHY INTERRUPT REQUEST (FLAG) REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
r	r	r	r	r	r	r	r
bit 15							bit 8

R-x	R-x	R-0	R/SC-0	R-0	R/SC-0	R-x	R-0
r	r	r	PLNKIF	r	PGIF	r	r
bit 7							bit 0

Legend:			
R = Readable bit	SC = Self-clearing bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Reserved:** Do not modify

bit 5 **Reserved:** Read as '0'

bit 4 **PLNKIF:** PHY Link Change Interrupt Flag bit
1 = PHY link status has changed since PHIR was last read; resets to '0' when read
0 = PHY link status has not changed since PHIR was last read

bit 3 **Reserved:** Read as '0'

bit 2 **PGIF:** PHY Global Interrupt Flag bit
1 = One or more enabled PHY interrupts have occurred since PHIR was last read; resets to '0' when read
0 = No PHY interrupts have occurred

bit 1 **Reserved:** Do not modify

bit 0 **Reserved:** Read as '0'

12.1.2 RECEIVE ERROR INTERRUPT FLAG (RXERIF)

The Receive Error Interrupt Flag (RXERIF) is used to indicate a receive buffer overflow condition. Alternately, this interrupt may indicate that too many packets are in the receive buffer and more cannot be stored without overflowing the EPKTCNT register.

When a packet is being received and the receive buffer runs completely out of space, or EPKTCNT is 255 and cannot be incremented, the packet being received will be aborted (permanently lost) and the EIR.RXERIF bit will be set to '1'. Once set, RXERIF can only be cleared by the host controller or by a Reset condition. If the receive error interrupt and INT interrupt are enabled (EIE.RXERIE = 1 and EIE.INTIE = 1), an interrupt is generated by driving the $\overline{\text{INT}}$ pin low. If the receive error interrupt is not enabled (EIE.RXERIE = 0 or EIE.INTIE = 0), the host controller may poll the ENC28J60 for the RXERIF and take appropriate action.

Normally, upon the receive error condition, the host controller would process any packets pending from the receive buffer and then make additional room for future packets by advancing the ERXRDPT registers (low byte first) and decrementing the EPKTCNT register. See **Section 7.2.4 "Freeing Receive Buffer Space"** for more information on processing packets. Once processed, the host controller should use the BFC command to clear the EIR.RXERIF bit.

12.1.3 TRANSMIT ERROR INTERRUPT FLAG (TXERIF)

The Transmit Error Interrupt Flag (TXERIF) is used to indicate that a transmit abort has occurred. An abort can occur because of any of the following:

1. Excessive collisions occurred as defined by the Retransmission Maximum (RETMAX) bits in the MACLCON1 register.
2. A late collision occurred as defined by the Collision Window (COLWIN) bits in the MACLCON2 register.
3. A collision after transmitting 64 bytes occurred (ESTAT.LATECOL set).
4. The transmission was unable to gain an opportunity to transmit the packet because the medium was constantly occupied for too long. The deferral limit (2.4287 ms) was reached and the MACON4.DEFER bit was clear.
5. An attempt to transmit a packet larger than the maximum frame length defined by the MAMXFL registers was made without setting the MACON3.HFRMEN bit or per packet POVERRIDE and PHUGEEN bits.

Upon any of these conditions, the EIR.TXERIF flag is set to '1'. Once set, it can only be cleared by the host controller or by a Reset condition. If the transmit error interrupt is enabled (EIE.TXERIE = 1 and EIE.INTIE = 1), an interrupt is generated by driving the $\overline{\text{INT}}$ pin low for one OSC1 period. If the transmit error interrupt is not enabled (EIE.TXERIE = 0 or EIE.INTIE = 0), the host controller may poll the ENC28J60 for the TXERIF and take appropriate action. Once the interrupt is processed, the host controller should use the BFC command to clear the EIR.TXERIF bit.

After a transmit abort, the TXRTS bit will be cleared, the ESTAT.TXABRT bit will be set and the transmit status vector will be written at ETXND + 1. The MAC will not automatically attempt to retransmit the packet. The host controller may wish to read the transmit status vector and LATECOL bit to determine the cause of the abort. After determining the problem and solution, the host controller should clear the LATECOL (if set) and TXABRT bits so that future aborts can be detected accurately.

In Full-Duplex mode, condition 5 is the only one that should cause this interrupt. Collisions and other problems related to sharing the network are not possible on full-duplex networks. The conditions which cause the transmit error interrupt meet the requirements of the transmit interrupt. As a result, when this interrupt occurs, TXIF will also be simultaneously set.

12.1.4 TRANSMIT INTERRUPT FLAG (TXIF)

The Transmit Interrupt Flag (TXIF) is used to indicate that the requested packet transmission has ended (ECON1.TXRTS has transitioned from '1' to '0'). Upon transmission completion, abort or transmission cancellation by the host controller, the EIR.TXIF flag will be set to '1'. If the host controller did not clear the TXRTS bit and the ESTAT.TXABRT bit is not set, then the packet was successfully transmitted. Once TXIF is set, it can only be cleared by the host controller or by a Reset condition. If the transmit interrupt is enabled (EIE.TXIE = 1 and EIE.INTIE = 1), an interrupt is generated by driving the $\overline{\text{INT}}$ pin low. If the transmit interrupt is not enabled (EIE.TXIE = 0 or EIE.INTIE = 0), the host controller may poll the ENC28J60 for the TXIF bit and take appropriate action. Once processed, the host controller should use the BFC command to clear the EIR.TXIF bit.

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12.1.5 LINK CHANGE INTERRUPT FLAG (LINKIF)

The LINKIF indicates that the link status has changed. The actual current link status can be obtained from the PHSTAT1.LLSTAT or PHSTAT2.LSTAT (see Register 3-5 and Register 3-6). Unlike other interrupt sources, the link status change interrupt is created in the integrated PHY module; additional steps must be taken to enable it.

By Reset default, LINKIF is never set for any reason. To receive it, the host controller must set the PHIE.PLNKIE and PGEIE bits. After setting the two PHY interrupt enable bits, the LINKIF bit will then shadow the contents of the PHIR.PGIF bit. The PHY only supports one interrupt, so the PGIF bit will always be the same as the PHIR.PLNKIF bit (when both PHY enable bits are set).

Once LINKIF is set, it can only be cleared by the host controller or by a Reset. If the link change interrupt is enabled (EIE.LINKIE = 1, EIE.INTIE = 1, PHIE.PLNKIE = 1 and PHIE.PGEIE = 1), an interrupt will be generated by driving the $\overline{\text{INT}}$ pin low. If the link change interrupt is not enabled (EIE.LINKIE = 0, EIE.INTIE = 0, PHIE.PLNKIE = 0 or PHIE.PGEIE = 0), the host controller may poll the ENC28J60 for the PHIR.PLNKIF bit and take appropriate action.

The LINKIF bit is read-only. Because reading from PHY registers requires non-negligible time, the host controller may instead set PHIE.PLNKIE and PHIE.PGEIE and then poll the EIR.LINKIF bit. Performing an MII read on the PHIR register will clear the LINKIF, PGIF and PLNKIF bits automatically and allow for future link status change interrupts. See **Section 3.3 "PHY Registers"** for information on accessing the PHY registers.

12.1.6 DMA INTERRUPT FLAG (DMAIF)

The DMA interrupt indicates that the DMA module has completed its memory copy or checksum calculation (ECON1.DMAST has transitioned from '1' to '0'). Additionally, this interrupt will be caused if the host controller cancels a DMA operation by manually clearing the DMAST bit. Once set, DMAIF can only be cleared by the host controller or by a Reset condition. If the DMA interrupt is enabled (EIE.DMAIE = 1 and EIE.INTIE = 1), an interrupt is generated by driving the $\overline{\text{INT}}$ pin low. If the DMA interrupt is not enabled (EIE.DMAIE = 0 or EIE.INTIE = 0), the host controller may poll the ENC28J60 for the DMAIF and take appropriate action. Once processed, the host controller should use the BFC command to clear the EIR.DMAIF bit.

12.1.7 RECEIVE PACKET PENDING INTERRUPT FLAG (PKTIF)

The Receive Packet Pending Interrupt Flag (PKTIF) is used to indicate the presence of one or more data packets in the receive buffer and to provide a notification means for the arrival of new packets. When the receive buffer has at least one packet in it, EIR.PKTIF will be set. In other words, this interrupt flag will be set anytime the Ethernet Packet Count register (EPKTCNT) is non-zero. If the receive packet pending interrupt is enabled (EIE.PKTIE = 1 and EIE.INTIE = 1), an interrupt will be generated by driving the $\overline{\text{INT}}$ pin low whenever a new packet is successfully received and written into the receive buffer. If the receive packet pending interrupt is not enabled (EIE.PKTIE = 0 or EIE.INTIE = 0), the host controller will not be notified when new packets arrive. However, it may poll the PKTIF bit and take appropriate action.

The PKTIF bit can only be cleared by the host controller or by a Reset condition. In order to clear PKTIF, the EPKTCNT register must be decremented to '0'. See **Section 7.2 "Receiving Packets"** for more information about clearing the EPKTCNT register. If the last data packet in the receive buffer is processed, EPKTCNT will become zero and the PKTIF bit will automatically be cleared.

12.2 Wake-On-LAN/Remote Wake-up

Wake-On-LAN or Remote Wake-up is useful in conserving system power. The host controller and other subsystems can be put in Low-Power mode and be woken up by the ENC28J60 when a wake-up packet is received from a remote station. The ENC28J60 must not be in Power-Save mode and the transmit and receive modules must be enabled in order to receive a wake-up packet. The ENC28J60 wakes up the host controller via the $\overline{INT}$ signal when the Interrupt Mask registers are properly configured. The receive filter can also be set up to only receive a specific wake-up packet (see Register 8-1 for available options). **Section 12.2.1 "Setup Steps for Waking Up on a Magic Packet"** shows the steps necessary in configuring the ENC28J60 to send an interrupt signal to the host controller upon the reception of a Magic packet.

12.2.1 SETUP STEPS FOR WAKING UP ON A MAGIC PACKET

1. Set ERXFCON.CRCEN and ERXFCON.MPEN.
2. Service all pending packets.
3. Set EIE.PKTIE and EIE.INTIE.
4. Set up the host controller to wake-up on an external interrupt $\overline{INT}$ signal.
5. Put the host controller and other subsystems to Sleep to save power.

Once a Magic packet is received, the EPKTCNT is incremented to '1', which causes the EIR.$\overline{PKTIF}$ bit to set. In turn, the ESTAT.INT bit is set and the $\overline{INT}$ signal is driven low, causing the host to wake-up.

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13.0 DIRECT MEMORY ACCESS CONTROLLER

The ENC28J60 incorporates a dual purpose DMA controller which can be used to copy data between locations within the 8-Kbyte memory buffer. It can also be used to calculate a 16-bit checksum which is compatible with various industry standard protocols, including TCP and IP.

When a DMA operation begins, the EDMAST register pair is copied into an Internal Source Pointer. The DMA will execute on one byte at a time and then increment the Internal Source Pointer. However, if a byte is processed and the Internal Source Pointer is equal to the Receive Buffer End Pointer, ERXND, the Source Pointer will not be incremented. Instead, the Internal Source Pointer will be loaded with the Receive Buffer Start Pointer, ERXST. In this way, the DMA will follow the circular FIFO structure of the receive buffer and received packets can be processed using one operation. The DMA operation will end when the Internal Source Pointer matches the EDMAND Pointer.

While any DMA operation is in progress, the DMA Pointers and the ECON1.CSUMEN bit should not be modified. The DMA operation can be canceled at any time by clearing the ECON1.DMAST bit. No registers will change; however, some memory bytes may already have been copied if a DMA copy was in progress.

Note 1: If the EDMAND Pointer cannot be reached because of the receive buffer wrapping behavior, the DMA operation will never end.

2: By design, the DMA module cannot be used to copy only one byte (EDMAST = EDMAND). An attempt to do so will overwrite all memory in the buffer and may never end.

13.1 Copying Memory

To copy memory within the buffer:

1. Appropriately program the EDMAST, EDMAND and EDMADST register pairs. The EDMAST registers should point to the first byte to copy from, the EDMAND registers should point to the last byte to copy and the EDMADST registers should point to the first byte in the destination range. The destination range will always be linear, never wrapping at any values except from 8191 to 0 (the 8-Kbyte memory boundary). Extreme care should be taken when programming the Start and End Pointers to prevent a never ending DMA operation which would overwrite the entire 8-Kbyte buffer.
2. If an interrupt at the end of the copy process is desired, set EIE.DMAIE and EIE.INTIE and clear EIR.DMAIF.
3. Verify that ECON1.CSUMEN is clear.
4. Start the DMA copy by setting ECON1.DMAST.

If a transmit operation is in progress (TXRTS set) while the DMAST bit is set, the ENC28J60 will wait until the transmit operation is complete before attempting to do the DMA copy. This possible delay is required because the DMA and transmission engine share the same memory access port.

When the copy is complete, the DMA hardware will clear the DMAST bit, set the DMAIF bit and generate an interrupt (if enabled). The Pointers and the EDMACS registers will not be modified.

After the DMA module has been initialized and has begun its copy, two main clock cycles will be required for each byte copied. As a result, if a maximum size 1518-byte packet was copied, the DMA module would require slightly more than 121.44 μs to complete. The time required to copy a minimum size packet of 64 bytes would be dominated by the time required to configure the DMA.

13.2 Checksum Calculations

The checksum calculation logic treats the source data as a series of 16-bit big-endian integers. If the source range contains an odd number of bytes, a padding byte of 00h is effectively added to the end of the series for purposes of calculating the checksum. The calculated checksum is the 16-bit one's complement of the one's complement sum of all 16-bit integers. For example, if the bytes included in the checksum were {89h, ABh, CDh}, the checksum would begin by computing 89ABh + CD00h. A carry out of the 16th bit would occur in the example, so in 16-bit one's complement arithmetic, it would be added back to the first bit. The resulting value of 56ACh would finally be complemented to achieve a checksum of A953h.

To calculate a checksum:

1. Program the EDMAST and EDMAND register pairs to point to the first and last bytes of buffer data to be included in the checksum. Care should be taken when programming these Pointers to prevent a never ending checksum calculation due to receive buffer wrapping.
2. To generate an optional interrupt when the checksum calculation is done, clear EIR.DMAIF, set EIE.DMAIE and set EIE.INTIE.
3. Start the calculation by setting ECON1.CSUMEN and ECON1.DMAST.

When the checksum is finished being calculated, the hardware will clear the DMAST bit, set the DMAIF bit and an interrupt will be generated if enabled. The DMA Pointers will not be modified and no memory will be written to. The EDMACSH and EDMACSL registers will contain the calculated checksum. The host controller may write this value into a packet, compare this value with a received checksum, or use it for other purposes.

Various protocols, such as TCP and IP, have a checksum field inside a range of data which the checksum covers. If such a packet is received and the host controller needs to validate the checksum, it can do the following:

1. Read the checksum from the packet and save it to a temporary location
2. Write zeros to the checksum field.
3. Calculate a new checksum using the DMA controller.
4. Compare the results with the saved checksum from step 1.

Writing to the receive buffer is permitted when the write address is protected by means of the ERXRDPT Pointers. See **Section 7.2 "Receiving Packets"** for additional information.

The IP checksum has unique mathematical properties which may be used in some cases to reduce the processing requirements further. Writing to the receive buffer may be unnecessary in some applications.

When operating the DMA in Checksum mode, it will take one main clock cycle for every byte included in the checksum. As a result, if a checksum over 1446 bytes were performed, the DMA module would require slightly more than 57.84 μs to complete the operation.

TABLE 13-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DMA CONTROLLER

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
EIE	INTIE	PKTIE	DMAIE	LINKIE	TXIE	r	TXERIE	RXERIE	13
EIR	—	PKTIF	DMAIF	LINKIF	TXIF	r	TXERIF	RXERIF	13
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	13
ERXNDL	RX End Low Byte (ERXND<7:0>)								13
ERXNDH	—	—	—	RX End High Byte (ERXND<12:8>)					13
EDMASTL	DMA Start Low Byte (EDMAST<7:0>)								13
EDMASTH	—	—	—	DMA Start High Byte (EDMAST<12:8>)					13
EDMANDL	DMA End Low Byte (EDMAND<7:0>)								13
EDMANDH	—	—	—	DMA End High Byte (EDMAND<12:8>)					13
EDMADSTL	DMA Destination Low Byte (EDMADST<7:0>)								13
EDMADSTH	—	—	—	DMA Destination High Byte (EDMADST<12:8>)					13
EDMACSL	DMA Checksum Low Byte (EDMACS<7:0>)								13
EDMACSH	DMA Checksum High Byte (EDMACS<15:8>)								13

Legend: — = unimplemented, read as '0'. Shaded cells are not used with the DMA controller.

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14.0 POWER-DOWN

The ENC28J60 may be commanded to power-down via the SPI interface. When powered down, it will no longer be able to transmit and receive any packets.

To maximize power savings:

1. Turn off packet reception by clearing ECON1.RXEN.
2. Wait for any in-progress packets to finish being received by polling ESTAT.RXBUSY. This bit should be clear before proceeding.
3. Wait for any current transmissions to end by confirming ECON1.TXRTS is clear.
4. Set ECON2.VRPS (if not already set).
5. Enter Sleep by setting ECON2.PWRSV. All MAC, MII and PHY registers become inaccessible as a result. Setting PWRSV also clears ESTAT.CLKRDY automatically.

In Sleep mode, all registers and buffer memory will maintain their states. The ETH registers and buffer memory will still be accessible by the host controller. Additionally, the clock driver will continue to operate. The CLKOUT function will be unaffected (see **Section 2.3 "CLKOUT Pin"**).

When normal operation is desired, the host controller must perform a slightly modified procedure:

1. Wake-up by clearing ECON2.PWRSV.
2. Wait at least 300 μs for the PHY to stabilize. To accomplish the delay, the host controller may poll ESTAT.CLKRDY and wait for it to become set.
3. Restore receive capability by setting ECON1.RXEN.

After leaving Sleep mode, there is a delay of many milliseconds before a new link is established (assuming an appropriate link partner is present). The host controller may wish to wait until the link is established before attempting to transmit any packets. The link status can be determined by polling the PHSTAT2.LSTAT bit. Alternatively, the link change interrupt may be used if it is enabled. See **Section 12.1.5 "Link Change Interrupt Flag (LINKIF)"** for additional details.

TABLE 14-1: SUMMARY OF REGISTERS USED WITH POWER-DOWN

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
ESTAT	INT	BUFER	r	LATECOL	—	RXBUSY	TXABRT	CLKRDY	13
ECON2	AUTOINC	PKTDEC	PWRSV	r	VRPS	—	—	—	13
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	13

Legend: — = unimplemented, read as '0', r = reserved bit. Shaded cells are not used for power-down.

NOTES:

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15.0 BUILT-IN SELF-TEST CONTROLLER

The ENC28J60 features a Built-in Self-Test (BIST) module which is designed to confirm proper operation of each bit in the 8-Kbyte memory buffer. Although it is primarily useful for testing during manufacturing, it remains present and available for diagnostic purposes by the user. The controller writes to all locations in the buffer memory and requires several pieces of hardware shared by normal Ethernet operations. Thus, the BIST should only be used on Reset or after necessary hardware is freed. When the BIST is used, the ECON1 register's DMAST, RXEN and TXRTS bits should all be clear.

The BIST controller is operated through four registers:

- EBSTCON register (control and status register)
- EBSTSD register (fill seed/initial shift value)
- EBSTCSH and EBSTCSL registers (high and low bytes of generated checksum)

The EBSTCON register (Register 15-1) controls the module's overall operation, selecting the testing modes and starting the self-test process. The bit pattern for memory tests is provided by the EBSTSD seed register; its content is either used directly, or as the seed for a pseudo-random number generator, depending on the Test mode.

REGISTER 15-1: EBSTCON: ETHERNET SELF-TEST CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSV2	PSV1	PSV0	PSEL	TMSEL1	TMSEL0	TME	BISTST
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **PSV2:PSV0:** Pattern Shift Value bits

When TMSEL<1:0> = 10:
The bits in EBSTSD will shift left by this amount after writing to each memory location.

When TMSEL<1:0> = 00, 01 or 11:
This value is ignored.

bit 4 **PSEL:** Port Select bit

1 = DMA and BIST modules will swap ports when accessing the memory
0 = Normal configuration

bit 3-2 **TMSEL1:TMSEL0:** Test Mode Select bits

11 = Reserved
10 = Pattern shift fill
01 = Address fill
00 = Random data fill

bit 1 **TME:** Test Mode Enable bit

1 = Enable Test mode
0 = Disable Test mode

bit 0 **BISTST:** Built-in Self-Test Start/Busy bit

1 = Test in progress; cleared automatically when test is done
0 = No test running

15.1 Using the BIST

When the BIST controller is started, it will fill the entire buffer with the data generated for the current test configuration and it will also calculate a checksum of the data as it is written. When the BIST is complete, the EBSTCS registers will be updated with the checksum. The host controller will be able to determine if the test passed or failed by using the DMA module to calculate a checksum of all memory. The resulting checksum generated by the DMA should match the BIST checksum. If after any properly executed test, the checksums differ, a hardware fault may be suspected.

The BIST controller supports 3 different operations:

- Random Data Fill
- Address Fill
- Pattern Shift Fill

The ports through which the BIST and DMA modules access the dual port SRAM can be swapped for each of the four Test modes to ensure proper read/write capability from both ports.

To use the BIST:

1. Program the EDMAST register pair to 0000h.
2. Program EDMAND and ERXND register pairs to 1FFFh.
3. Configure the DMA for checksum generation by setting CSUMEN in ECON1.
4. Write the seed/initial shift value byte to the EBSTSD register (this is not necessary if Address Fill mode is used).
5. Enable Test mode, select the desired test, select the desired port configuration for the test.
6. Start the BIST by setting EBSTCON.BISTST.
7. Start the DMA checksum by setting DMAST in ECON1. The DMA controller will read the memory at the same rate the BIST controller will write to it, so the DMA can be started any time after the BIST is started.
8. Wait for the DMA to complete by polling the DMAST bit or receiving the DMA interrupt (if enabled).
9. Compare the EDMACS registers with the EBSTCS registers.

To ensure full testing, the test should be redone with the Port Select bit, PSEL, altered. When not using Address Fill mode, additional tests may be done with different seed values to gain greater confidence that the memory is working as expected.

At any time during a test, the test can be canceled by clearing the BISTST, DMAST and TME bits. While the BIST is filling memory, the EBSTSD register should not be accessed, nor should any configuration changes occur. When the BIST completes its memory fill and checksum generation, the BISTST bit will automatically be cleared.

The BIST module requires one main clock cycle for each byte that it writes into the RAM. The DMA module's checksum implementation requires the same time but it can be started immediately after the BIST is started. As a result, the minimum time required to do one test pass is slightly greater than 327.68 μs.

15.2 Random Data Fill Mode

In Random Data Fill mode, the BIST controller will write pseudo-random data into the buffer. The random data is generated by a Linear Feedback Shift Register (LFSR) implementation. The random number generator is seeded by the initial contents of the EBSTSD register and the register will have new contents when the BIST is finished.

Because of the LFSR implementation, an initial seed of zero will generate a continuous pattern of zeros. As a result, a non-zero seed value will likely perform a more extensive memory test. Selecting the same seed for two separate trials will allow a repeat of the same test.

15.3 Address Fill Mode

In Address Fill mode, the BIST controller will write the low byte of each memory address into the associated buffer location. As an example, after the BIST is operated, the location 0000h should have 00h in it, location 0001h should have 01h in it, location 0E2Ah should have 2Ah in it and so on. With this fixed memory pattern, the BIST and DMA modules should always generate a checksum of F807h. The host controller may use Address Fill mode to confirm that the BIST and DMA modules themselves are both operating as intended.

15.4 Pattern Shift Fill Mode

In Pattern Shift Fill mode, the BIST controller writes the value of EBSTSD into memory location 0000h. Before writing to location 0001h, it shifts the contents of EBSTSD to the left by the value specified by the PSV2:PSV0 bits in EBSTCON. Bits that leave the most significant end of EBSTSD are wrapped around to the least significant side. This shift is repeated for each new address. As a result of shifting the data, a checkerboard pattern can be written into the buffer memory to confirm that adjacent memory elements do not affect each other when accessed.

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TABLE 15-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE SELF-TEST CONTROLLER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	13
ERXNDL	RX End Low Byte (ERXND<7:0>)								13
ERXNDH	—	—	—	RX End High Byte (ERXND<12:8>)					13
EDMASTL	DMA Start Low Byte (EDMAST<7:0>)								13
EDMASTH	—	—	—	DMA Start High Byte (EDMAST<12:8>)					13
EDMANDL	DMA End Low Byte (EDMAND<7:0>)								13
EDMANDH	—	—	—	DMA End High Byte (EDMAND<12:8>)					13
EDMACSL	DMA Checksum Low Byte (EDMACS<7:0>)								13
EDMACSH	DMA Checksum High Byte (EDMACS<15:8>)								13
EBSTSD	Built-in Self-Test Fill Seed (EBSTSD<7:0>)								14
EBSTCON	PSV2	PSV1	PSV0	PSEL	TMSEL1	TMSEL0	TME	BISTST	14
EBSTCSL	Built-in Self-Test Checksum Low Byte (EBSTCS<7:0>)								14
EBSTCSH	Built-in Self-Test Checksum High Byte (EBSTCS<15:8>)								14

Legend: — = unimplemented, read as '0'. Shaded cells are not used.

NOTES:

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16.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage temperature ..... -65°C to +150°C

Ambient temperature under bias ..... -40°C to +85°C (Industrial)
0°C to +70°C (Commercial)

Voltage on V_{DD}, V_{DDOSC}, V_{DDPLL}, V_{DDRX}, and V_{DDTX}, with respect to V_{SS} ..... -0.3V to 3.6V

Voltage on $\overline{RESET}$, $\overline{CS}$, SCK and SI, with respect to V_{SS} ..... -0.3V to 6.0V

Voltage on CLKOUT, SO, OSC1, OSC2, LEDA and LEDB, with respect to V_{SS} ..... -0.3V to V_{DD} + 0.3V

Voltage on TPIN+/- and TPOUT+/- with respect to V_{SS} ..... -0.3V to 5.0V

V_{CAP} with respect to V_{SS} **(Note 1)** ..... -0.3V to 2.75V

ESD protection on all pins ..... 2 kV

Current sourced or sunk by LEDA, LEDB ..... 12 mA

Current sourced or sunk by CLKOUT ..... 8 mA

Current sourced or sunk by $\overline{INT}$ and SO ..... 4 mA

Note 1: V_{CAP} is not designed to supply an external load. No external voltage should be applied to this pin.

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

16.1 DC Characteristics: ENC28J60 (Industrial and Commercial)

DC CHARACTERISTICS			Standard Operating Conditions -40°C ≤ TA ≤ +85°C, 3.10V ≤ VDD ≤ 3.60V (Industrial) 0°C ≤ TA ≤ +70°C, 3.10V ≤ VDD ≤ 3.60V (Commercial)				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	3.10	3.30	3.60	V	
D002	VPOR	**VDD Power-on Reset Voltage**	—	—	0.7	V	See section on Power-on Reset for details
D003	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details
	VIH	**Input High Voltage**					
D004		SCK, $\overline{CS}$, SI, $\overline{RESET}$	2.25	—	5.5	V	
D005		OSC1	0.7 VDD	—	VDD	V	
	VIL	**Input Low Voltage**					
D006		SCK, $\overline{CS}$, SI, $\overline{RESET}$	VSS	—	1.0	V	
D007		OSC1	VSS	—	0.3 VDD	V	
	VOH	**Output High Voltage**					
		LEDA, LEDB	VDD – 0.7	—	—	V	IOH = -12.0 mA (**Note 1**)
		CLKOUT	VDD – 0.7	—	—	V	IOH = -8.0 mA (**Note 1**)
		$\overline{INT}$, SO	VDD – 0.7	—	—	V	IOH = -4.0 mA (**Note 1**)
	VOL	**Output Low Voltage**					
		LEDA, LEDB	—	—	0.4	V	IOL = 12.0 mA
		CLKOUT	—	—	0.4	V	IOL = 8.0 mA
		$\overline{INT}$, SO	—	—	0.4	V	IOL = 4.0 mA
	RPU	**Weak Pull-up Resistance**	74K	—	173K	Ω	
	IIL	**Input Leakage Current**					
		All input pins except OSC1	—	—	±1	µA	$\overline{CS}$ = $\overline{RESET}$ = VDD, VSS ≤ VPIN ≤ VDD, pins in high-impedance state (**Note 1**)
		OSC1 pin	—	—	±200	µA	OSC1 = VDD (**Note 1**)
	IDD	**Operating Current**					
		Transmitting Ethernet packets	—	160	180	mA	VDD = 3.30V, FSCK = 10 MHz, SO = Open, LEDA and LEDB open, ECON2<PWRSV> = 0
		Active, not transmitting Ethernet packets	—	120	—	mA	VDD = 3.30V, LEDA and LEDB open, ECON2<PWRSV> = 0
	IDDS	**Standby Current** (Sleep mode)	—	1.2	2.0	mA	$\overline{CS}$ = VDD, Inputs tied to VDD or VSS, VDD = 3.3V, TA = 25°C, ECON2<PWRSV> = 1

Note 1: Negative current is defined as current sourced by the pin.

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TABLE 16-1: AC CHARACTERISTICS: ENC28J60 (INDUSTRIAL AND COMMERCIAL)

AC CHARACTERISTICS	Standard Operating Conditions -40°C ≤ TA ≤ +85°C, 3.10V ≤ VDD ≤ 3.60V (Industrial) 0°C ≤ TA ≤ +70°C, 3.10V ≤ VDD ≤ 3.60V (Commercial)

TABLE 16-2: OSCILLATOR TIMING CHARACTERISTICS

Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
	FOSC	Clock In Frequency	25	25	MHz	
	TOSC	Clock In Period	40	40	ns	
	TDUTY	Duty Cycle (external clock input)	40	60	%	
	Δf	Clock Tolerance	—	±50	ppm	

TABLE 16-3: RESET AC CHARACTERISTICS

Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
	trl	$\overline{\text{RESET}}$ Pin High Time (between Reset events)	2	—	µs	
	tRSTLOW	$\overline{\text{RESET}}$ Pin Low Time to trigger Reset	400	—	ns	

TABLE 16-4: CLKOUT PIN AC CHARACTERISTICS

Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
	t_{h}CLKOUT	CLKOUT Pin High Time	16.5	—	ns	TDUTY = 50% (**Note 1**)
	t_{l}CLKOUT	CLKOUT Pin Low Time	16.5	—	ns	TDUTY = 50% (**Note 1**)
	t_{r}CLKOUT	CLKOUT Pin Rise Time	—	3	ns	Measured from 0.1 VDD to 0.9 VDD, Load = 10 pF (**Note 1**)
	t_{f}CLKOUT	CLKOUT Pin Fall Time	—	4	ns	Measured from 0.9 VDD to 0.1 VDD, Load = 10 pF (**Note 1**)

Note 1: CLKOUT prescaler is set to divide by one.

TABLE 16-5: REQUIREMENTS FOR EXTERNAL MAGNETICS

Parameter	Min	Norm	Max	Units	Conditions
RX Transformer Turns Ratio	—	1:1	—	—	
TX Transformer Turns Ratio	—	1:1	—	—	Transformer Center Tap = 3.3V
Insertion Loss	0.0	0.6	1.1	dB	
Primary Inductance	350	—	—	µH	8 mA bias
Transformer Isolation	—	1.5	—	kV	
Differential to Common Mode Rejection	40	—	—	dB	0.1 to 10 MHz
Return Loss	-16	—	—	dB	

FIGURE 16-1: SPI INPUT TIMING

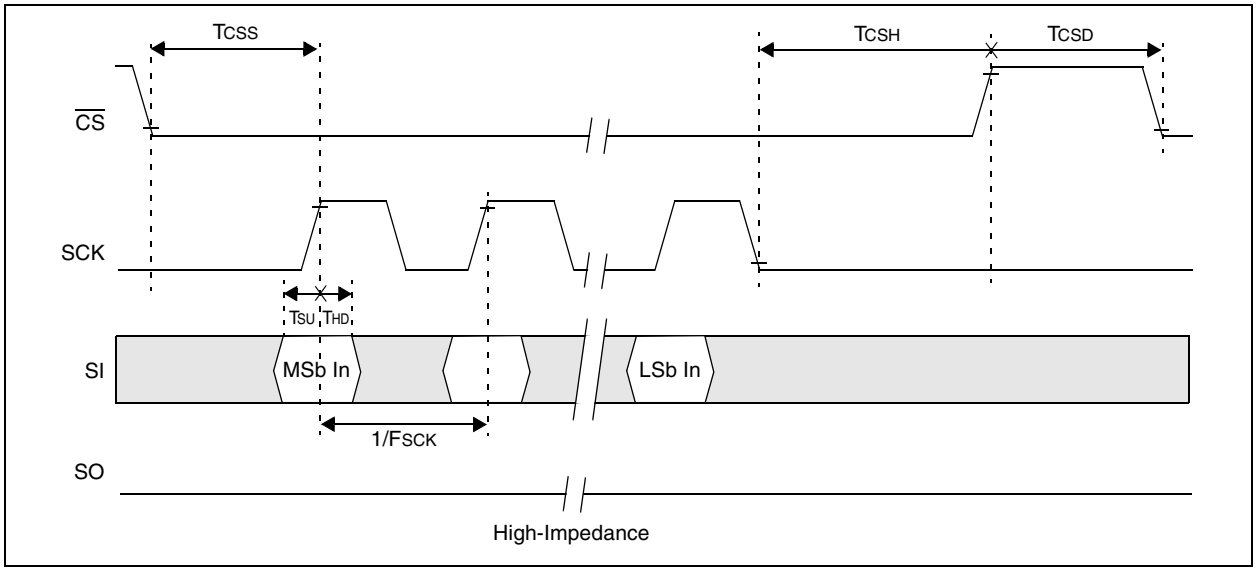


FIGURE 16-2: SPI OUTPUT TIMING

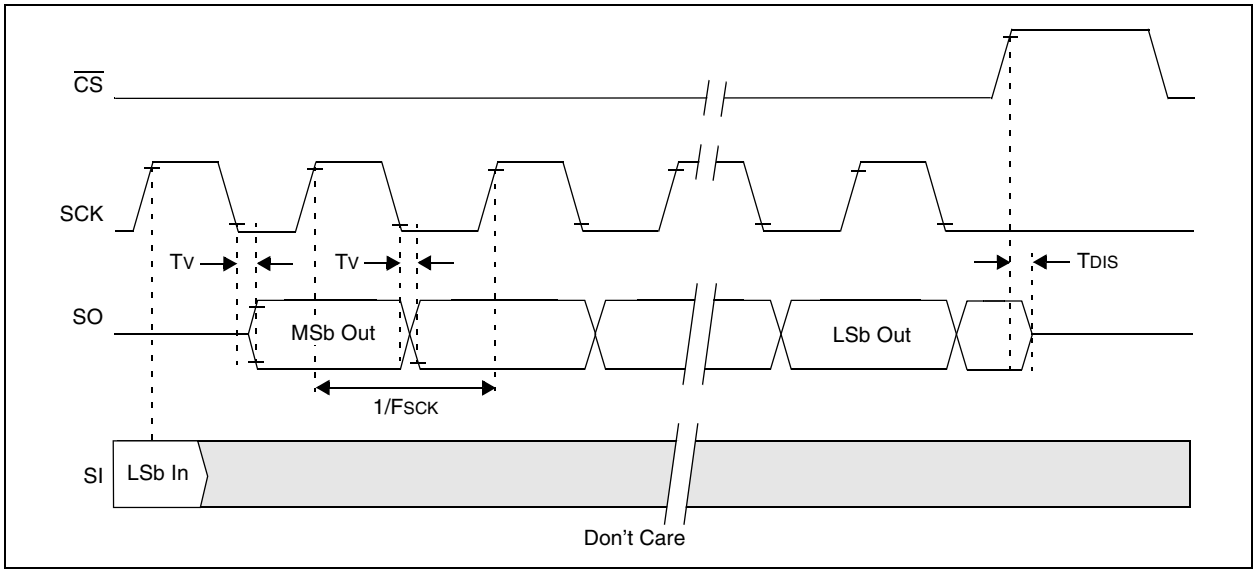


TABLE 16-6: SPI INTERFACE AC CHARACTERISTICS

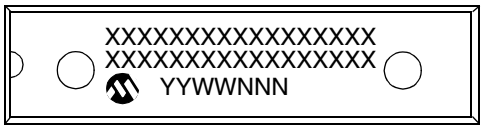
Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
	FSCK	Clock Frequency	DC	20	MHz	
1	TCSS	$\overline{CS}$ Setup Time	50	—	ns	
2	TCSH	$\overline{CS}$ Hold Time	10	—	ns	ETH registers and memory buffer
			210	—	ns	MAC and MII registers
3	TCSD	$\overline{CS}$ Disable Time	50	—	ns	
4	TSU	Data Setup Time	10	—	ns	
5	THD	Data Hold Time	10	—	ns	
6	TV	Output Valid from Clock Low	—	10	ns	SO Load = 30 pF
7	TDIS	Output Disable Time	—	10	ns	SO Load = 30 pF

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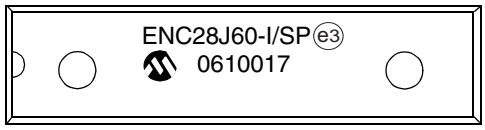
17.0 PACKAGING INFORMATION

17.1 Package Marking Information

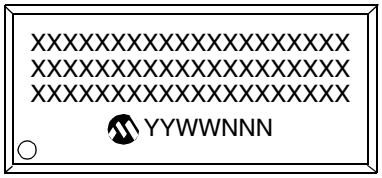
28-Lead SPDIP



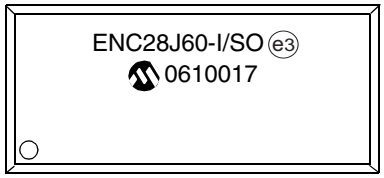
Example



28-Lead SOIC



Example



28-Lead SSOP



Example



28-Lead QFN



Example



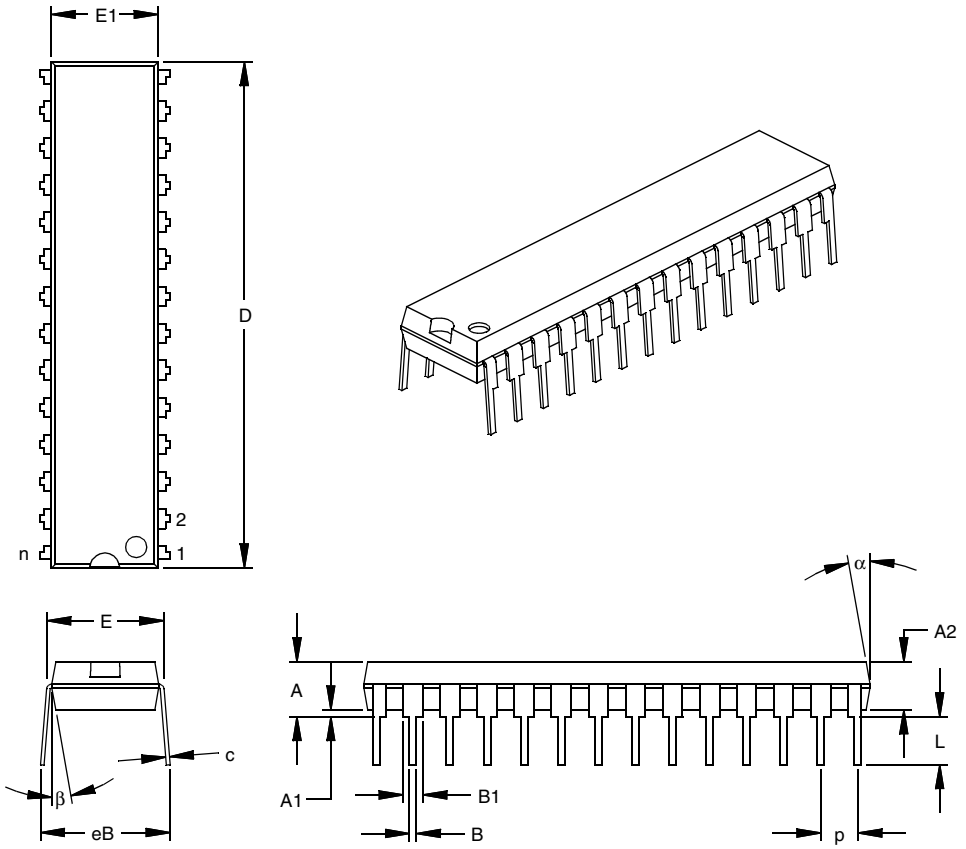
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

17.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-line (SP) – 300 mil Body (PDIP)

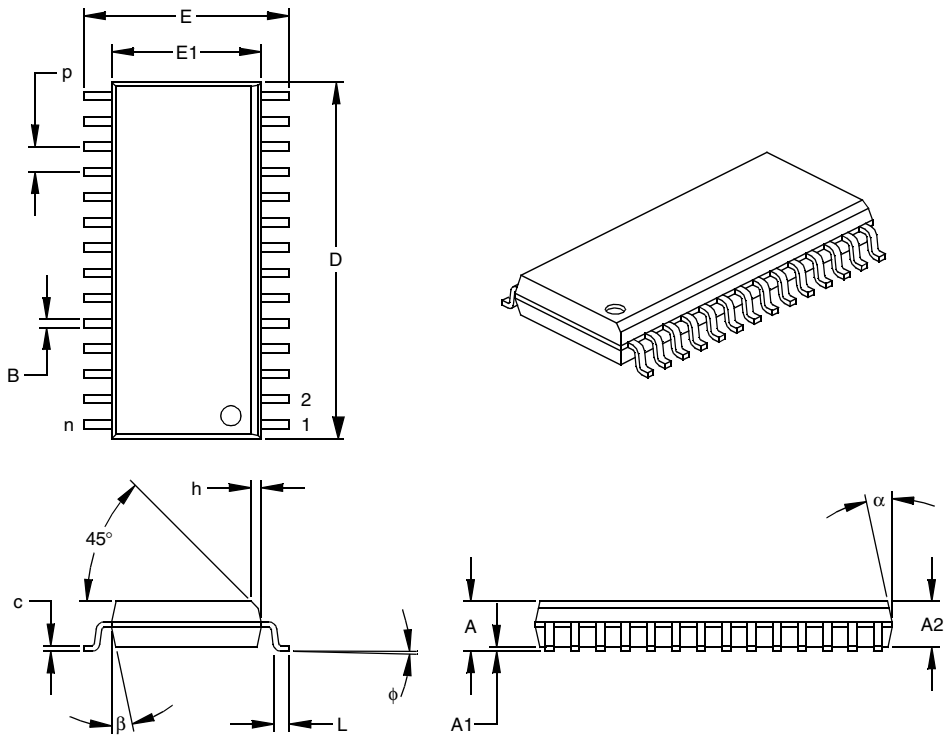


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	B	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-095
Drawing No. C04-070

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28-Lead Plastic Small Outline (SO) – Wide, 300 mil Body (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter

§ Significant Characteristic

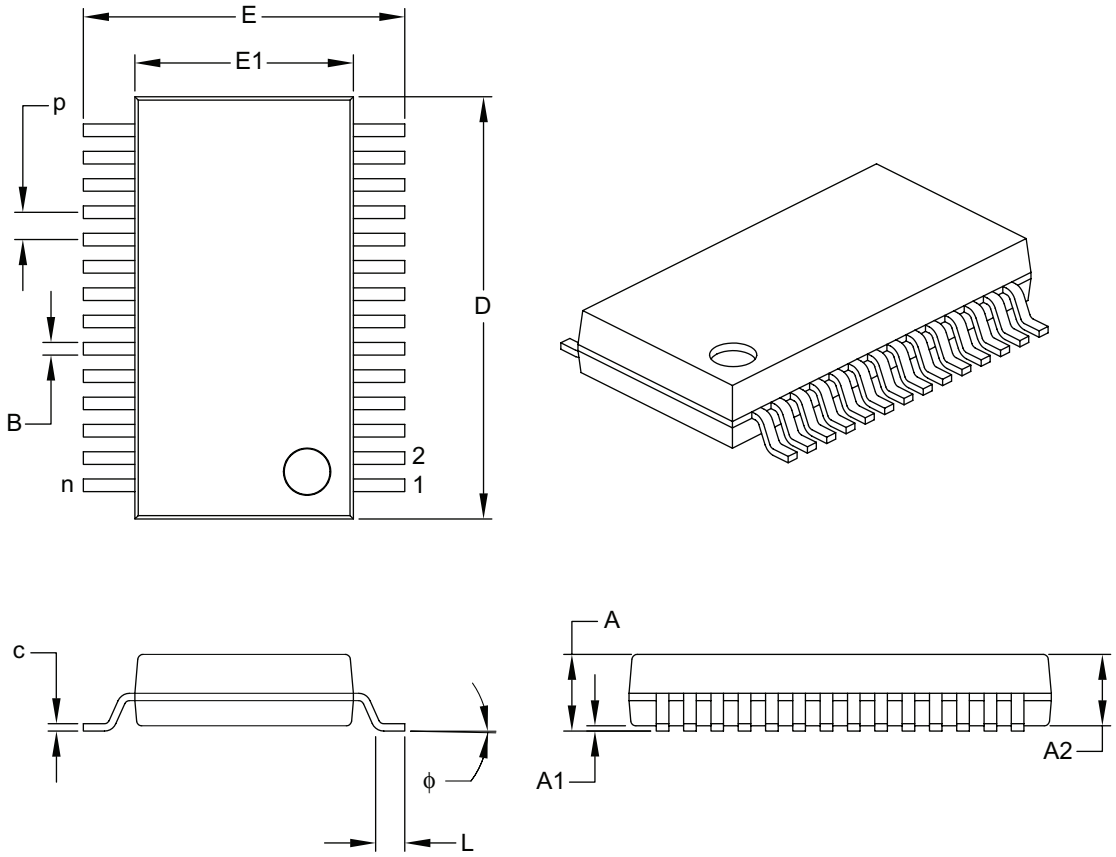
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-052

28-Lead Plastic Shrink Small Outline (SS) – 209 mil Body, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS *		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.0
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.295	.307	.323	7.49	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.390	.402	.413	9.90	10.20	10.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95
Lead Thickness	c	.004	-	.010	0.09	-	0.25
Foot Angle	ϕ	0°	4°	8°	0°	4°	8°
Lead Width	B	.009	-	.015	0.22	-	0.38

***** Controlling Parameter

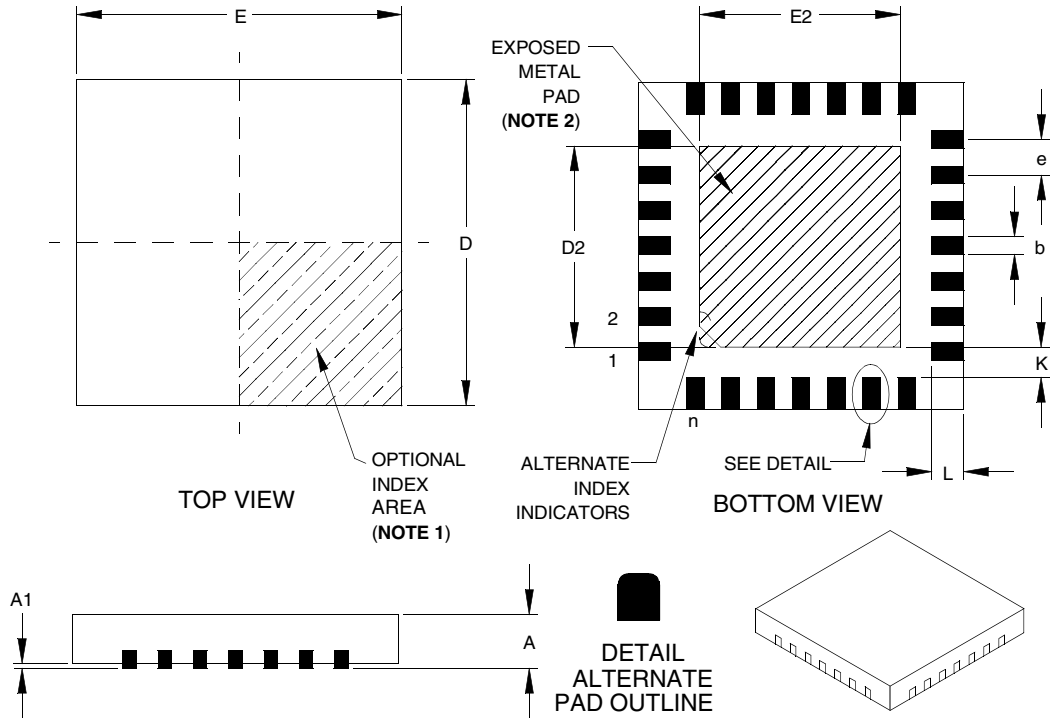
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-073 Revised 1-12-06

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28-Lead Plastic Quad Flat No Lead Package (ML) 6x6 mm Body (QFN) – With 0.55 mm Contact Length (Saw Singulated)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	e	.026 BSC			0.65 BSC		
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3	.008 REF			0.20 REF		
Overall Width	E	.232	.236	.240	5.90	6.00	6.10
Exposed Pad Width	E2	.153	.167	.169	3.89	4.24	4.29
Overall Length	D	.232	.236	.240	5.90	6.00	6.10
Exposed Pad Length	D2	.153	.167	.169	3.89	4.24	4.29
Contact Width	β	.009	.011	.013	0.23	0.28	0.33
Contact Length §	L	.018	.022	.024	0.45	0.55	0.65
Contact-to-Exposed Pad §	K	.008	–	–	0.20	–	–

***** Controlling Parameter

§ Significant Characteristic

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Exposed pad varies according to die attach paddle size.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

JEDEC equivalent: MO-220

Drawing No. C04-105

Revised 09-12-05

NOTES:

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Package	SP =	SPDIP (Skinny Plastic DIP)
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