ALPHA & OMEGA SEMICONDUCTOR

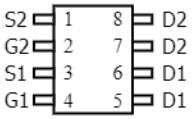
AO4828
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

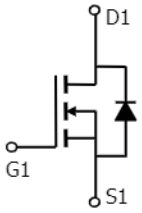
The AO4828 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. *Standard Product AO4828 is Pb-free (meets ROHS & Sony 259 specifications). AO4828L is a Green Product ordering option. AO4828 and AO4828L are electrically identical.*

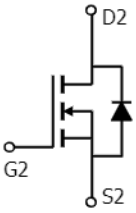
Features

V_{DS} (V) = 60V
I_D = 4.5A (V_{GS} = 10V)
$R_{DS(ON)}$ < 56mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 77mΩ (V_{GS} = 4.5V)



SOIC-8





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	4.5	A
	T_A=70°C		3.6	
Pulsed Drain Current [B]		I_{DM}	20	
Power Dissipation	T_A=25°C	P_D	2	W
	T_A=70°C		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		74	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	35	60	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	2.1	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=4.5A		46	56	mΩ
		T_J=125°C		80	100	
		V_{GS}=4.5V, I_D=3A		64	77	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=4.5A		11		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		450	540	pF
C_{oss}	Output Capacitance			60		pF
C_{rss}	Reverse Transfer Capacitance			25		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.65	2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=4.5A		8.5	10.5	nC
Q_g(4.5V)	Total Gate Charge			4.3	5.5	nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			2.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=6.7Ω, R_{GEN}=3Ω		4.7		ns
t_r	Turn-On Rise Time			2.3		ns
$t_{D(off)}$	Turn-Off DelayTime			15.7		ns
t_f	Turn-Off Fall Time			1.9		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=4.5A, dI/dt=100A/µs		27.5	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=4.5A, dI/dt=100A/µs		32		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev 3: June 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

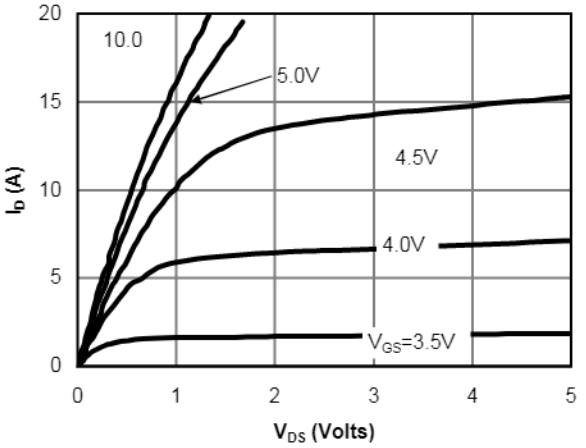


Fig 1: On-Region Characteristics

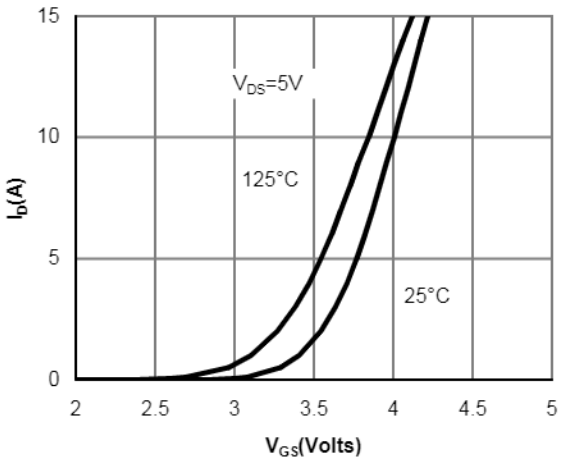


Figure 2: Transfer Characteristics

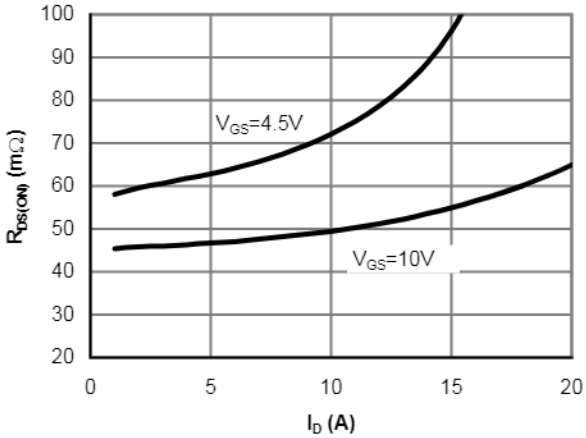


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

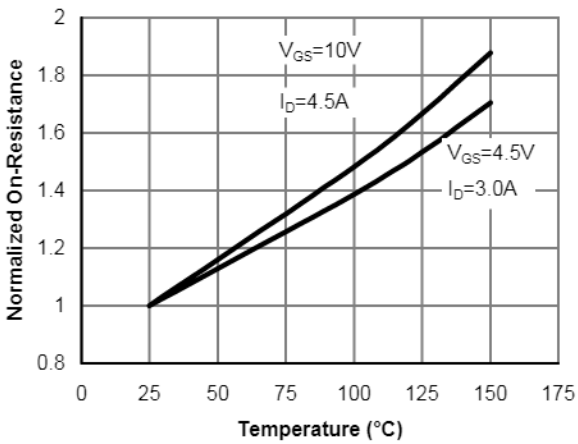


Figure 4: On-Resistance vs. Junction Temperature

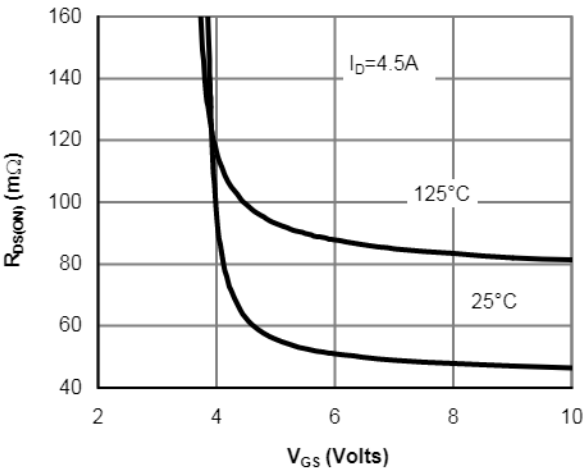


Figure 5: On-Resistance vs. Gate-Source Voltage

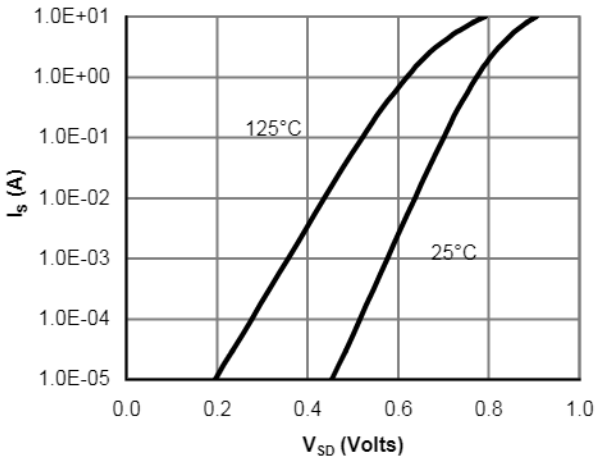


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

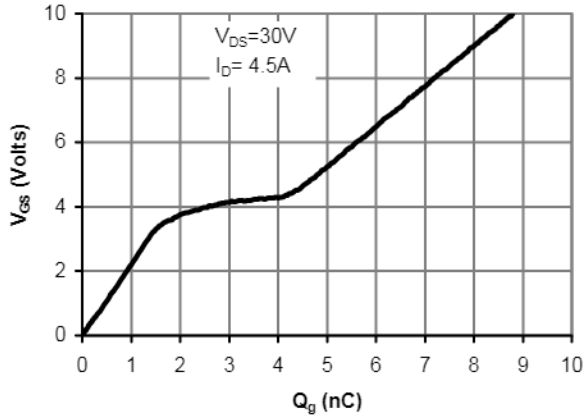


Figure 7: Gate-Charge Characteristics

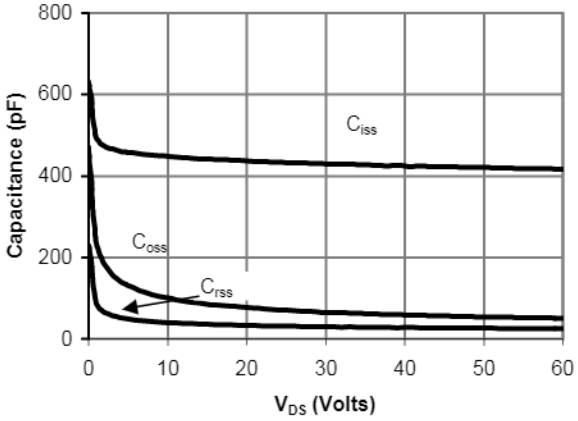


Figure 8: Capacitance Characteristics

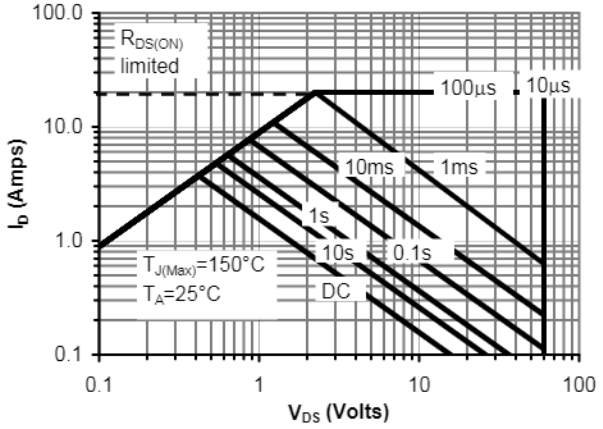


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

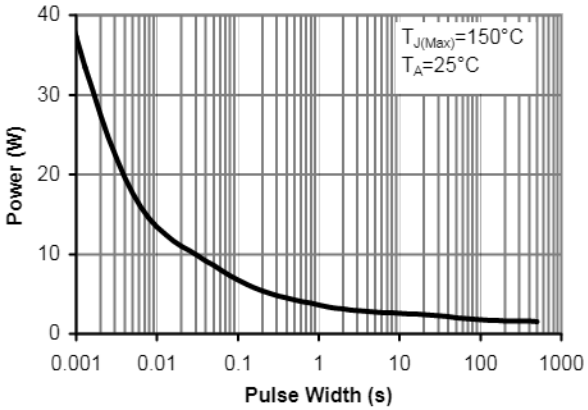


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

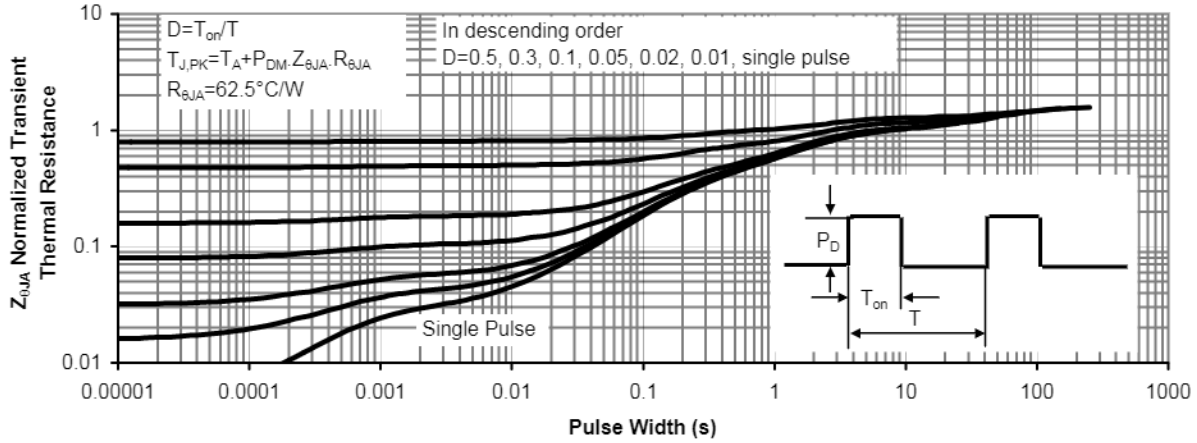


Figure 11: Normalized Maximum Transient Thermal Impedance