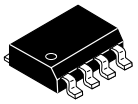
Critical Conduction Mode PFC Controller

FAN7930C



SOIC8
CASE 751EB

Description

The FAN7930C is an active power factor correction (PFC) controller for boost PFC applications that operate in critical conduction mode (CRM). It uses a voltage−mode PWM that compares an internal ramp signal with the error amplifier output to generate a MOSFET turn−off signal. Because the voltage−mode CRM PFC controller does not need rectified AC line voltage information, it saves the power loss of an input voltage−sensing network necessary for a current−mode CRM PFC controller.

FAN7930C provides over−voltage protection (OVP), open−feedback protection, over−current protection (OCP), input−voltage−absent detection, and under−voltage lockout protection (UVLO). The PFC−ready pin can be used to trigger other power stages when PFC output voltage reaches the proper level with hysteresis. The FAN7930C can be disabled if the INV pin voltage is lower than 0.45 V and the operating current decreases to a very low level. Using a new variable on−time control method, total harmonic distortion (THD) is lower than in conventional CRM boost PFC ICs.

Features

- PFC−Ready Signal
- V_{IN}−Absent Detection
- Maximum Switching Frequency Limitation
- Internal Soft−Start and Startup without Overshoot
- Internal Total Harmonic Distortion (THD) Optimizer
- Precise Adjustable Output Over−Voltage Protection
- Open−Feedback Protection and Disable Function
- Zero−Current Detector (ZCD)
- 150 μs Internal Startup Timer
- MOSFET Over−Current Protection (OCP)
- Under−Voltage Lockout with 3.5 V Hysteresis
- Low Startup and Operating Current
- Totem−Pole Output with High State Clamp
- +500/−800 mA Peak Gate Drive Current
- 8−Pin, Small Outline Package (SOP)

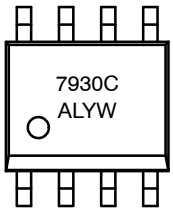
Applications

- Adapter
- Ballast
- LCD TV, CRT TV
- SMPS

Related Resources

- AN−8035/D − Design Consideration for Boundary Conduction Mode PFC Using FAN7930

MARKING DIAGRAM



7930C = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

See detailed ordering and shipping information on page X of this data sheet.

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ORDERING INFORMATION

Part Number	Operating Temperature Range	Top Mark	Package	Shipping†
FAN7930CMX−G	−40 to +125°C	7930C	8−Lead, Small Outline Package (SOP) (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

APPLICATION DIAGRAM

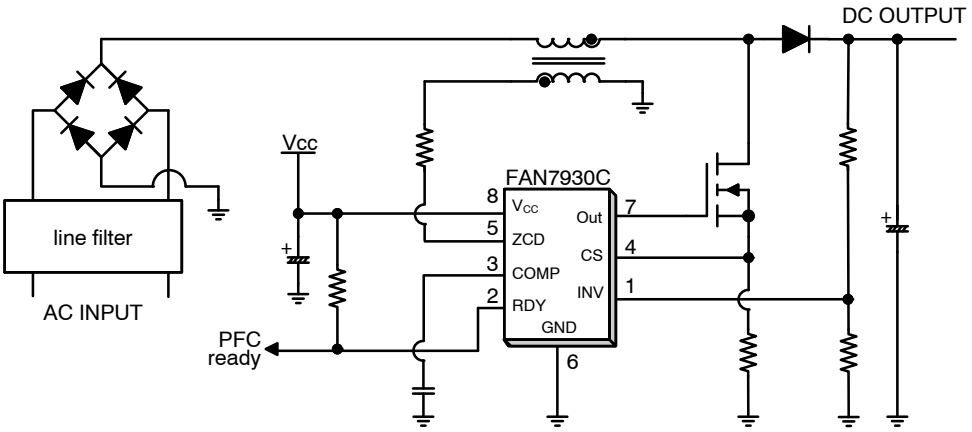


Figure 1. Typical Boost PFC Application

INTERNAL BLOCK DIAGRAM

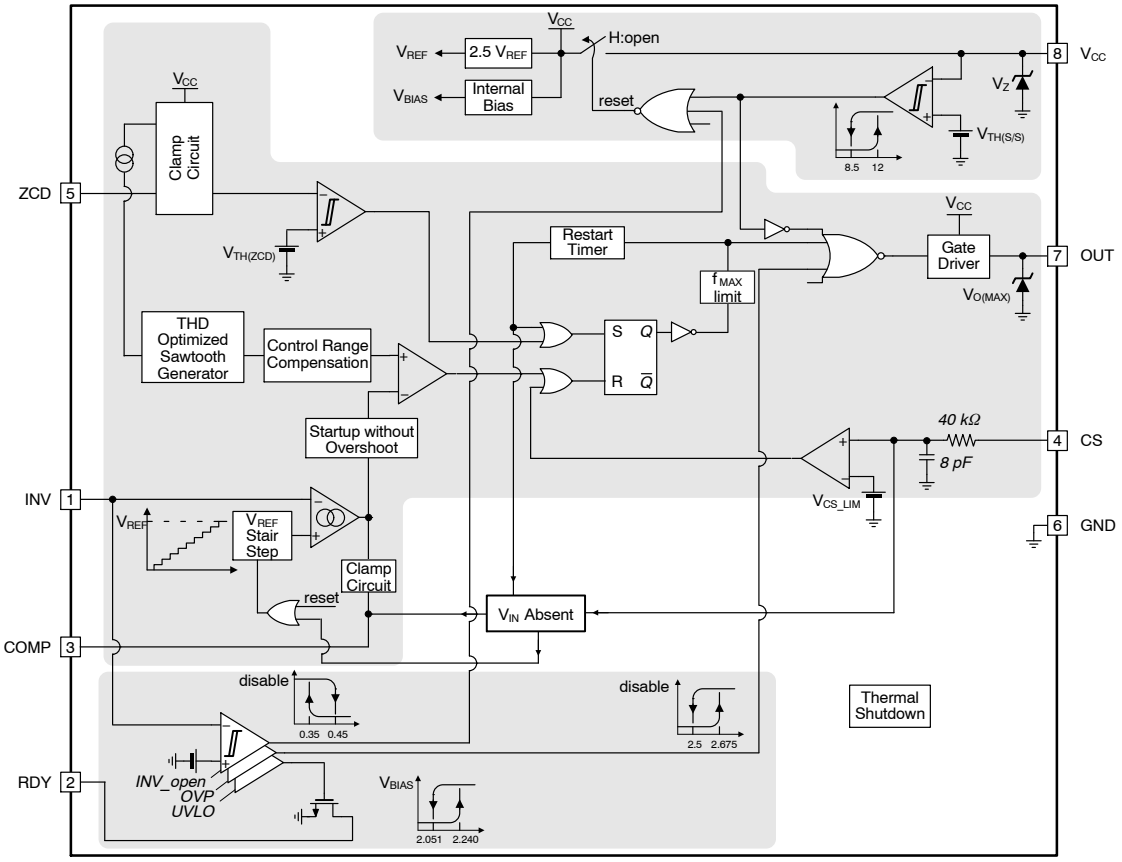


Figure 2. Functional Block Diagram

PIN CONFIGURATION

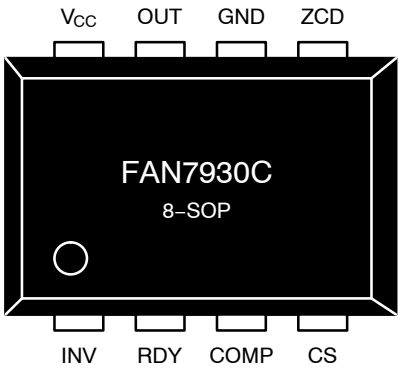


Figure 3. Pin Configuration (Top View)

PIN DEFINITIONS

Pin No.	Name	Description
1	INV	This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5 V.
2	RDY	This pin is used to detect PFC output voltage reaching a pre−determined value. When output voltage reaches 89% of rated output voltage, this pin is pulled HIGH, which is an (open−drain) output type.
3	COMP	This pin is the output of the transconductance error amplifier. Components for the output voltage compensation should be connected between this pin and GND.
4	CS	This pin is the input of the over−current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise.
5	ZCD	This pin is the input of the zero−current detection (ZCD) block. If the voltage of this pin goes higher than 1.5 V, then goes lower than 1.4 V, the MOSFET is turned on.
6	GND	This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
7	OUT	This pin is the gate drive output. The peak sourcing and sinking current levels are +500 mA and −800 mA, respectively. For proper operation, the stray inductance in the gate driving path must be minimized.
8	V_{CC}	This is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		–	V_Z	V
I_{OH}, I_{OL}	Peak Drive Output Current		−800	+500	mA
I_{CLAMP}	Driver Output Clamping Diodes $V_O > V_{CC}$ or $V_O < -0.3$ V		−10	+10	mA
I_{DET}	Detector Clamping Diodes		−10	+10	mA
V_{IN}	RDY Pin (Note 1)		–	V_Z	V
	Error Amplifier Input, Output and ZCD (Note 1)		−0.3	8.0	
	CS Input Voltage (Note 2)		−10.0	6.0	
T_J	Operating Junction Temperature		–	+150	°C
T_A	Operating Temperature Range		−40	+125	°C
T_{STG}	Storage Temperature Range		−65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114	–	2.5	kV
		Charged Device Model, JESD22−C101	–	2.0	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When this pin is supplied by external power sources by accident, its maximum allowable current is 50 mA.
2. In case of DC input, the acceptable input range is −0.3 V~6 V: within 100 ns −10 V~6 V is acceptable, but electrical specifications are not guaranteed during such a short time.

THERMAL IMPEDANCE

Symbol	Parameter	Min	Max	Unit
Θ_{JA}	Thermal Resistance, Junction−to−Ambient (Note 3)	150	–	°C/W

3. Regarding the test environment and PCB type, please refer to JESD51−2 and JESD51−10.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V and T_A = −40°C~+125°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} SECTION						
V_{START}	Start Threshold Voltage	V_{CC} Increasing	11	12	13	V
V_{STOP}	Stop Threshold Voltage	V_{CC} Decreasing	7.5	8.5	9.5	V
HY_{UVLO}	UVLO Hysteresis		3.0	3.5	4.0	V
V_Z	Zener Voltage	I_{CC} = 20 mA	20	22	24	V
V_{OP}	Recommended Operating Range		13	–	20	V
SUPPLY CURRENT SECTION						
I_{START}	Startup Supply Current	$V_{CC} = V_{START} - 0.2$ V	–	120	190	μA
I_{OP}	Operating Supply Current	Output Not Switching	–	1.5	3.0	mA
I_{DOP}	Dynamic Operating Supply Current	50 kHz, C_l = 1 nF	–	2.5	4.0	mA
I_{OPDIS}	Operating Current at Disable	V_{INV} = 0 V	90	160	230	μA
ERROR AMPLIFIER SECTION						
V_{REF1}	Voltage Feedback Input Threshold1	T_A = 25°C	2.465	2.500	2.535	V
ΔV_{REF1}	Line Regulation	V_{CC} = 14 V~20 V	–	0.1	10.0	mV
ΔV_{REF2}	Temperature Stability of V_{REF1} (Note 4)		–	20	–	mV
$I_{EA,BS}$	Input Bias Current	V_{INV} = 1 V~4 V	−0.5	–	0.5	μA
$I_{EAS,SR}$	Output Source Current	$V_{INV} = V_{REF} - 0.1$ V	–	−12	–	μA
$I_{EAS,SK}$	Output Sink Current	$V_{INV} = V_{REF} + 0.1$ V	–	12	–	μA
V_{EAH}	Output Upper Clamp Voltage	V_{INV} = 1 V, V_{CS} = 0 V	6.0	6.5	7.0	V
V_{EAZ}	Zero−Duty Cycle Output Voltage		0.9	1.0	1.1	V
g_m	Transconductance (Note 4)		90	115	140	μmho

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V and T_A = −40°C~+125°C, unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MAXIMUM ON−TIME SECTION						
$t_{ON,MAX1}$	Maximum On−Time Programming 1	T_A = 25°C, V_{ZCD} = 1 V	35.5	41.5	47.5	μs
$t_{ON,MAX2}$	Maximum On−Time Programming 2	T_A = 25°C, I_{ZCD} = 0.469 mA	11.2	13.0	14.8	μs
CURRENT−SENSE SECTION						
V_{CS}	Current−Sense Input Threshold Voltage Limit		0.7	0.8	0.9	V
$I_{CS,BS}$	Input Bias Current	V_{CS} = 0 V~1 V	−1.0	−0.1	1.0	μA
$t_{CS,D}$	Current−Sense Delay to Output (Note 4)	dV/dt = 1 V/100 ns, from 0 V to 5 V	−	350	500	ns
ZERO−CURRENT DETECT SECTION						
V_{ZCD}	Input Voltage Threshold (Note 4)		1.35	1.50	1.65	V
HY_{ZCD}	Detect Hysteresis (Note 4)		0.05	0.10	0.15	V
V_{CLAMPH}	Input High Clamp Voltage	I_{DET} = 3 mA	5.5	6.2	7.5	V
V_{CLAMPL}	Input Low Clamp Voltage	I_{DET} = −3 mA	0	0.65	1.00	V
$I_{ZCD,BS}$	Input Bias Current	V_{ZCD} = 1 V~5 V	−1.0	−0.1	1.0	μA
$I_{ZCD,SR}$	Source Current Capability (Note 4)	T_A = 25°C	−	−	−4	mA
$I_{ZCD,SK}$	Sink Current Capability (Note 4)	T_A = 25°C	−	−	10	mA
$t_{ZCD,D}$	Maximum Delay From ZCD to Output Turn−On (Note 4)	dV/dt = −1 V/100 ns, from 5 V to 0 V	100	−	200	ns
OUTPUT SECTION						
V_{OH}	Output Voltage High	I_O = −100 mA, T_A = 25°C	9.2	11.0	12.8	V
V_{OL}	Output Voltage Low	I_O = 200 mA, T_A = 25°C	−	1.0	2.5	V
t_{RISE}	Rising Time (Note 4)	C_{IN} = 1 nF	−	50	100	ns
t_{FALL}	Falling Time (Note 4)	C_{IN} = 1 nF	−	50	100	ns
$V_{O,MAX}$	Maximum Output Voltage	V_{CC} = 20 V, I_O = 100 μA	11.5	13.0	14.5	V
$V_{O,UVLO}$	Output Voltage with UVLO Activated	V_{CC} = 5 V, I_O = 100 μA	−	−	1	V
RESTART / MAXIMUM SWITCHING FREQUENCY LIMIT SECTION						
t_{RST}	Restart Timer Delay		50	150	300	μs
f_{MAX}	Maximum Switching Frequency (Note 4)		250	300	350	kHz
RDY PIN						
$I_{RDY,SK}$	Output Sink Current		1	2	4	mA
$V_{RDY,SAT}$	Output Saturation Voltage	$I_{RDY,SK}$ = 2 mA	−	320	500	mV
$I_{RDY,LK}$	Output Leakage Current	Output High Impedance	−	−	1	μA
SOFT−START TIMER SECTION						
t_{SS}	Internal Soft−Soft (Note 4)		3	5	7	ms
UVLO SECTION						
V_{RDY}	Output Ready Voltage		2.166	2.240	2.314	V
HY_{RDY}	Output Ready Hysteresis		−	0.189	−	V
PROTECTIONS						
V_{OVP}	OVP Threshold Voltage	T_A = 25°C	2.620	2.675	2.730	V
HY_{OVP}	OVP Hysteresis	T_A = 25°C	0.120	0.175	0.230	V
V_{EN}	Enable Threshold Voltage		0.40	0.45	0.50	V
HY_{EN}	Enable Hysteresis		0.05	0.10	0.15	V
T_{SD}	Thermal Shutdown Temperature (Note 4)		125	140	155	°C
T_{HYS}	Hysteresis Temperature of TSD (Note 4)			60		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. These parameters, although guaranteed by design, are not production tested.

COMPARISON OF FAN7530 AND FAN7930C

Function	FAN7530	FAN7930C	FAN7930C Advantages
PFC Ready Pin	None	Integrated	• No External Circuit for PFC Output UVLO • Reduce Power Loss and BOM Cost Caused by PFC Out UVLO Circuit • Versatile Open−Drain Pin
Frequency Limit	None	Integrated	• Abnormal CCM Operation Prohibited • Abnormal Inductor Current Accumulation Can Be Prohibited
V_{IN}−Absent Detection	None	Integrated	• Increase System Reliability by Testing for Input Supply Voltage • Guarantee Stable Operation at Short Electric Power Failure
Soft−Start and Startup without Overshoot	None	Integrated	• Reduce Voltage and Current Stress at Startup • Eliminate Audible Noise due to Unwanted OVP Triggering
Control Range Compensation	None	Integrated	• Can Avoid Burst Operation at Light Load and High Input Voltage • Reduce Probability of Audible Noise Due to Burst Operation
THD Optimizer	External	Internal	• No External Resistor Needed
TSD	None	140°C with 60°C Hysteresis	• Stable and Reliable TSD Operation • Converter Temperature Range Limited Range

COMPARISON OF FAN7530C AND FAN7930B

Function	FAN7530C	FAN7930B	Remark
RDY Pin	Integrated	None	• User Choice for the Use of Number #2 Pin
RDY Pin	None	Integrated	

TYPICAL PERFORMANCE CHARACTERISTICS

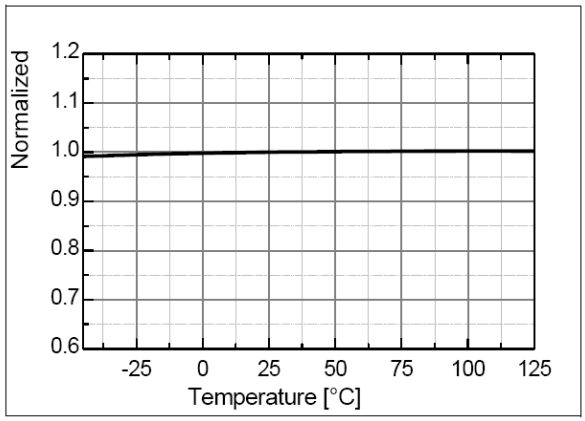


Figure 4. Voltage Feedback Input Threshold 1 (V_{REF1}) vs. T_A

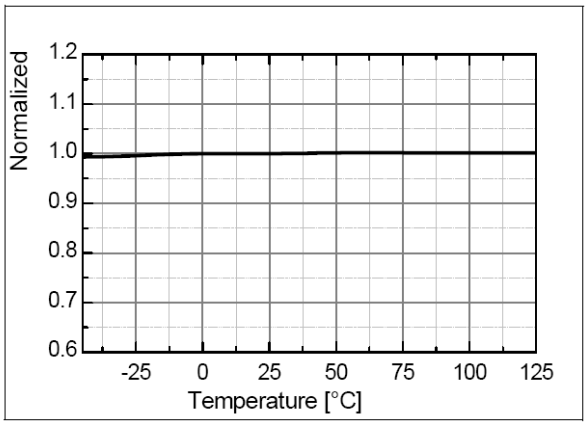


Figure 5. Start Threshold Voltage (V_{START}) vs. T_A

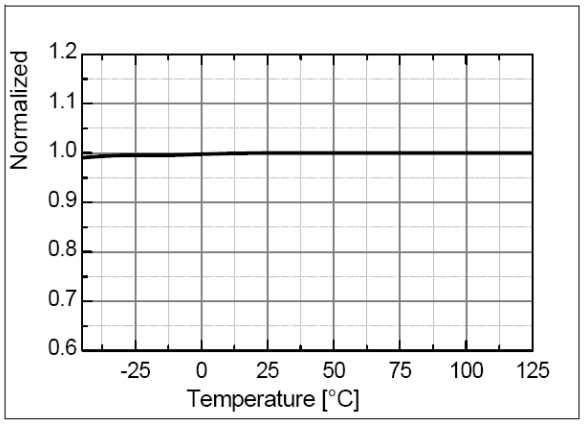


Figure 6. Stop Threshold Voltage (V_{STOP}) vs. T_A

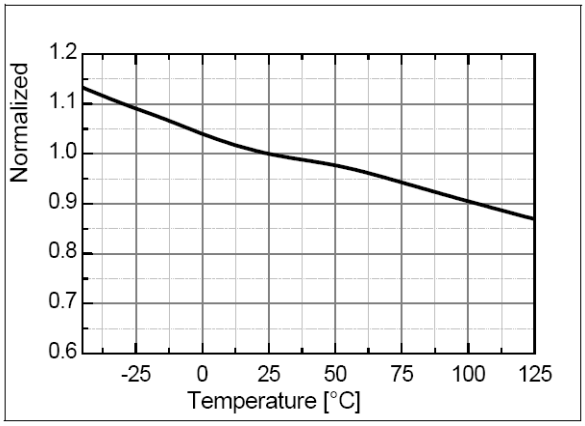


Figure 7. Startup Supply Current (I_{START}) vs. T_A

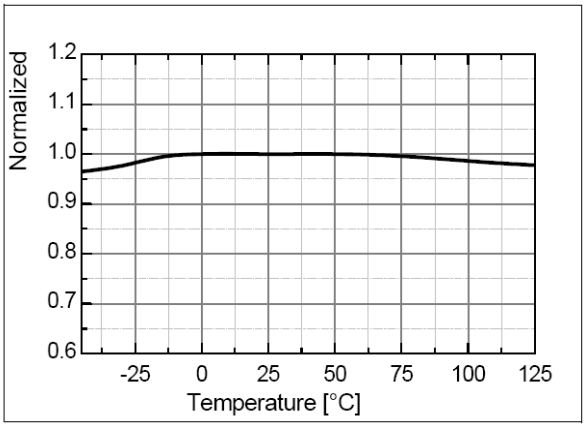


Figure 8. Operating Supply Current (I_{OP}) vs. T_A

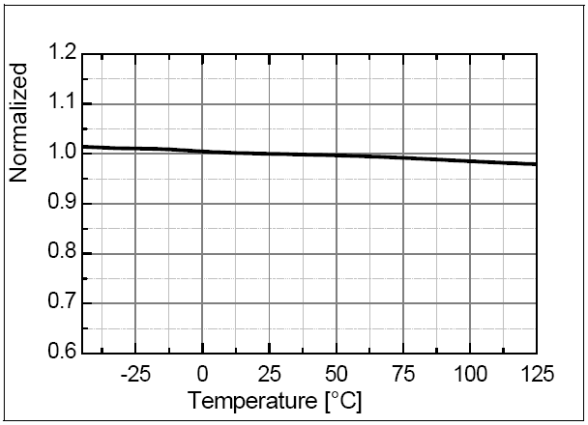


Figure 9. Output Upper Clamp Voltage (V_{EAH}) vs. T_A

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

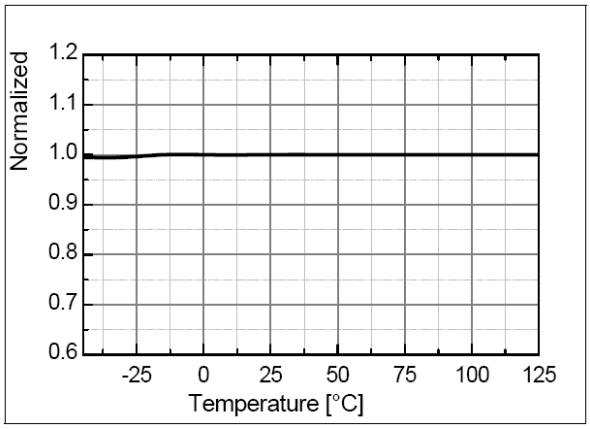


Figure 10. Zero Duty Cycle Output Voltage (V_{EAZ}) vs. T_A

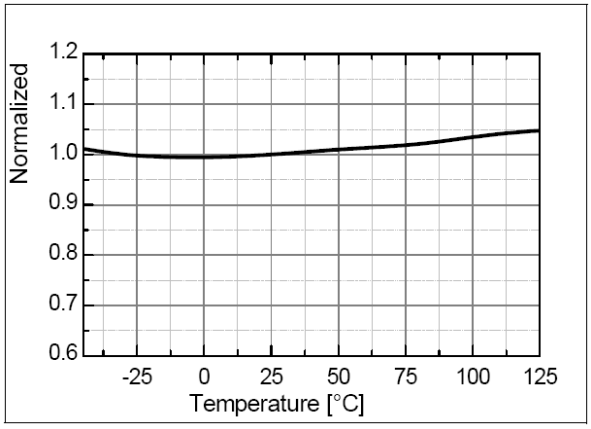


Figure 11. Maximum On−Time Program 1 ($t_{ON,MAX1}$) vs. T_A

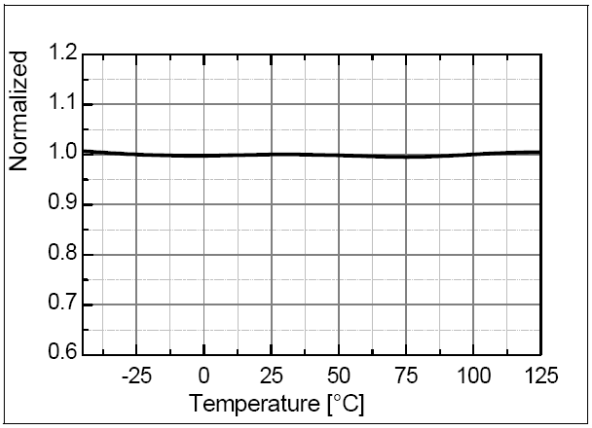


Figure 12. Maximum On−Time Program 2 ($t_{ON,MAX2}$) vs. T_A

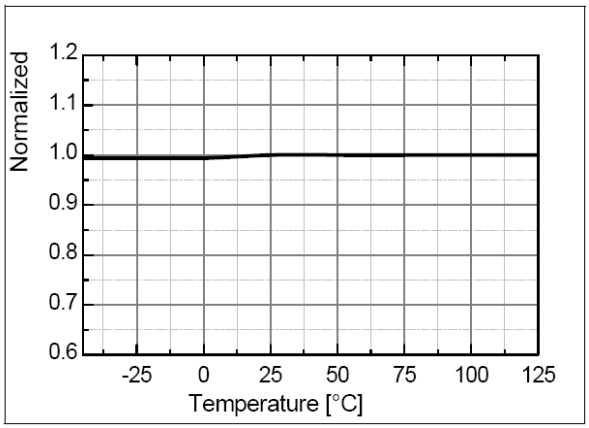


Figure 13. Current−Sense Input Threshold Voltage Limit (V_{CS}) vs. T_A

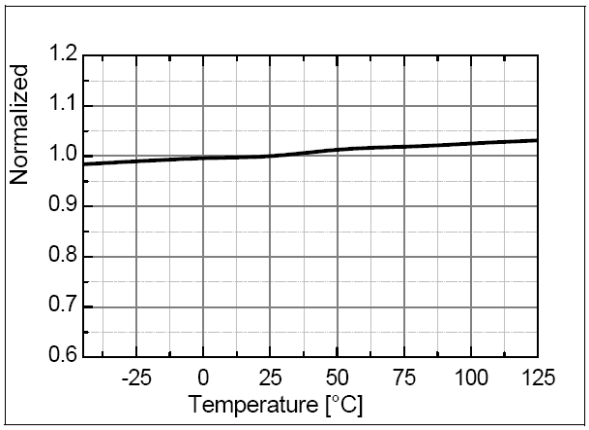


Figure 14. Input High Clamp Voltage (V_{CLAMPH}) vs. T_A

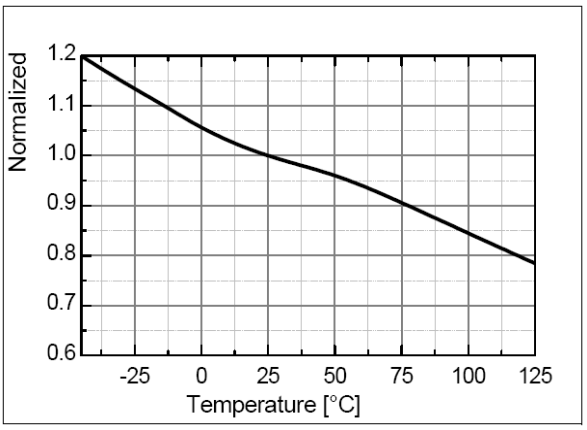


Figure 15. Input Low Clamp Voltage (V_{CLAMPL}) vs. T_A

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

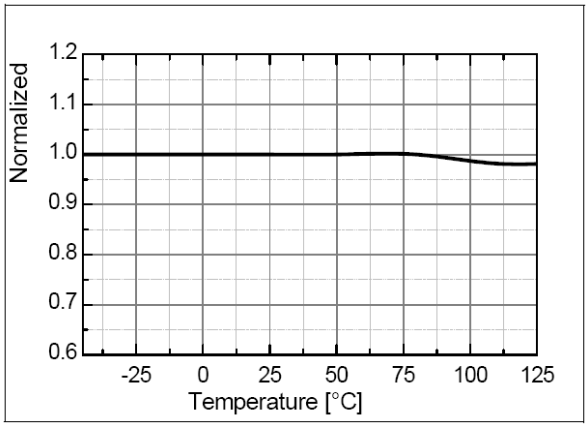


Figure 16. Output Voltage High (V_{OH}) vs. T_A

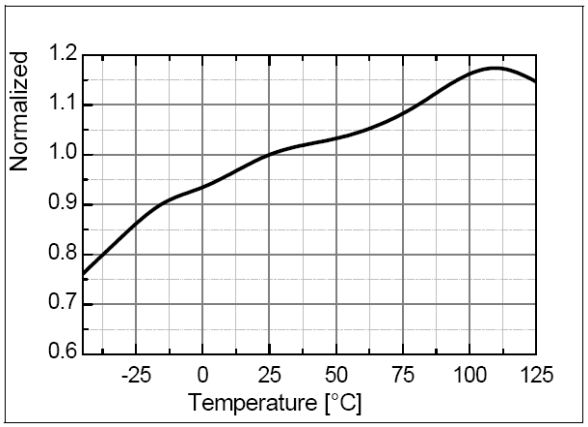


Figure 17. Output Voltage Low (V_{OL}) vs. T_A

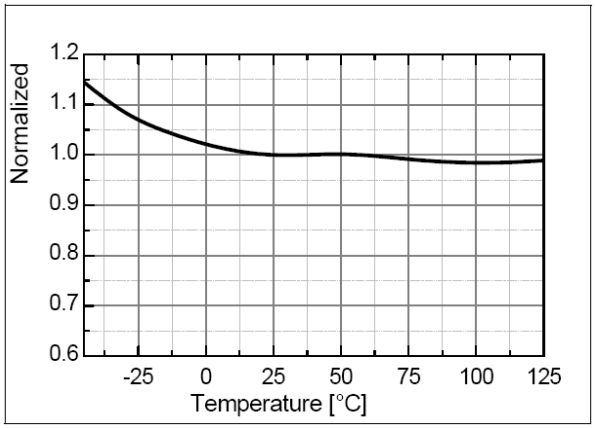


Figure 18. Restart Timer Delay (t_{RST}) vs. T_A

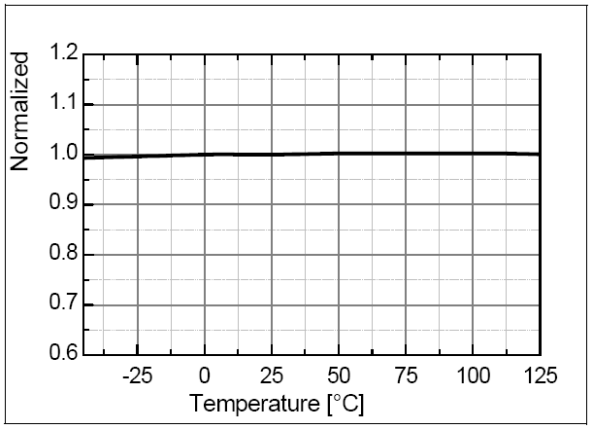


Figure 19. Output Ready Voltage (V_{RDY}) vs. T_A

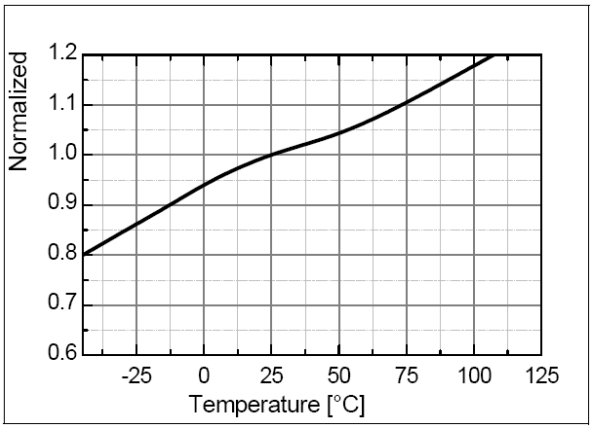


Figure 20. Output Saturation Voltage ($V_{RDY,SAT}$) vs. T_A

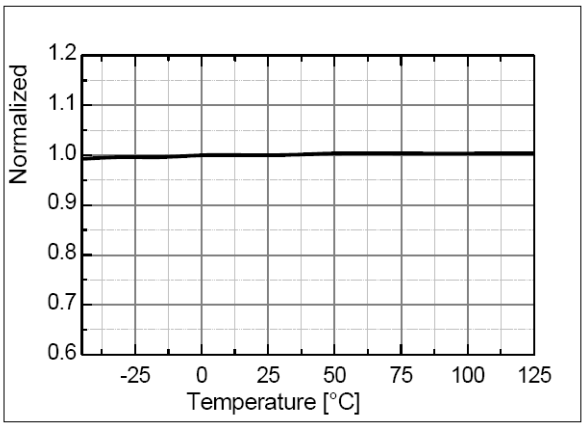


Figure 21. OVP Threshold Voltage (V_{OVP}) vs. T_A

APPLICATIONS INFORMATION

Startup

Normally, supply voltage (V_{CC}) of a PFC block is fed from the additional power supply, which can be called standby power. Without this standby power, auxiliary winding for zero current detection can be used as a supply source. Once the supply voltage of the PFC block exceeds 12 V, internal operation is enabled until he voltage drops to 8.5 V. If VCC exceeds V_Z, 20 mA current is sinking from V_{CC}.

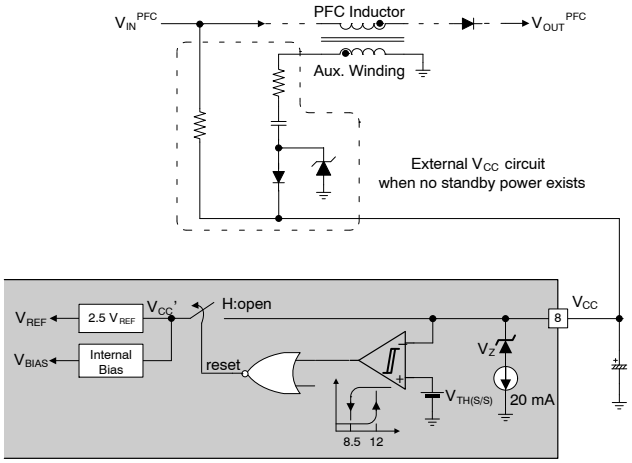


Figure 22. Startup Circuit

INV Block

Scaled–down voltage from the output is the input for the INV pin. Many functions are embedded based on the INV pin: transconductance amplifier, output OVP comparator, disable comparator, and output UVLO comparator.

For the output voltage control, a transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage–controlled current source) aids the implementation of the OV P and disable functions. The output current of the amplifier changes according to the voltage difference of the inverting and non–inverting input of the amplifier. To cancel down the line input voltage effect on power factor correction, the effective control response of the PFC block should be slower than the line frequency and this conflicts with the transient response of controller. Two–pole one–zero type compensation can meet both requirements.

The OVP comparator shuts down the output drive block when the voltage of the INV pin is higher than 2.675 V and there is 0. 175 V hysteresis. The disable comparator disables operation when the voltage of the inverting input is lower than 0.35 V and there is 100 mV hysteresis. An external small–signal MOSFET can be used to disable the IC, as show n in Figure 23. The IC operating current decreases to reduce pow er consumption if the IC is disabled. Figure 24 is the timing chart of the internal circuit near the INV pin when rated PFC output voltage is 390 V_{DC} and V_{CC} supply voltage is 15 V.

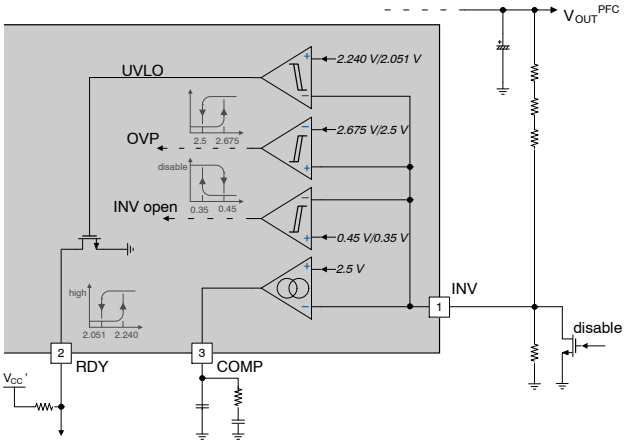


Figure 23. Circuit Around INV Pin

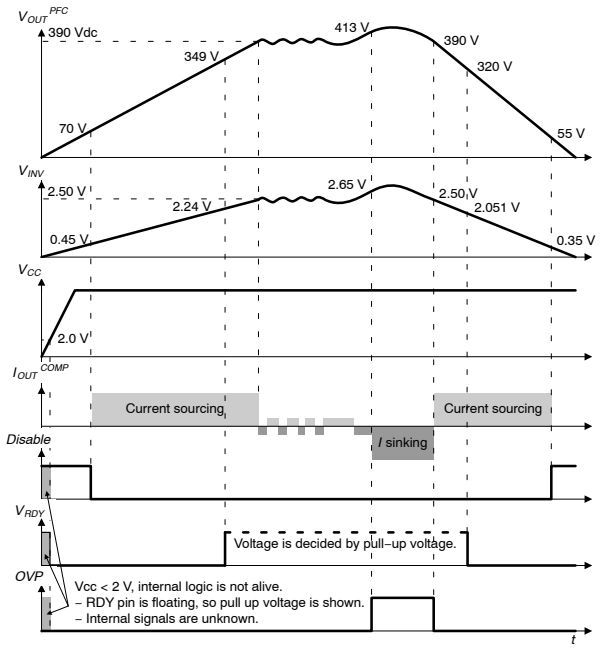


Figure 24. Timing Chart for INV Block

RDY Output

When the INV voltage is higher than 2.24 V, RDY output is triggered HIGH and lasts until the INV voltage is lower than 2.051 V. When input AC voltage is quite high, for example 240 V_{AC}, PFC output voltage is always higher than RDY threshold, regardless of boost converter operation. In this case, the INV voltage is already higher than 2.24 V before PFC V_{CC} touches V_{START}; however, RDY output is not triggered to HIGH until V_{CC} touches V_{START}. After boost converter operation stops, RDY is not pulled LOW because the INV voltage is higher than the RDY threshold. When V_{CC} of the PFC drops below 5 V, RDY is pulled LOW even though PFC output voltage is higher than threshold. The RDY pin output is open drain, so needs an external pull–up resistor to supply the proper power source. The RDY pin output remains floating until V_{CC} is higher than 2 V.

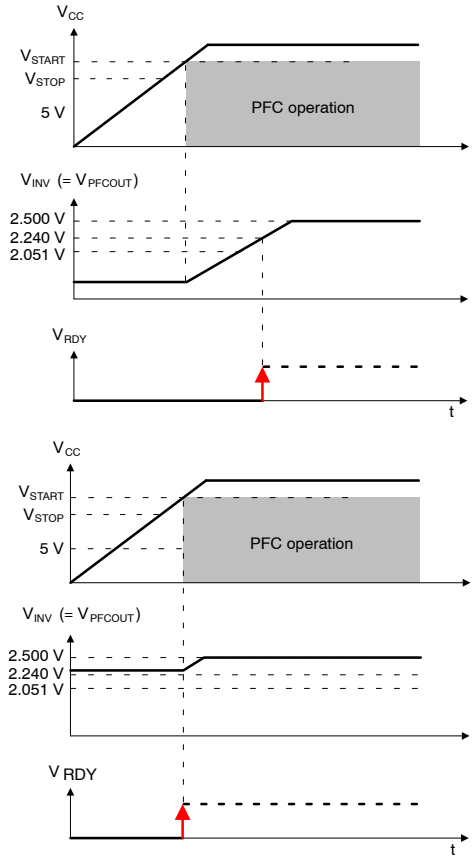


Figure 25. Two Cases of RDY Triggered HIGH

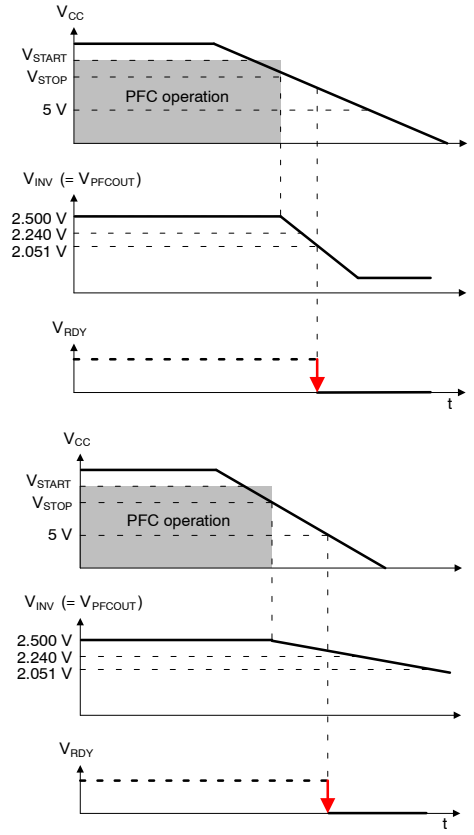


Figure 26. Two Cases of RDY Triggered LOW

Control Range Compensation

On time is controlled by the output voltage compensator with FAN7930C. Due to this when input voltage is high and load is light, control range becomes narrow compared to when input voltage is low. That control range decrease is inversely proportional to the double square of the input voltage (control range $\alpha \frac{1}{\text{input voltage}^2}$). Thus at high line, unwanted burst operation easily happens at light load and audible noise may be generated from the boost inductor or inductor at input filter. Different from the other converters, burst operation in PFC block is not needed because the PFC block itself is normally disabled during standby mode. To reduce unwanted burst operation at light load, an internal control range compensation function is implemented and shows no burst operation until 5% load at high line

Zero−Current Detection

Zero−current detection (ZCD) generates the turn−on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. When the power switch turns on, negative voltage is induced at the auxiliary winding due to the opposite winding direction *(see Equation 2)*. Positive voltage is induced *(see Equation 3)* when the power switch turns off.

$$\text{control range } \alpha \frac{1}{\text{input voltage}^2} \quad \text{(eq. 1)}$$

$$V_{AUX} = -\frac{T_{AUX}}{T_{IND}} \cdot V_{AC} \quad \text{(eq. 2)}$$

$$V_{AUX} = \frac{T_{AUX}}{T_{IND}} \cdot (V_{PFCOUT} - V_{AC}) \quad \text{(eq. 3)}$$

where:

V_{AUX} is the auxiliary winding voltage;
T_{IND} is boost inductor turns;
T_{IND} auxiliary winding turns;
V_{AC} is input voltage for PFC converter; and
V_{OUT_PFC} is output voltage from the PFC converter.

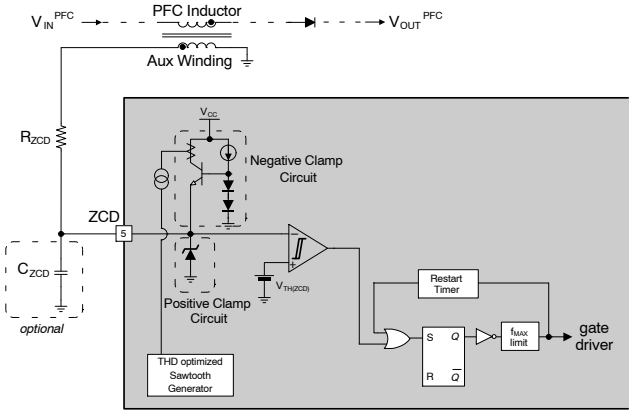


Figure 27. Circuit Near ZCD

Because auxiliary winding voltage can swing from negative to positive voltage, the internal block in ZCD pin has both positive and negative voltage clamping circuits. When the auxiliary voltage is negative, an internal circuit clamps the negative voltage at the ZCD pin around 0.65 V by sourcing current to the serial resistor between the ZCD pin and the auxiliary winding. When the auxiliary voltage is higher than 6.5 V current is sinked through a resistor from the auxiliary winding to the ZCD pin.

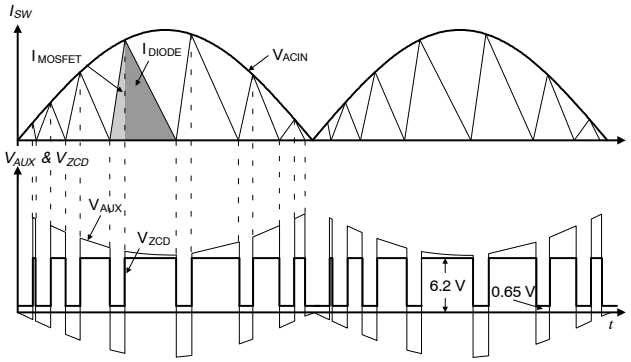


Figure 28. Auxiliary Voltage Depends on MOSFET Switching

The auxiliary winding voltage is used to check the boost inductor current zero instance. When boost inductor current becomes zero, there is a resonance between boost inductor and all capacitors at the MOSFET drain pin: including C_{OSS} of the MOSFET; an external capacitor at the D–S pin to reduce the voltage rising and falling slope of the MOSFET; a parasitic capacitor at inductor; and so on to improve performance. Resonated voltage is reflected to the auxiliary winding and can be used for detecting zero current of boost inductor and valley position of MOSFET voltage stress. For valley detection, a minor delay by the resistor and capacitor is needed. A capacitor increases the noise immunity at the ZCD pin. If ZCD voltage is higher than 1.5 V, an internal ZCD comparator output becomes HIGH and LOW when the ZCD goes below 1.4 V. At the falling edge of comparator output, internal logic turns on the MOSFET.

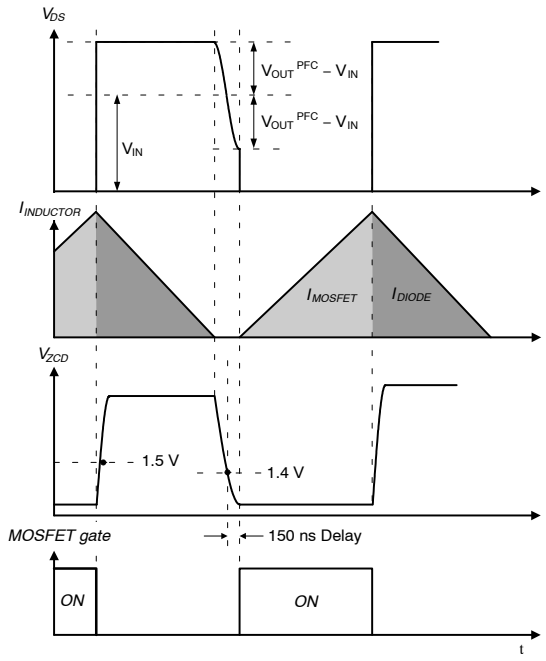


Figure 29. Auxiliary Voltage Threshold

When no ZCD signal is available, the PFC controller cannot turn on the MOSFET, so the controller checks every switching off time and forces MOSFET turn on when the off time is longer than 150 μs. This restart timer triggers MOSFET turn–on at startup and may be used at the input voltage zero–cross period.

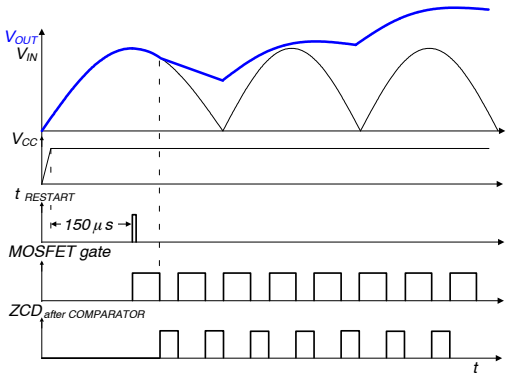


Figure 30. Restart Timer at Startup

Because the MOSFET turn−on depends on the ZCD input, switching frequency may increase to higher than several megahertz due to the mis−triggering or noise on the nearby ZCD pin. If the switching frequency is higher than needed for critical conduction mode (CRM), operation mode shifts to continuous conduction mode (CCM). In CCM, unlike CRM where the boost inductor current is reset to zero at the next switch on; inductor current builds up at every switching cycle and can be raised to very high current that exceeds the current rating of the power switch or diode. This can seriously damage the power switch. To avoid this, maximum switching frequency limitation is embedded. If ZCD signal is applied again within 3.3 μs after the previous rising edge of gate signal, this signal is ignored internally and FAN7930C waits for another ZCD signal. This slightly degrades the power factor performance at light load and high input voltage.

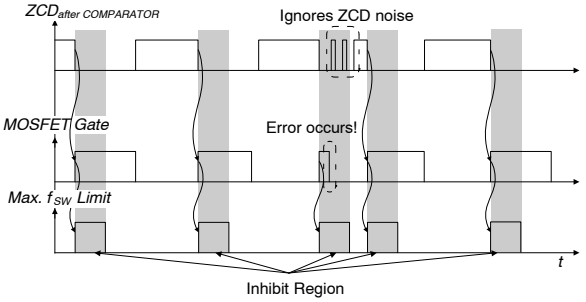


Figure 31. Maximum Switching Frequency Limit Operation

Control

The scaled output is compared with the internal reference voltage and sinking or sourcing current is generated from the COMP pin by the transconductance amplifier. The error amplifier output is compared with the internal saw tooth waveform to give proper turn−on time based on the controller.

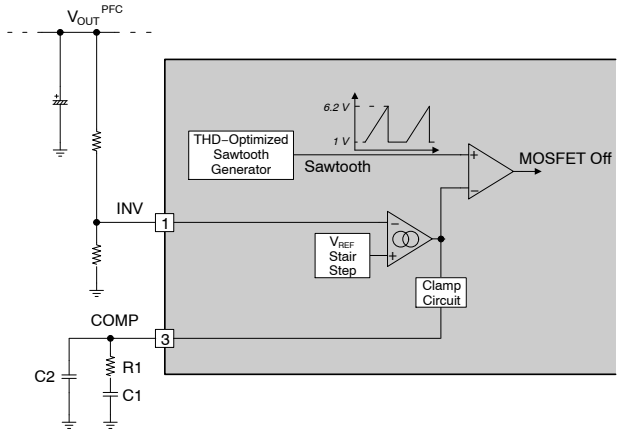


Figure 32. Control Circuit

Unlike a conventional voltage−mode PWM controller, FAN7930C turns on the MOSFET at the falling edge of ZCD signal. The "ON" instant is determined by the external signal and the turn−on time lasts until the error amplifier output (V_{COMP}) and saw tooth waveform meet. When load is heavy, output voltage decreases, scaled output decreases, COMP voltage increases to compensate low output, turn−on time lengthens to give more inductor turn−on time, and increased inductor current raises the output voltage. This is how a PFC negative feedback controller regulates output.

The maximum of V_{COMP} is limited to 6.5 V, which dictates the maximum turn−on time. Switching stops when V_{COMP} is lower than 1.0 V.

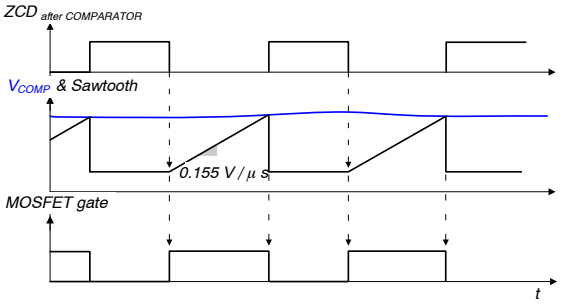


Figure 33. Turn−On Time Determination

The roles of PFC controller are regulating output voltage and input current shaping to increase power factor. Duty control based on the output voltage should be fast enough to compensate output voltage dip or overshoot. For the power factor, however, the control loop must not react to the fluctuating AC input voltage. These two requirements conflict; therefore, when designing a feedback loop, the feedback loop should be least ten times slower than AC line frequency. That slow response is made by C1 at the compensator. R1 makes gain boost around operation region and C2 attenuates gain at higher frequency. Boost gain by R1 helps raise the response time and improves phase margin.

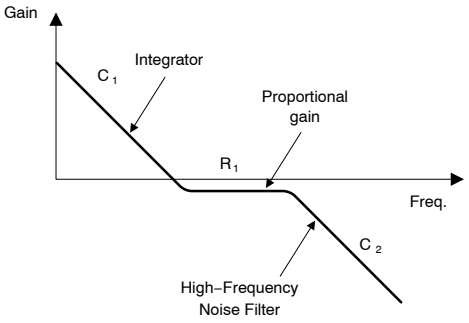


Figure 34. Compensators Gain Curve

For the transconductance error amplifier side, gain changes based on differential input. When the error is large, gain is large to suppress the output dip or peak quickly. When the error is small, low gain is used to improve power factor performance.

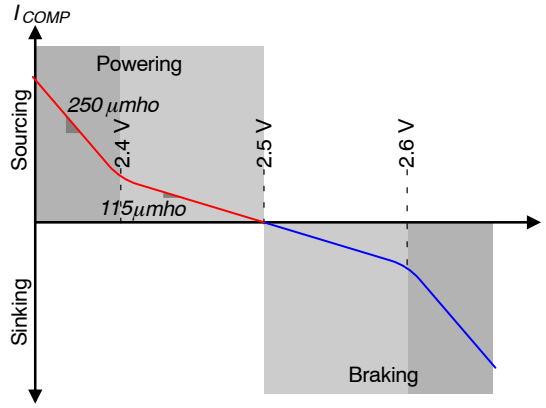


Figure 35. Gain Characteristic

Soft−Start

When V_{CC} reaches VSTART, the internal reference voltage is increased like a stair step for 5 ms. As a result, V_{COMP} is also raised gradually and MOSFET turn−on time increases smoothly. This reduces voltage and current stress on the power switch during startup.

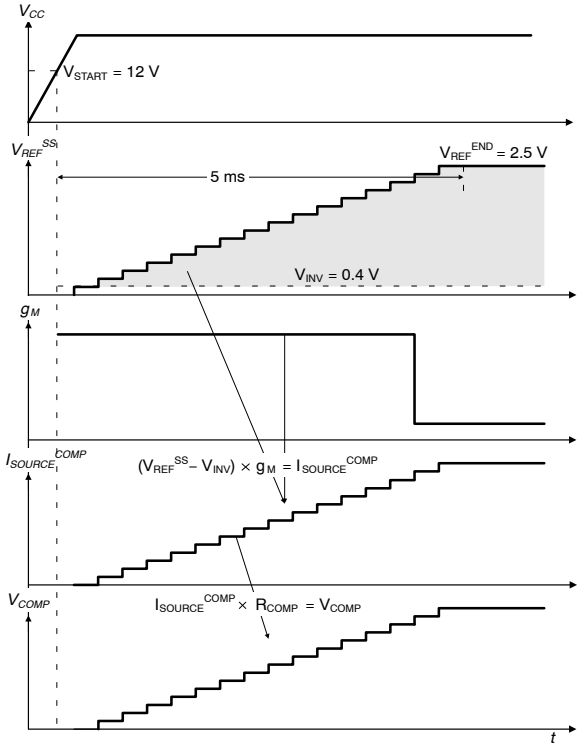


Figure 36. Soft−Start Sequence

Startup without Overshoot

Feedback control speed of PFC is quite slow. Due to the slow response, there is a gap between output voltage and feedback control. That is why over−voltage protection (OVP) is critical at the PFC controller and voltage dip caused by fast load changes from light to heavy is diminished by a bulk capacitor. OV P is triggered during startup phase.

Operation on and off by OV P at startup may cause audible noise and can increase voltage stress at startup, which is normally higher than in normal operation. This operation is improved when soft−start time is very long. However, too much startup time enlarges the output voltage building time at light load. FA N7930C has overshoot protection at startup. During startup, the feedback loop is controlled by an internal proportional gain controller and, when the output voltage reaches the rated value, it switches to an external compensator after a transition time of 30 ms. This internal proportional gain controller eliminates overshoot at startup and an external conventional compensator takes over successfully afterward.

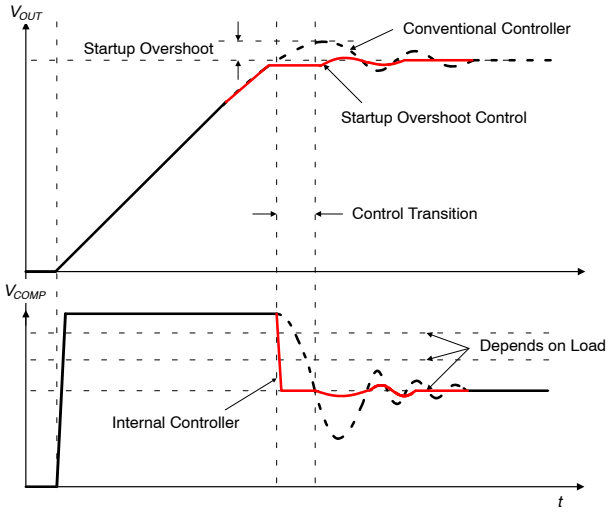


Figure 37. Startup without Overshoot

THD Optimization

Total Harmonic Distortion (THD) is the factor that dictates how closely input current shape matches sinusoidal form. The turn−on time of the PFC controller is almost constant over one AC line period due to the extremely low feedback control response. The turn−off time is determined by the current decrease slope of the boost inductor made by the input voltage and output voltage. Once inductor current becomes zero, resonance between C_{OSS} and the boost inductor makes oscillating waveforms at the drain pin and auxiliary winding. By checking the auxiliary winding voltage through the ZCD pin, the controller can check the zero current of boost inductor. At the same time, a minor delay is inserted to deter mine the valley position of drain voltage. The input and output voltage difference is at its maximum at the zero cross point of AC input voltage. The current decrease slope is steep near the zero cross region and more negative inductor current flows during a drain voltage valley detection time. Such a negative inductor current cancels down the positive current flows and input current becomes zero, called “zero−cross distortion” in PFC.

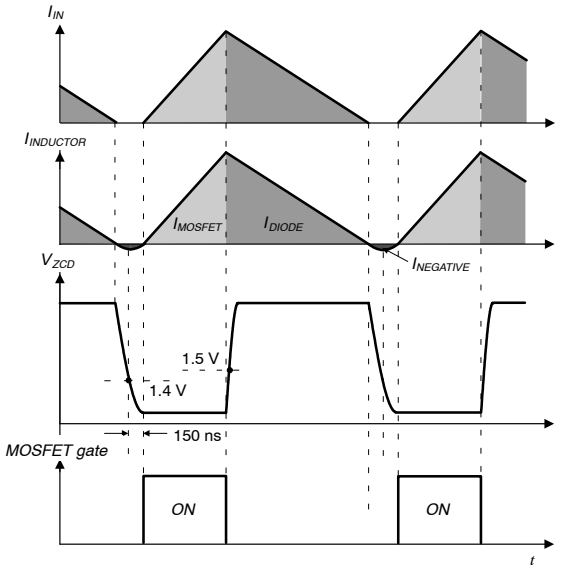


Figure 38. Input and Output Current Near Input Voltage Peak

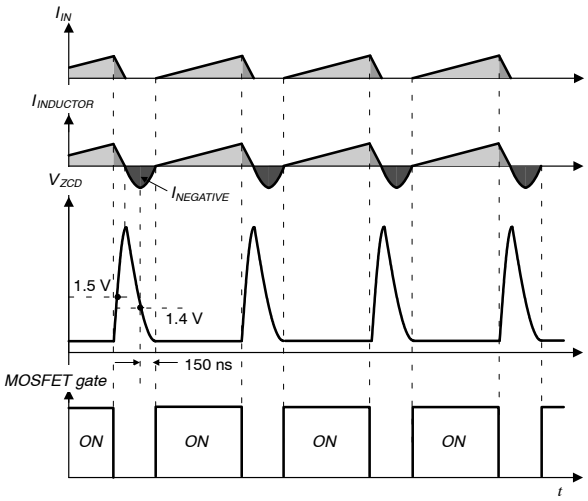


Figure 39. Input and Output Current Near Input Voltage Peak Zero Cross

To improve this, lengthened turn–on time near the zero cross region is a well–known technique, though the method may vary and may be proprietary. FA N7930C optimizes this by sourcing current through the ZCD pin. Auxiliary winding voltage becomes negative when the MOSFET turns on and is proportional to input voltage. The negative clamping circuit of ZCD outputs the current to maintain the ZCD voltage at a fixed value. The sourcing current from the ZCD is directly proportional to the input voltage. Some portion of this current is applied to the internal saw tooth generator, together with a fixed–current source. Theoretically, the fixed–current source and the capacitor at saw tooth generator determine the maximum turn–on time when no current is sourcing at ZCD clamp circuit and available turn–on time gets shorter proportional to the ZCD sourcing current.

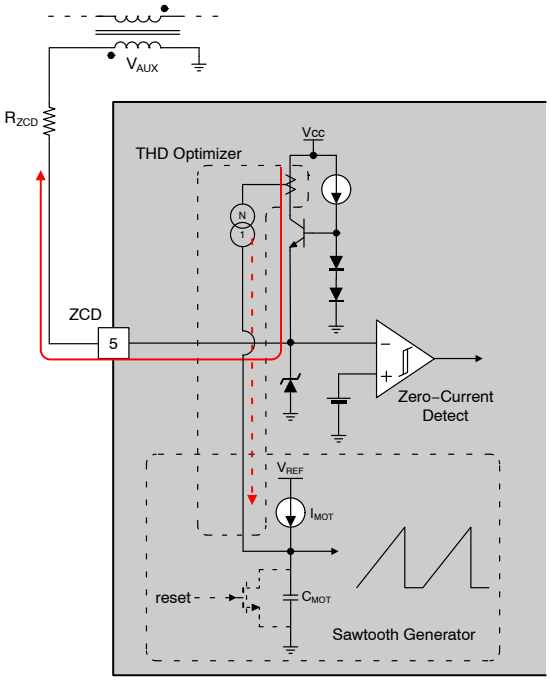


Figure 40. Circuit of THD Optimizer

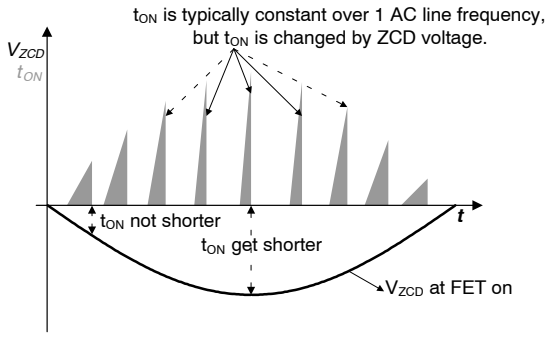


Figure 41. Effect of THD Optimizer

By THD optimizer, turn–on time over one AC line period is proportionally changed, depending on input voltage. Near zero cross, lengthened turn–on time improves THD performance.

V_{IN}–Absent Detection

To save power loss caused by input voltage sensing resistors and to optimize THD, the FA N7930C omits AC input voltage detection. Therefore, no information about AC input is available from the internal controller. In many cases, the V_{CC} of PFC controller is supplied by an independent power source, like standby power. In this scheme, some mismatch may exist. For example, when the electric power is suddenly interrupted during two or three AC line periods; V_{CC} is still live during that time, but output voltage drops because there is no input power source. Consequently, the control loop tries to compensate for the output voltage drop and V_{COMP} reaches its maximum. This lasts until AC input voltage is live again. When AC input voltage is live again,

high V_{COMP} allows high switching current and more stress is put on the MOSFET and diode. To protect against this, FAN7930C checks if the input AC voltage exists. If input does not exist, soft−start is reset and waits until AC input is live again. Soft−start manages the turn−on time for smooth operation when it detects AC input is applied again and applies less voltage and current stress on startup.

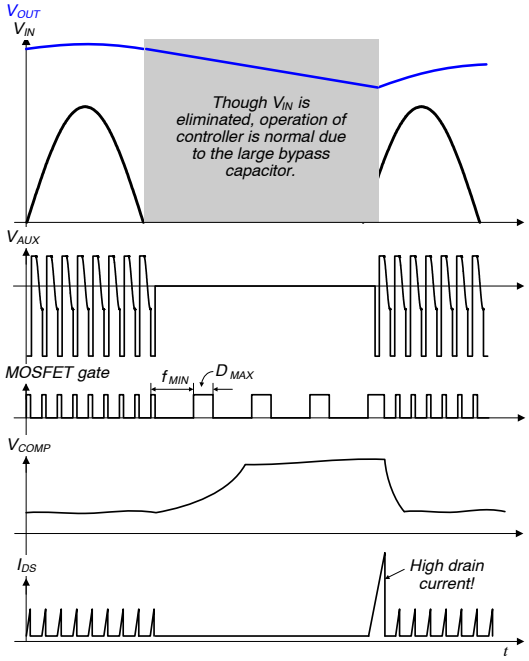


Figure 42. Without V_{IN}−Absent Circuit

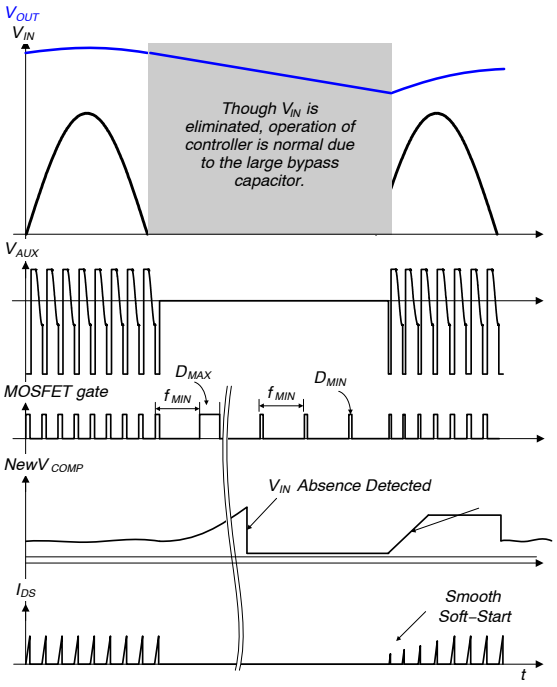


Figure 43. With V_{IN}−Absent Circuit

Current Sense

The MOSFET current is sensed using an external sensing resistor for over−current protection. If the CS pin voltage is higher than 0.8 V, the over−current protection comparator generates a protection signal. An internal RC filter of 40 kΩ and 8 pF is included to filter switching noise.

Gate Driver Output

FAN7930C contains a single totem−pole output stage designed for a direct drive of the power MOSFET. The drive output is capable of up to +500 / −800 mA peak current with a typical rise and fall time of 50 ns with 1 nF load. The output voltage is clamped to 13 V to protect the MOSFET gate even if the V_{CC} voltage is higher than 13 V.

PCB LAYOUT GUIDE

PFC block normally handles high switching current and the voltage low energy signal path can be affected by the high energy path. Cautious PCB layout is mandatory for stable operation.

1. The gate drive path should be as short as possible. The closed−loop that starts from the gate driver, MOSFET gate, and MOSFET source to ground of PFC controller should be as close as possible. This is also crossing point between power ground and signal ground. Power ground path from the bridge diode to the output bulk capacitor should be short and wide. The sharing position between power ground and signal ground should be only at one position to avoid ground loop noise. Signal path of the PFC controller should be short and wide for external components to contact.
2. The PFC output voltage sensing resistor is normally high to reduce current consumption. This path can be affected by external noise. To reduce noise potential at the INV pin, a shorter path for output sensing is recommended. If a shorter path is not possible, place some dividing resistors between PFC output and the INV pin — closer to the INV pin is better. Relative high voltage close to the INV pin can be helpful.
3. The ZCD path is recommended close to auxiliary winding from boost inductor and to the ZCD pin. If that is difficult, place a small capacitor (below 50 pF) to reduce noise.
4. The switching current sense path should not share with another path to avoid interference. Some additional components may be needed to reduce the noise level applied to the CS pin.
5. A stabilizing capacitor for V_{CC} is recommended as close as possible to the V_{CC} and ground pins. If it is difficult, place the SMD capacitor as close to the corresponding pins as possible.

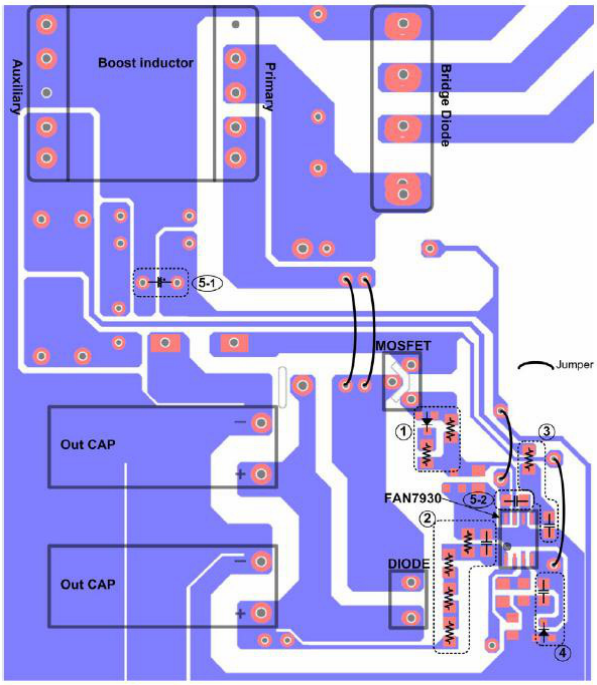


Figure 44. Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

TYPICAL APPLICATION CIRCUIT

Application	Device	Input Voltage Range	Rated Output Power	Output Voltage (Maximum Current)
LCD TV Power Supply	FAN7930C	90 – 265 V_{AC}	195 W	390 V (0.5 A)

Features

- Average efficiency of 25%, 50%, 75%, and 100% load conditions is higher than 95% at universal input.
- Power factor at rated load is higher than 0.98 at universal input.
- Total Harmonic Distortion (THD) at rated load is lower than 15% at universal input.

Key Design Notes

- When auxiliary V_{CC} supply is not available, V_{CC} power can be supplied through Zero Current Detect (ZCD) winding. The power consumption of R103 is quite high, so its power rating needs checking.
- Because the input bias current of INV pin is almost zero, output voltage sensing resistors (R112~R115) should be as high as possible. However, too−high resistance makes the node susceptible to noise. Resistor values need to strike a balance between power consumption and noise immunity.
- Quick charge diode (D106) can be eliminated if output diode inrush current capability is sufficient. Even without D106, system operation is normal due to the controller's highly reliable protection features.

Schematic

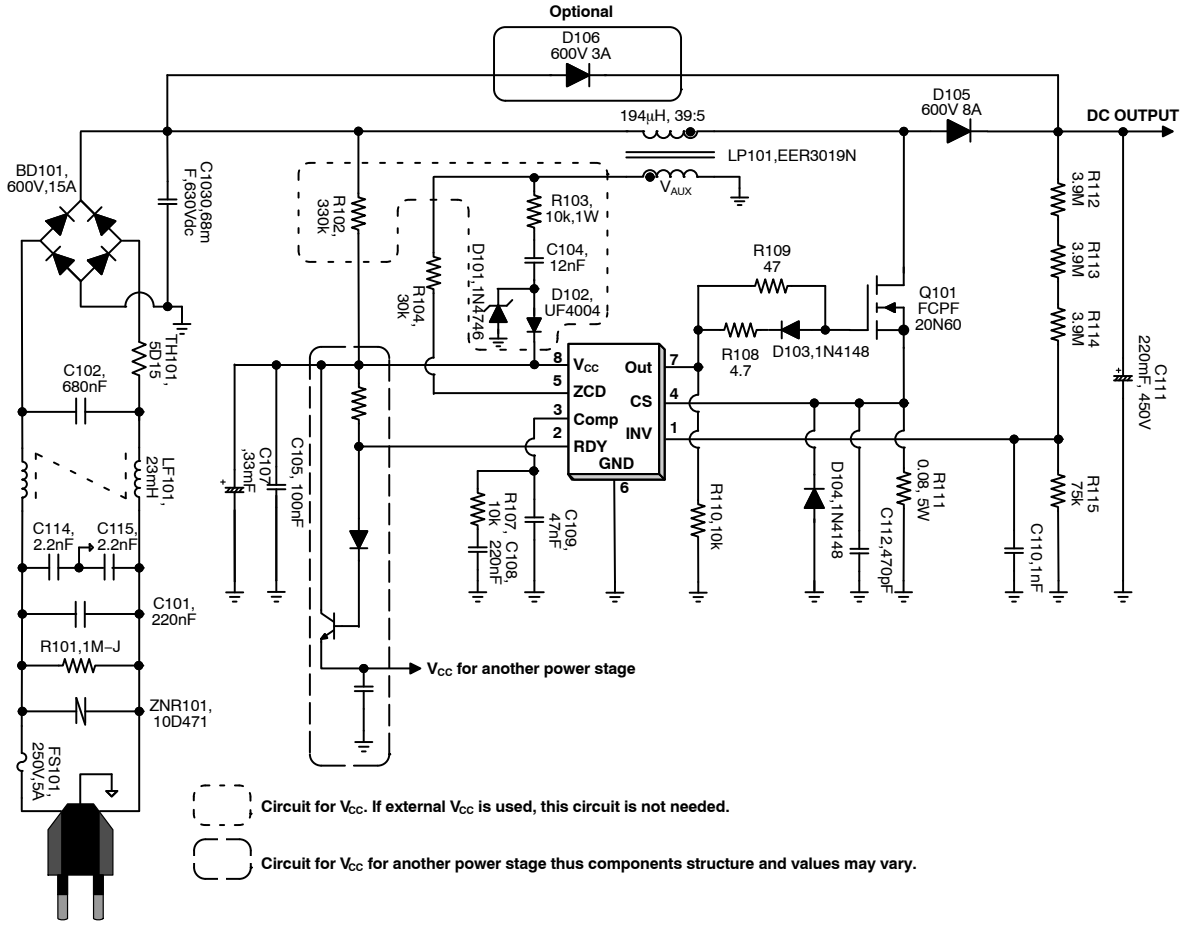


Figure 45. Demonstration Circuit

Transformer

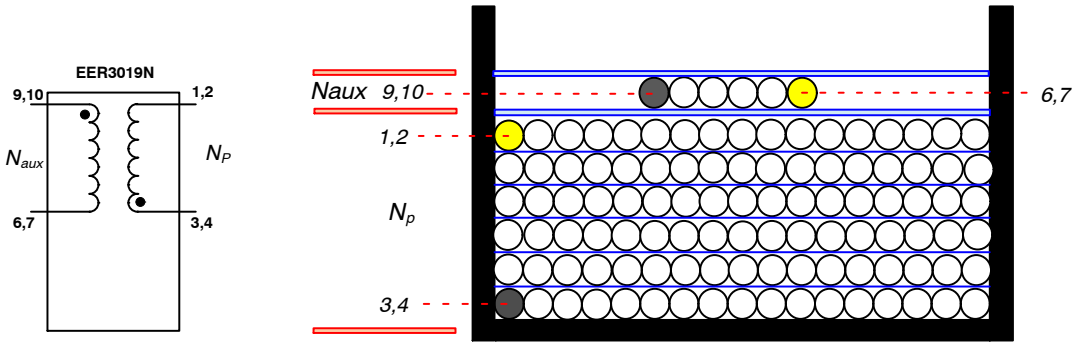


Figure 46. Transformer Schematic Diagram

Winding Specification

WINDING SPECIFICATION

Position	No	Pin (S → F)	Wire	Turns	Winding Method
Bottom	Np	3, 4 → 1, 2	0.1φ x 50	39	Solenoid Winding
	Insulation: Polyester Tape t = 0.05 mm, 3 Layers				
Top	NAUX	9, 10 → 6, 7	0.3φ	5	Solenoid Winding
	Insulation: Polyester Tape t = 0.05 mm, 4 Layers				

Electrical Characteristics

ELECTRICAL CHARACTERISTICS

	Pin	Specification	Remark
Inductance	3, 4 → 1, 2	194 μH ±5%	100 kHz, 1 V

Core & Bobbin

Core: EER3019, Samhwa (PL−7) (Ae = 137.0 mm^2)
Bobbin: EER3019

BILL OF MATERIALS

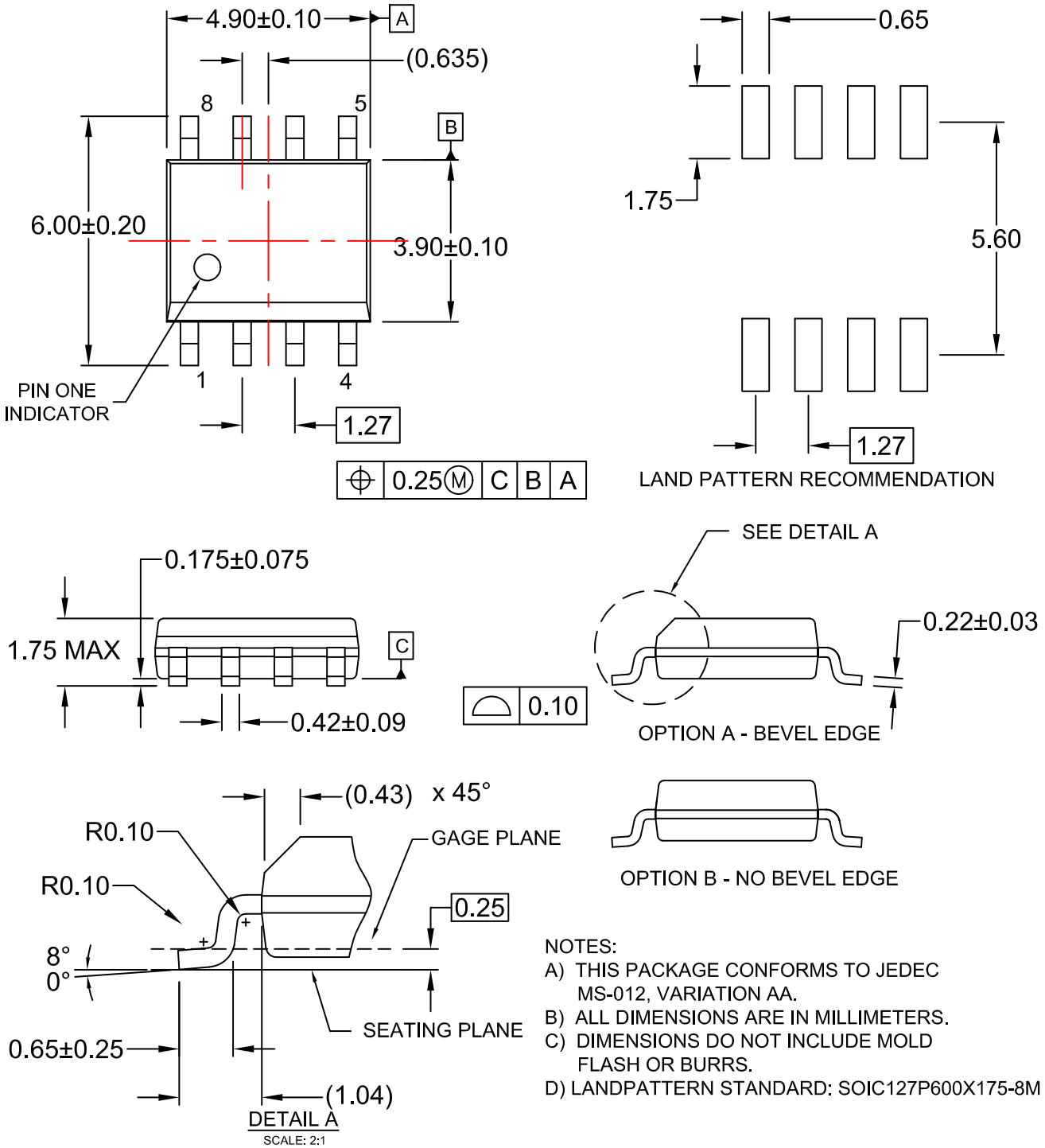
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Part #	Value	Note	Part #	Value	Note
Resistor			*Switch*		
R101	1 MΩ	1 W	Q101	FCPF20N60	20 A, 600 V, SUPERFET®
R102	330 kΩ	1/2 W	*Diode*		
R103	10 kΩ	1 W	D101	1N4746	1 W, 18 V, Zener Diode
R104	30 kΩ	1/4 W	D102	UF4004	1 A, 400 V Glass Passivated High−Efficiency Rectifier
R107	10 kΩ	1/4 W	D103	1N4148	1 A, 100 V Small−Signal Diode
R108	4.7 kΩ	1/4 W	D104	1N4148	1 A, 100 V Small−Signal Diode
R109	47 kΩ	1/4 W	D105		8 A, 600 V, General−Purpose Rectifier
R110	10 kΩ	1/4 W	D106		3 A, 600 V, General−Purpose Rectifier
R111	0.80 kΩ	5 W			
R112, 113, 114	3.9 kΩ	1/4 W	IC101	FAN7930C	CRM PFC Controller
R115	75 kΩ	1/4 W			
Capacitor			*Fuse*		
C101	220 nF / 275 V_{AC}	Box Capacitor	FS101	5 A / 250 V	
C102	680 nF / 275 V_{AC}	Box Capacitor	*NTC*		
C103	0.68 μF / 630 V	Box Capacitor	TH101	5D−15	
C104	12 nF / 50 V	Ceramic Capacitor	*Bridge Diode*		
C105	100 nF / 50 V	SMD (1206)	BD101		15 A, 600 V
C107	33 μF / 50 V	Electrolytic Capacitor	*Line Filter*		
C108	220 nF / 50 V	Ceramic Capacitor	LF101	23 mH	
C109	47 nF / 50 V	Ceramic Capacitor	*Transformer*		
C110	1 nF / 50 V	Ceramic Capacitor	T1	EER3019	Ae = 137.0 mm^2
C112	47 nF / 50 V	Ceramic Capacitor	*ZNR*		
C111	220 μF / 450 V	Electrolytic Capacitor	ZNR101	10D471	
C114	2.2 nF / 450 V	Box Capacitor			
C115	2.2 nF / 450 V	Box Capacitor			

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SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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