LM75A

Digital temperature sensor and thermal watchdog

Rev. 04 — 10 July 2007 Product data sheet

1. General description

The LM75A is a temperature-to-digital converter using an on-chip band gap temperature sensor and Sigma-delta A-to-D conversion technique. The device is also a thermal detector providing an overtemperature detection output. The LM75A contains a number of data registers: Configuration register (Conf) to store the device settings such as device operation mode, OS operation mode, OS polarity and OS fault queue as described in Section 7 “Functional description”; temperature register (Temp) to store the digital temp reading, and set-point registers (Tos and Thyst) to store programmable overtemperature shutdown and hysteresis limits, that can be communicated by a controller via the 2-wire serial I^2C-bus interface. The device also includes an open-drain output (OS) which becomes active when the temperature exceeds the programmed limits. There are three selectable logic address pins so that eight devices can be connected on the same bus without address conflict.

The LM75A can be configured for different operation conditions. It can be set in normal mode to periodically monitor the ambient temperature, or in shutdown mode to minimize power consumption. The OS output operates in either of two selectable modes: OS comparator mode or OS interrupt mode. Its active state can be selected as either HIGH or LOW. The fault queue that defines the number of consecutive faults in order to activate the OS output is programmable as well as the set-point limits.

The temperature register always stores an 11-bit 2's complement data giving a temperature resolution of 0.125 °C. This high temperature resolution is particularly useful in applications of measuring precisely the thermal drift or runaway.

The device is powered-up in normal operation mode with the OS in comparator mode, temperature threshold of 80 °C and hysteresis of 75 °C, so that it can be used as a stand-alone thermostat with those pre-defined temperature set points.

2. Features

- Pin-for-pin replacement for industry standard LM75 and offers improved temperature resolution of 0.125 °C and specification of a single part over power supply range from 2.8 V to 5.5 V
- Small 8-pin package types: SO8 and TSSOP8
- I^2C-bus interface with up to 8 devices on the same bus
- Power supply range from 2.8 V to 5.5 V
- Temperatures range from −55 °C to +125 °C
- 11-bit ADC that offers a temperature resolution of 0.125 °C

founded by Philips

- Temperature accuracy of:
  - ±2 °C from –25 °C to +100 °C
  - ±3 °C from –55 °C to +125 °C
- Programmable temperature threshold and hysteresis set points
- Supply current of 3.5 μA in shutdown mode for power conservation
- Stand-alone operation as thermostat at power-up
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

3. Applications

- System thermal management
- Personal computers
- Electronics equipment
- Industrial controllers

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LM75AD	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
LM75ADP	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
LM75AD	LM75A	T_{amb} = –55 °C to +125 °C
LM75ADP	L75A	T_{amb} = –55 °C to +125 °C

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5. Block diagram

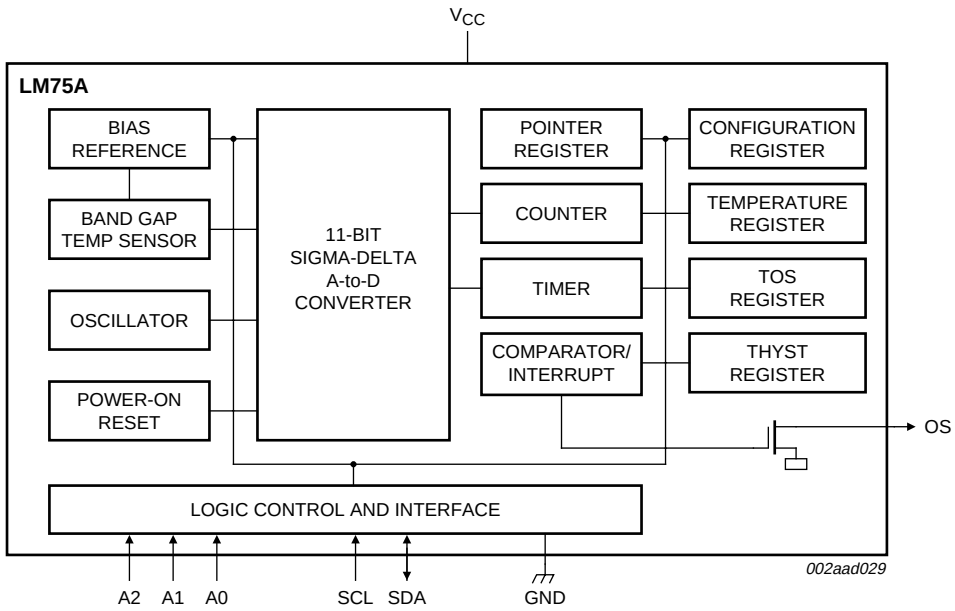


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

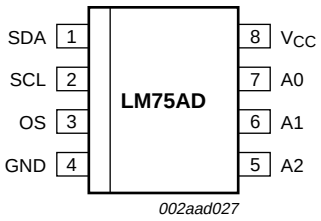


Fig 2. Pin configuration for SO8

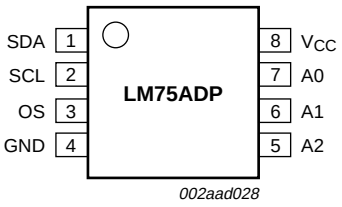


Fig 3. Pin configuration for TSSOP8

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SDA	1	Digital I/O. I^2C-bus serial bidirectional data line; open-drain.
SCL	2	Digital input. I^2C-bus serial clock input.
OS	3	Overtemp Shutdown output; open-drain.
GND	4	Ground. To be connected to the system ground.
A2	5	Digital input. User-defined address bit 2.

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Table 3. Pin description *...continued*

Symbol	Pin	Description
A1	6	Digital input. User-defined address bit 1.
A0	7	Digital input. User-defined address bit 0.
V_{CC}	8	Power supply.

7. Functional description

7.1 General operation

The LM75A uses the on-chip band gap sensor to measure the device temperature with the resolution of 0.125 °C and stores the 11-bit 2's complement digital data, resulted from 11-bit A-to-D conversion, into the device Temp register. This Temp register can be read at any time by a controller on the I^2C-bus. Reading temperature data does not affect the conversion in progress during the read operation.

The device can be set to operate in either mode: normal or shutdown. In normal operation mode, the temp-to-digital conversion is executed every 100 ms and the Temp register is updated at the end of each conversion. In shutdown mode, the device becomes idle, data conversion is disabled and the Temp register holds the latest result; however, the device I^2C-bus interface is still active and register write/read operation can be performed. The device operation mode is controllable by programming bit B0 of the configuration register. The temperature conversion is initiated when the device is powered-up or put back into normal mode from shutdown.

In addition, at the end of each conversion in normal mode, the temperature data (or Temp) in the Temp register is automatically compared with the overtemperature shutdown threshold data (or Tos) stored in the Tos register, and the hysteresis data (or Thyst) stored in the Thyst register, in order to set the state of the device OS output accordingly. The device Tos and Thyst registers are write/read capable, and both operate with 9-bit 2's complement digital data. To match with this 9-bit operation, the Temp register uses only the 9 MSB bits of its 11-bit data for the comparison.

The way that the OS output responds to the comparison operation depends upon the OS operation mode selected by configuration bit B1, and the user-defined fault queue defined by configuration bits B3 and B4.

In OS comparator mode, the OS output behaves like a thermostat. It becomes active when the Temp exceeds the T_{os}, and is reset when the Temp drops below the T_{hyst}. Reading the device registers or putting the device into shutdown does not change the state of the OS output. The OS output in this case can be used to control cooling fans or thermal switches.

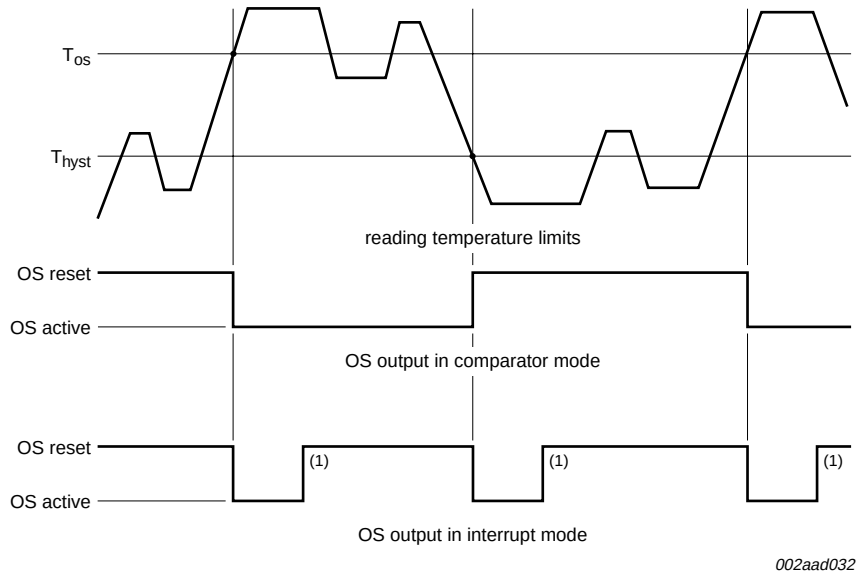
In OS interrupt mode, the OS output is used for thermal interruption. When the device is powered-up, the OS output is first activated only when the Temp exceeds the T_{os}; then it remains active indefinitely until being reset by a read of any register. Once the OS output has been activated by crossing T_{os} and then reset, it can be activated again only when the Temp drops below the T_{hyst}; then again, it remains active indefinitely until being reset by a read of any register. The OS interrupt operation would be continued in this sequence: T_{os} trip, Reset, T_{hyst} trip, Reset, T_{os} trip, Reset, T_{hyst} trip, Reset, etc.

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In both cases, comparator mode and interrupt mode, the OS output is activated only if a number of consecutive faults, defined by the device fault queue, has been met. The fault queue is programmable and stored in the two bits, B3 and B4, of the Configuration register. Also, the OS output active state is selectable as HIGH or LOW by setting accordingly the configuration register bit B2.

At power-up, the device is put into normal operation mode, the T_{os} is set to 80 °C, the T_{hyst} is set to 75 °C, the OS active state is selected LOW and the fault queue is equal to 1. The temp reading data is not available until the first conversion is completed in about 100 ms.

The OS response to the temperature is illustrated in Figure 4.



(1) OS is reset by either reading register. It is assumed that the fault queue is met at each T_{os} and T_{hyst} crossing point.

Fig 4. OS response to temperature

7.2 I²C-bus serial interface

The LM75A can be connected to a compatible 2-wire serial interface I²C-bus as a slave device under the control of a controller or master device, using two device terminals, SCL and SDA. The controller must provide the SCL clock signal and write/read data to/from the device through the SDA terminal. Notice that if the I²C-bus common pull-up resistors have not been installed as required for I²C-bus, then an external pull-up resistor, about 10 kΩ, is needed for each of these two terminals. The bus communication protocols are described in Section 7.10.

7.3 Slave address

The LM75A slave address on the I²C-bus is partially defined by the logic applied to the device address pins A2, A1 and A0. Each of them is typically connected either to GND for logic 0, or to V_{CC} for logic 1. These pins represent the three LSB bits of the device 7-bit address. The other four MSB bits of the address data are preset to '1001' by hard wiring inside the LM75A. Table 4 shows the device's complete address and indicates that up to

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8 devices can be connected to the same bus without address conflict. Because the input pins, SCL, SDA and A2 to A0, are not internally biased, it is important that they should not be left floating in any application.

Table 4. Address table

1 = HIGH; 0 = LOW.

MSB						LSB
1	0	0	1	A2	A1	A0

7.4 Register list

The LM75A contains four data registers beside the pointer register as listed in Table 5. The pointer value, read/write capability and default content at power-up of the registers are also shown in Table 5.

Table 5. Register table

Register name	Pointer value	R/W	POR state	Description
Conf	01h	R/W	00h	Configuration register: contains a single 8-bit data byte; to set the device operating condition; default = 0.
Temp	00h	read only	n/a	Temperature register: contains two 8-bit data bytes; to store the measured Temp data.
Tos	03h	R/W	5000h	Overtemperature shutdown threshold register: contains two 8-bit data bytes; to store the overtemperature shutdown T_{os} limit; default = 80 °C.
Thyst	02h	R/W	4B00h	Hysteresis register: contains two 8-bit data bytes; to store the hysteresis T_{hyst} limit; default = 75 °C.

7.4.1 Pointer register

The Pointer register contains an 8-bit data byte, of which the two LSB bits represent the pointer value of the other four registers, and the other 6 MSB bits are equal to 0, as shown in Table 6 and Table 7. The Pointer register is not accessible to the user, but is used to select the data register for write/read operation by including the pointer data byte in the bus command.

Table 6. Pointer register

B7	B6	B5	B4	B3	B2	B[1:0]
0	0	0	0	0	0	pointer value

Table 7. Pointer value

B1	B0	Selected register
0	0	Temperature register (Temp)
0	1	Configuration register (Conf)
1	0	Hysteresis register (Thyst)
1	1	Overtemperature shutdown register (Tos)

Because the Pointer value is latched into the Pointer register when the bus command (which includes the pointer byte) is executed, a read from the LM75A may or may not include the pointer byte in the statement. To read again a register that has been recently read and the pointer has been preset, the pointer byte does not have to be included. To

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read a register that is different from the one that has been recently read, the pointer byte must be included. However, a write to the LM75A must always include the pointer byte in the statement. The bus communication protocols are described in Section 7.10.

At power-up, the Pointer value is equal to 0 and the Temp register is selected; users can then read the Temp data without specifying the pointer byte.

7.4.2 Configuration register

The Configuration register (Conf) is a write/read register and contains an 8-bit non-complement data byte that is used to configure the device for different operation conditions. Table 8 shows the bit assignments of this register.

Table 8. Conf register

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
B[7:5]	reserved	R/W	000*	reserved for manufacturer's use; should be kept as zeroes for normal operation
B[4:3]	OS_F_QUE[1:0]	R/W		OS fault queue programming
			00*	queue value = 1
			01	queue value = 2
			10	queue value = 4
			11	queue value = 6
B2	OS_POL	R/W		OS polarity selection
			0*	OS active LOW
			1	OS active HIGH
B1	OS_COMP_INT	R/W		OS operation mode selection
			0*	OS comparator
			1	OS interrupt
B0	SHUTDOWN	R/W		device operation mode selection
			0*	normal
			1	shutdown

7.4.3 Temperature register

The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 9 shows the bit arrangement of the Temp data in the data bytes.

Table 9. Temp register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X

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When reading register Temp, all 16 bits of the two data bytes (MSByte and LSByte) are provided to the bus and must be all collected by the controller to complete the bus operation. However, only the 11 most significant bits should be used, and the 5 least significant bits of the LSByte are zero and should be ignored. One of the ways to calculate the Temp value in °C from the 11-bit Temp data is:

1. If the Temp data MSByte bit D10 = 0, then the temperature is positive and Temp value (°C) = +(Temp data) × 0.125 °C.
2. If the Temp data MSByte bit D10 = 1, then the temperature is negative and Temp value (°C) = –(2's complement of Temp data) × 0.125 °C.

Examples of the Temp data and value are shown in Table 10.

Table 10. Temp register value

11-bit binary (2's complement)	Hexadecimal value	Decimal value	Value
011 1111 1000	3F8	1016	+127.000 °C
011 1111 0111	3F7	1015	+126.875 °C
011 1111 0001	3F1	1009	+126.125 °C
011 1110 1000	3E8	1000	+125.000 °C
000 1100 1000	0C8	200	+25.000 °C
000 0000 0001	001	1	+0.125 °C
000 0000 0000	000	0	0.000 °C
111 1111 1111	7FF	–1	–0.125 °C
111 0011 1000	738	–200	–25.000 °C
110 0100 1001	649	–439	–54.875 °C
110 0100 1000	648	–440	–55.000 °C

Obviously, for 9-bit Temp data application in replacing the industry standard LM75, just use only 9 MSB bits of the two bytes and disregard 7 LSB of the LSByte. The 9-bit Temp data with 0.5 °C resolution of the LM75A is defined exactly in the same way as for the standard LM75 and it is here similar to the Tos and Thyst registers.

7.4.4 Overtemperature shutdown threshold (Tos) and hysteresis (Thyst) registers

These two registers, are write/read registers, and also called set-point registers. They are used to store the user-defined temperature limits, called overtemperature shutdown threshold (Tos) and hysteresis temperature (Thyst), for the device watchdog operation. At the end of each conversion the Temp data will be compared with the data stored in these two registers in order to set the state of the device OS output; see Section 7.1.

Each of the set-point registers contains two 8-bit data bytes consisting of one MSByte and one LSByte the same as register Temp. However, only 9 bits of the two bytes are used to store the set-point data in 2's complement format with the resolution of 0.5 °C. Table 11 and Table 12 show the bit arrangement of the Tos data and Thyst data in the data bytes.

Notice that because only 9-bit data are used in the set-point registers, the device uses only the 9 MSB of the Temp data for data comparison.

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Table 11. Tos register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X

Table 12. Thyst register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X

When a set-point register is read, all 16 bits are provided to the bus and must be collected by the controller to complete the bus operation. However, only the 9 most significant bits should be used and the 7 LSB of the LSByte are equal to zero and should be ignored.

Table 13 shows examples of the limit data and value.

Table 13. Tos and Thyst limit data and value

11-bit binary (2's complement)	Hexadecimal value	Decimal value	Value
0 1111 1010	0FA	250	+125.0 °C
0 0011 0010	032	50	+25.0 °C
0 0000 0001	001	1	+0.5 °C
0 0000 0000	000	0	0.0 °C
1 1111 1111	1FF	–1	–0.5 °C
1 1100 1110	1CE	–50	–25.0 °C
1 1001 0010	192	–110	–55.0 °C

7.5 OS output and polarity

The OS output is an open-drain output and its state represents results of the device watchdog operation as described in Section 7.1. In order to observe this output state, an external pull-up resistor is needed. The resistor should be as large as possible, up to 200 kΩ, to minimize the Temp reading error due to internal heating by the high OS sinking current.

The OS output active state can be selected as HIGH or LOW by programming bit B2 (OS_POL) of register Conf: setting bit OS_POL to logic 1 selects OS active HIGH and setting bit B2 to logic 0 sets OS active LOW. At power-up, bit OS_POL is equal to logic 0 and the OS active state is LOW.

7.6 OS comparator and interrupt modes

As described in Section 7.1, the device OS output responds to the result of the comparison between register Temp data and the programmed limits, in registers Tos and Thyst, in different ways depending on the selected OS mode: OS comparator or OS interrupt. The OS mode is selected by programming bit B1 (OS_COMP_INT) of register Conf: setting bit OS_COMP_INT to logic 1 selects the OS interrupt mode, and setting to logic 0 selects the OS comparator mode. At power-up, bit OS_COMP_INT is equal to logic 0 and the OS comparator is selected.

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The main difference between the two modes is that in OS comparator mode, the OS output becomes active when Temp has exceeded T_{os} and reset when Temp has dropped below T_{hyst}, reading a register or putting the device into shutdown mode does not change the state of the OS output; while in OS interrupt mode, once it has been activated either by exceeding T_{os} or dropping below T_{hyst}, the OS output will remain active indefinitely until reading a register, then the OS output is reset.

Temperature limits T_{os} and T_{hyst} must be selected so that $T_{os} > T_{hyst}$. Otherwise, the OS output state will be undefined.

7.7 OS fault queue

Fault queue is defined as the number of faults that must occur consecutively to activate the OS output. It is provided to avoid false tripping due to noise. Because faults are determined at the end of data conversions, fault queue is also defined as the number of consecutive conversions returning a temperature trip. The value of fault queue is selectable by programming the two bits B4 and B3 (OS_F_QUE[1:0]) in register Conf. Notice that the programmed data and the fault queue value are not the same. Table 14 shows the one-to-one relationship between them. At power-up, fault queue data = 0 and fault queue value = 1.

Table 14. Fault queue table

Fault queue data		Fault queue value
OS_F_QUE[1]	**OS_F_QUE[0]**	**Decimal**
0	0	1
0	1	2
1	0	4
1	1	6

7.8 Shutdown mode

The device operation mode is selected by programming bit B0 (SHUTDOWN) of register Conf. Setting bit SHUTDOWN to logic 1 will put the device into shutdown mode. Resetting bit SHUTDOWN to logic 0 will return the device to normal mode.

In shutdown mode, the device draws a small current of approximately 3.5 μA and the power dissipation is minimized; the temperature conversion stops, but the I^2C-bus interface remains active and register write/read operation can be performed. The OS output remains unchanged.

7.9 Power-up default and power-on reset

The LM75A always powers-up in its default state with:

- Normal operation mode
- OS comparator mode
- T_{os} = 80 °C
- T_{hyst} = 75 °C
- OS output active state is LOW
- Pointer value is logic 0

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When the power supply voltage is dropped below the device power-on reset level of approximately 1.9 V (POR) and then rises up again, the device will be reset to its default condition as listed above.

7.10 Protocols for writing and reading the registers

The communication between the host and the LM75A must strictly follow the rules as defined by the I^2C-bus management. The protocols for LM75A register read/write operations are illustrated in Figure 5 to Figure 10 together with the following definitions:

1. Before a communication, the I^2C-bus must be free or not busy. It means that the SCL and SDA lines must both be released by all devices on the bus, and they become HIGH by the bus pull-up resistors.
2. The host must provide SCL clock pulses necessary for the communication. Data is transferred in a sequence of 9 SCL clock pulses for every 8-bit data byte followed by 1-bit status of the acknowledgement.
3. During data transfer, except the START and STOP signals, the SDA signal must be stable while the SCL signal is HIGH. It means that the SDA signal can be changed only during the LOW duration of the SCL line.
4. S: START signal, initiated by the host to start a communication, the SDA goes from HIGH to LOW while the SCL is HIGH.
5. RS: RE-START signal, same as the START signal, to start a read command that follows a write command.
6. P: STOP signal, generated by the host to stop a communication, the SDA goes from LOW to HIGH while the SCL is HIGH. The bus becomes free thereafter.
7. W: write bit, when the write/read bit = LOW in a write command.
8. R: read bit, when the write/read bit = HIGH in a read command.
9. A: device acknowledge bit, returned by the LM75A. It is LOW if the device works properly and HIGH if not. The host must release the SDA line during this period in order to give the device the control on the SDA line.
10. A': master acknowledge bit, not returned by the device, but set by the master or host in reading 2-byte data. During this clock period, the host must set the SDA line to LOW in order to notify the device that the first byte has been read for the device to provide the second byte onto the bus.
11. NA: Not Acknowledge bit. During this clock period, both the device and host release the SDA line at the end of a data transfer, the host is then enabled to generate the STOP signal.
12. In a write protocol, data is sent from the host to the device and the host controls the SDA line, except during the clock period when the device sends the device acknowledgement signal to the bus.
13. In a read protocol, data is sent to the bus by the device and the host must release the SDA line during the time that the device is providing data onto the bus and controlling the SDA line, except during the clock period when the master sends the master acknowledgement signal to the bus.

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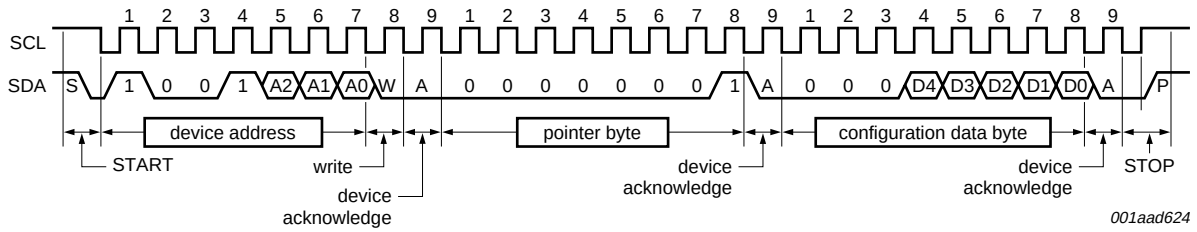


Fig 5. Write configuration register (1-byte data)

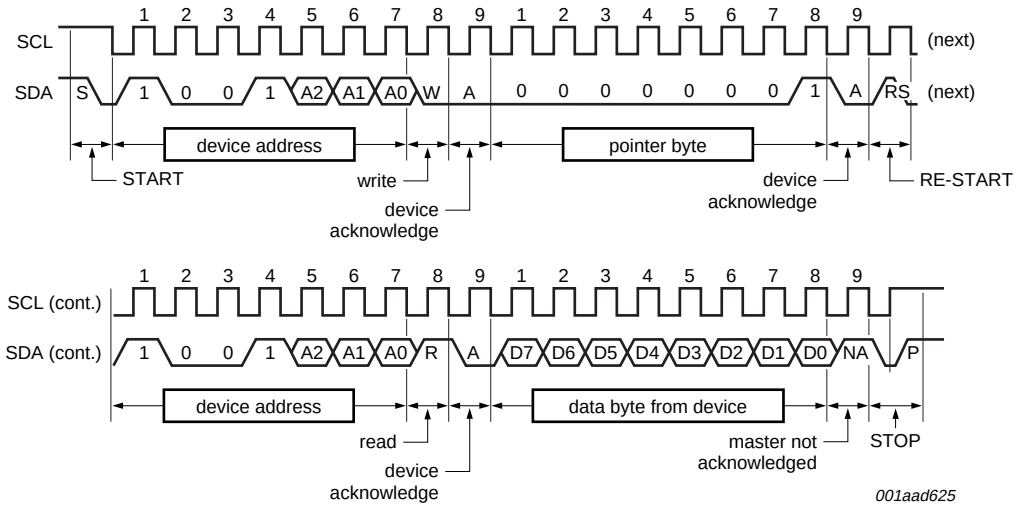


Fig 6. Read configuration register including pointer byte (1-byte data)

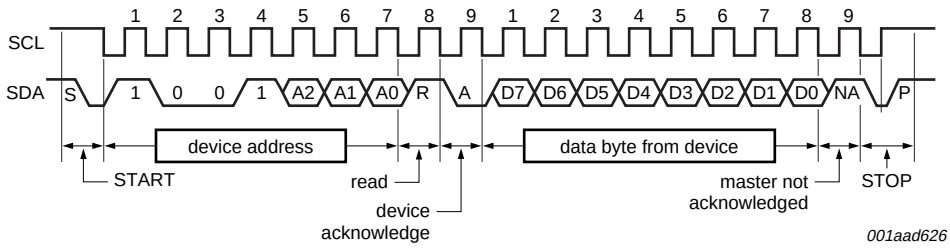


Fig 7. Read configuration register with preset pointer (1-byte data)

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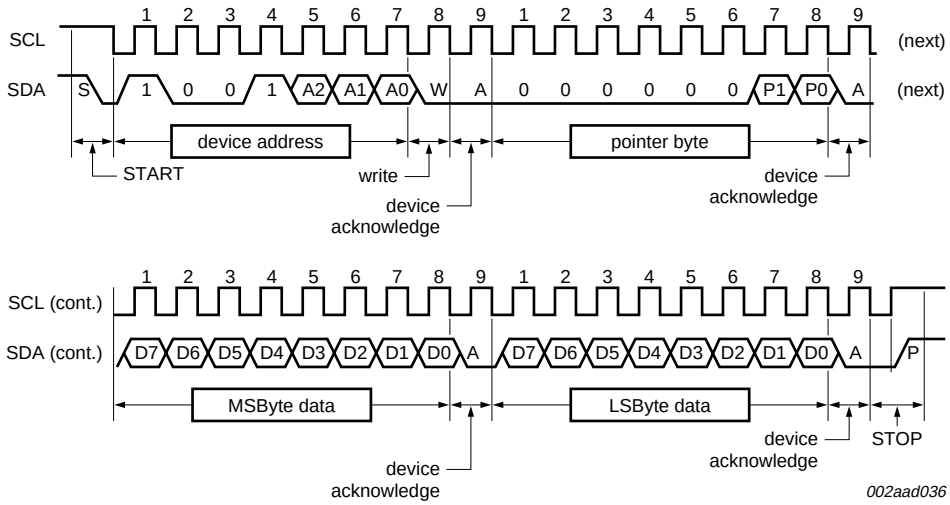


Fig 8. Write Tos or Thyst register (2-byte data)

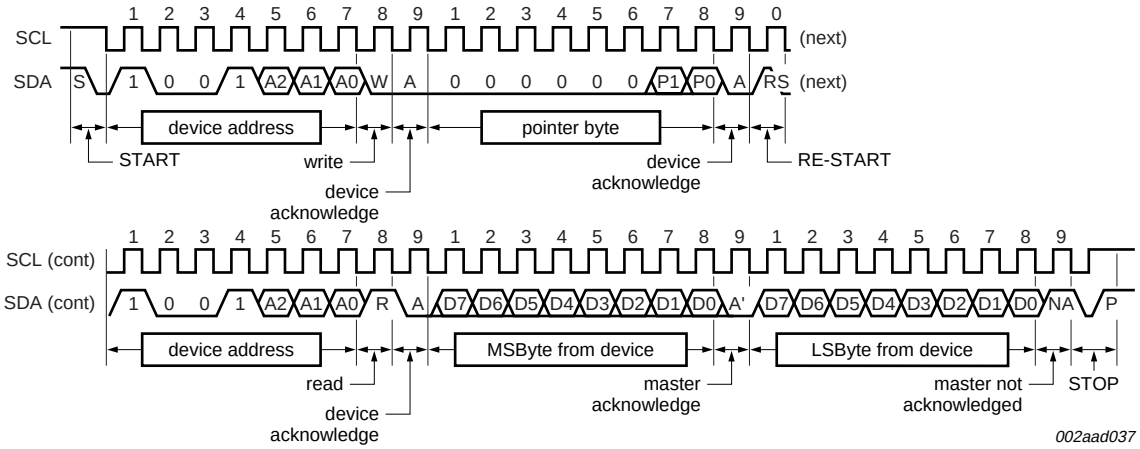


Fig 9. Read Temp, Tos or Thyst register including pointer byte (2-byte data)

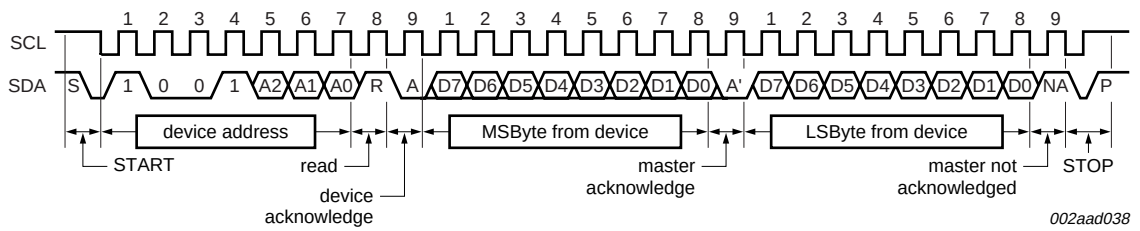


Fig 10. Read Temp, Tos or Thyst register with preset pointer (2-byte data)

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8. Application design-in information

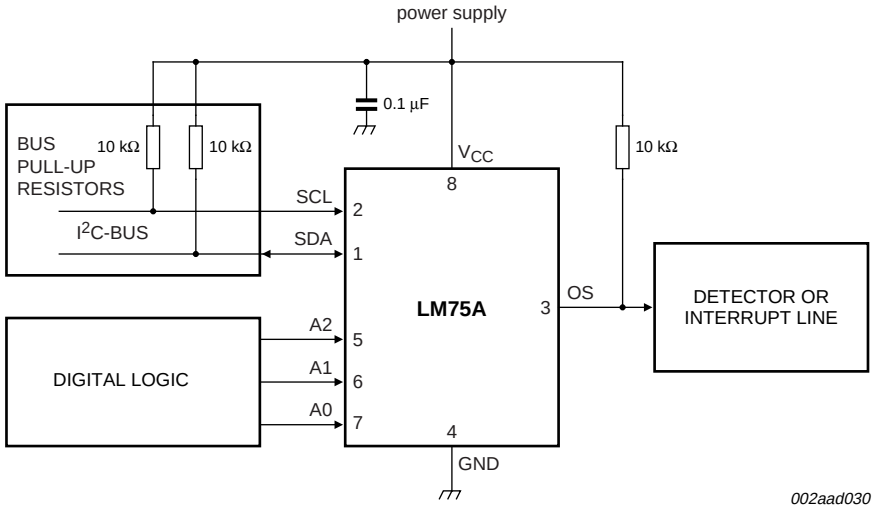


Fig 11. Typical application

9. Limiting values

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+6.0	V
	voltage at input pins		–0.3	+6.0	V
	current at input pins		–5.0	+5.0	mA
$I_{O(sink)}$	output sink current	on pin OS	-	10.0	mA
V_O	output voltage	on pin OS	–0.3	+6.0	V
V_{esd}	electrostatic discharge voltage	human body model	-	2000	V
		machine model	-	200	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C

10. Recommended operating conditions

Table 16. Recommended operating characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.8	-	5.5	V
T_{amb}	ambient temperature		–55	-	+125	°C

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11. Static characteristics

Table 17. Static characteristics

V_{CC} = 2.8 V to 5.5 V; T_{amb} = −55 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{ACC}	temperature accuracy	T_{amb} = −25 °C to +100 °C	−2	-	+2	°C
		T_{amb} = −55 °C to +125 °C	−3	-	+3	°C
T_{res}	temperature resolution	11-bit digital temp data	-	0.125	-	°C
$T_{CONV(T)}$	temperature conversion time	normal mode	-	100	-	ms
I_{DD}	supply current	normal mode: I²C-bus inactive	-	100	-	µA
		normal mode: I²C-bus active	-	-	1.0	mA
		shutdown mode	-	3.5	-	µA
V_{IH}	HIGH-level input voltage	digital pins (SCL, SDA, A2 to A0)	$0.7 \times V_{CC}$	-	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage	digital pins	−0.3	-	$0.3 \times V_{CC}$	V
V_{IHYS}	input voltage hysteresis	SCL and SDA pins	-	300	-	mV
		A2, A1, A0 pins	-	150	-	mv
I_{IH}	HIGH-level input current	digital pins; $V_I = V_{CC}$	−1.0	-	+1.0	µA
I_{IL}	LOW-level input current	digital pins; V_I = 0 V	−1.0	-	+1.0	µA
V_{OL}	LOW-level output voltage	SDA and OS pins; I_{OL} = 3 mA	-	-	0.4	V
		I_{OL} = 4 mA	-	-	0.8	V
I_{LO}	output leakage current	SDA and OS pins; $V_{OH} = V_{CC}$	-	-	10	µA
OSQ	OS fault queue	programmable	1	-	6	Conv[2]
T_{os}	overtemperature shutdown threshold	default value	-	80	-	°C
T_{hyst}	hysteresis temperature	default value	-	75	-	°C
C_i	input capacitance	digital pins	-	20	-	pF

[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] “Conv” = device A-to-D conversion.

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12. Dynamic characteristics

Table 18. I^2C-bus interface dynamic characteristics[1]

V_{CC} = 2.8 V to 5.5 V; T_{amb} = −55 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{CLK}	SCL clock period	see Figure 12		2.5	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			100	-	-	ns
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time		[2]	0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			100	-	-	ns
t_f	fall time	SDA and OS outputs; C_L = 400 pF; I_{OL} = 3 mA		-	250	-	ns

[1] These specifications are guaranteed by design and not tested in production.

[2] The data hold time minimum value is 10 ns for the SCL clock period of 10 µs or higher.

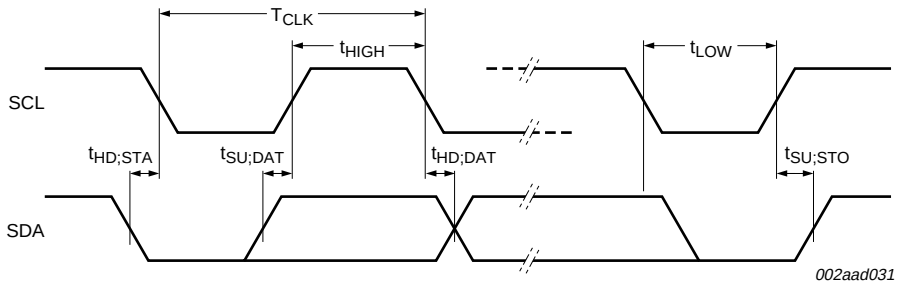
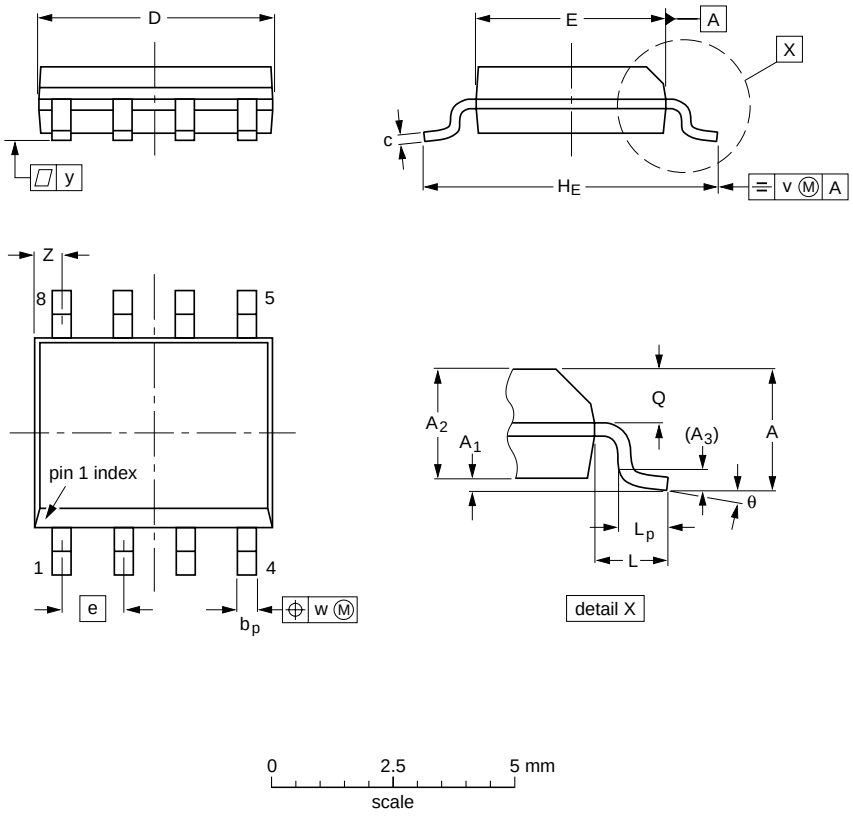


Fig 12. Timing diagram

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13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

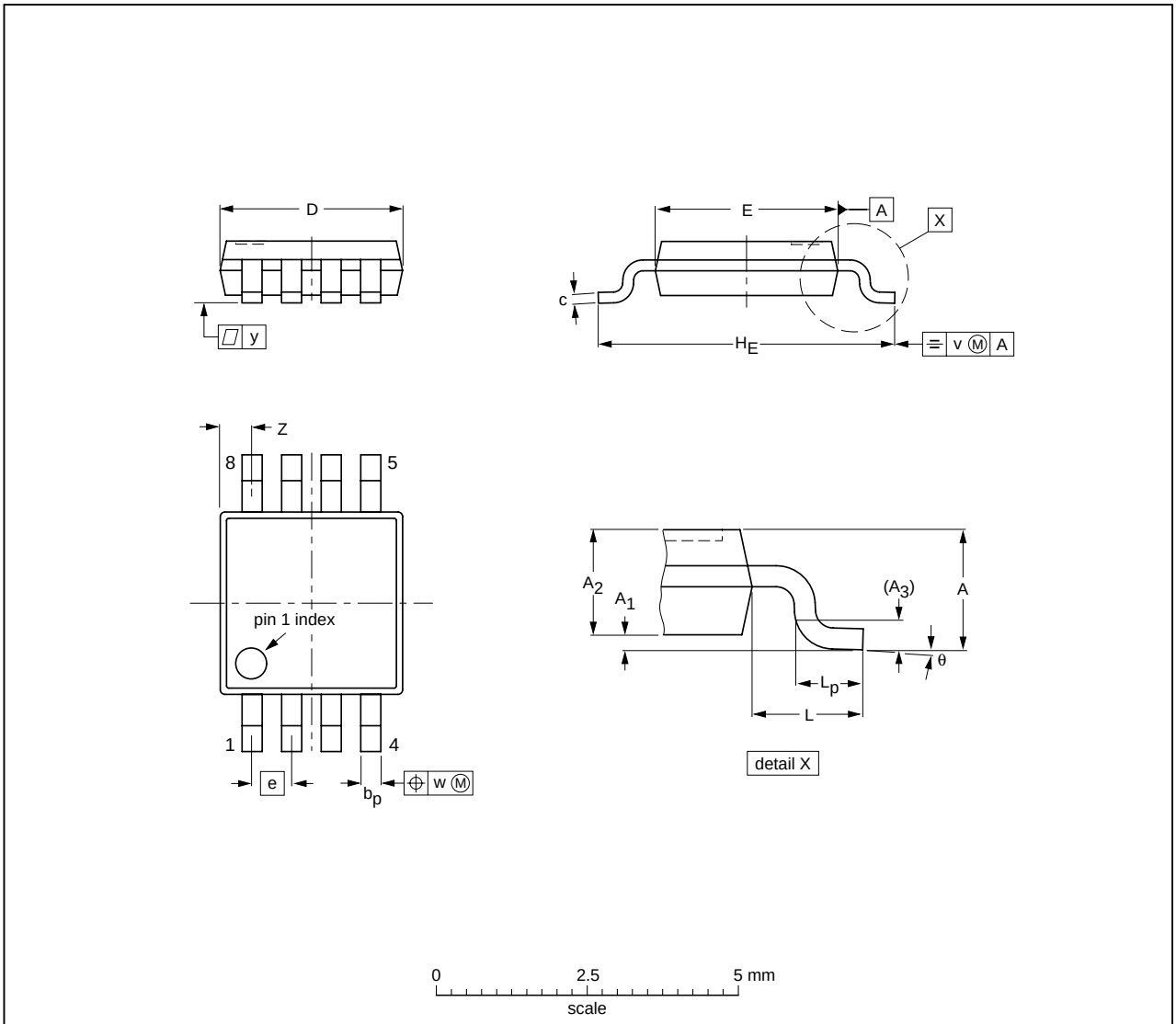
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT96-1 (SO8)

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TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 14. Package outline SOT505-1 (TSSOP8)

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14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19 and 20

Table 19. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

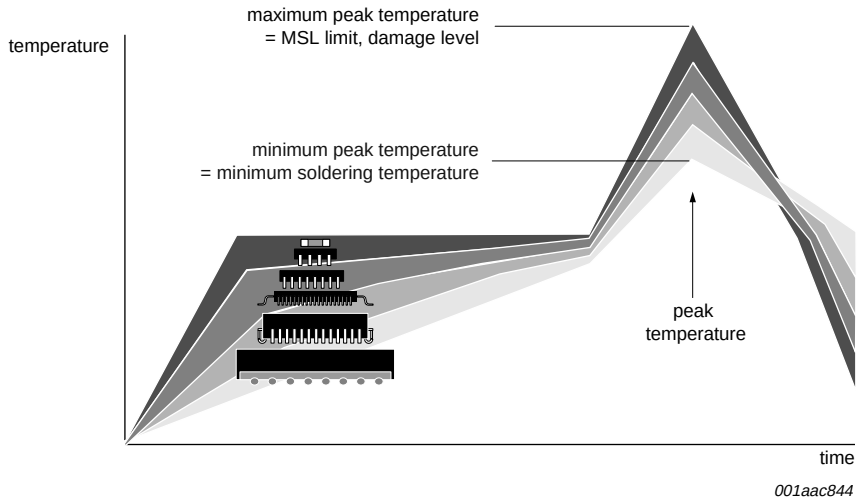
Table 20. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 15.

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MSL: Moisture Sensitivity Level

Fig 15. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 21. Abbreviations

Acronym	Description
A-to-D	Analog-to-Digital
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LSB	Lease Significant Bit
LSByte	Least Significant Byte
MM	Machine Model
MSB	Most Significant Bit
MSByte	Most Significant Byte
POR	Power-On Reset

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16. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LM75A_4	20070710	Product data sheet	-	LM75A_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • added (new) Section 4.1 “Ordering options” • added separate pin configuration drawings for SO8 and TSSOP8 (Figure 2 and Figure 3) • Table 15 “Limiting values”: – table title changed from “Absolute maximum ratings” to Table 15 “Limiting values” – symbol and parameter descriptions modified to new presentation standards • Table 18 “I^2C-bus interface dynamic characteristics[1]”: – parameter descriptions modified to new presentation standards – added Table note 2 and its reference at $t_{HD;DAT}$			
LM75A_3	20060627	Product data sheet	-	LM75A_2
LM75A_2 (9397 750 14174)	20041005	Product data sheet	-	LM75A_1
LM75A_1 (9397 750 08571)	20010716	Product data	ECN 853-2266 26719 dated 16 July 2001	-

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17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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