MCP4921/4922

12-Bit DAC with SPI™ Interface

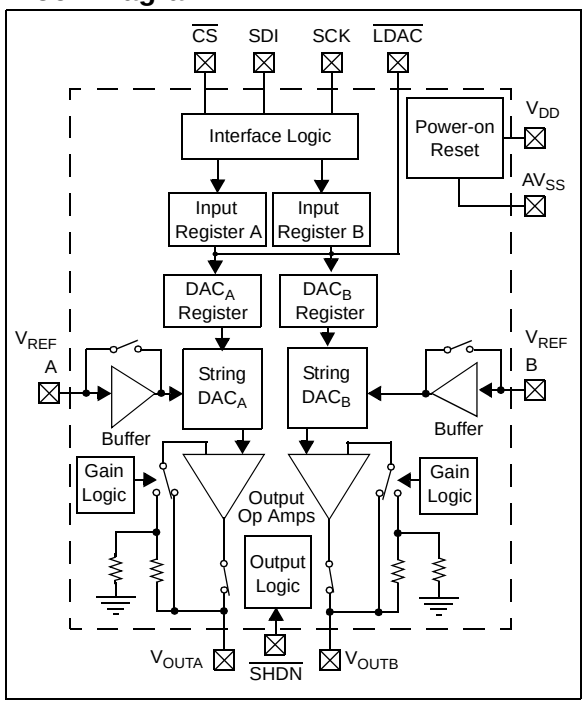
Features

- 12-Bit Resolution
- ±0.2 LSB DNL (typ)
- ±2 LSB INL (typ)
- Single or Dual Channel
- Rail-to-Rail Output
- SPI™ Interface with 20 MHz Clock Support
- Simultaneous Latching of the Dual DACs w/$\overline{\text{LDAC}}$
- Fast Settling Time of 4.5 µs
- Selectable Unity or 2x Gain Output
- 450 kHz Multiplier Mode
- External V_{REF} Input
- 2.7V to 5.5V Single-Supply Operation
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Digitally-Controlled Multiplier/Divider
- Portable Instrumentation (Battery-Powered)
- Motor Feedback Loop Control

Block Diagram



Description

The Microchip Technology Inc. MCP492X are 2.7 – 5.5V, low-power, low DNL, 12-Bit Digital-to-Analog Converters (DACs) with optional 2x buffered output and SPI interface.

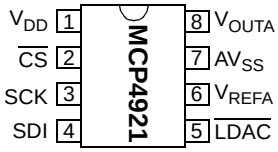
The MCP492X are DACs that provide high accuracy and low noise performance for industrial applications where calibration or compensation of signals (such as temperature, pressure and humidity) are required.

The MCP492X are available in the extended temperature range and PDIP, SOIC, MSOP and TSSOP packages.

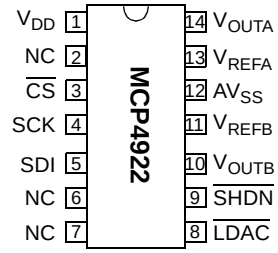
The MCP492X devices utilize a resistive string architecture, with its inherent advantages of low DNL error, low ratio metric temperature coefficient and fast settling time. These devices are specified over the extended temperature range. The MCP492X include double-buffered inputs, allowing simultaneous updates using the $\overline{\text{LDAC}}$ pin. These devices also incorporate a Power-On Reset (POR) circuit to ensure reliable power-up.

Package Types

8-Pin PDIP, SOIC, MSOP



14-Pin PDIP, SOIC, TSSOP



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 6.5V
All inputs and outputs w.r.t ..... AV_{SS} –0.3V to V_{DD}+0.3V
Current at Input Pins .....±2 mA
Current at Supply Pins .....±50 mA
Current at Output Pins .....±25 mA
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-55°C to +125°C
ESD protection on all pins .....≥ 4 kV (HBM), ≥ 400V (MM)
Maximum Junction Temperature (T_J) .....+150°C

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5V AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, AV_{SS} = 0V, V_{REF} = 2.048V, output buffer gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF T_A = -40 to +85°C. Typical values at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Input Voltage	V_{DD}	2.7	—	5.5		
Input Current - **MCP4921** - **MCP4922**	I_{DD}	— —	175 350	350 700	µA	Input unbuffered, digital inputs grounded, output unloaded, code at 0x000
Hardware Shutdown Current	I_{SHDN}	—	0.3	2	µA	
Software Shutdown Current	I_{SHDN_SW}	—	3.3	6	µA	
Power-on-Reset Threshold	V_{POR}	—	2.0	—	V	
DC Accuracy						
Resolution	n	12	—	—	Bits	
INL Error	INL	-12	2	12	LSB	
DNL	DNL	-0.75	±0.2	+0.75	LSB	Device is Monotonic
Offset Error	V_{OS}	—	±0.02	1	% of FSR	Code 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	— —	0.16 -0.44	— —	ppm/°C ppm/°C	-45°C to 25°C +25°C to 85°C
Gain Error	g_E	—	-0.10	1	% of FSR	Code 0xFFFh, not including offset error.
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	
Input Amplifier (V_{REF} Input)						
Input Range - Buffered Mode	V_{REF}	0.040	—	V_{DD} – 0.040	V	**Note 1**
Input Range - Unbuffered Mode	V_{REF}	0	—	V_{DD}	V	Code = 2048 V_{REF} = 0.2v p-p, f = 100 Hz and 1 kHz
Input Impedance	R_{VREF}	—	165	—	kΩ	Unbuffered Mode
Input Capacitance - Unbuffered Mode	C_{VREF}	—	7	—	pF	
Multiplier Mode -3 dB Bandwidth	f_{VREF}	—	450	—	kHz	V_{REF} = 2.5V ±0.2Vp-p, Unbuffered, G = 1
	f_{VREF}	—	400	—	kHz	V_{REF} = 2.5V ±0.2 Vp-p, Unbuffered, G = 2
Multiplier Mode - Total Harmonic Distortion	THD_{VREF}	—	-73	—	dB	V_{REF} = 2.5V ±0.2Vp-p, Frequency = 1 kHz

Note 1: By design, not production tested.
2: Too small to quantify.

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5V AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, AV_{SS} = 0V, V_{REF} = 2.048V, output buffer gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF T_A = -40 to +85°C. Typical values at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output Amplifier						
Output Swing	V_{OUT}	—	0.010 to V_{DD} – 0.040	—		Accuracy is better than 1 LSB for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	θm	—	66	—	degrees	
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	15	24	mA	
Settling Time	$t_{settling}$	—	4.5	—	µs	Within 1/2 LSB of final value from 1/4 to 3/4 full-scale range
Dynamic Performance						
DAC-to-DAC Crosstalk		—	10	—	nV-s	**Note 2**
Major Code Transition Glitch		—	45	—	nV-s	1 LSB change around major carry (0111...1111 to 1000...0000)
Digital Feedthrough		—	10	—	nV-s	**Note 2**
Analog Crosstalk		—	10	—	nV-s	**Note 2**

Note 1: By design, not production tested.
2: Too small to quantify.

3V AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 3V, AV_{SS} = 0V, V_{REF} = 2.048V external, output buffer gain (G) = 1x, R_L = 5 kΩ to GND, C_L = 100 pF T_A = -40 to +85°C. Typical values at 25°C

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Input Voltage	V_{DD}	2.7	—	5.5		
Input Current - **MCP4921**	I_{DD}	—	125	250	µA	Input unbuffered, digital inputs grounded, output unloaded, code at 0x000
- **MCP4922**		—	250	500		
Hardware Shutdown Current	I_{SHDN}	—	0.25	2	µA	
Software Shutdown Current	I_{SHDN_SW}	—	2	6	µA	
Power-On Reset threshold	V_{POR}	—	2.0	—	V	
DC Accuracy						
Resolution	n	12	—	—	Bits	
INL Error	INL	-12	±3	+12	LSB	
DNL	DNL	-0.75	±0.3	+0.75	LSB	Device is Monotonic
Offset Error	V_{OS}	—	±0.02	1	% of FSR	Code 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	—	0.5	—	ppm/°C	-45°C to 25°C
		—	-0.77	—	ppm/°C	+25°C to 85°C
Gain Error	g_E	—	-0.15	1	% of FSR	Code 0xFFFh, not including offset error.
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	
Input Amplifier (V_{REF} Input)						
Input Range - Buffered Mode	V_{REF}	0.040	—	V_{DD}-0.040	V	**Note 1**
Input Range - Unbuffered Mode	V_{REF}	0	—	V_{DD}	V	Code = 2048, V_{REF} = 0.2v p-p, f = 100 Hz and 1 kHz
Input Impedance	R_{VREF}	—	165	—	kΩ	Unbuffered Mode

Note 1: By design, not production tested.
2: Too small to quantify.

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3V AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 3V, AV_{SS} = 0V, V_{REF} = 2.048V external, output buffer gain (G) = 1x, R_L = 5 kΩ to GND, C_L = 100 pF T_A = -40 to +85°C. Typical values at 25°C

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Capacitance – Unbuffered Mode	C_{VREF}	—	7	—	pF	
Multiplier Mode -3 dB Bandwidth	f_{VREF}	—	440	—	kHz	V_{REF} = 2.048V ±0.1 Vp-p, unbuffered, G = 1
	f_{VREF}	—	390	—	kHz	V_{REF} = 2.048V ±0.1 Vp-p, unbuffered, G = 2
Multiplier Mode – Total Harmonic Distortion	THD_{VREF}	—	-73	—	dB	V_{REF} = 2.5V ±0.1 Vp-p, Frequency = 1 kHz
Output Amplifier						
Output Swing	V_{OUT}	—	0.010 to V_{DD} – 0.040	—		Accuracy is better than 1 LSB for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	θ_m	—	66	—	degrees	
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	14	24	mA	
Settling Time	$t_{settling}$	—	4.5	—	µs	Within 1/2 LSB of final value from 1/4 to 3/4 full-scale range
Dynamic Performance						
DAC-to-DAC Crosstalk		—	10	—	nV-s	**Note 2**
Major Code Transition Glitch		—	45	—	nV-s	1 LSB change around major carry (0111...1111 to 1000...0000)
Digital Feedthrough		—	10	—	nV-s	**Note 2**
Analog Crosstalk		—	10	—	nV-s	**Note 2**

Note 1: By design, not production tested.
2: Too small to quantify.

5V EXTENDED TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, AV_{SS} = 0V, V_{REF} = 2.048V, output buffer gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Input Voltage	V_{DD}	2.7	—	5.5		
Input Current - **MCP4921**	I_{DD}	—	200	—	µA	Input unbuffered, digital inputs grounded, output unloaded, code at 0x000
- **MCP4922**		—	400	—		
Hardware Shutdown Current	I_{SHDN}	—	1.5	—	µA	
Software Shutdown Current	I_{SHDN_SW}	—	5	—	µA	
Power-On Reset threshold	V_{POR}	—	1.85	—	V	
DC Accuracy						
Resolution	n	12	—	—	Bits	
INL Error	INL	—	±4	—	LSB	
DNL	DNL	—	±0.25	—	LSB	Device is Monotonic
Offset Error	V_{OS}	—	±0.02	—	% of FSR	Code 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	—	-5	—	ppm/°C	+25°C to +125°C

Note 1: By design, not production tested.
2: Too small to quantify.

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5V EXTENDED TEMPERATURE SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, AV_{SS} = 0V, V_{REF} = 2.048V, output buffer gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Gain Error	g_E	—	-0.10	—	% of FSR	Code 0xFFFh, not including offset error
Gain Error Temperature Coefficient	$\Delta G/°C$	—	-3	—	ppm/°C	
Input Amplifier (V_{REF} Input)						
Input Range - Buffered Mode	V_{REF}	—	0.040 to V_{DD}- 0.040	—	V	**Note 1** Code = 2048, V_{REF} = 0.2v p-p, f = 100 Hz and 1 kHz
Input Range - Unbuffered Mode	V_{REF}	0	—	V_{DD}	V	
Input Impedance	R_{VREF}	—	174	—	kΩ	Unbuffered Mode
Input Capacitance - Unbuffered Mode	C_{VREF}	—	7	—	pF	
Multiplying Mode -3 dB Bandwidth	f_{VREF}	—	450	—	kHz	V_{REF} = 2.5V ±0.1 Vp-p, Unbuffered, G=1
	f_{VREF}	—	400	—	kHz	V_{REF} = 2.5V ±0.1 Vp-p, Unbuffered, G = 2
Multiplying Mode - Total Harmonic Distortion	THD_{VREF}	—	—	—	dB	V_{REF} = 2.5V ±0.1Vp-p, Frequency = 1 kHz
Output Amplifier						
Output Swing	V_{OUT}	—	0.010 to V_{DD} – 0.040	—		Accuracy is better than 1 LSB for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	θm	—	66	—	degrees	
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	17	—	mA	
Settling Time	$t_{settling}$	—	4.5	—	µs	Within 1/2 LSB of final value from 1/4 to 3/4 full-scale range
Dynamic Performance						
DAC to DAC Crosstalk		—	10	—	nV-s	**Note 2**
Major Code Transition Glitch		—	45	—	nV-s	1 LSB change around major carry (0111...1111 to 1000...0000)
Digital Feedthrough		—	10	—	nV-s	**Note 2**
Analog Crosstalk		—	10	—	nV-s	**Note 2**

Note 1: By design, not production tested.

2: Too small to quantify.

AC CHARACTERISTICS (SPI TIMING SPECIFICATIONS)

Electrical Specifications: Unless otherwise indicated, V_{DD}= 2.7V – 5.5V, T_A= -40 to +125°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Schmitt Trigger High-Level Input Voltage (All digital input pins)	V_{IH}	0.7 V_{DD}	—	—	V	
Schmitt Trigger Low-Level Input Voltage (All digital input pins)	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.05 V_{DD}	—		
Input Leakage Current	$I_{LEAKAGE}$	-1	—	1	µA	$\overline{SHDN}$ = $\overline{LDAC}$ = $\overline{CS}$ = SDI = SCK + V_{REF} = V_{DD} or AV_{SS}
Digital Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_{CLK} = 1 MHz **(Note 1)**
Clock Frequency	F_{CLK}	—	—	20	MHz	T_A = +25°C **(Note 1)**
Clock High Time	t_{HI}	15	—	—	ns	**Note 1**
Clock Low Time	t_{LO}	15	—	—	ns	**Note 1**
$\overline{CS}$ Fall to First Rising CLK Edge	t_{CSSR}	40	—	—	ns	Applies only when $\overline{CS}$ falls with CLK high. **(Note 1)**
Data Input Setup Time	t_{SU}	15	—	—	ns	**Note 1**
Data Input Hold Time	t_{HD}	10	—	—	ns	**Note 1**
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	15	—	—	ns	**Note 1**
$\overline{CS}$ High Time	t_{CSH}	15	—	—	ns	**Note 1**
$\overline{LDAC}$ Pulse Width	t_{LD}	100	—	—	ns	**Note 1**
$\overline{LDAC}$ Setup Time	t_{LS}	40	—	—	ns	**Note 1**
SCK Idle Time before $\overline{CS}$ Fall	t_{IDLE}	40	—	—	ns	**Note 1**

Note 1: By design and characterization, not production tested.

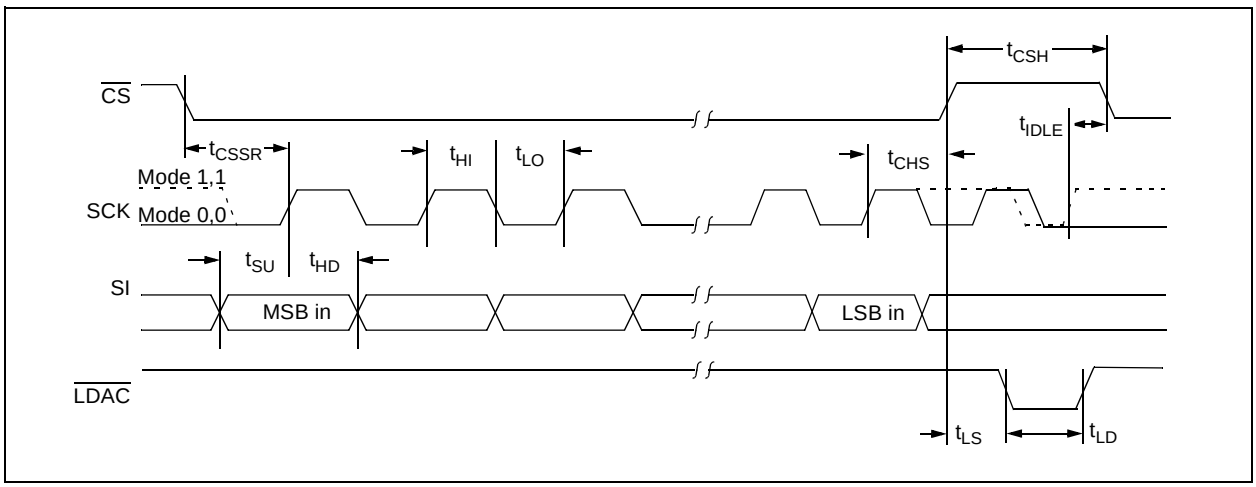


FIGURE 1-1: *SPI™ Input Timing.*

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, AV_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP492X family of DACs operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of 150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V , AV_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

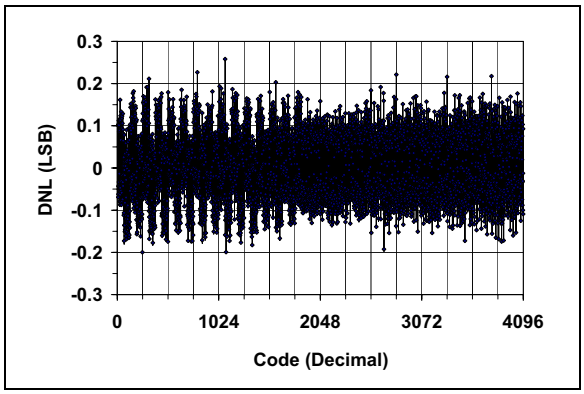


FIGURE 2-1: *DNL vs. Code.*

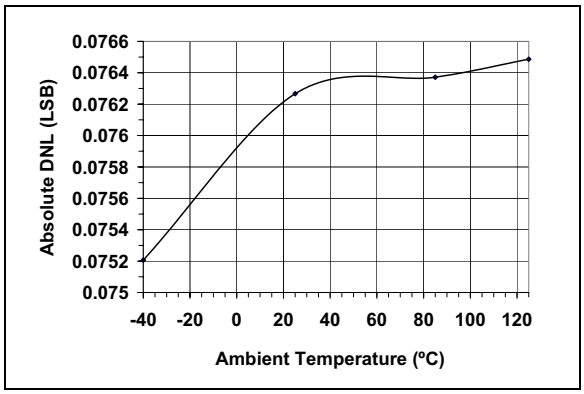


FIGURE 2-4: *Absolute DNL vs. Ambient Temperature.*

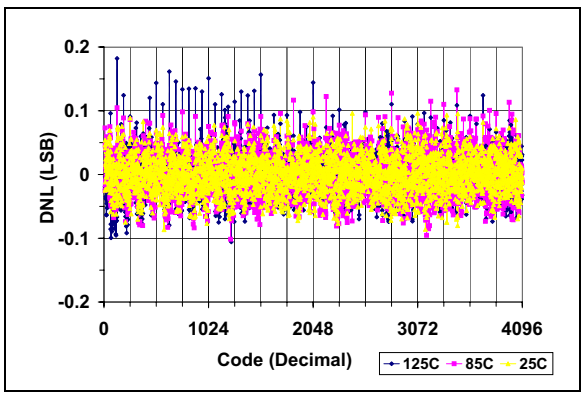


FIGURE 2-2: *DNL vs. Code and Ambient Temperature.*

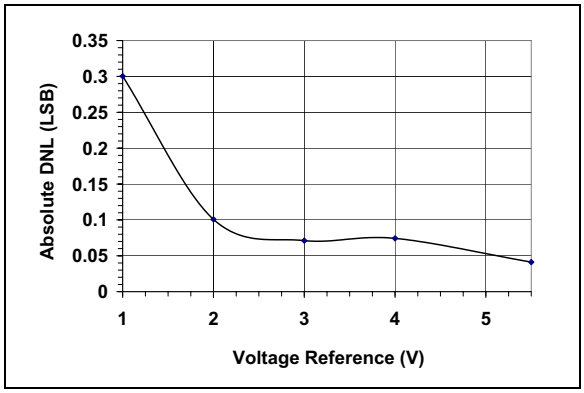


FIGURE 2-5: *Absolute DNL vs. Voltage Reference.*

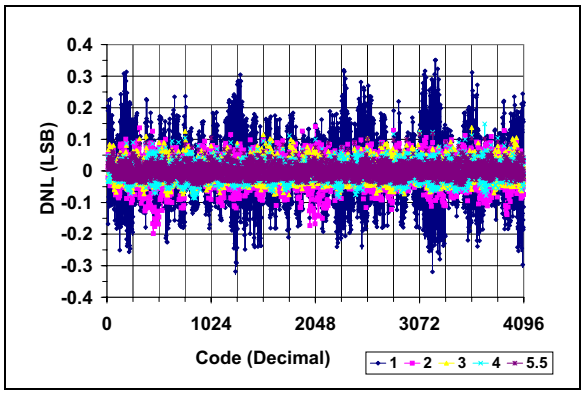


FIGURE 2-3: *DNL vs. Code and V_{REF}, Gain=1.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V , AV_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

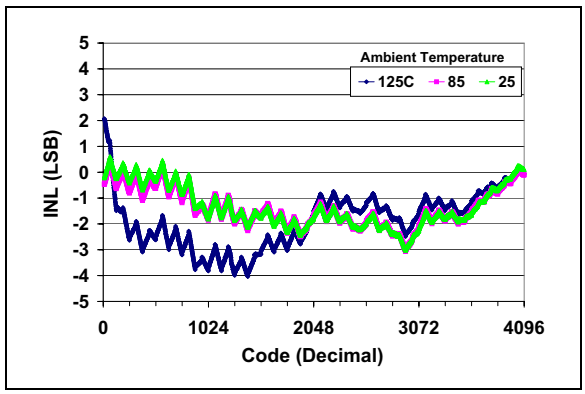


FIGURE 2-6: *INL vs. Code and Ambient Temperature.*

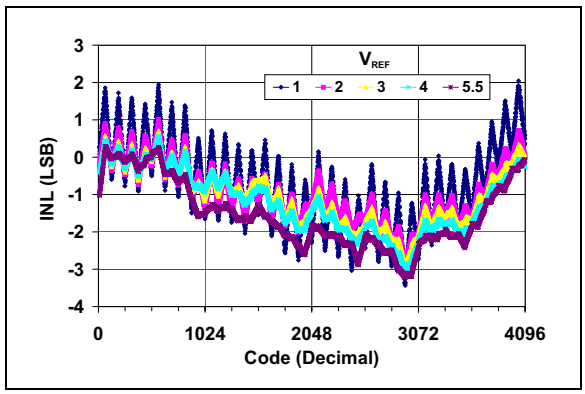


FIGURE 2-9: *INL vs. Code and V_{REF}*

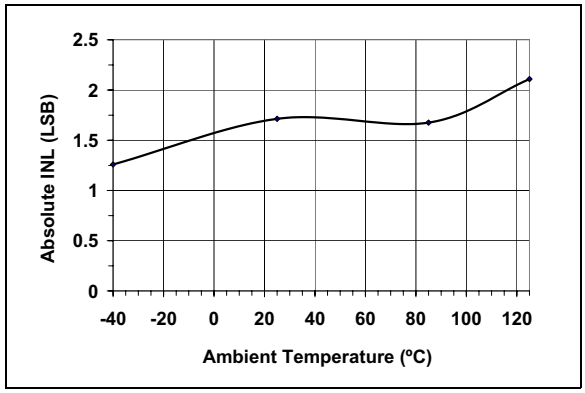


FIGURE 2-7: *Absolute INL vs. Ambient Temperature.*

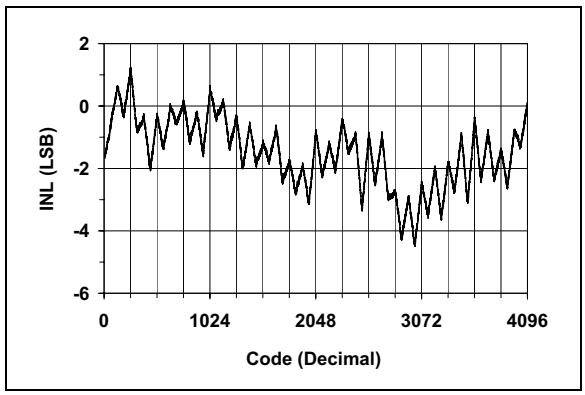


FIGURE 2-10: *INL vs. Code.*

Note:	Single device graph (Figure 2-10) for illustration of 64 code effect.

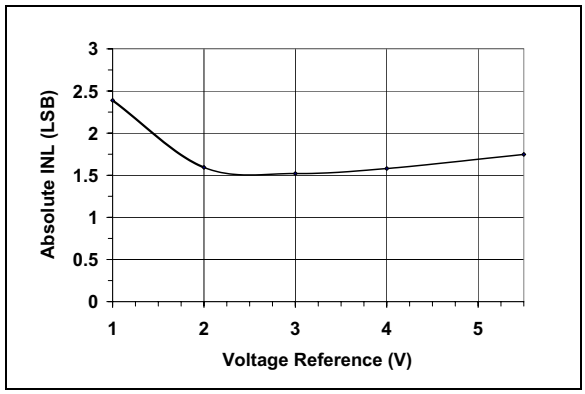


FIGURE 2-8: *Absolute INL vs. V_{REF}*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, AV_{SS} = 0V, V_{REF} = 2.048V, Gain = 2.

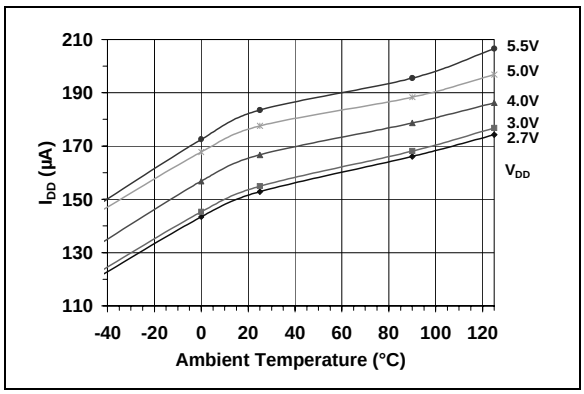


FIGURE 2-11: *MCP4921 I_{DD} vs. Ambient Temperature and V_{DD}.*

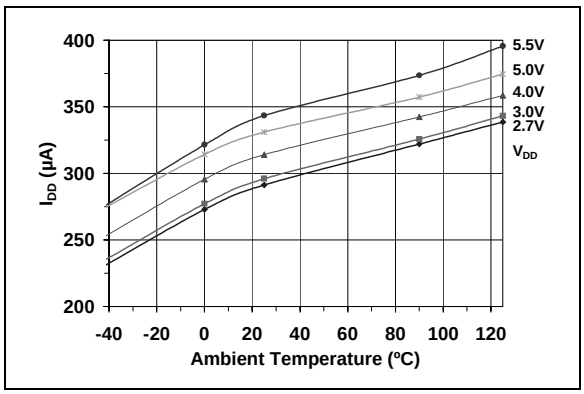


FIGURE 2-14: *MCP4922 I_{DD} vs. Ambient Temperature and V_{DD}.*

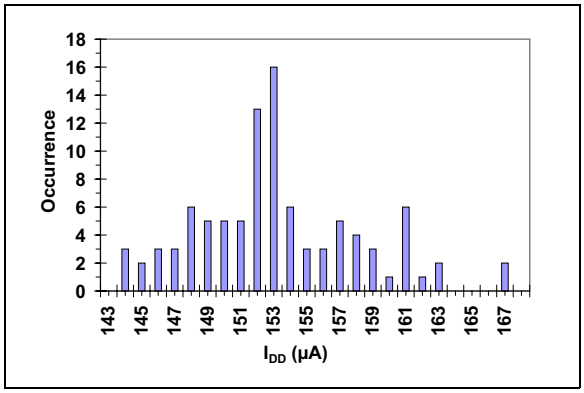


FIGURE 2-12: *MCP4921 I_{DD} Histogram (V_{DD} = 2.7V).*

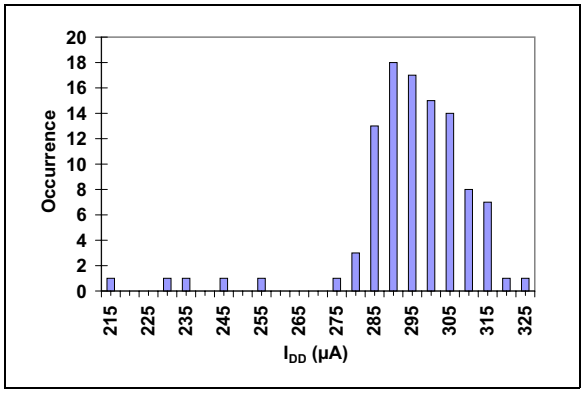


FIGURE 2-15: *MCP4922 I_{DD} Histogram (V_{DD} = 2.7V).*

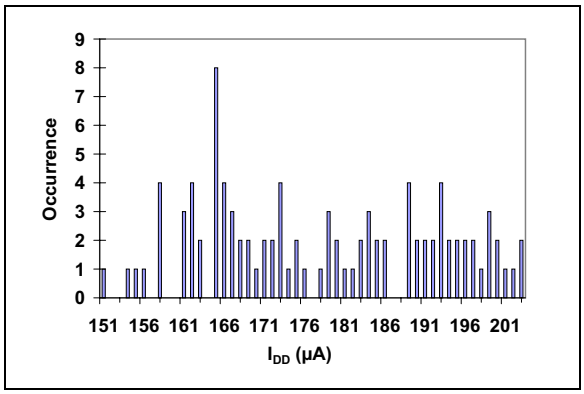


FIGURE 2-13: *MCP4921 I_{DD} Histogram (V_{DD} = 5.0V).*

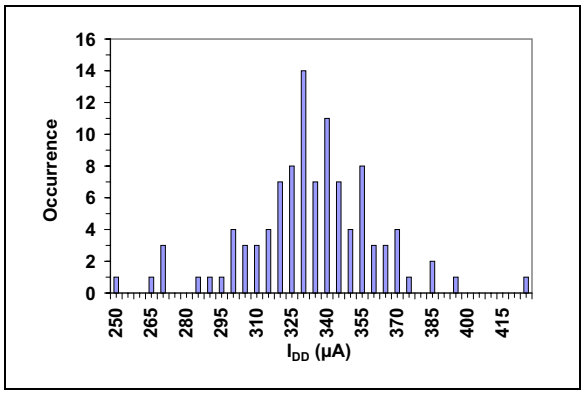


FIGURE 2-16: *MCP4922 I_{DD} Histogram (V_{DD} = 5.0V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V , AV_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

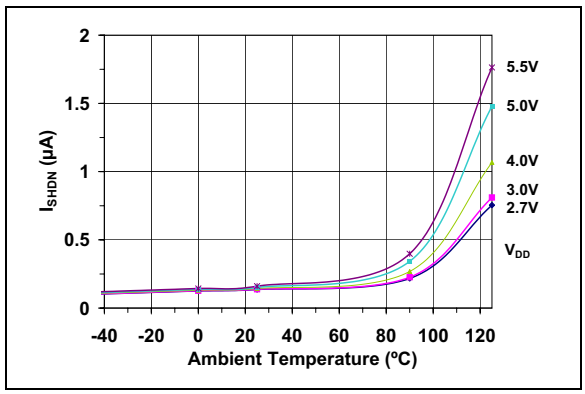


FIGURE 2-17: *Hardware Shutdown Current vs. Ambient Temperature and V_{DD}.*

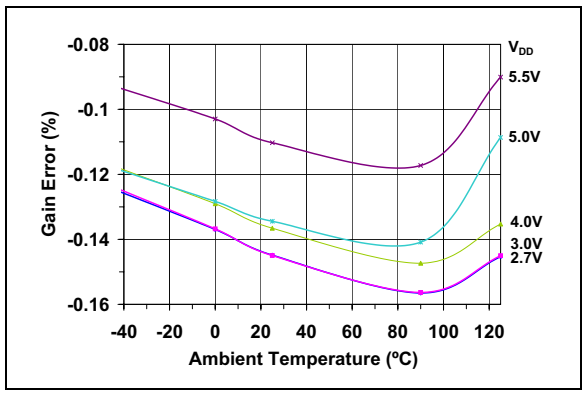


FIGURE 2-20: *Gain Error vs. Ambient Temperature and V_{DD}.*

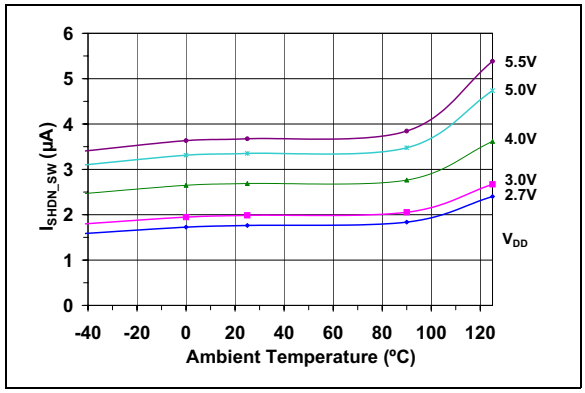


FIGURE 2-18: *Software Shutdown Current vs. Ambient Temperature and V_{DD}.*

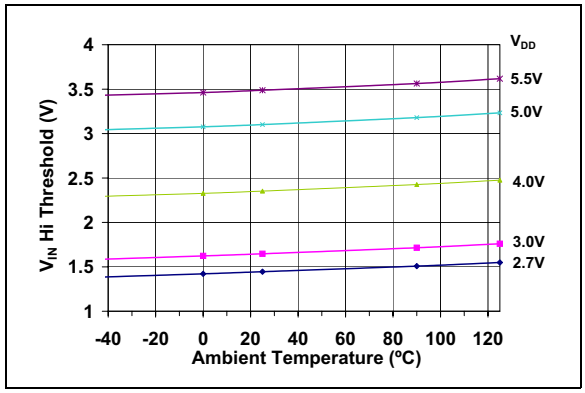


FIGURE 2-21: *V_{IN} High Threshold vs Ambient Temperature and V_{DD}.*

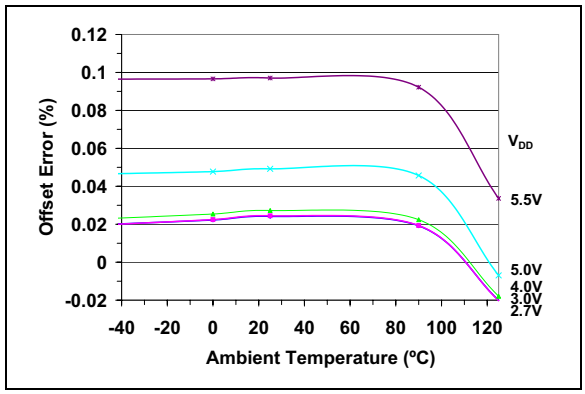


FIGURE 2-19: *Offset Error vs. Ambient Temperature and V_{DD}.*

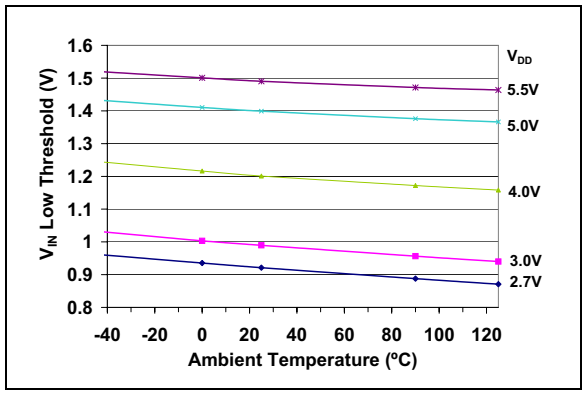


FIGURE 2-22: *V_{IN} Low Threshold vs Ambient Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V , AV_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

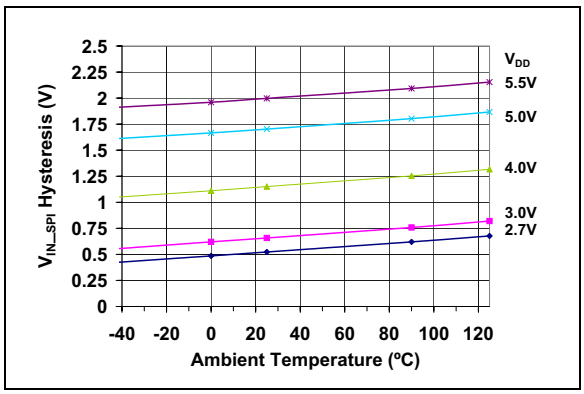


FIGURE 2-23: *Input Hysteresis vs. Ambient Temperature and V_{DD}.*

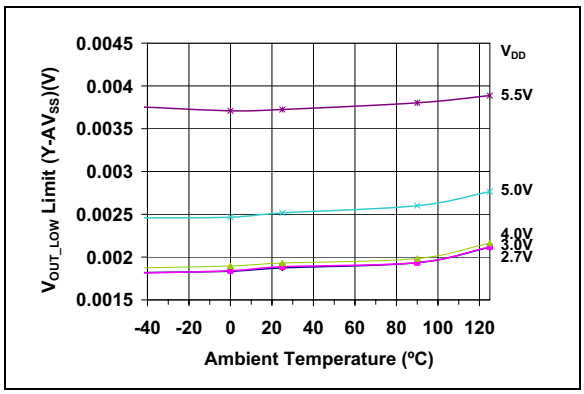


FIGURE 2-26: *V_{OUT} Low Limit vs. Ambient Temperature and V_{DD}.*

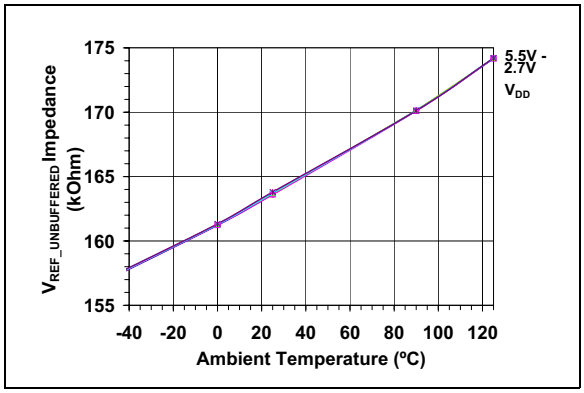


FIGURE 2-24: *V_{REF} Input Impedance vs. Ambient Temperature and V_{DD}.*

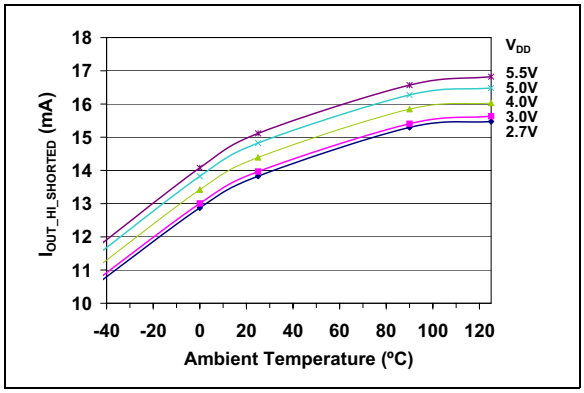


FIGURE 2-27: *I_{OUT} High Short vs. Ambient Temperature and V_{DD}.*

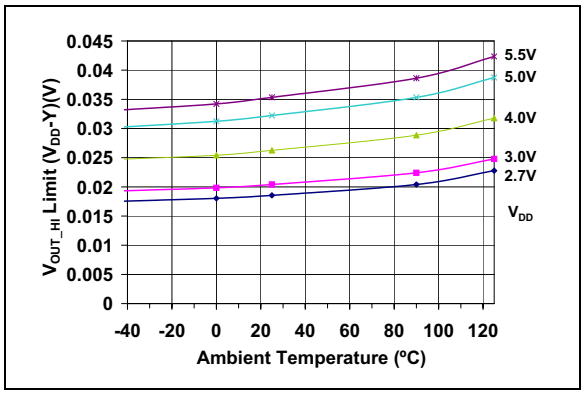


FIGURE 2-25: *V_{OUT} High Limit vs. Ambient Temperature and V_{DD}.*

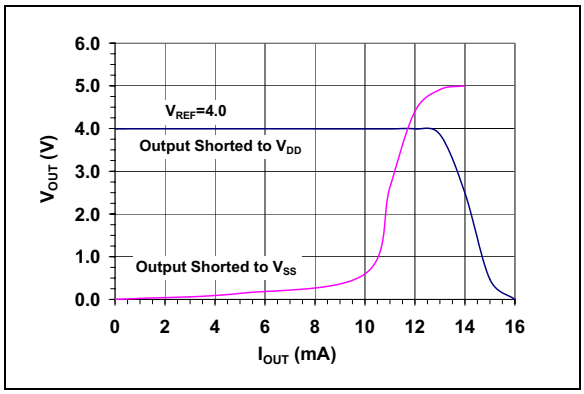


FIGURE 2-28: *I_{OUT} vs V_{OUT}. Gain = 1.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V , AV_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

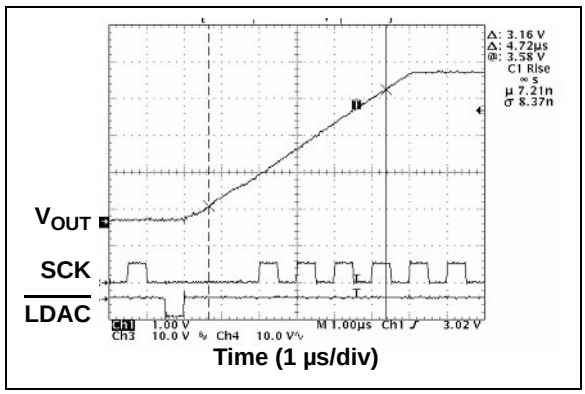


FIGURE 2-29: *V_{OUT} Rise Time 100%.*

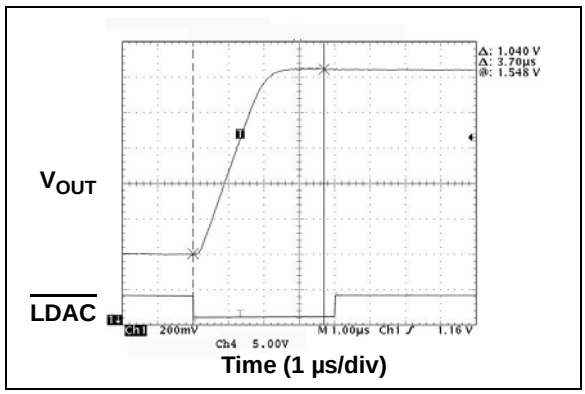


FIGURE 2-32: *V_{OUT} Rise Time 25% - 75%*

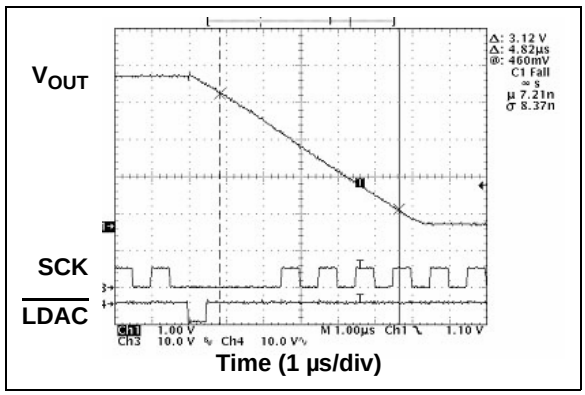


FIGURE 2-30: *V_{OUT} Fall Time.*

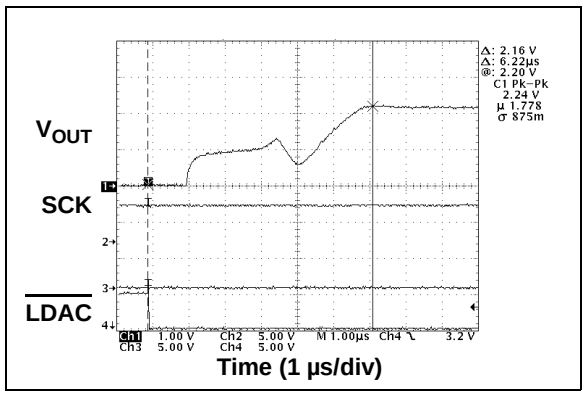


FIGURE 2-33: *V_{OUT} Rise Time Exit Shutdown.*

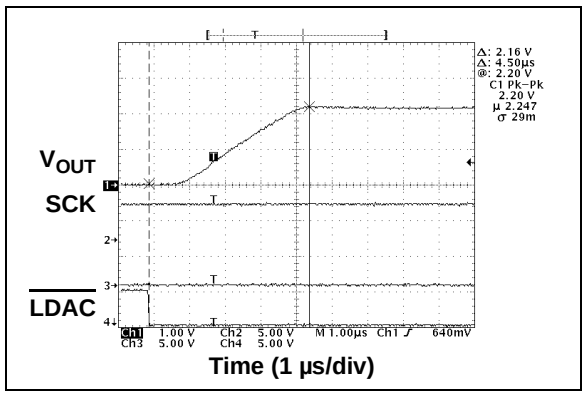


FIGURE 2-31: *V_{OUT} Rise Time 50%.*

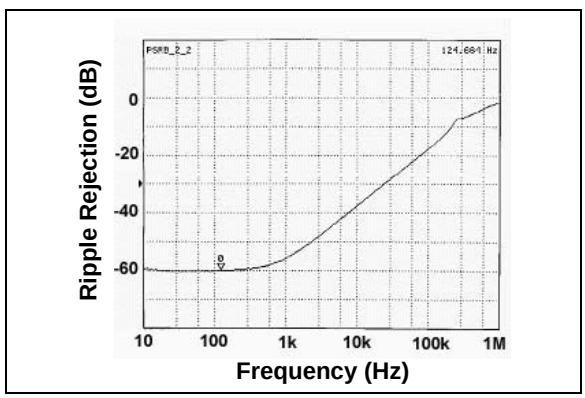


FIGURE 2-34: *PSRR vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V , AV_{SS} = 0V, V_{REF} = 2.50V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

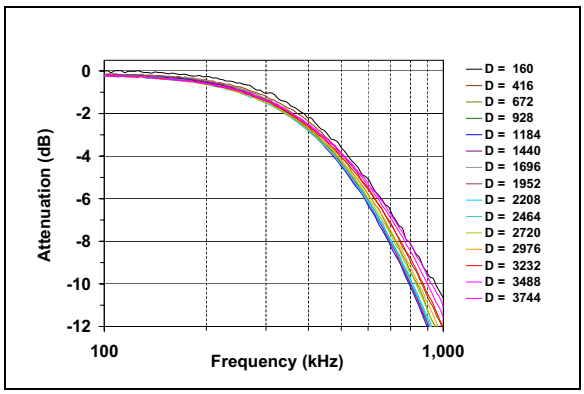


FIGURE 2-35: *Multiplier Mode Bandwidth.*

Figure 2-35 calculation:
Attenuation (dB) = 20 log (V_{OUT}/V_{REF}) – 20 log (G(D/4096))

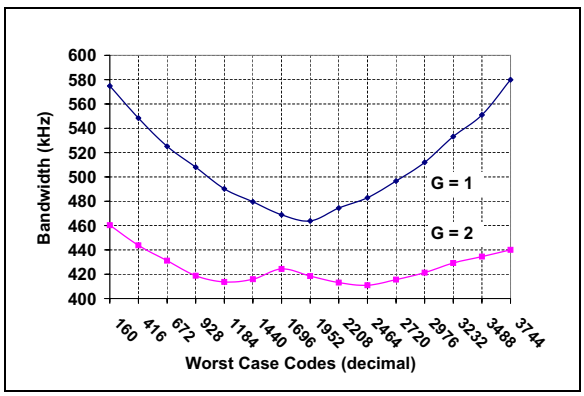


FIGURE 2-36: *-3 db Bandwidth vs. Worst Codes.*

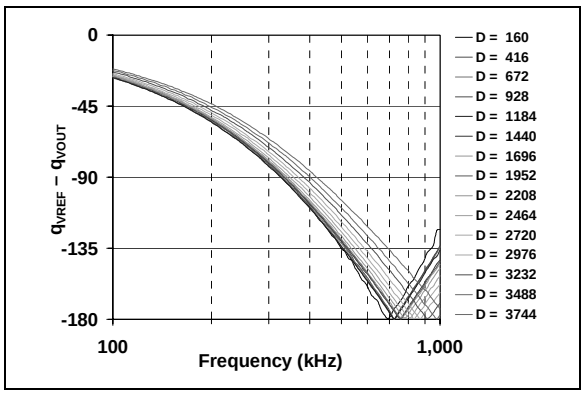


FIGURE 2-37: *Phase Shift.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP4921 Pin No.	MCP4922 Pin No.	Symbol	Function
1	1	V_{DD}	Positive Power Supply Input (2.7V to 5.5V)
—	2	NC	No Connection
2	3	$\overline{CS}$	Chip Select Input
3	4	SCK	Serial Clock Input
4	5	SDI	Serial Data Input
—	6	NC	No Connection
—	7	NC	No Connection
5	8	$\overline{LDAC}$	Syncronization input used to transfer DAC settings from serial latches to the output latches.
—	9	$\overline{SHDN}$	Hardware Shutdown Input
—	10	V_{OUTB}	DAC_B Output
—	11	V_{REFB}	DAC_B Voltage Input (AV_{SS} to V_{DD})
7	12	AV_{SS}	Analog ground
6	13	V_{REFA}	DAC_A Voltage Input (AV_{SS} to V_{DD})
8	14	V_{OUTA}	DAC_A Output

3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive power supply input. The input power supply is relative to AV_{SS} and can range from 2.7V to 5.5V. A decoupling capacitor on V_{DD} is recommended to achieve maximum performance.

3.2 Chip Select ($\overline{CS}$)

$\overline{CS}$ is the chip select input, which requires an active-low signal to enable serial clock and data functions.

3.3 Serial Clock Input (SCK)

SCK is the SPI compatible serial clock input.

3.4 Serial Data Input (SDI)

SDI is the SPI compatible serial data input.

3.5 Latch DAC Input ($\overline{LDAC}$)

$\overline{LDAC}$ (the latch DAC syncronization input) transfers the input latch registers to the DAC registers (output latches) when low. Can also be tied low if transfer on the rising edge of $\overline{CS}$ is desired.

3.6 Hardware Shutdown Input ($\overline{SHDN}$)

$\overline{SHDN}$ is the hardware shutdown input that requires an active-low input signal to configure the DACs in their low-power Standby mode.

3.7 DAC_x Outputs (V_{OUTA}, V_{OUTB})

V_{OUTA} and V_{OUTB} are DAC outputs. The DAC output amplifier drives these pins with a range of AV_{SS} to V_{DD}.

3.8 DAC_X Voltage Reference Inputs (V_{REFA}, V_{REFB})

V_{REFA} and V_{REFB} are DAC voltage reference inputs. The analog signal on these pins is utilized to set the reference voltage on the string DAC. The input signal can range from AV_{SS} to V_{DD}.

3.9 Analog Ground (AV_{SS})

AV_{SS} is the analog ground pin.

4.0 GENERAL OVERVIEW

The MCP492X devices are voltage output string DACs. These devices include input amplifiers, rail-to-rail output amplifiers, reference buffers, shutdown and reset-management circuitry. Serial communication conforms to the SPI protocol. The MCP492X operates from 2.7V to 5.5V supplies.

The coding of these devices is straight binary and the ideal output voltage is given by Equation 4-1, where *G* is the selected gain (1x or 2x), D_N represents the digital input value and *n* represents the number of bits of resolution (n = 12).

EQUATION 4-1: LSB SIZE

$$V_{OUT} = \frac{V_{REF} G D_N}{2^n}$$

1 LSB is the ideal voltage difference between two successive codes. Table 4-1 illustrates how to calculate LSB.

TABLE 4-1: LSB SIZES

Device	V_{REF}, GAIN	LSB SIZE
MCP492X	External V_{REF}, 1x	V_{REF}/4096
MCP492X	External V_{REF}, 2x	2 V_{REF}/4096

4.0.1 INL ACCURACY

INL error for these devices is the maximum deviation between an actual code transition point and its corresponding ideal transition point once offset and gain errors have been removed. These endpoints are from 0x000 to 0xFFF. Refer to Figure 4-1.

Positive INL means transition(s) later than ideal. Negative INL means transition(s) earlier than ideal.

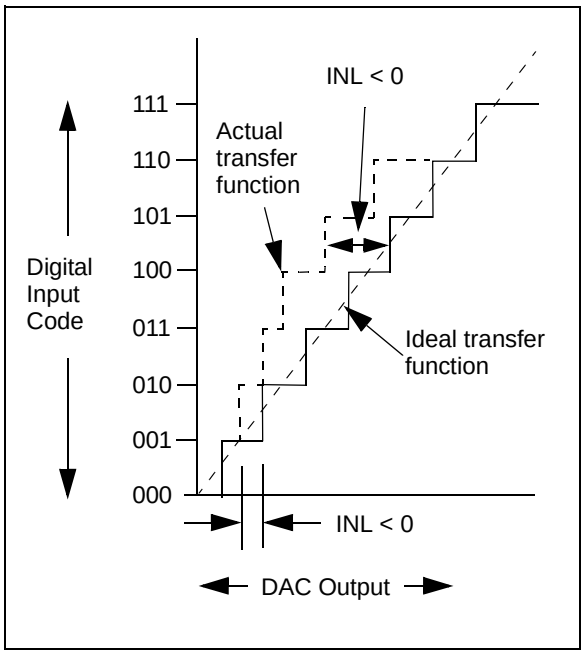


FIGURE 4-1: *INL Accuracy.*

4.0.2 DNL ACCURACY

DNL error is the measure of variations in code widths from the ideal code width. A DNL error of zero would imply that every code is exactly 1 LSB wide.

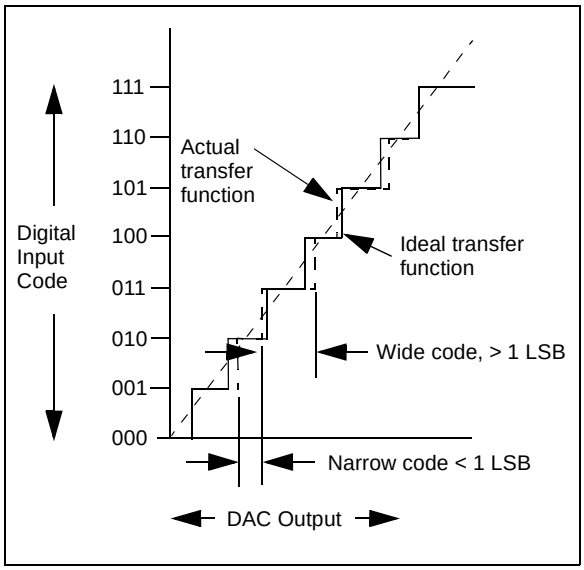


FIGURE 4-2: *DNL Accuracy.*

4.0.3 OFFSET ERROR

Offset error is the deviation from zero voltage output when the digital input code is zero.

4.0.4 GAIN ERROR

Gain error is the deviation from the ideal output, V_{REF}– 1 LSB, excluding the effects of offset error.

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4.1 Circuit Descriptions

4.1.1 OUTPUT AMPLIFIERS

The DACs' outputs are buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to **Section 1.0 "Electrical Characteristics"** for range and load conditions.

In addition to resistive load driving capability, the amplifier will also drive high capacitive loads without oscillation. The amplifiers' strong outputs allow V_{OUT} to be used as a programmable voltage reference in a system.

Selecting a gain of 2 reduces the bandwidth of the amplifier in Multiplying mode. Refer to **Section 1.0 "Electrical Characteristics"** for the Multiplying mode bandwidth for given load conditions.

4.1.1.1 Programmable Gain Block

The rail-to-rail output amplifier has configurable gain allowing optimal full-scale outputs for differing voltage reference inputs. The output amplifier gain has two selections, a gain of 1 V/V ($\overline{GA}$ = 1) or a gain of 2 V/V ($\overline{GA}$ = 0).

The output range is ideally 0.000V to 4095/4096 * V_{REF} when G = 1, and 0.000 to 4095/4096 * V_{REF} when G = 2. The default value for this bit is a gain of 2, yielding an ideal full-scale output of 0.000V to 4.096V when utilizing a 2.048V V_{REF}. Note that the near rail-to-rail CMOS output buffer's ability to approach AV_{SS} and V_{DD} establish practical range limitations. The output swing specification in **Section 1.0 "Electrical Characteristics"** defines the range for a given load condition.

4.1.2 VOLTAGE REFERENCE AMPLIFIERS

The input buffer amplifiers for the MCP492X devices provide low offset voltage and low noise. A configuration bit for each DAC allows the V_{REF} input to bypass the input buffer amplifiers, achieving a Buffered or Unbuffered mode. The default value for this bit is unbuffered. Buffered mode provides a very high input impedance, with only minor limitations on the input range and frequency response. Unbuffered mode provides a wide input range (0V to V_{DD}), with a typical input impedance of 165 kΩ w/7 pF.

4.1.3 POWER-ON RESET CIRCUIT

The Power-On Reset (POR) circuit ensures that the DACs power-up with $\overline{SHDN}$ = 0 (high-impedance). The devices will continue to have a high-impedance output until a valid write command is performed to either of the DAC registers and the $\overline{LDAC}$ pin meets the input low threshold.

If the power supply voltage is less than the POR threshold (V_{POR} = 2.0V, typical), the DACs will be held in their reset state. They will remain in that state until V_{DD} > V_{POR} and a subsequent write command is received.

Figure 4-3 shows a typical power supply transient pulse and the duration required to cause a reset to occur, as well as the relationship between the duration and trip voltage. A 0.1 µF decoupling capacitor mounted as close as possible to the V_{DD} pin provides additional transient immunity.

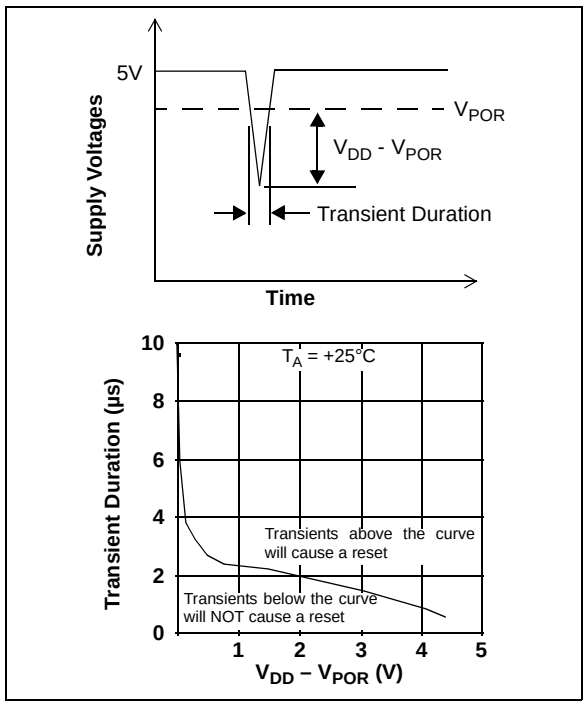


FIGURE 4-3: *Typical Transient Response.*

4.1.4 SHUTDOWN MODE

Shutdown mode can be entered by using either hardware or software commands. The hardware pin ($\overline{SHDN}$) is only available on the MCP4922. During Shutdown mode, the supply current is isolated from most of the internal circuitry. The serial interface remains active, thus allowing a write command to bring the device out of Shutdown mode. When the output amplifiers are shut down, the feedback resistance (typically 500 kΩ) produces a high-impedance path to AV_{SS}. The device will remain in Shutdown mode until the $\overline{SHDN}$ pin is brought high and a write command with $\overline{SD}$ = 1 is latched into the device. When a DAC is changed from Shutdown to Active mode, the output settling time takes < 10 µs, but greater than the standard Active mode settling time (4.5 µs).

5.0 SERIAL INTERFACE

5.1 Overview

The MCP492X family is designed to interface directly with the Serial Peripheral Interface (SPI) port, available on many microcontrollers, and supports Mode 0,0 and Mode 1,1. Commands and data are sent to the device via the SDI pin, with data being clocked-in on the rising edge of SCK. The communications are unidirectional and, thus, data cannot be read out of the MCP492X. The $\overline{CS}$ pin must be held low for the duration of a write command. The write command consists of 16 bits and is used to configure the DAC's control and data latches. Register 5-1 details the input registers used to configure and load the DAC_A and DAC_B registers. Refer to Figure 1-1 and **Section 1.0 "Electrical Characteristics"** AC Electrical Characteristics table for detailed input and output timing specifications for both Mode 0,0 and Mode 1,1 operation.

5.2 Write Command

The write command is initiated by driving the $\overline{CS}$ pin low, followed by clocking the four configuration bits and the 12 data bits into the SDI pin on the rising edge of SCK. The $\overline{CS}$ pin is then raised, causing the data to be latched into the selected DAC's input registers. The MCP492X utilizes a double-buffered latch structure to allow both DAC_A's and DAC_B's outputs to be syncronized with the $\overline{LDAC}$ pin, if desired. Upon the $\overline{LDAC}$ pin achieving a low state, the values held in the DAC's input registers are transferred into the DACs' output registers. The outputs will transition to the value and held in the DAC_X register.

All writes to the MCP492X are 16-bit words. Any clocks past 16 will be ignored. The most significant four bits are configuration bits. The remaining 12 bits are data bits. No data can be transferred into the device with $\overline{CS}$ high. This transfer will only occur if 16 clocks have been transferred into the device. If the rising edge of $\overline{CS}$ occurs prior, shifting of data into the input registers will be aborted.

REGISTER 5-1: WRITE COMMAND REGISTER

Upper Half:							
W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x
$\overline{A}$/B	BUF	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8
bit 15							bit 8

Lower Half:							
W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
D7	D6	D5	D4	D3	D2	D1	D0
bit 7							bit 0

bit 15 **$\overline{A}$/B:** DAC_A or DAC_B Select bit
1 = Write to DAC_B
0 = Write to DAC_A

bit 14 **BUF:** V_{REF} Input Buffer Control bit
1 = Buffered
0 = Unbuffered

bit 13 **$\overline{GA}$:** Output Gain Select bit
1 = 1x ($V_{OUT} = V_{REF} * D/4096$)
0 = 2x ($V_{OUT} = 2 * V_{REF} * D/4096$)

bit 12 **$\overline{SHDN}$:** Output Power Down Control bit
1 = Output Power Down Control bit
0 = Output buffer disabled, Output is high impedance

bit 11-0 **D11:D0:** DAC Data bits
12 bit number "D" which sets the output value. Contains a value between 0 and 4095.

Legend			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

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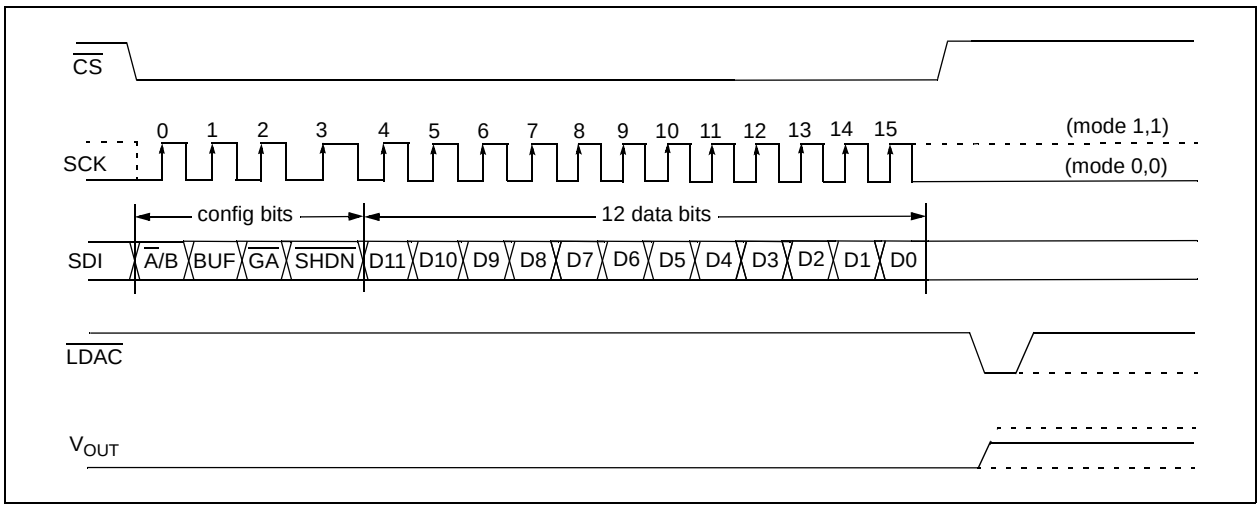


FIGURE 5-1: *Write Command.*

6.0 TYPICAL APPLICATIONS

Note:	At the time of this data sheet's release, circuit examples had not completed testing. Your results may vary.

The MCP492X devices are general purpose DACs intended to be used in applications where a precision, low-power DAC with moderate bandwidth is required.

Applications generally suited for the MCP492X devices include:

- Set Point or Offset Trimming
- Sensor Calibration
- Digitally-Controlled Multiplier/Divider
- Portable Instrumentation (Battery Powered)
- Motor Feedback Loop Control

6.1 Digital Interface

The MCP492X utilizes a 3-wire syncronous serial protocol to transfer the DACs' setup and output values from the digital source. The serial protocol can be interfaced to SPI™ or Microwire peripherals common on many microcontrollers, including Microchip's PICmicro® MCUs & dsPIC™ DSC family of microcontrollers. In addition to the three serial connections ($\overline{CS}$, SCK and SDI), the $\overline{LDAC}$ signal syncronizes when the serial settings are latched into the DAC's output from the serial input latch. Figure 6-1 illustrates the required connections. Note that $\overline{LDAC}$ is active-low. If desired, this input can be tied low to reduce the required connections from 4 to 3. Write commands will be latched directly into the output latch when a valid 16 clock transmission has been received and $\overline{CS}$ has been raised.

6.2 Power Supply Considerations

The typical application will require a by-pass capacitor in order to filter high-frequency noise. The noise can be induced onto the power supply's traces or as a result of changes on the DAC's output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 6-1 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close to the device power pin (V_{DD}) as possible (within 4 mm).

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, AV_{DD} and AV_{SS} should reside on the analog plane.

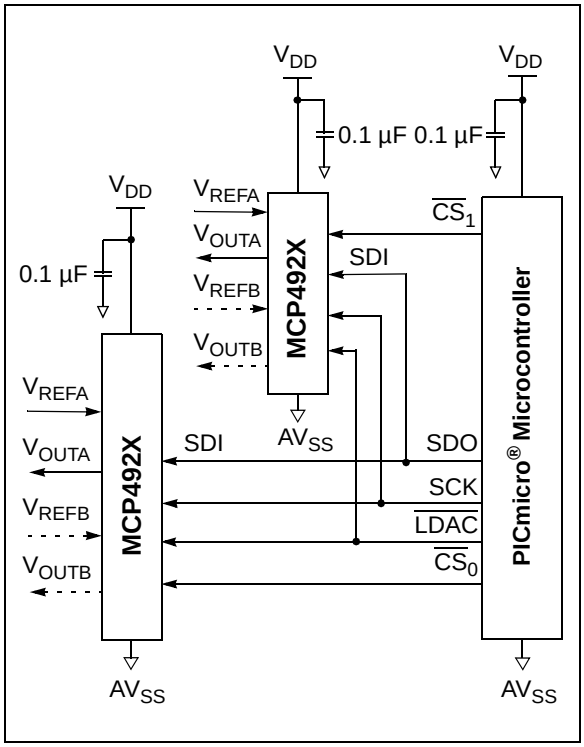


FIGURE 6-1: *Typical Connection Diagram.*

6.3 Layout Considerations

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP492X's performance. Careful board layout will minimize these effects and increase the signal-to-noise ratio (SNR). Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

Breadboards and wire-wrapped boards are not recommended if low noise is desired.

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6.4 Single-Supply Operation

The MCP492X is a rail-to-rail (R-R) input and output DAC designed to operate with a V_{DD} range of 2.7V to 5.5V. Its output amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of an external buffer for most applications.

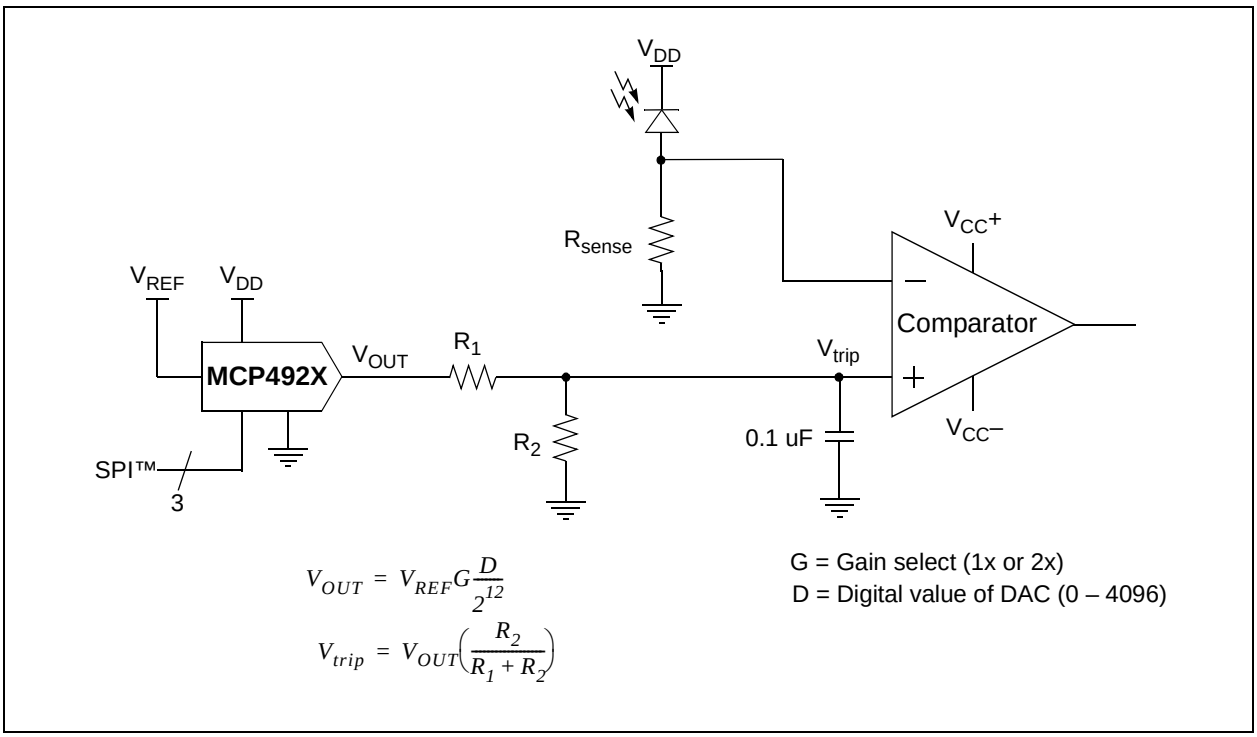
6.4.1 DC SET POINT OR CALIBRATION

A common application for a DAC with the MCP492X's performance is digitally-controlled set points and/or calibration of variable parameters, such as sensor offset or slope. 12-bit resolution provides 4096 output steps. If a 4.096V V_{REF} is provided, an LSB would represent 1 mV of resolution. If a smaller output step size is desired, the output range would need to be reduced.

6.4.1.1 Decreasing The Output Step Size

If the output range is reduced relative to AV_{SS}, simply reducing V_{REF} will reduce the magnitude of each output step. If the application is calibrating the threshold of a diode, transistor or resistor tied to AV_{SS} or V_{REF}, a theshold range of 0.8V may be desired to provide 200 µV resolution. Two common methods to achieve a 0.8V range is to either reduce V_{REF} to 0.82V or use a voltage divider on the DAC's output. If a V_{REF} is available with the desired output value, using that V_{REF} is an option. Occasionally, when using a low-voltage V_{REF}, the noise floor causes SNR error that is intolerable. The voltage divider method provides some advantages when V_{REF} needs to be very low or when the desired output voltage is not available. In this case, a larger value V_{REF} is used while two resistors scale the output range down to the precise desired level. Using a common V_{REF} output has availability and cost advantages. Example 6-1 illustrates this concept. Note that the voltage divider can be connected to AV_{SS} or V_{REF}, depending on the application's requirements.

The MCP492X's low, ±0.75 (max.) DNL performance is critical to meeting calibration accuracy in production.



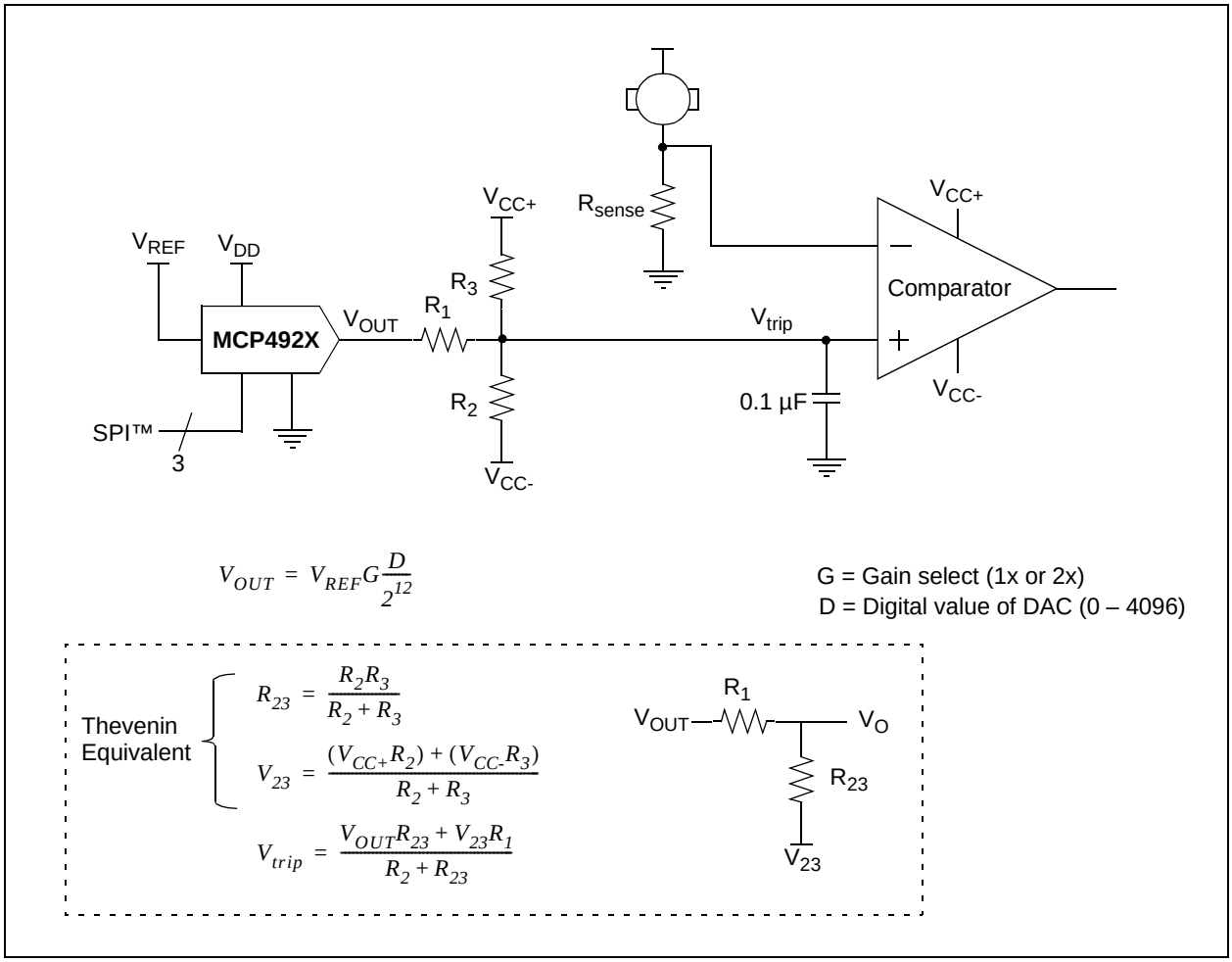
EXAMPLE 6-1: *Set Point or Threshold Calibration.*

6.4.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, rarely does the sensor utilize the entire output range of the DAC. If the LSB size is adequate to meet the application’s accuracy needs, then the resolution is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near V_{REF} or AV_{SS}, then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Example 6-2 and Example 6-4 illustrates this concept.

The MCP492X’s low, ±0.75 (max.) DNL performance is critical to meet calibration accuracy in production.



$$V_{OUT} = V_{REF} G \frac{D}{2^{12}}$$

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{(V_{CC+} R_2) + (V_{CC-} R_3)}{R_2 + R_3}$$

$$V_{trip} = \frac{V_{OUT} R_{23} + V_{23} R_1}{R_2 + R_{23}}$$

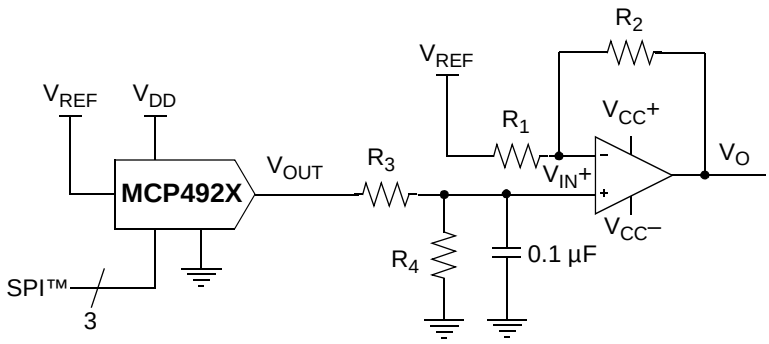
EXAMPLE 6-2: *Single-Supply “Window” DAC.*

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6.5 Bipolar Operation

Bipolar operation is achievable using the MCP492X by using an external operational amplifier (op amp). This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Example 6-3 illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R4 can be tied to V_{REF}, instead of AV_{SS}, if a higher offset is desired. Note that a pull-up to V_{REF} could be used, instead of R_4, if a higher offset is desired.



$$V_{OUT} = V_{REF} G \frac{D}{2^{12}}$$

$$V_{IN+} = \frac{V_{OUT} R_4}{R_3 + R_4}$$

$$V_O = V_{IN+}\left(1 + \frac{R_2}{R_1}\right) - V_{REF}\left(\frac{R_2}{R_1}\right)$$

G = Gain select (1x or 2x)
D = Digital value of DAC (0 – 4096)

EXAMPLE 6-3: *Digitally-Controlled Bipolar Voltage Source.*

6.5.1 DESIGN A BIPOLAR DAC USING EXAMPLE 6-3

An output step magnitude of 1 mV with an output range of ±2.05V is desired for a particular application.

1. Calculate the range: +2.05V – (-2.05V) = 4.1V.
2. Calculate the resolution needed:
   4.1V/1 mV = 4100

   Since 2^{12} = 4096, 12-bit resolution is desired.
3. The amplifier gain (R_2/R_1), multiplied by V_{REF}, must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values (R_1+R_2), the V_{REF} source needs to be determined first. If a V_{REF} of 4.1V is used, solve for the gain by setting the DAC to 0, knowing that the output needs to be -2.05V. The equation can be simplified to:

$$\frac{-R_2}{R_1} = \frac{-2.05}{V_{REF}} = \frac{-2.05}{4.1} \qquad \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

4. Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + 0.5V_{REF}}{1.5V_{REF}} = \frac{2}{3}$$

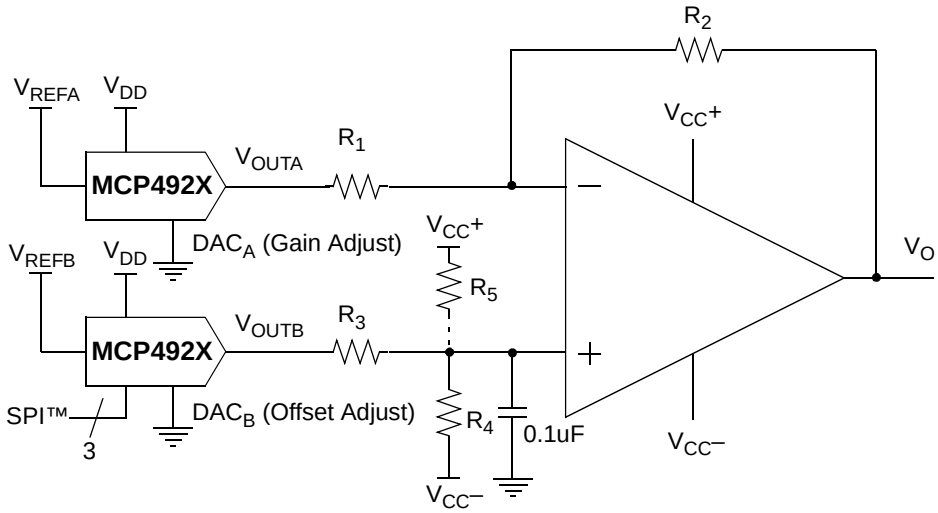
If R_4 = 20 kΩ, then R_3 = 10 kΩ

6.6 Selectable Gain and Offset Bipolar Voltage Output Using A Dual DAC

In some applications, precision digital control of the output range is desirable. Example 6-4 illustrates how to use the MCP4922 to achieve this in a bipolar or single-supply application.

This circuit is typically used in Multiplier mode and is ideal for linearizing a sensor whose slope and offset varies. Refer to **Section 6.9 "Using Multiplier Mode"** for more information on Multiplier mode.

The equation to design a bipolar "window" DAC would be utilized if R_3, R_4 and R_5 are populated.



$$V_{OUTB} = (V_{REFB}G_B)\frac{D_B}{2^{12}} \qquad V_{OUTA} = (V_{REFA}G_A)\frac{D_A}{2^{12}}$$

$$V_{IN+} = \frac{V_{OUTB}R_4 + V_{CC-}R_3}{R_3 + R_4}$$

$$V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{OUTA}\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

AV_{SS} = GND

G = Gain select (1x or 2x)

D = Digital value of DAC (0 – 4096)

Bipolar "Window" DAC using R_4 and R_5

Thevenin Equivalent

$$V_{45} = \frac{V_{CC+}R_4 + V_{CC-}R_5}{R_4 + R_5} \qquad R_{45} = \frac{R_4R_5}{R_4 + R_5}$$

$$V_{IN+} = \frac{V_{OUTB}R_{45} + V_{45}R_3}{R_3 + R_{45}} \qquad V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{OUTA}\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

EXAMPLE 6-4: *Bipolar Voltage Source With Selectable Gain and Offset.*

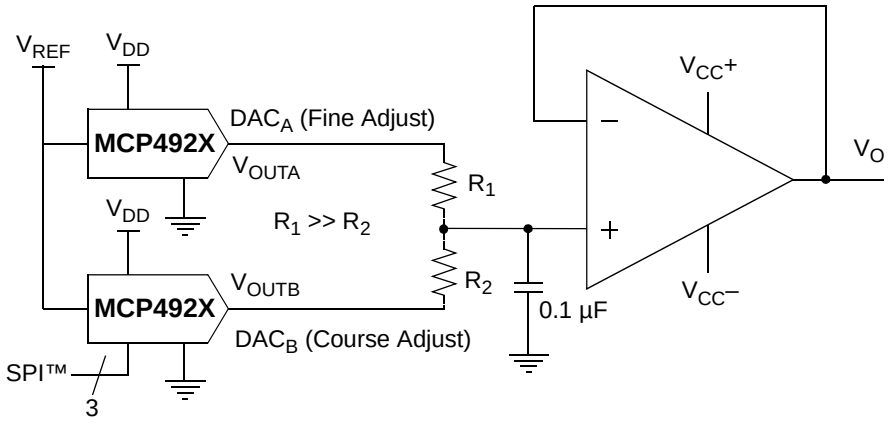
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6.7 Designing A Double-Precision DAC Using A Dual DAC

Example 6-5 illustrates how to design a single-supply voltage output capable of up to 24-bit resolution from a dual 12-bit DAC. This design is simply a voltage divider with a buffered output.

As an example, if a similar application to the one developed in **Section 6.5.1 "Design a bipolar dac using Example 6-3"** required a resolution of 1 µV instead of 1 mV and a range of 0V to 4.1V, then 12-bit resolution would not be adequate.

1. Calculate the resolution needed: 4.1V/1uV = 4.1e06. Since 2^{22} = 4.2e06, 22-bit resolution is desired. Since DNL = ±0.75 LSB, this design can be attempted with the MCP492X.
2. Since DAC_B's V_{OUTB} has a resolution of 1 mV, its output only needs to be "pulled" 1/1000 to meet the 1 µV target. Dividing V_{OUTA} by 1000 would allow the application to compensate for DAC_B's DNL error.
3. If R_2 is 100Ω, then R_1 needs to be 100 kΩ.
4. The resulting transfer function is not perfectly linear, as shown in the equation of Example 6-5.



$$V_{OUTA} = V_{REFA} G_A \frac{D_A}{2^{12}} \qquad V_{OUTB} = V_{REFB} G_B \frac{D_B}{2^{12}}$$

G = Gain select (1x or 2x)
D = Digital value of DAC (0 – 4096)

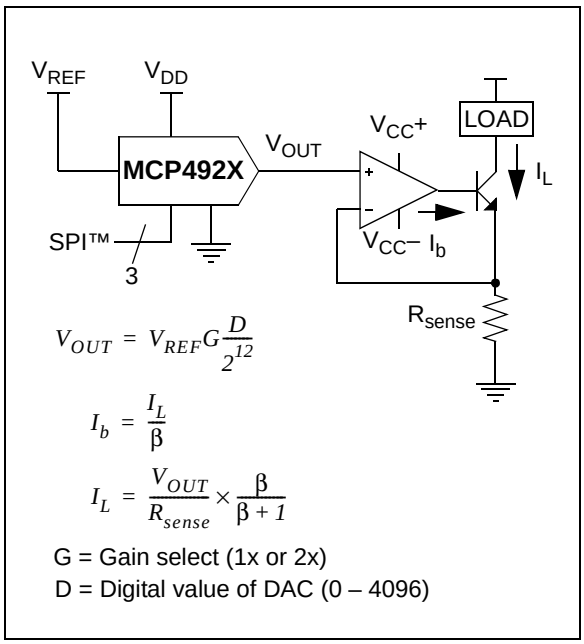
$$V_O = \frac{V_{OUTA} R_2 + V_{OUTB} R_1}{R_1 + R_2}$$

EXAMPLE 6-5: *Simple, Double-Precision DAC.*

6.8 Building A Programmable Current Source

Example 6-6 illustrates a variation on a voltage follower design where a sense resistor is used to convert the DAC's voltage output into a digitally-selectable current source.

Adding the resistor network from Example 6-2 would be advantageous in this application. The smaller R_{sense} is, the less power dissipated across it. However, this also reduces the resolution that the current can be controlled with. The voltage divider, or "window", DAC configuration would allow the range to be reduced, thus increasing resolution around the range of interest. When working with very small sensor voltages, plan on eliminating the amplifier's offset error by storing the DAC's setting under known sensor conditions.



$$V_{OUT} = V_{REF} G \frac{D}{2^{12}}$$

$$I_b = \frac{I_L}{\beta}$$

$$I_L = \frac{V_{OUT}}{R_{sense}} \times \frac{\beta}{\beta + 1}$$

G = Gain select (1x or 2x)
D = Digital value of DAC (0 – 4096)

EXAMPLE 6-6: *Digitally-Controlled Current Source.*

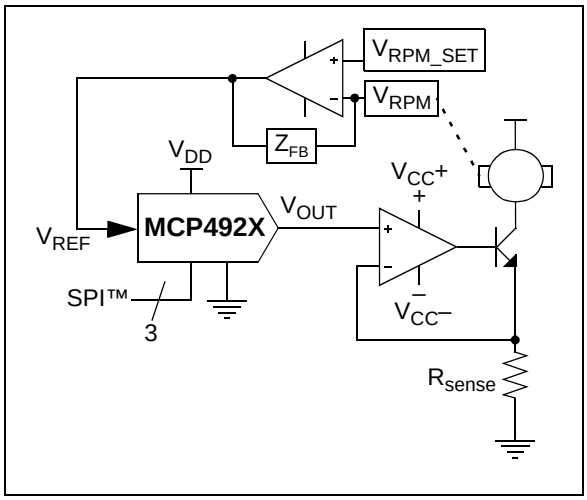
6.9 Using Multiplier Mode

The MCP492X is ideally suited for use as a multiplier/ divider in a signal chain. Common applications include: precision programmable gain/attenuator amplifiers and loop controls (motor feedback). The wide input range (0V – V_{DD}) is an Unbuffered mode and near R-R range in Buffered mode: the > 400 kHz bandwidth, selectible 1x/2x gain and its low power consumption give maximum flexibility to meet the application's needs.

To configure the MCP492X in Multiplier mode, connect the input signal to V_{REF} and serially configure the DAC's input buffer, gain and output value. The DAC's output can utilize any of Examples 6-1 to 6-6, depending on the application requirements. Example 6-7 is an illustration of how the DAC can operate in a motor control feedback loop.

If the Gain Select bit is configured for 1x mode ($\overline{GA}$ = 1), the resulting input signal will be attenuated by D/4096. If the Gain Select bit is configured for 2x mode ($\overline{GA}$ = 0), codes < 2048 attenuate the signal, while codes > 2048 gain the signal. $V_{OUT} = V_{IN}$ (D/2048).

A 12-bit DAC provides significantly more gain/attenuation resolution when compared to typical Programmable Gain Amplifiers. Adding an op amp to buffer the output, as illustrated in Examples 6-2 to 6-6, extends the output range and power to meet the precise needs of the application.



EXAMPLE 6-7: *Multiplier Mode.*

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7.0 DEVELOPMENT SUPPORT

7.1 Evaluation & Demonstration Boards

The Mixed Signal PICtail™ Board supports the MCP492X family of devices. Please refer to www.microchip.com for further information on this products capabilities and availability.

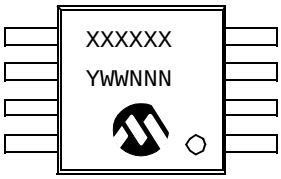
7.2 Application Notes and Tech Briefs

Application notes illustrating the performace and implementation of the MCP492X are planned but currently not released. Please refer to www.microchip.com for further information.

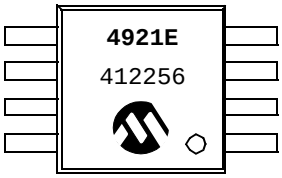
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

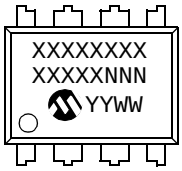
8-Lead MSOP



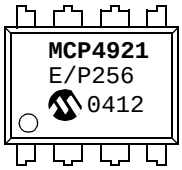
Example:



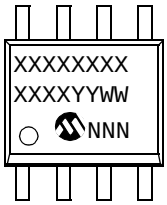
8-Lead PDIP (300 mil)



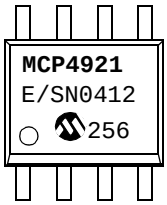
Example:



8-Lead SOIC (150 mil)



Example:



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

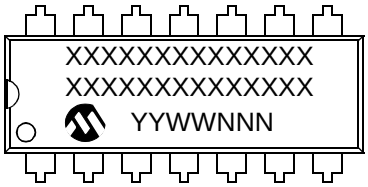
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

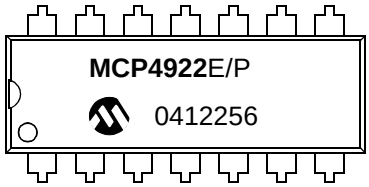
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Package Marking Information (Continued)

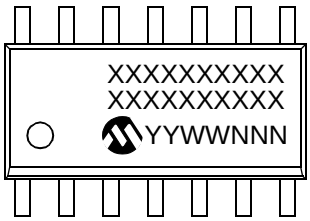
14-Lead PDIP (300 mil) **(MCP4922)**



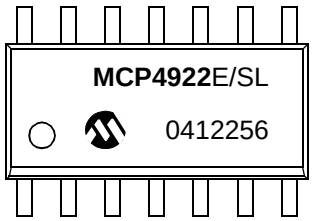
Example:



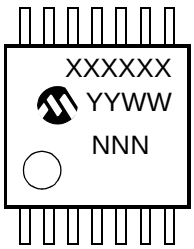
14-Lead SOIC (150 mil) **(MCP4922)**



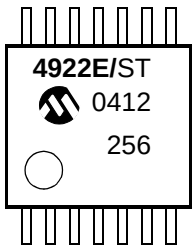
Example:



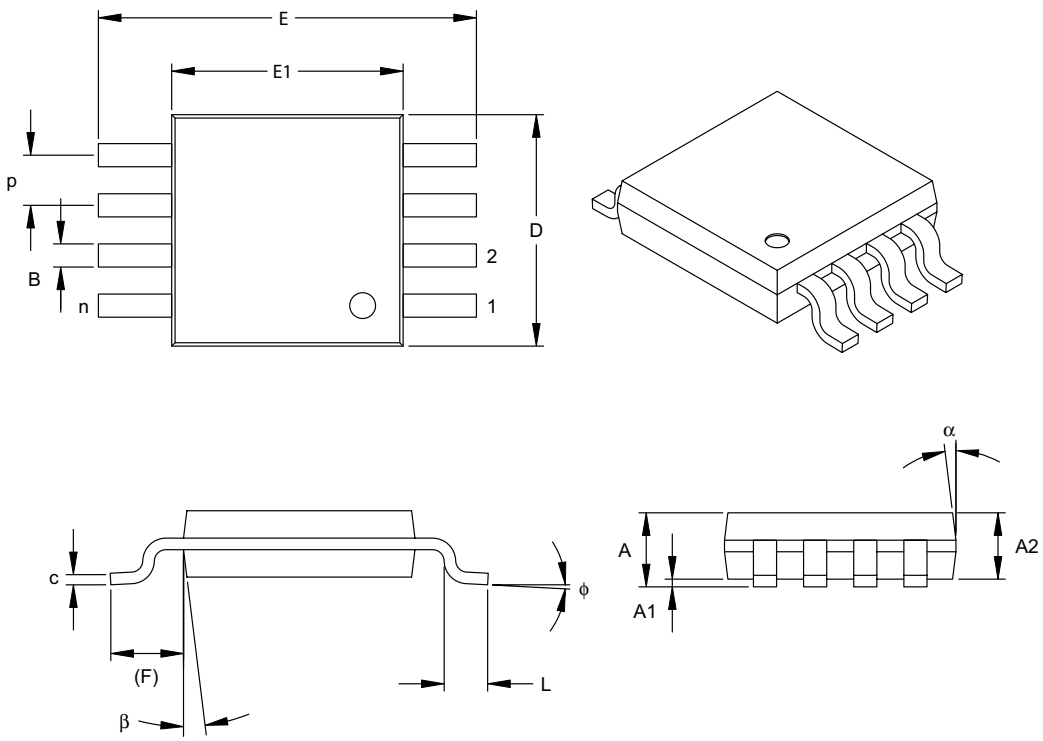
14-Lead TSSOP **(MCP4922)**



Example:



8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

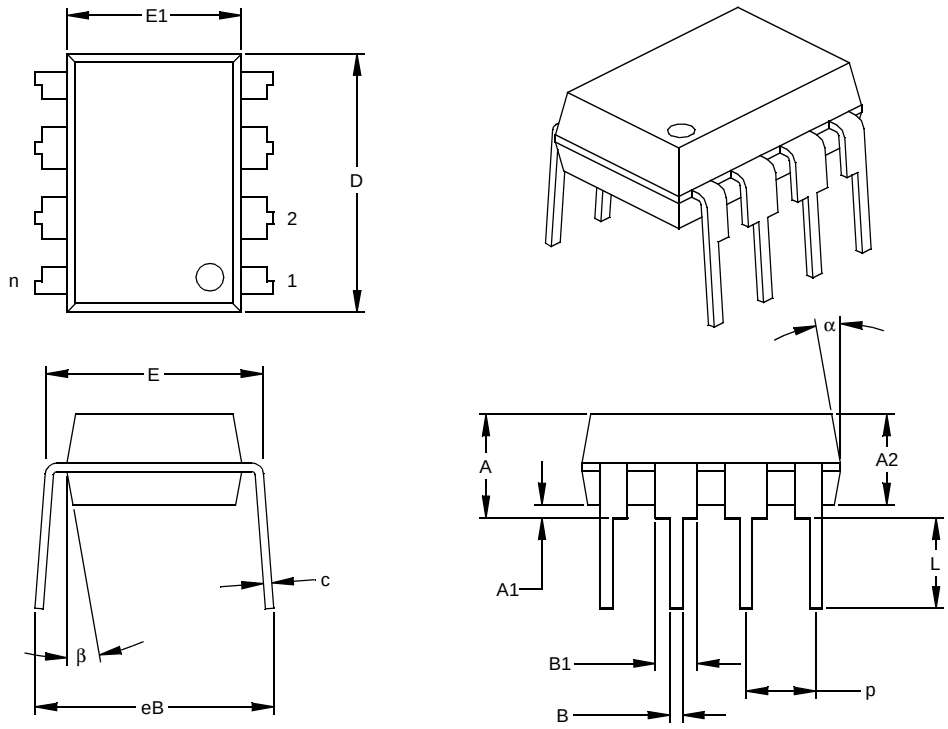
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

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8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

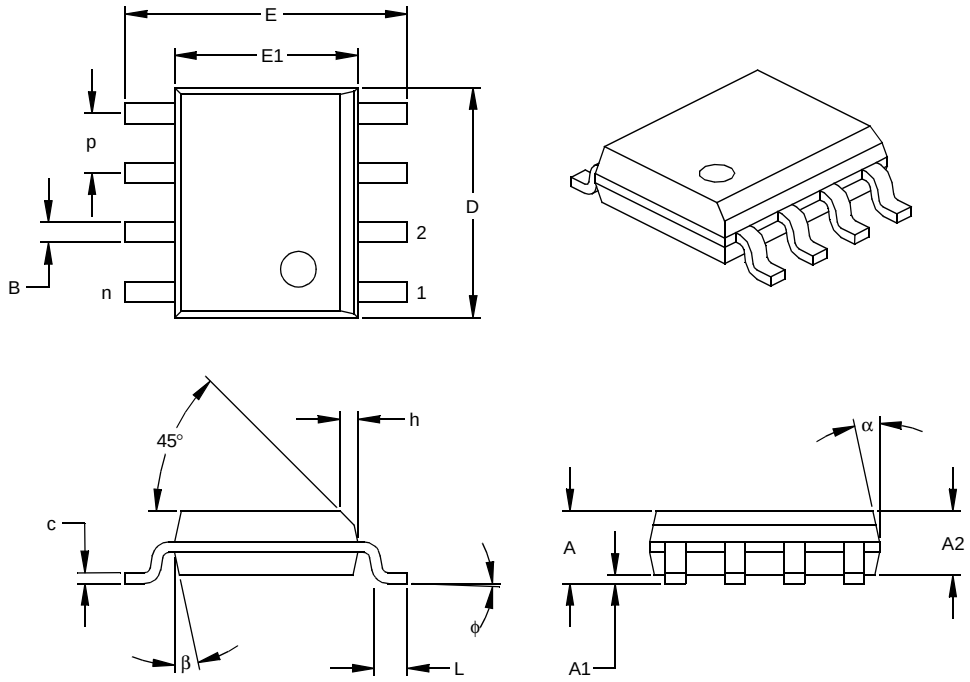


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



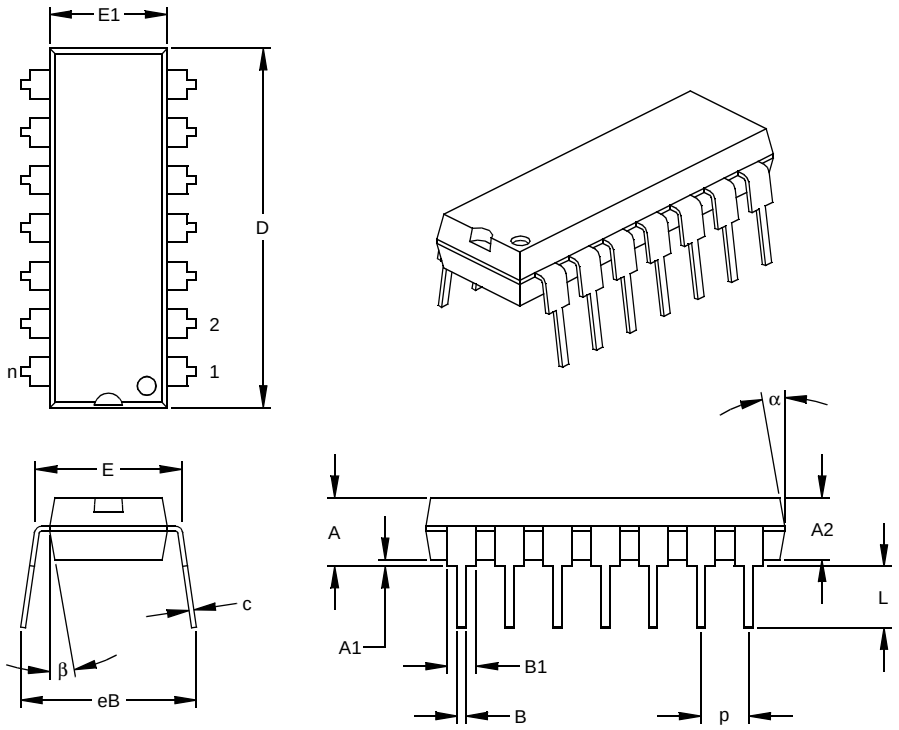
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

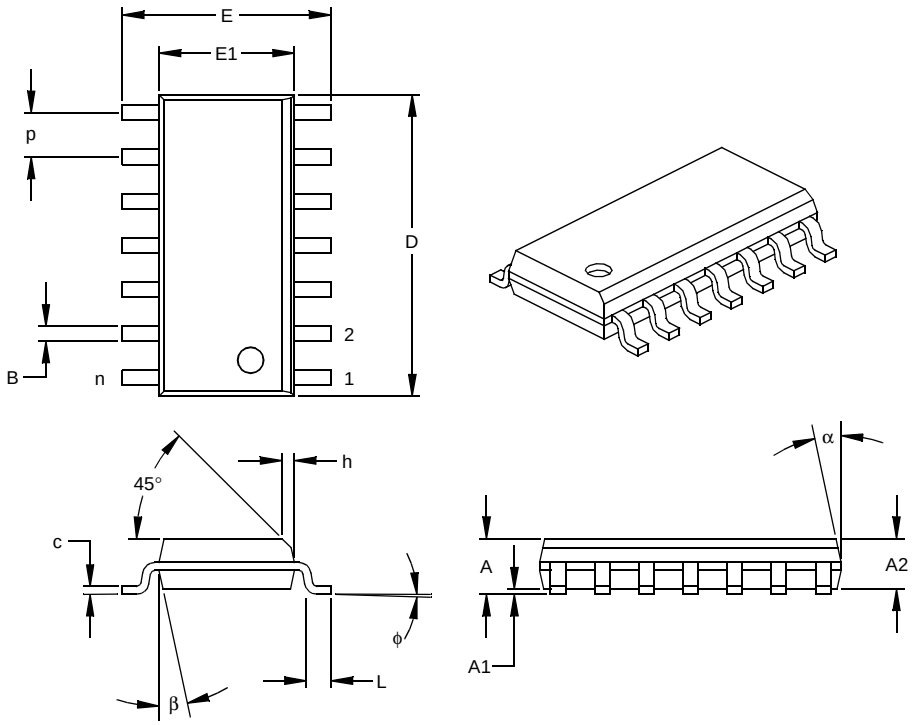


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



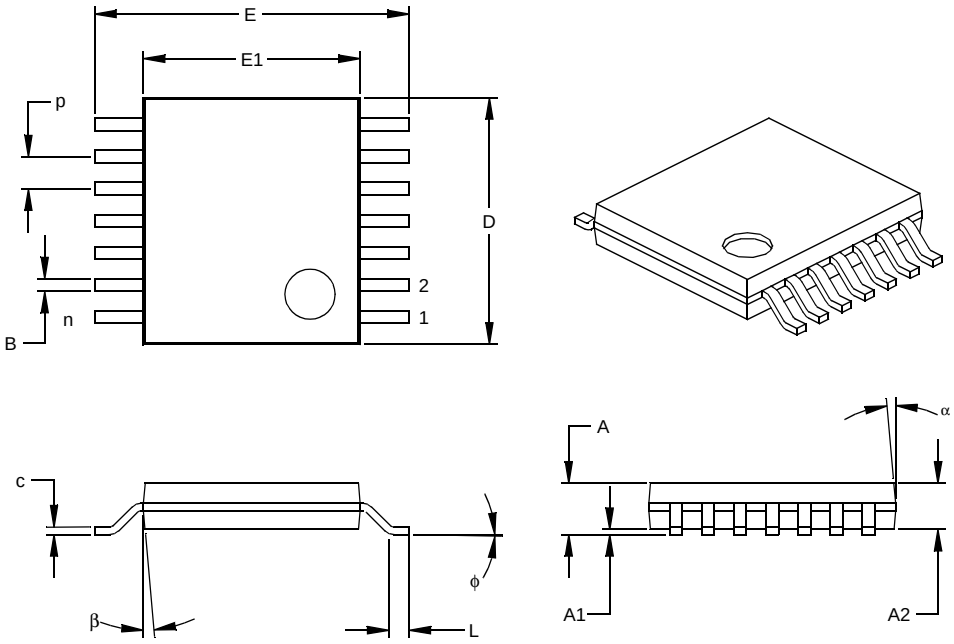
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

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14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP4921:	12-Bit DAC with SPI Interface
	MCP4921T:	12-Bit DAC with SPI Interface (Tape and Reel) (SOIC, MSOP)
	MCP4922:	12-Bit DAC with SPI Interface
	MCP4922T:	12-Bit DAC with SPI Interface (Tape and Reel) (SOIC, MSOP)
Temperature Range:	E =	-40°C to +125°C
Package:	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC, (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a)	MCP4921T-E/SN:	Tape and Reel Extended Temperature, 8LD SOIC package.
b)	MCP4921T-E/MS:	Tape and Reel Extended Temperature, 8LD MSOP package.
c)	MCP4921-E/SN:	Extended Temperature, 8LD SOIC package.
d)	MCP4921-E/MS:	Extended Temperature, 8LD MSOP package.
e)	MCP4921-E/P:	Extended Temperature, 8LD PDIP package.
a)	MCP4922T-E/SL:	Tape and Reel Extended Temperature, 14LD SOIC package.
b)	MCP4922T-E/ST:	Tape and Reel Extended Temperature, 14LD TSSOP package.
c)	MCP4922-E/P:	Extended Temperature, 14LD PDIP package.
d)	MCP4922-E/SL:	Extended Temperature, 14LD SOIC package.
e)	MCP4922-E/ST:	Extended Temperature, 14LD TSSOP package.

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