

xx555 Precision Timers

1 Features

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up to 200 mA
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Fingerprint Biometrics
- Iris Biometrics
- RFID Reader

3 Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
xx555	PDIP (8)	9.81 mm × 6.35 mm
	SOP (8)	6.20 mm × 5.30 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

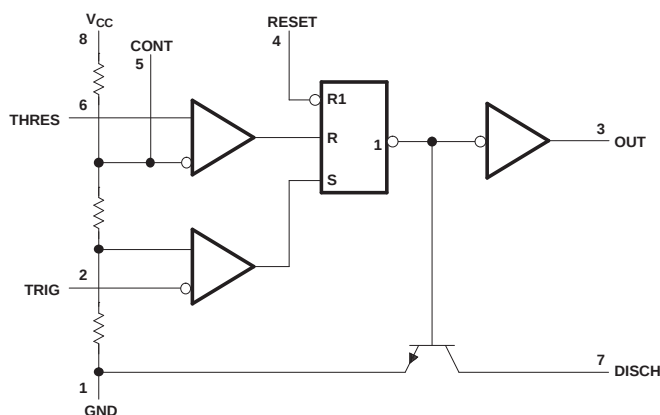


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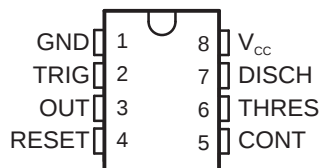
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5 Revision History

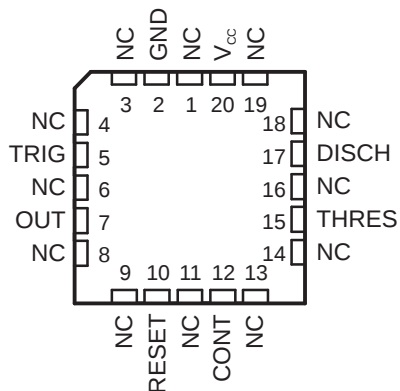
Changes from Revision H (June 2010) to Revision I	Page
• Updated document to new TI enhanced data sheet format.	1
• Deleted Ordering Information table.	1
• Added Military Disclaimer to Features list.	1
• Added Applications.	1
• Added Device Information table.	1
• Moved T_{stg} to Handling Ratings table.	4
• Added DISCH switch on-state voltage parameter.	5
• Added Device and Documentation Support section.	19
• Added ESD warning.	19
• Added Mechanical, Packaging, and Orderable Information section.	19

6 Pin Configuration and Functions

NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)



SE555...FK PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D, P, PS, PW, JG	FK		
	NO.			
CONT	5	12	I/O	Controls comparator thresholds, Outputs 2/3 VCC, allows bypass capacitor connection
DISCH	7	17	O	Open collector output to discharge timing capacitor
GND	1	2	–	Ground
NC		1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	–	No internal connection
OUT	3	7	O	High current timer output signal
RESET	4	10	I	Active low reset input forces output and discharge low.
THRES	6	15	I	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	5	I	Start of timing input. TRIG < ½ CONT sets output high and discharge open
V _{CC}	8	20	–	Input supply voltage, 4.5 V to 16 V. (SE555 maximum is 18 V)

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾			18	V
V _I	Input voltage	CONT, RESET, THRES, TRIG		V _{CC}	V
I _O	Output current			±225	mA
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package		97	°C/W
		P package		85	
		PS package		95	
		PW package		149	
θ _{JC}	Package thermal impedance ⁽⁵⁾⁽⁶⁾	FK package		5.61	°C/W
		JG package		14.5	
T _J	Operating virtual junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1,6 mm (1/16 in) from case for 60 s	JG package		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A) / θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Maximum power dissipation is a function of T_{J(max)}, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is P_D = (T_{J(max)} - T_C) / θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with MIL-STD-883.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	NA555, NE555, SA555	4.5	16	V
		SE555	4.5	18	
V _I	Input voltage	CONT, RESET, THRES, and TRIG		V _{CC}	V
I _O	Output current			±200	mA
T _A	Operating free-air temperature	NA555	-40	105	°C
		NE555	0	70	
		SA555	-40	85	
		SE555	-55	125	

7.4 Electrical Characteristics

 $V_{CC} = 5\text{ V to }15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	$V_{CC} = 15\text{ V}$		9.4	10	10.6	8.8	10	11.2	V
	$V_{CC} = 5\text{ V}$		2.7	3.3	4	2.4	3.3	4.2	
THRES current ⁽¹⁾				30	250		30	250	nA
TRIG voltage level	$V_{CC} = 15\text{ V}$		4.8	5	5.2	4.5	5	5.6	V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	3		6				
	$V_{CC} = 5\text{ V}$		1.45	1.67	1.9	1.1	1.67	2.2	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			1.9				
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	μA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	$T_A = -55^\circ\text{C to }125^\circ\text{C}$				1.1				
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			-0.4	-1		-0.4	-1.5	
DISCH switch off-state current				20	100		20	100	nA
DISCH switch on-state voltage	$V_{CC} = 5\text{ V}$, $I_O = 8\text{ mA}$						0.15	0.4	V
CONT voltage (open circuit)	$V_{CC} = 15\text{ V}$		9.6	10	10.4	9	10	11	V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	9.6		10.4				
	$V_{CC} = 5\text{ V}$		2.9	3.3	3.8	2.6	3.3	4	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	2.9		3.8				
Low-level output voltage	$V_{CC} = 15\text{ V}$, $I_{OL} = 10\text{ mA}$			0.1	0.15		0.1	0.25	V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			0.2				
	$V_{CC} = 15\text{ V}$, $I_{OL} = 50\text{ mA}$			0.4	0.5		0.4	0.75	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			1				
	$V_{CC} = 15\text{ V}$, $I_{OL} = 100\text{ mA}$			2	2.2		2	2.5	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			2.7				
	$V_{CC} = 15\text{ V}$, $I_{OL} = 200\text{ mA}$			2.5			2.5		
	$V_{CC} = 5\text{ V}$, $I_{OL} = 3.5\text{ mA}$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$			0.35				
				0.1	0.2		0.1	0.35	
	$V_{CC} = 5\text{ V}$, $I_{OL} = 5\text{ mA}$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$			0.8				
				0.15	0.25		0.15	0.4	
High-level output voltage	$V_{CC} = 15\text{ V}$, $I_{OH} = -100\text{ mA}$		13	13.3		12.75	13.3		V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	12						
	$V_{CC} = 15\text{ V}$, $I_{OH} = -200\text{ mA}$			12.5			12.5		
	$V_{CC} = 5\text{ V}$, $I_{OH} = -100\text{ mA}$		3	3.3		2.75	3.3		
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	2						
Supply current	Output low, No load	$V_{CC} = 15\text{ V}$		10	12		10	15	mA
		$V_{CC} = 5\text{ V}$		3	5		3	6	
	Output high, No load	$V_{CC} = 15\text{ V}$		9	10		9	13	
		$V_{CC} = 5\text{ V}$		2	4		2	5	

(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of [Figure 12](#). For example, when $V_{CC} = 5\text{ V}$, the maximum value is $R = R_A + R_B \neq 3.4\text{ M}\Omega$, and for $V_{CC} = 15\text{ V}$, the maximum value is $10\text{ M}\Omega$.

7.5 Operating Characteristics

 $V_{CC} = 5\text{ V to }15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval ⁽²⁾	Each timer, monostable ⁽³⁾	$T_A = 25^\circ\text{C}$		0.5	1.5 ⁽⁴⁾		1	3	%
	Each timer, astable ⁽⁵⁾			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable ⁽³⁾	$T_A = \text{MIN to MAX}$		30	100 ⁽⁴⁾		50		ppm/ °C
	Each timer, astable ⁽⁵⁾			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable ⁽³⁾	$T_A = 25^\circ\text{C}$		0.05	0.2 ⁽⁴⁾		0.1	0.5	%/V
	Each timer, astable ⁽⁵⁾			0.15			0.3		
Output-pulse rise time		$C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$		100	200 ⁽⁴⁾		100	300	ns
Output-pulse fall time		$C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$		100	200 ⁽⁴⁾		100	300	ns

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
- (2) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
- (3) Values specified are for a device in a monostable circuit similar to [Figure 9](#), with the following component values: $R_A = 2\text{ k}\Omega$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$.
- (4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (5) Values specified are for a device in an astable circuit similar to [Figure 12](#), with the following component values: $R_A = 1\text{ k}\Omega$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$.

7.6 Typical Characteristics

Data for temperatures below -40°C and above 105°C are applicable for SE555 circuits only.

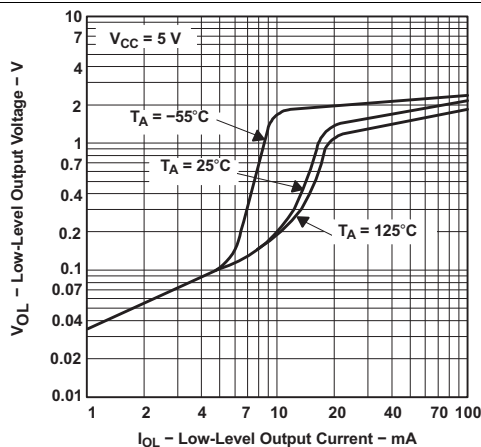


Figure 1. Low-Level Output Voltage vs Low-Level Output Current

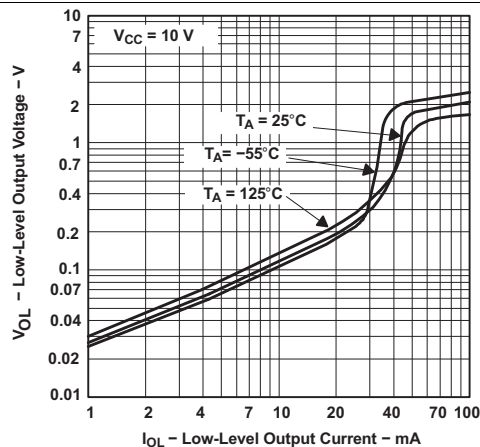


Figure 2. Low-Level Output Voltage vs Low-Level Output Current

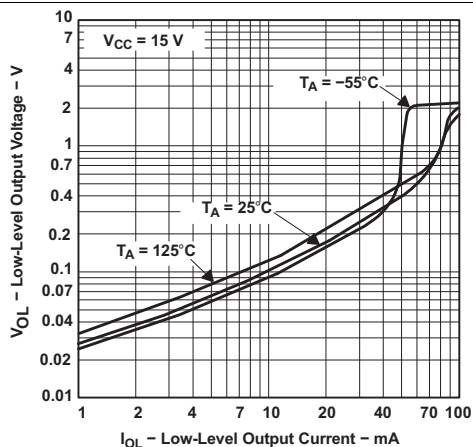


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

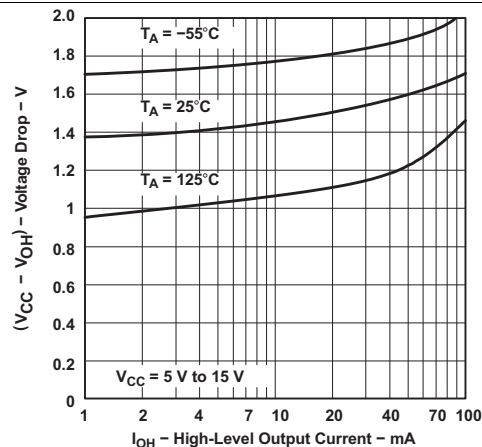


Figure 4. Drop Between Supply Voltage and Output vs High-Level Output Current

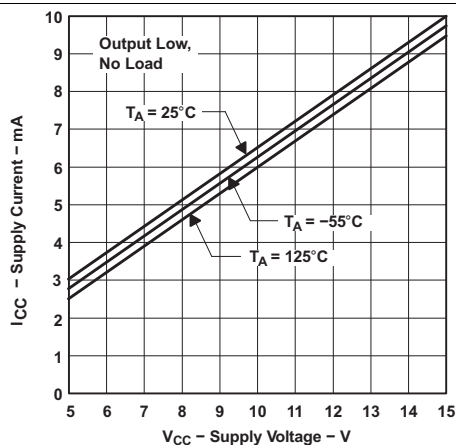


Figure 5. Supply Current vs Supply Voltage

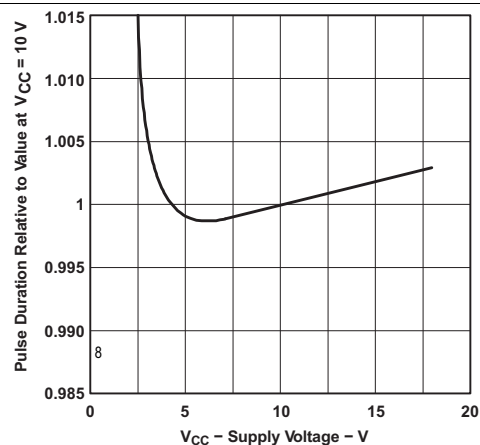


Figure 6. Normalized Output Pulse Duration (Monostable Operation) vs Supply Voltage

Typical Characteristics (continued)

Data for temperatures below -40°C and above 105°C are applicable for SE555 circuits only.

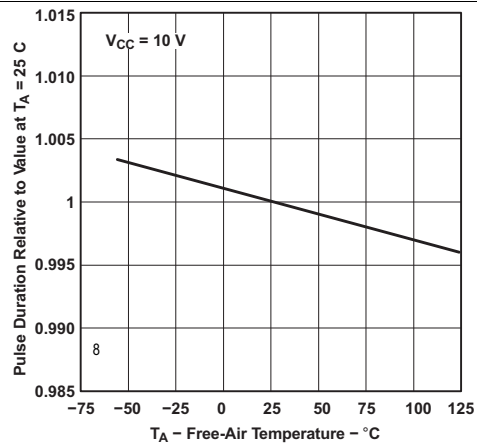


Figure 7. Normalized Output Pulse Duration (Monostable Operation) vs Free-Air Temperature

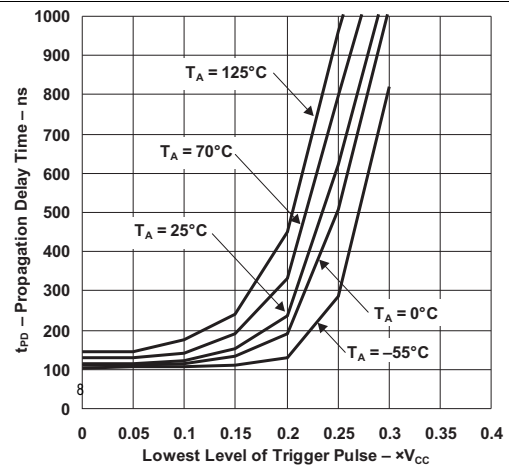
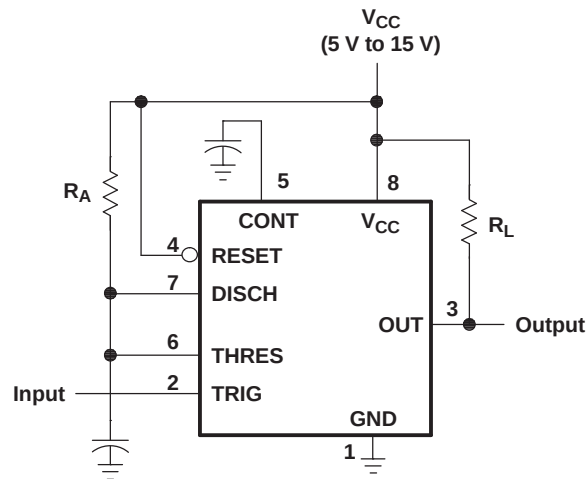


Figure 8. Propagation Delay Time vs Lowest Voltage Level of Trigger Pulse

Feature Description (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10 μs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 μs , which limits the minimum monostable pulse width to 10 μs . Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_A C$. [Figure 11](#) is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC} . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC} .

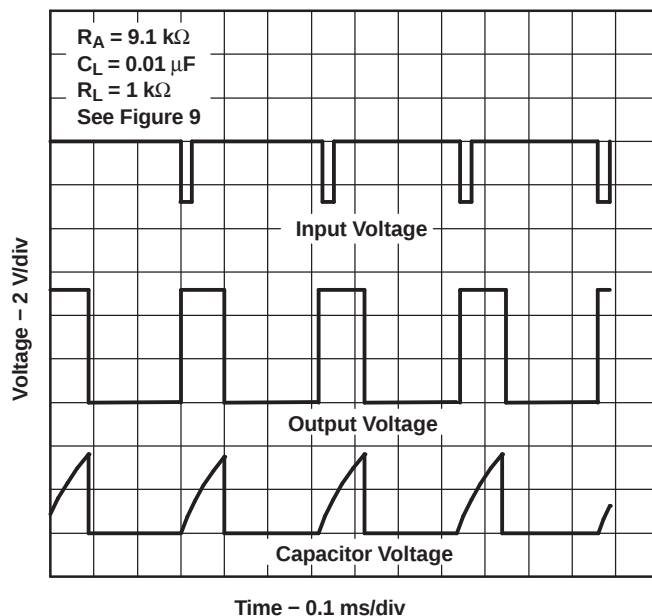


Figure 10. Typical Monostable Waveforms

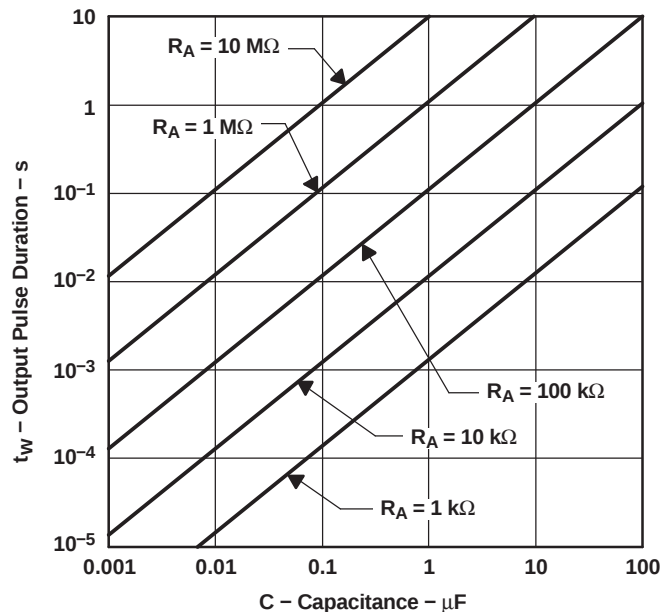


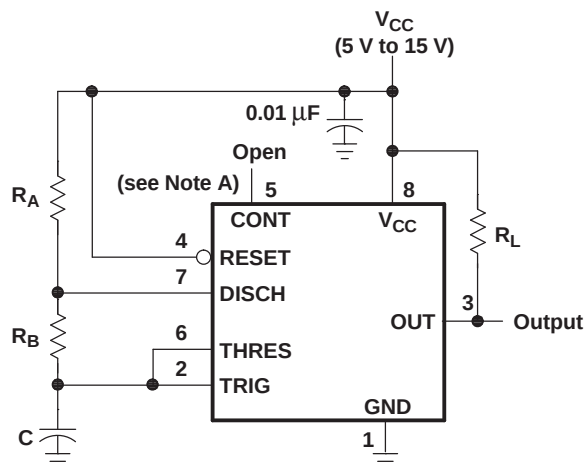
Figure 11. Output Pulse Duration vs Capacitance

Feature Description (continued)

8.3.2 A-stable Operation

As shown in Figure 12, adding a second resistor, R_B , to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

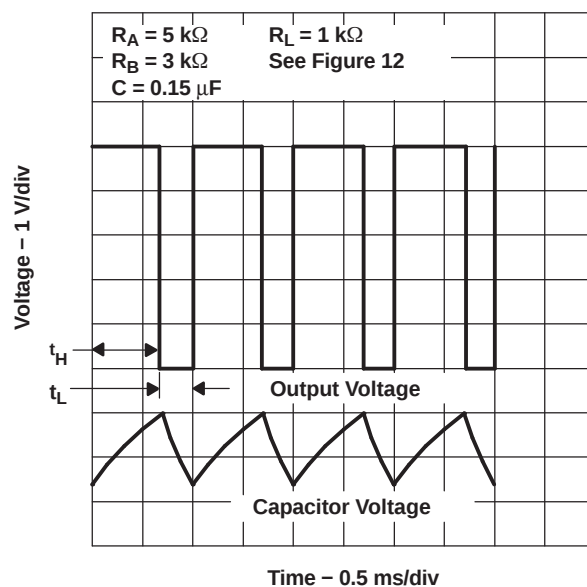


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Feature Description (continued)

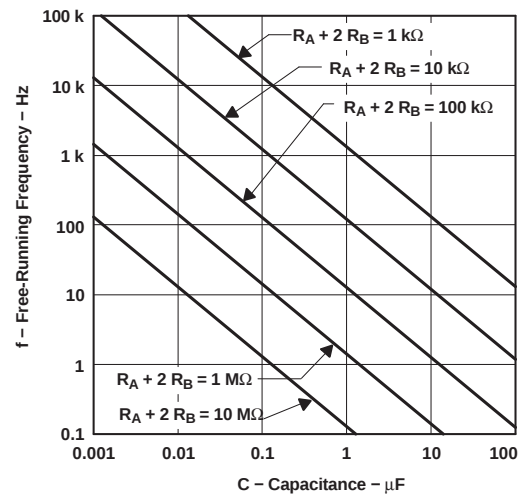


Figure 14. Free-Running Frequency

8.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of [Figure 9](#) can be made to operate as a frequency divider. [Figure 15](#) shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.

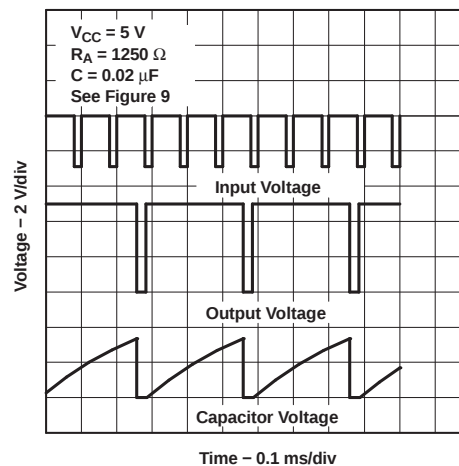


Figure 15. Divide-by-Three Circuit Waveforms

8.4 Device Functional Modes

Table 1. Function Table

RESET	TRIGGER VOLTAGE ⁽¹⁾	THRESHOLD VOLTAGE ⁽¹⁾	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V _{CC}	Irrelevant	High	Off
High	>1/3 V _{CC}	>2/3 V _{CC}	Low	On
High	>1/3 V _{CC}	<2/3 V _{CC}	As previously established	

(1) Voltage levels shown are nominal.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

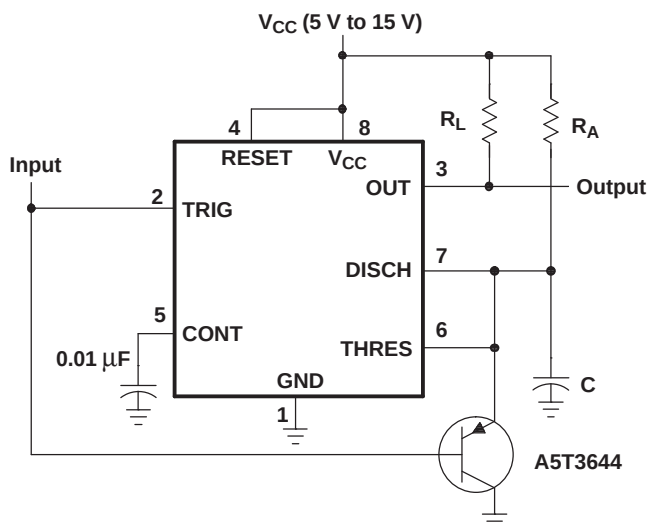
9.1 Application Information

The xx555 timer devices use resistor and capacitor charging delay to provide a programmable time delay or operating frequency. This section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Missing-Pulse Detector

The circuit shown in [Figure 16](#) can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in [Figure 17](#).



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 16. Circuit for Missing-Pulse Detector

9.2.1.1 Design Requirements

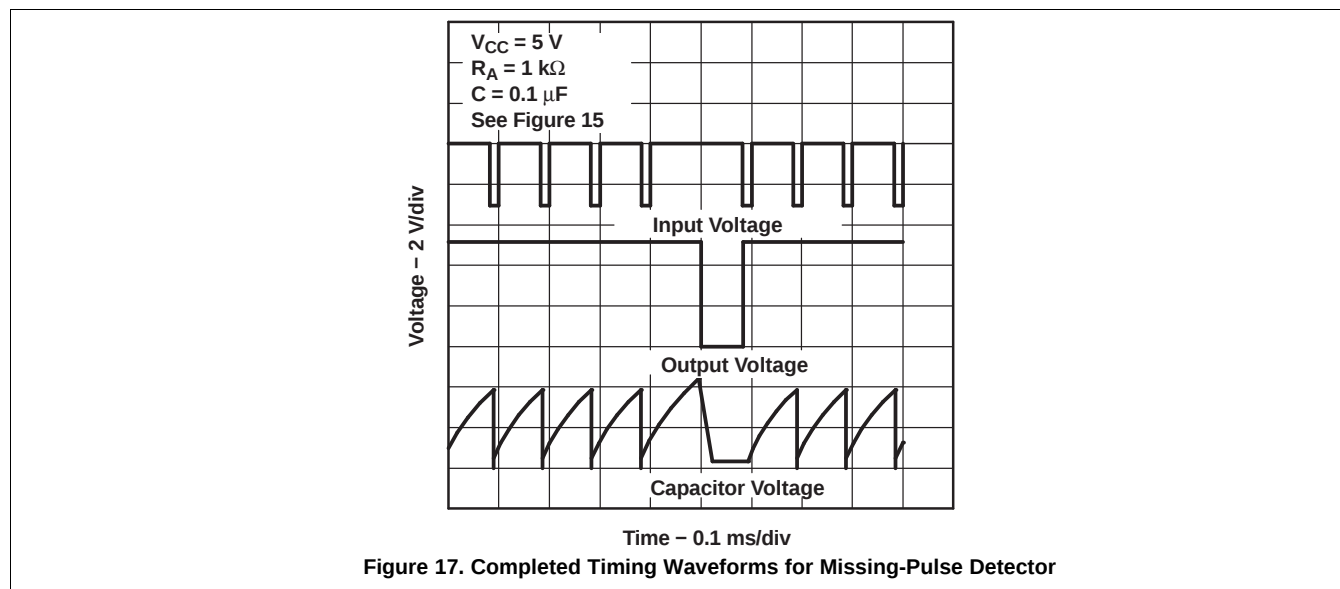
Input fault (missing pulses) must be input high. Input stuck low will not be detected because timing capacitor "C" will remain discharged.

9.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C > [\text{maximum normal input high time}]$. R_L improves V_{OH} , but it is not required for TTL compatibility.

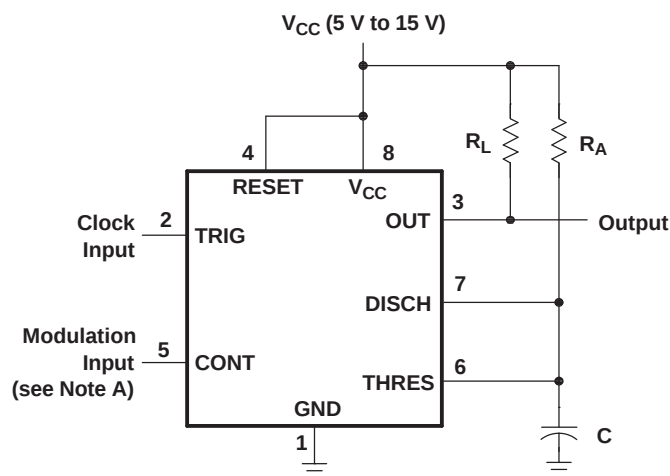
Typical Applications (continued)

9.2.1.3 Application Curves



9.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
 NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

Typical Applications (continued)

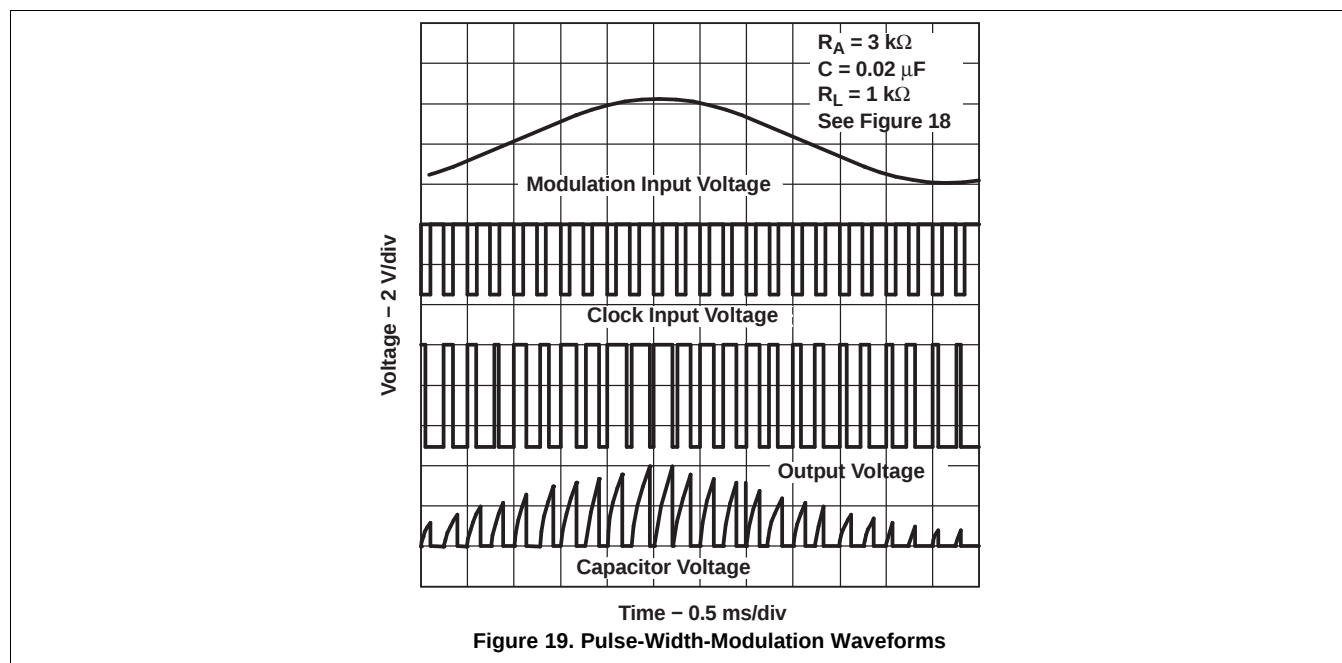
9.2.2.1 Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than $1/3 V_{CC}$. Modulation input can vary from ground to V_{CC} . The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is based RC on an negative exponential curve.

9.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH} , but it is not required for TTL compatibility.

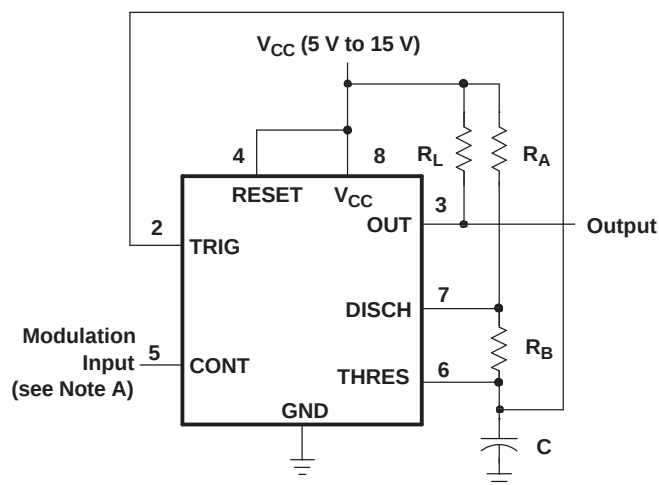
9.2.2.3 Application Curves



9.2.3 Pulse-Position Modulation

As shown in [Figure 20](#), any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. [Figure 21](#) shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

Typical Applications (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

9.2.3.1 Design Requirements

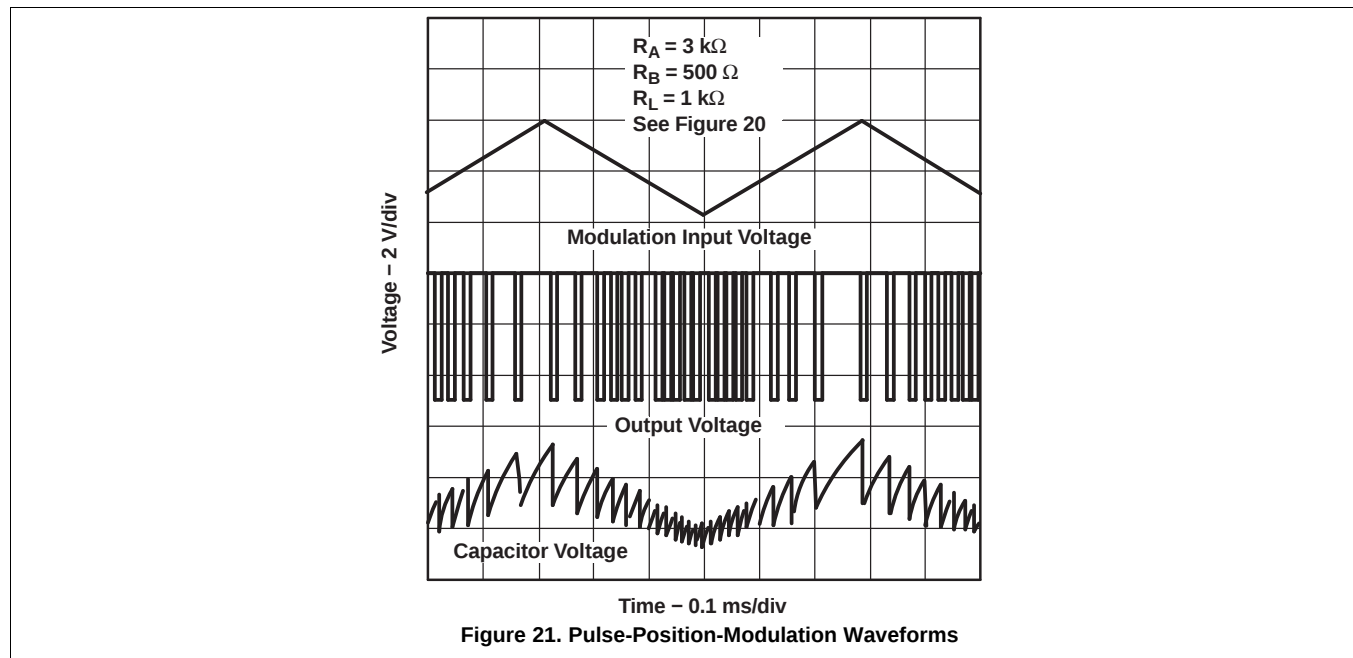
Both DC and AC coupled modulation input will change the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle will vary with the modulation voltage.

9.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in A-stable Operation section. R_L improves V_{OH} , but it is not required for TTL compatibility.

Typical Applications (continued)

9.2.3.3 Application Curves



9.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

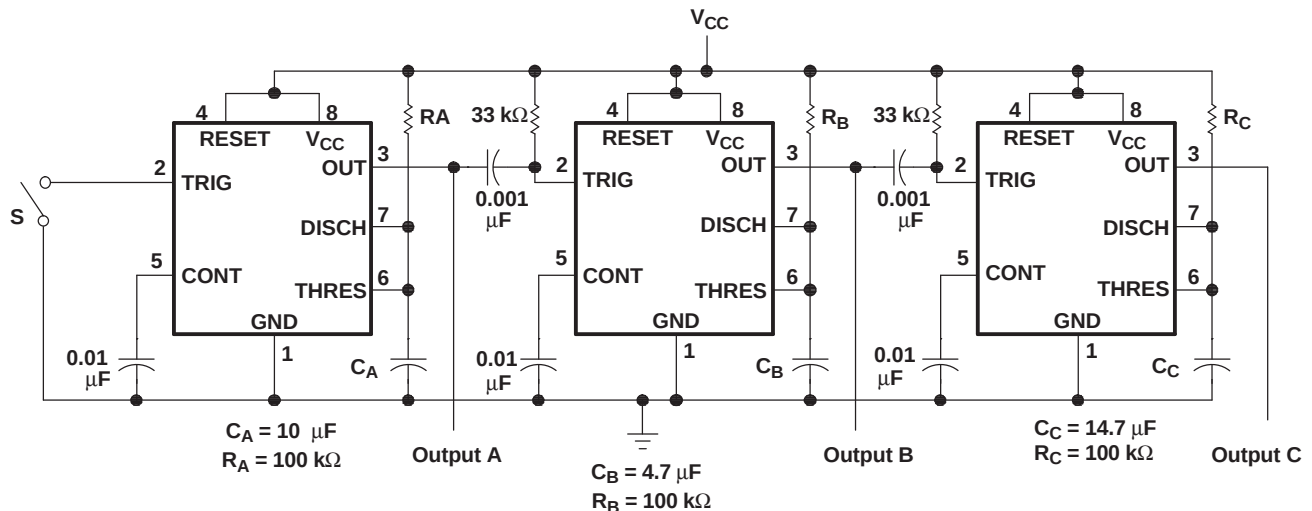


Figure 22. Sequential Timer Circuit

Typical Applications (continued)

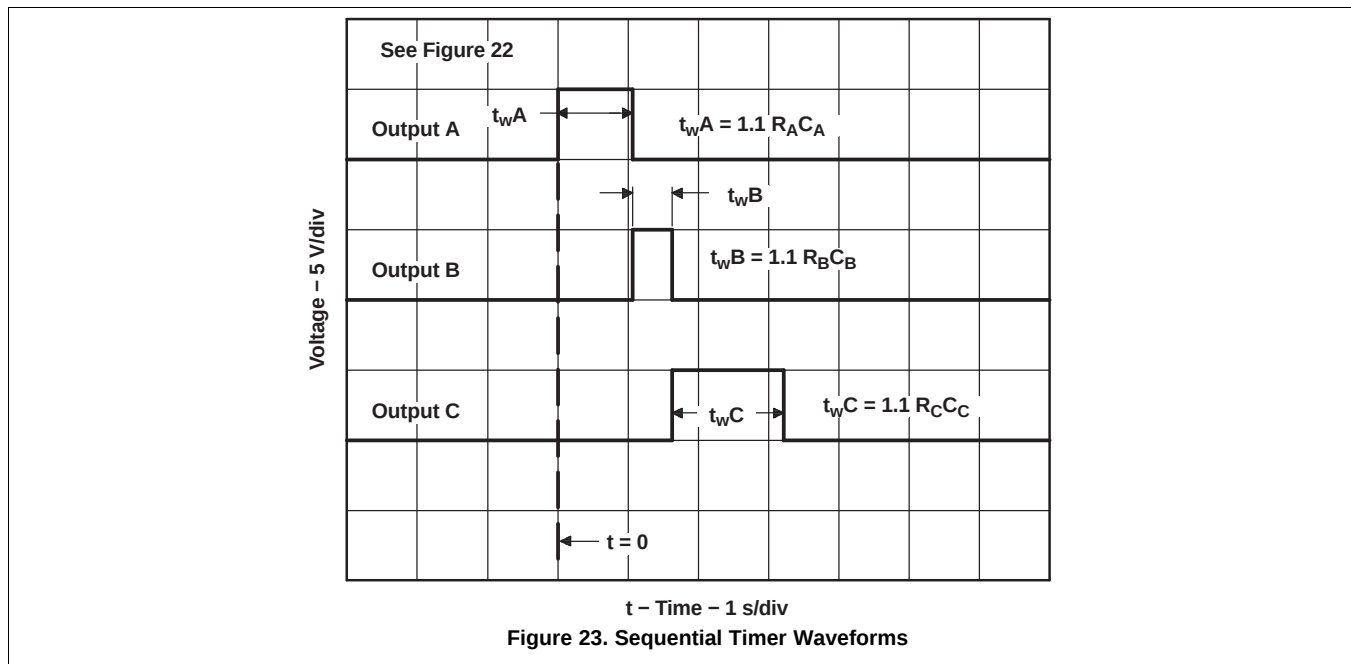
9.2.4.1 Design Requirements

The sequential timer application chains together multiple mono-stable timers. The joining components are the 33-kΩ resistors and 0.001-μF capacitors. The output high to low edge passes a 10-μs start pulse to the next monostable.

9.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula. $t_w = 1.1 \times R \times C$.

9.2.4.3 Application Curves



10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 16 V. (18 V for SE555). A bypass capacitor is highly recommended from VCC to ground pin; ceramic 0.1 μF capacitor is sufficient.

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
NA555	Click here	Click here	Click here	Click here	Click here
NE555	Click here	Click here	Click here	Click here	Click here
SA555	Click here	Click here	Click here	Click here	Click here
SE555	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/10901BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10901BPA	Samples
M38510/10901BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10901BPA	Samples
NA555D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA555	Samples
NA555DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA555	Samples
NA555DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA555	Samples
NA555P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-40 to 105	NA555P	Samples
NA555PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	NA555P	Samples
NE555D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	NE555P	Samples
NE555PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	NE555P	Samples
NE555PS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		N555	Samples
NE555PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PSRE4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE555PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
SA555D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SA555P	Samples
SA555PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SA555P	Samples
SE555D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SE555FKB	Samples
SE555JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SE555JG	Samples
SE555JGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SE555JGB	Samples
SE555P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	SE555P	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SE555, SE555M :

- Catalog : [SE555](#)
- Military : [SE555M](#)
- Space : [SE555-SP](#), [SE555-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

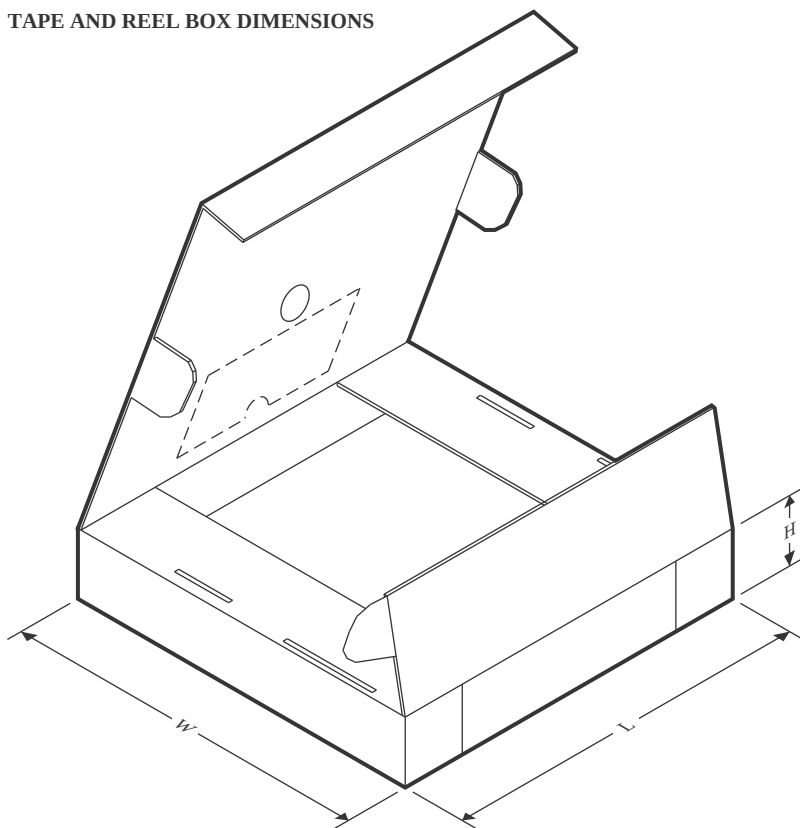
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
NE555PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SE555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

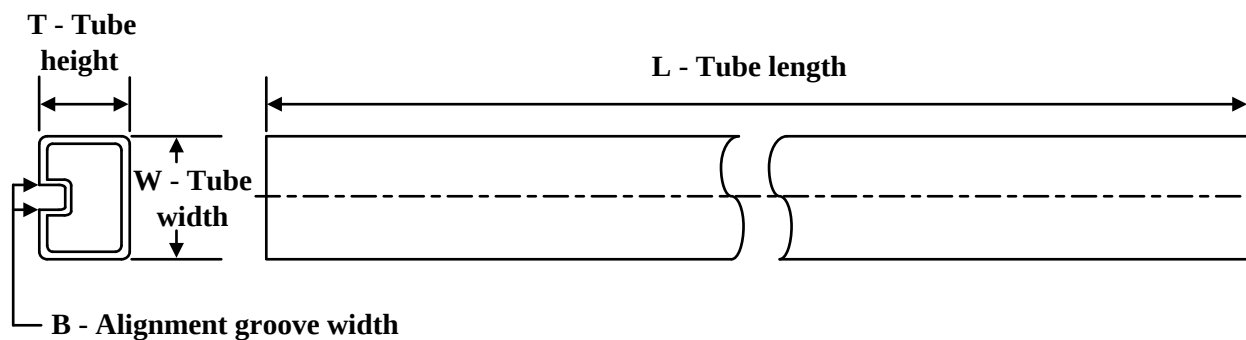
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NA555DR	SOIC	D	8	2500	356.0	356.0	35.0
NA555DR	SOIC	D	8	2500	340.5	336.1	25.0
NE555DR	SOIC	D	8	2500	340.5	336.1	25.0
NE555DR	SOIC	D	8	2500	364.0	364.0	27.0
NE555DR	SOIC	D	8	2500	356.0	356.0	35.0
NE555DRG4	SOIC	D	8	2500	340.5	336.1	25.0
NE555DRG4	SOIC	D	8	2500	356.0	356.0	35.0
NE555PSR	SO	PS	8	2000	356.0	356.0	35.0
NE555PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
SA555DR	SOIC	D	8	2500	340.5	336.1	25.0
SA555DRG4	SOIC	D	8	2500	340.5	336.1	25.0
SE555DR	SOIC	D	8	2500	350.0	350.0	43.0
SE555DRG4	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



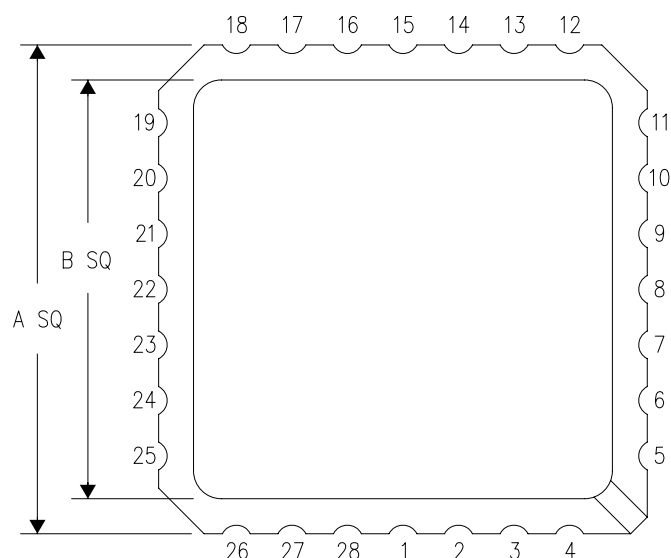
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
NA555D	D	SOIC	8	75	506.6	8	3940	4.32
NA555D	D	SOIC	8	75	507	8	3940	4.32
NA555DG4	D	SOIC	8	75	506.6	8	3940	4.32
NA555DG4	D	SOIC	8	75	507	8	3940	4.32
NA555P	P	PDIP	8	50	506	13.97	11230	4.32
NA555P	P	PDIP	8	50	506.1	9	600	5.4
NA555PE4	P	PDIP	8	50	506	13.97	11230	4.32
NE555D	D	SOIC	8	75	507	8	3940	4.32
NE555D	D	SOIC	8	75	506.6	8	3940	4.32
NE555DG4	D	SOIC	8	75	506.6	8	3940	4.32
NE555DG4	D	SOIC	8	75	507	8	3940	4.32
NE555P	P	PDIP	8	50	506.1	9	600	5.4
NE555P	P	PDIP	8	50	506	13.97	11230	4.32
NE555PE4	P	PDIP	8	50	506	13.97	11230	4.32
NE555PS	PS	SOP	8	80	530	10.5	4000	4.1
NE555PW	PW	TSSOP	8	150	530	10.2	3600	3.5
NE555PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5
SA555D	D	SOIC	8	75	507	8	3940	4.32
SA555DE4	D	SOIC	8	75	507	8	3940	4.32
SA555DG4	D	SOIC	8	75	507	8	3940	4.32
SA555P	P	PDIP	8	50	506	13.97	11230	4.32
SA555PE4	P	PDIP	8	50	506	13.97	11230	4.32
SE555D	D	SOIC	8	75	505.46	6.76	3810	4
SE555DG4	D	SOIC	8	75	505.46	6.76	3810	4
SE555FKB	FK	LCCC	20	1	506.98	12.06	2030	NA
SE555P	P	PDIP	8	50	506	13.97	11230	4.32

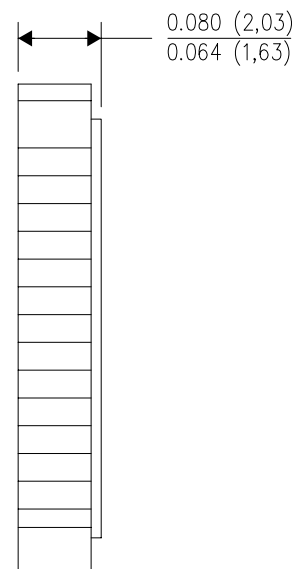
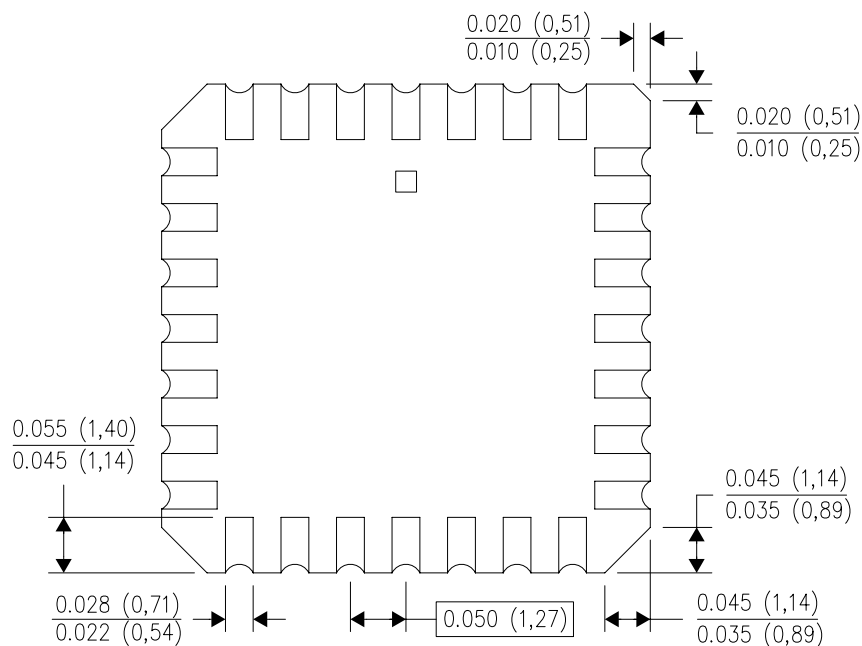
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

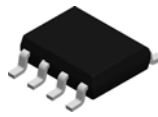


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

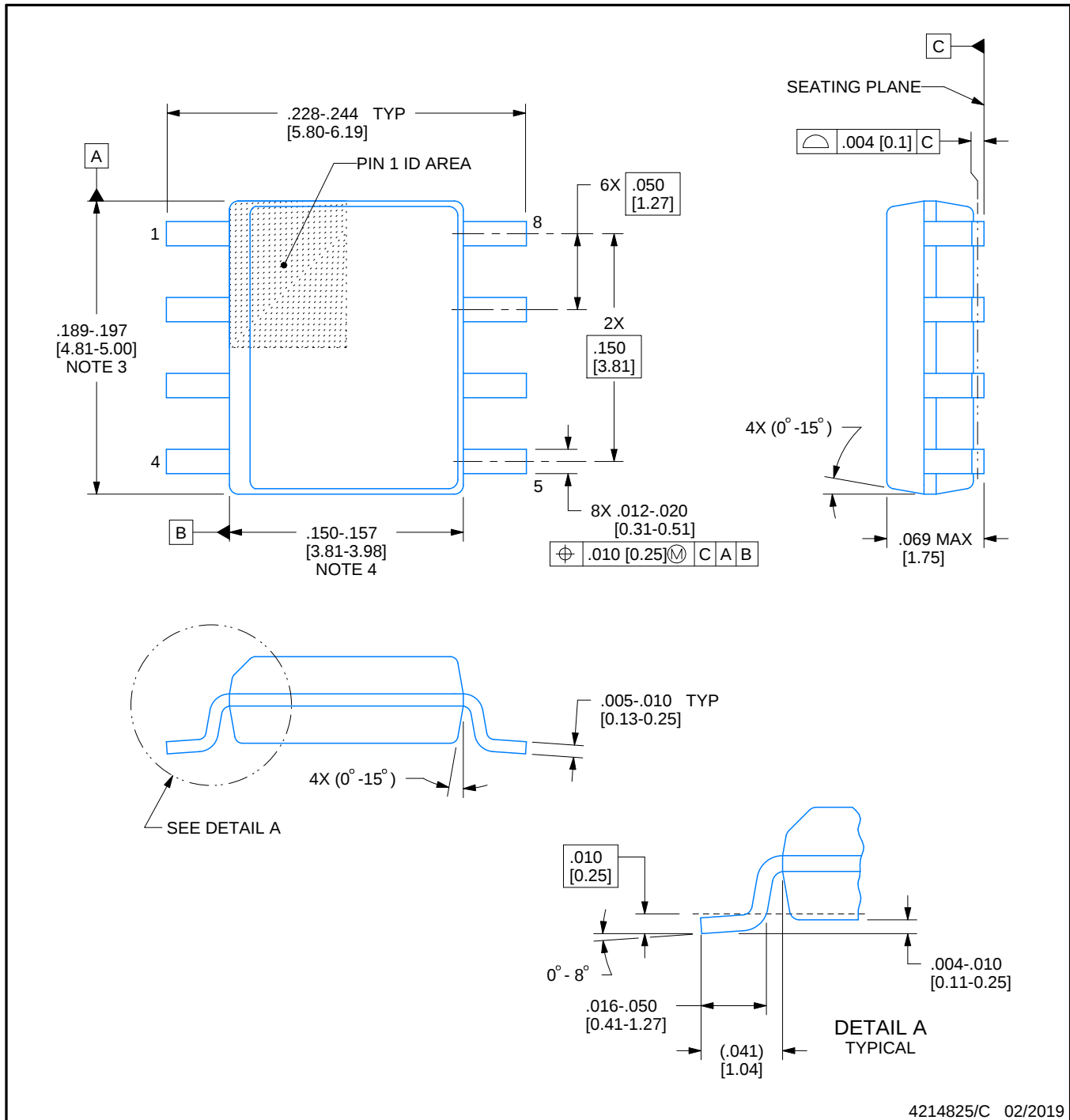


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

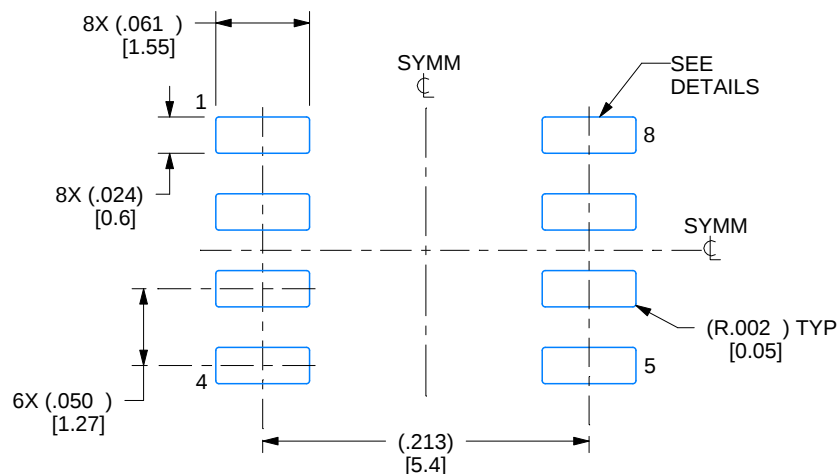
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

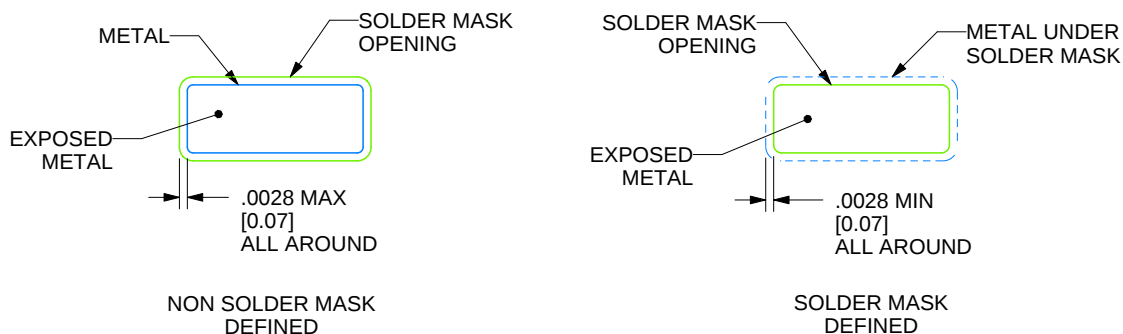
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

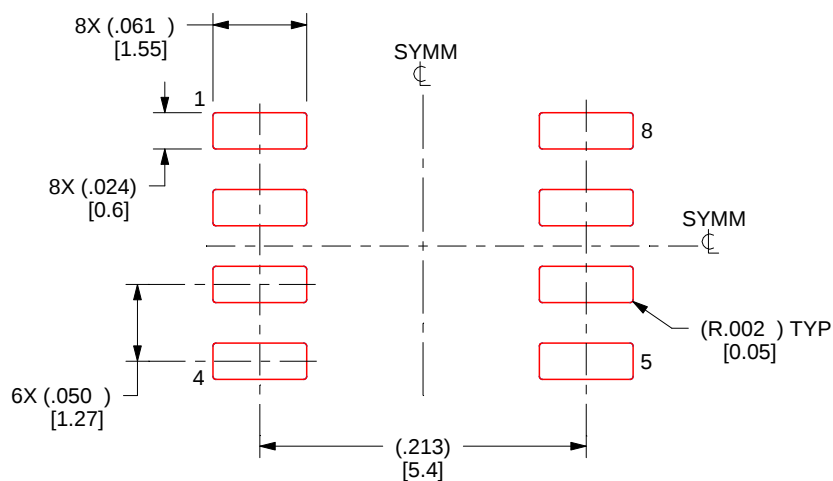
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

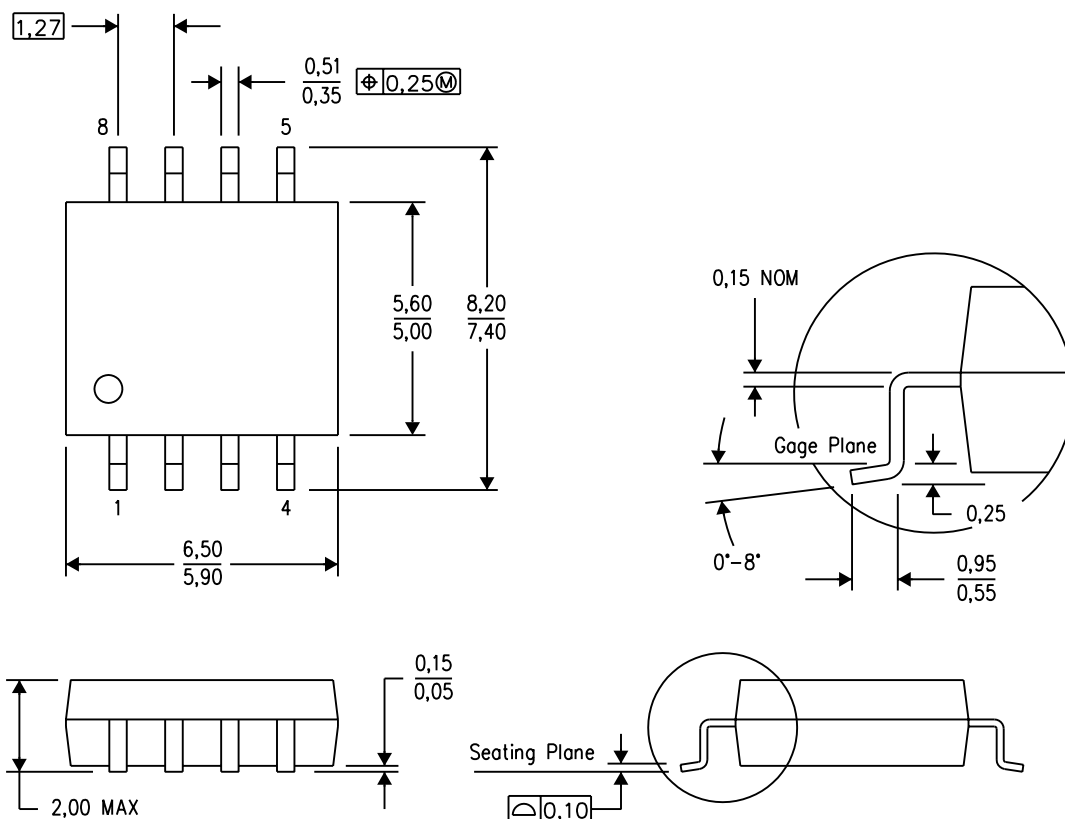
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

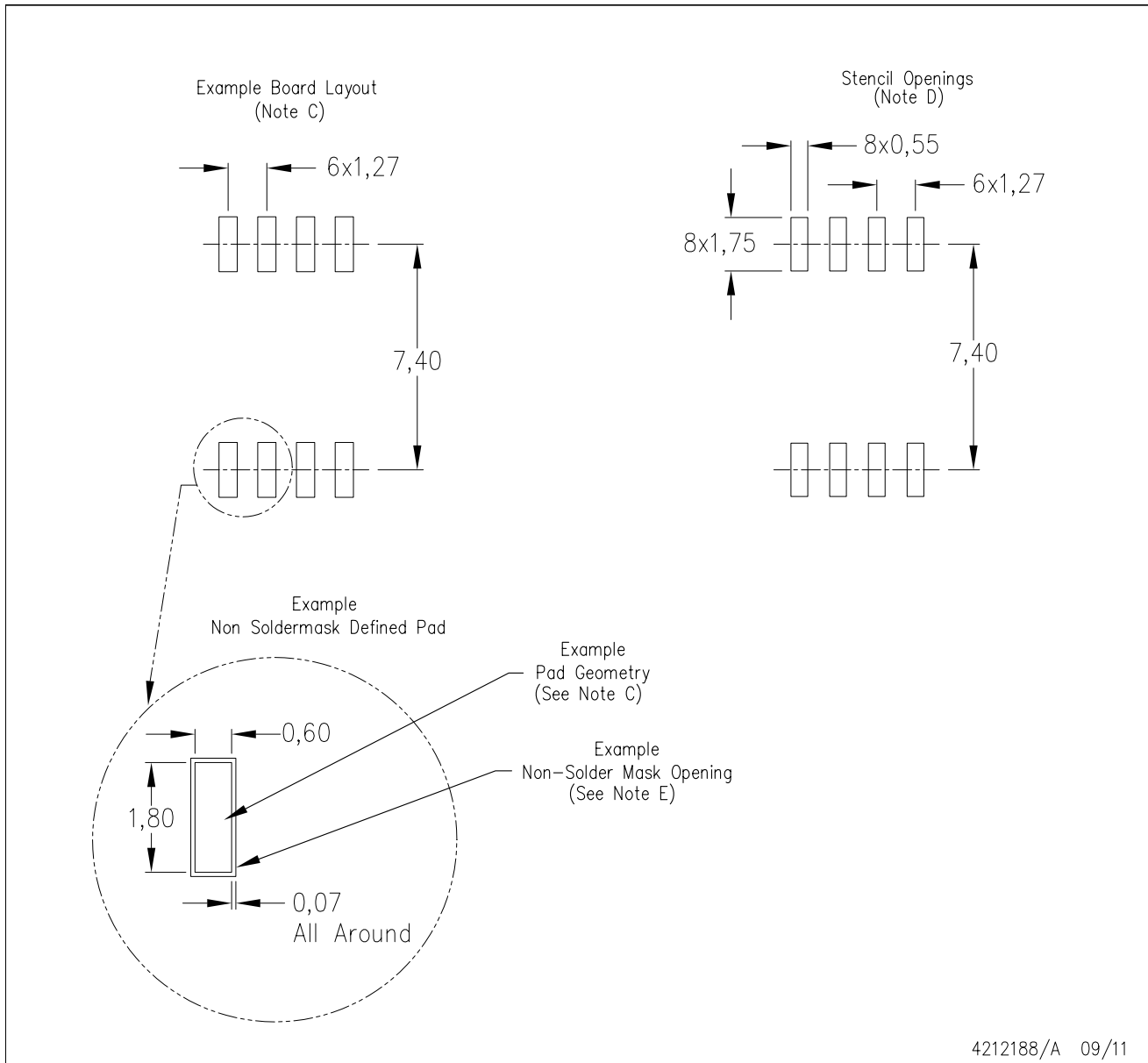


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

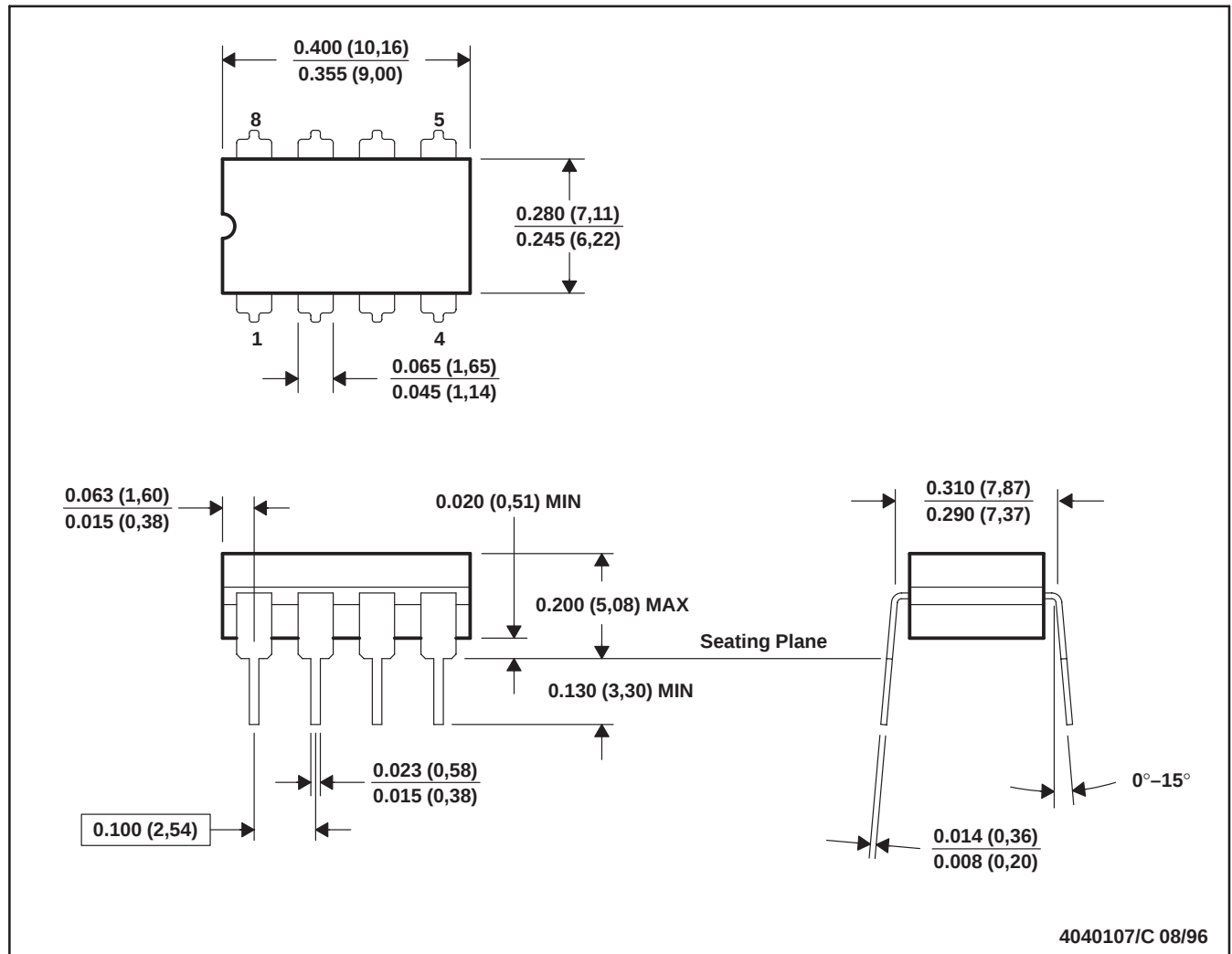
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

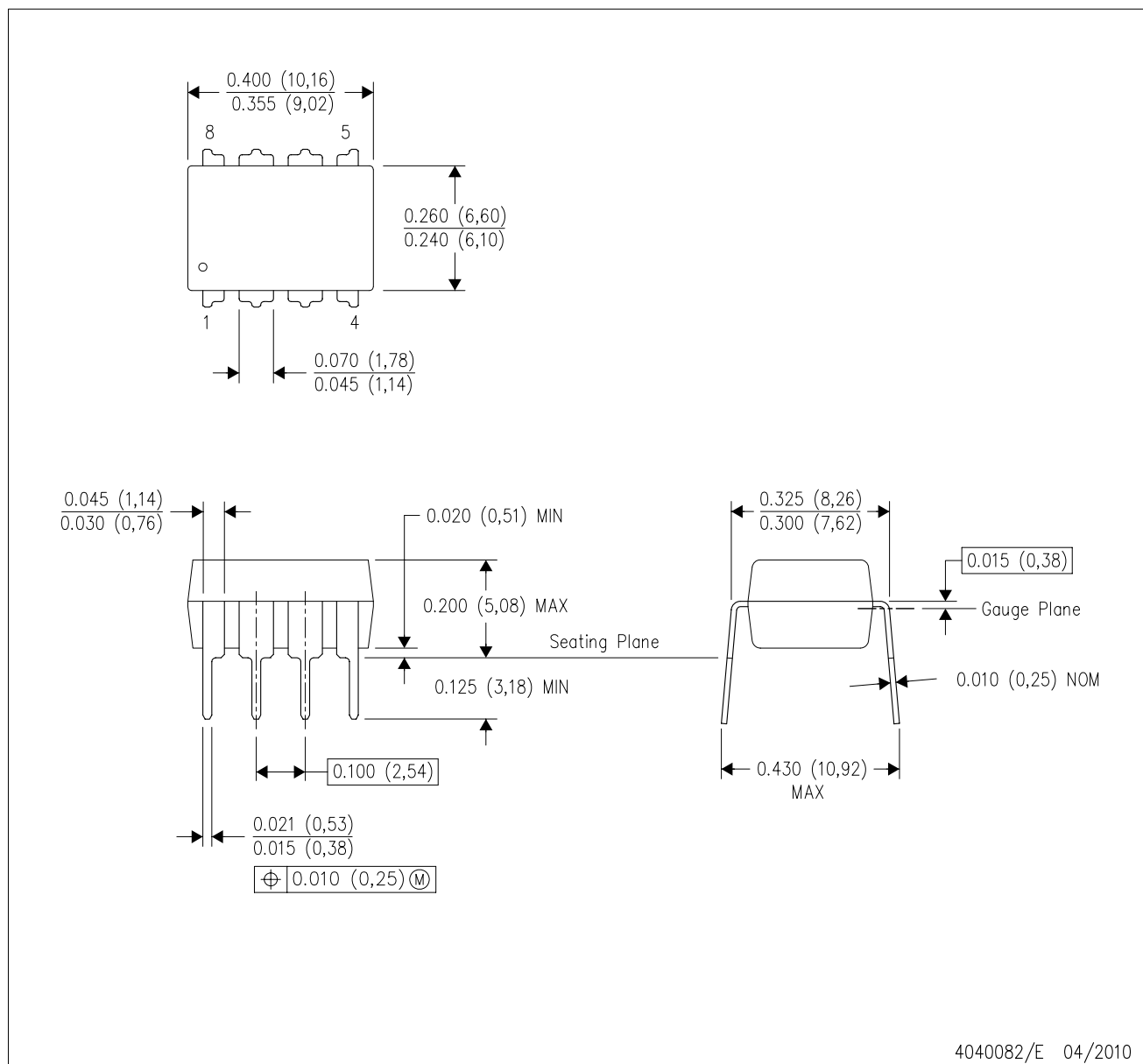
CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

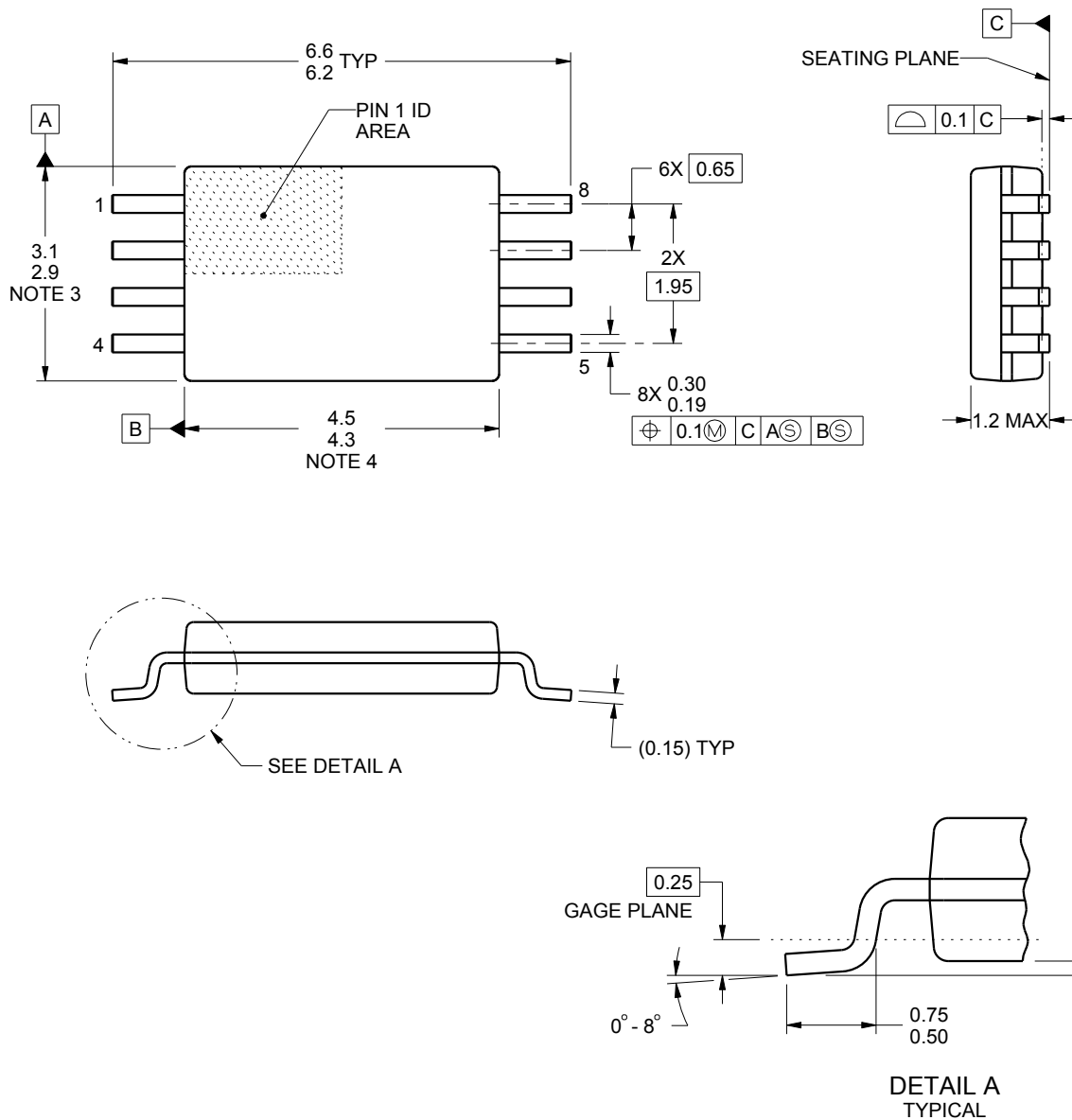
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

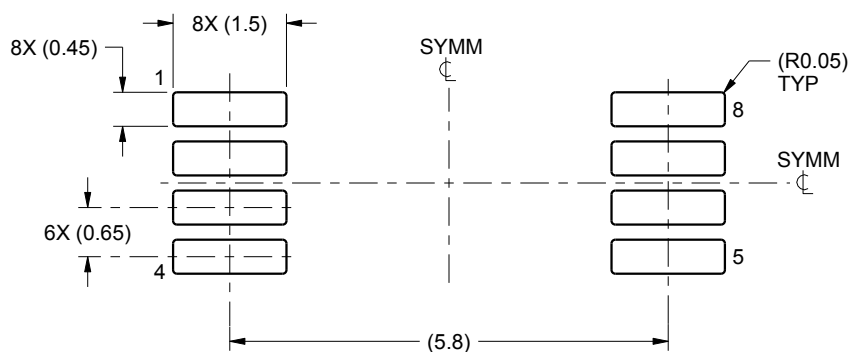
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

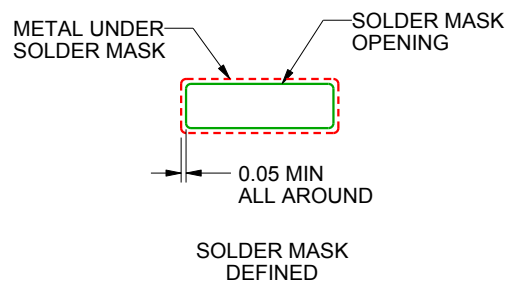
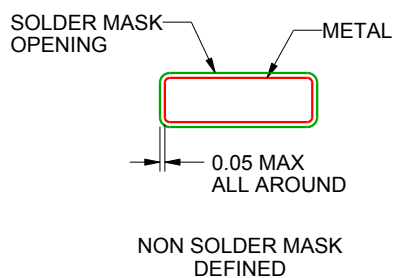
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

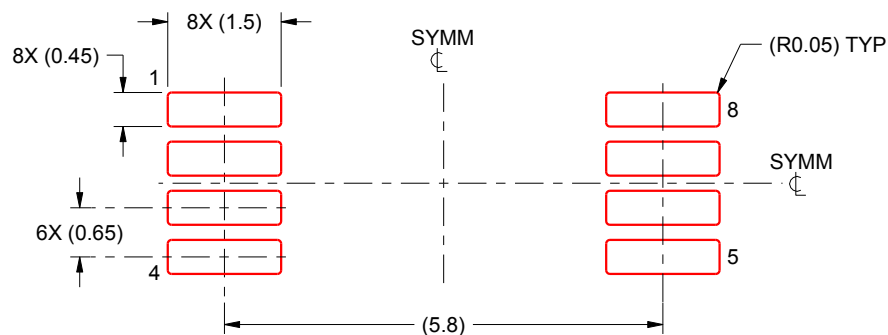
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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