NCP1251

Current-Mode PWM Controller for Off-line Power Supplies

The NCP1251 is a highly integrated PWM controller capable of delivering a rugged and high performance offline power supply in a tiny TSOP−6 package. With a supply range up to 28 V, the controller hosts a jittered 65 kHz or 100 kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts to decrease, the controller automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while limiting the peak current.

Over Power Protection (OPP) is a difficult exercise especially when no−load standby requirements drive the converter specifications. The ON proprietary integrated OPP lets you harness the maximum delivered power without affecting your standby performance simply via two external resistors. A latched Over Voltage Protection (OVP) is combined on the same pin. For ease of implementation, a latched OVP also monitors the V_{CC} line. They offer an efficient protection in case of optocoupler destruction or adverse open loop operation.

Finally, a timer−based short−circuit protection offers the best protection scheme, letting you precisely select the protection trip point irrespective of a loose coupling between the auxiliary and the power windings.

Features

- Fixed−Frequency 65 or 100 kHz Current−Mode Control Operation
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Frequency Foldback Down to 26 kHz and Skip−Cycle in Light Load Conditions
- Internal Ramp Compensation
- Internal Fixed 4 ms Soft−Start
- 100 ms Timer−Based Auto−Recovery Short−Circuit Protection
- Frequency Jittering in Normal and Frequency Foldback Modes
- Option for Auto−Recovery or Latched Short−Circuit Protection
- OVP Input for Improved Robustness
- Up to 28 V V_{CC} Operation
- Latched or Auto−Recovery OVP Protection on V_{CC}
- +300 mA / −500 mA Source/Sink Drive Capability
- Less than 100 mW Standby Power at High Line
- EPS 2.0 Compliant
- These are Pb−Free Devices

Typical Applications

- ac−dc Converters for TVs, Set−top Boxes and Printers
- Offline Adapters for Notebooks and Netbooks

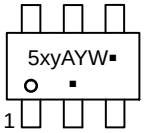
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM



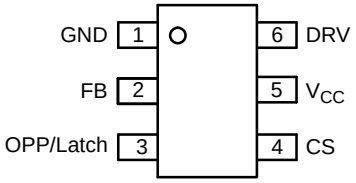
TSOP−6
(SOT23−6)
SN SUFFIX
CASE 318G
STYLE 13



5xy	= Specific Device Code
x	= A or U
y	= A, 2, C, D, or F
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2015

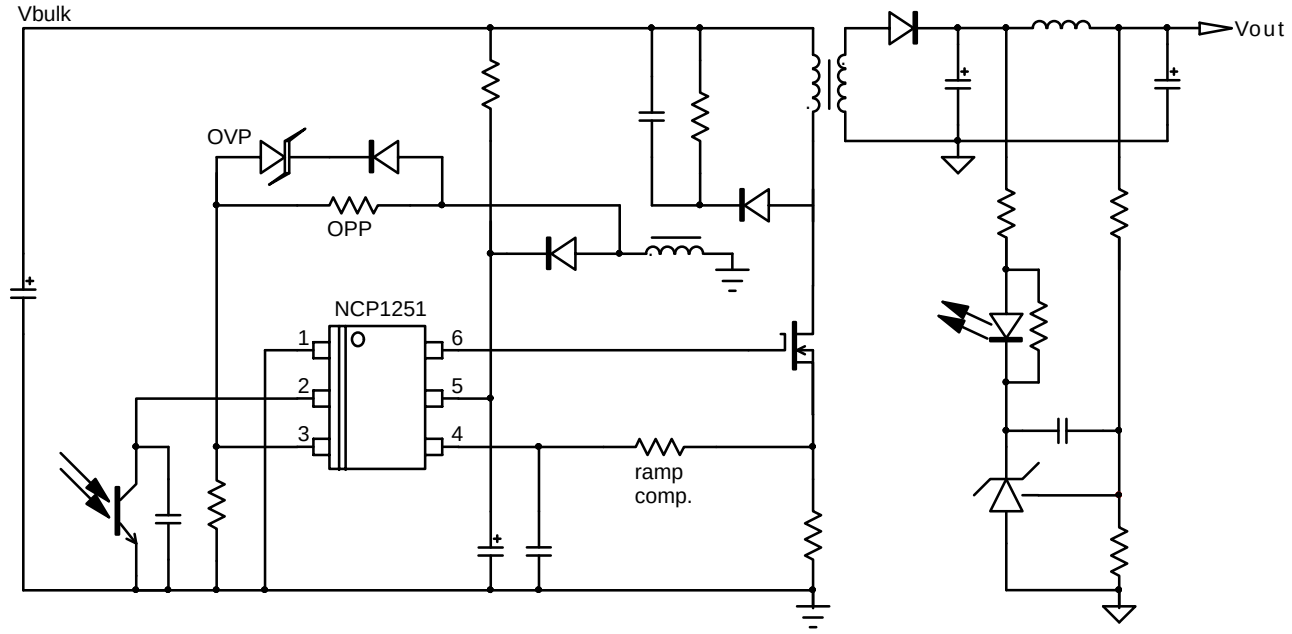


Figure 1. Typical Application Example

Pin N°	Pin Name	Function	Pin Description
1	GND	–	The controller ground.
2	FB	Feedback pin	Hooking an optocoupler collector to this pin will allow regulation.
3	OPP/OVP	Adjust the Over Power Protection Latches off the part	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level. When brought above 3 V, the part is fully latched off.
4	CS	Current sense + ramp compensation	This pin monitors the primary peak current but also offers a means to introduce ramp compensation.
5	V_{CC}	Supplies the controller	This pin is connected to an external auxiliary voltage and supplies the controller. When the V_{CC} exceeds a certain level, the part permanently latches off.
6	DRV	Driver output	The driver's output to an external MOSFET gate.

OPTIONS

Controller	Frequency	OCP	V_{CC} OVP	OVP/OTP
NCP1251ASN65T1G	65 kHz	Latched	Latched	Latched
NCP1251BSN65T1G	65 kHz	Autorecovery	Latched	Latched
NCP1251CSN65T1G	65 kHz	Autorecovery	Autorecovery	Latched
NCP1251FSN65T1G	65 kHz	Autorecovery	Latched	Latched
NCP1251ASN100T1G	100 kHz	Latched	Latched	Latched
NCP1251BSN100T1G	100 kHz	Autorecovery	Latched	Latched

NOTE: F version has a different foldback scheme for improved efficiency.

ORDERING INFORMATION

Device	Package Marking	OCP Protection	V_{CC} OVP Protection	Switching Frequency	Package	Shipping†
NCP1251ASN65T1G	5AA	Latch	Latch	65 kHz	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NCP1251BSN65T1G	5A2	Autorecovery	Latch	65 kHz		
NCP1251CSN65T1G	5AE	Autorecovery	Autorecovery	65 kHz		
NCP1251FSN65T1G	5AF	Autorecovery	Latch	65 kHz		
NCP1251ASN100T1G	5AC	Latch	Latch	100 kHz		
NCP1251BSN100T1G	5AD	Autorecovery	Latch	100 kHz		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

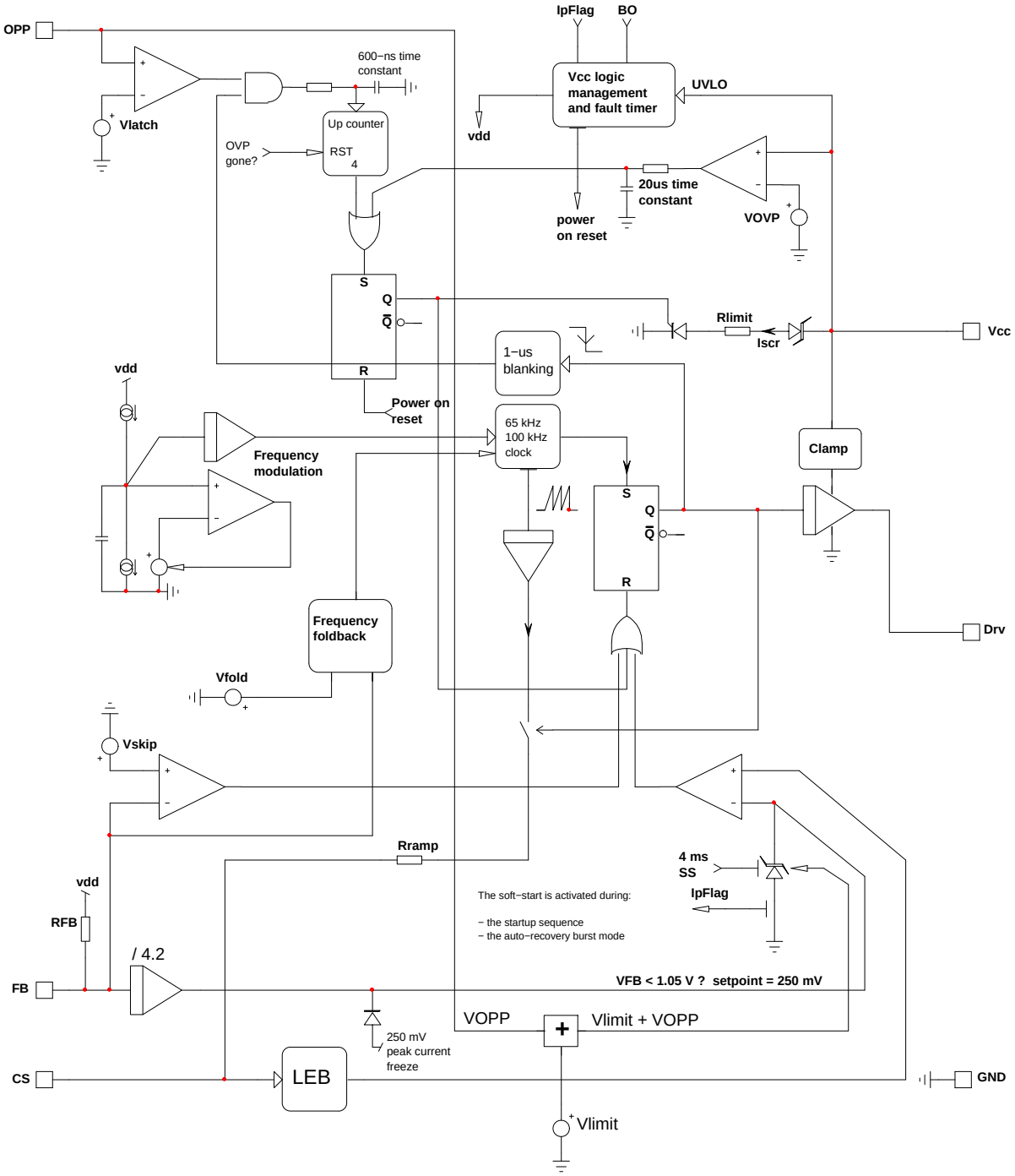


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{CC}	Power Supply voltage, V_{CC} pin, continuous voltage	28	V
$V_{DRVtran}$	Maximum DRV pin voltage when DRV in H state, transient voltage (Note 1)	V_{CC} + 0.3	V
	Maximum voltage on low power pins CS, FB and OPP	−0.3 to 10	V
IOPP	Maximum injected negative current into the OPP pin (pin 3)	−2	mA
I_{SCR}	Maximum continuous current into the V_{CC} pin while in latch mode	3	mA
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	360	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model (HBM), all pins	2	kV
	ESD Capability, Machine Model (MM)	200	V
	ESD Capability, Charged Device Model (CDM)	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The transient voltage is a voltage spike injected to DRV pin being in high state. Maximum transient duration is 100 ns.
2. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per JESD22, Method A114E. Machine Model Method 200 V per JESD22, Method A115A. Charged Device Model per JEDEC Standard JESD22−C101D
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
VCC_{ON}	V_{CC} increasing level at which driving pulses are authorized	5	16	18	20	V
$VCC_{(min)}$	V_{CC} decreasing level at which driving pulses are stopped	5	8.2	8.8	9.4	V
VCC_{HYST}	Hysteresis VCC_{ON} − $VCC_{(min)}$	5	6.0			V
V_{ZENER}	Clamped V_{CC} when latched off / burst mode activation @ I_{CC} = 500 μA	5		7.0		V
ICC1	Start−up current	5			15	μA
ICC2	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 65 kHz and C_L = 0 nF	5		1.4	2.2	mA
ICC3	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 65 kHz and C_L = 1 nF	5		2.1	3.0	mA
ICC2	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 100 kHz and C_L = 0 nF	5		1.7	2.5	mA
ICC3	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 100 kHz and C_L = 1 nF	5		3.1	4.0	mA
ICCstby	Internal IC consumption while in skip cycle (V_{CC} = 12 V, driving a typical 6 A/600 V MOSFET)	5		550		μA
ICC_{LATCH}	Current flowing into V_{CC} pin that keeps the controller latched (Note 4) T_J = −40°C to +125°C T_J = 0°C to +125°C	5	 40 32			μA
R_{lim}	Current−limit resistor in series with the latch SCR	5		4.0		kΩ
DRIVE OUTPUT						
T_r	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	6		40		ns
T_f	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	6		30		ns
R_{OH}	Source resistance	6		13		Ω
R_{OL}	Sink resistance	6		6.0		Ω
I_{source}	Peak source current, V_{GS} = 0 V – (Note 5)	6		300		mA
I_{sink}	Peak sink current, V_{GS} = 12 V – (Note 5)	6		500		mA
V_{DRVlow}	DRV pin level at V_{CC} close to $VCC_{(min)}$ with a 33 kΩ resistor to GND	6	8.0			V
$V_{DRVhigh}$	DRV pin level at V_{CC} = 28 V – DRV unloaded	6	10	12	14	V
CURRENT COMPARATOR						
I_{IB}	Input Bias Current @ 0.8 V input level on pin 4	4		0.02		μA
V_{Limit1}	Maximum internal current setpoint – T_J = 25°C – pin 3 grounded	4	0.744	0.8	0.856	V
V_{Limit2}	Maximum internal current setpoint – T_J = −40°C to 125°C – pin 3 grounded	4	0.72	0.8	0.88	V
V_{fold}	Default internal voltage set point for frequency foldback trip point – 45% of V_{limit}	3		357		mV
V_{freeze}	Internal peak current setpoint freeze (≈31% of V_{limit})	3		250		mV
T_{DEL}	Propagation delay from current detection to gate off−state	4		100	150	ns
T_{LEB}	Leading Edge Blanking Duration	4		300		ns
TSS	Internal soft−start duration activated upon startup, auto−recovery	−		4		ms
IOPPo	Setpoint decrease for pin 3 biased to –250 mV – (Note 6)	3		31.3		%
IOOPv	Voltage setpoint for pin 3 biased to −250 mV – (Note 6), T_J = 25°C	3	0.51	0.55	0.60	V
IOOPv	Voltage setpoint for pin 3 biased to −250 mV – (Note 6), T_J = −40°C to 125°C	3	0.50	0.55	0.62	V
IOPPs	Setpoint decrease for pin 3 grounded	3		0		%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. For design robustness, we recommend to inject 60 μA as a minimum at the lowest input line voltage.
5. Guaranteed by design
6. See characterization table for linearity over negative bias voltage
7. A 1 MΩ resistor is connected from pin 3 to the ground for the measurement.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
INTERNAL OSCILLATOR						
f_{OSC}	Oscillation frequency (65 kHz version)	−	61	65	71	kHz
f_{OSC}	Oscillation frequency (100 kHz version)	−	92	100	108	kHz
D_{max}	Maximum duty−cycle	−	76	80	84	%
f_{jitter}	Frequency jittering in percentage of f_{OSC}	−		±5		%
f_{swing}	Swing frequency	−		240		Hz
FEEDBACK SECTION						
R_{up}	Internal pull−up resistor	2		20		kΩ
R_{eq}	Equivalent ac resistor from FB to GND	2		16		kΩ
I_{ratio}	Pin 2 to current setpoint division ratio	−		4.2		
V_{freeze}	Feedback voltage below which the peak current is frozen	2		1.05		V
FREQUENCY FOLDBACK						
V_{fold}	Frequency foldback level on the feedback pin – ≈45% of maximum peak current	−		1.5		V
V_{foldF}	Frequency foldback level on the feedback pin – ≈59% of maximum peak current (F version only)	−		1.9		V
F_{trans}	Transition frequency below which skip−cycle occurs	−	22	26	30	kHz
$V_{fold,end}$	End of frequency foldback feedback level, $F_{sw} = F_{min}$			350		mV
$V_{foldF,end}$	End of frequency foldback feedback level, $F_{sw} = F_{min}$ (F version only)			1.5		V
V_{skip}	Skip−cycle level voltage on the feedback pin	−		300		mV
Skip hysteresis	Hysteresis on the skip comparator – (Note 5)	−		30		mV
INTERNAL SLOPE COMPENSATION						
V_{ramp}	Internal ramp level @ 25°C – (Note 7)	4		2.5		V
R_{ramp}	Internal ramp resistance to CS pin	4		20		kΩ
PROTECTIONS						
V_{latch}	Latching level input	3	2.7	3	3.3	V
$T_{latch−blank}$	Blanking time after drive turn off	1		1.0		μs
$T_{latch−count}$	Number of clock cycles before latch confirmation	−		4.0		
$T_{latch−del}$	OVP detection time constant	1		600		ns
Timer	Internal auto−recovery fault timer duration	−	100	130	160	ms
V_{OVP}	Latched Over voltage protection on the V_{CC} rail	5	24	25.5	27	V
T_{OVPdel}	Delay before OVP on V_{CC} confirmation	5		20		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. For design robustness, we recommend to inject 60 μA as a minimum at the lowest input line voltage.
5. Guaranteed by design
6. See characterization table for linearity over negative bias voltage
7. A 1 MΩ resistor is connected from pin 3 to the ground for the measurement.

TYPICAL CHARACTERISTICS

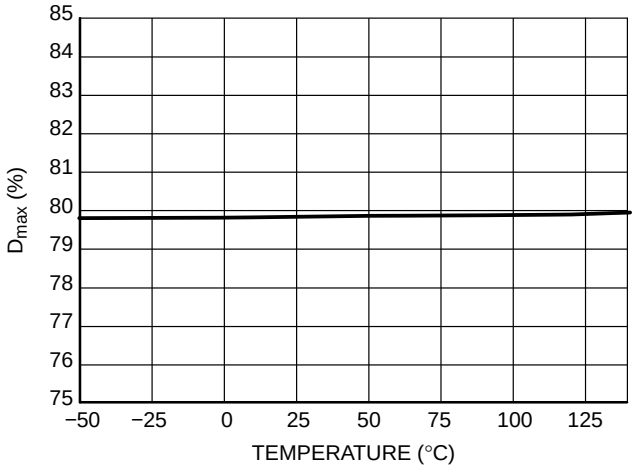


Figure 3.

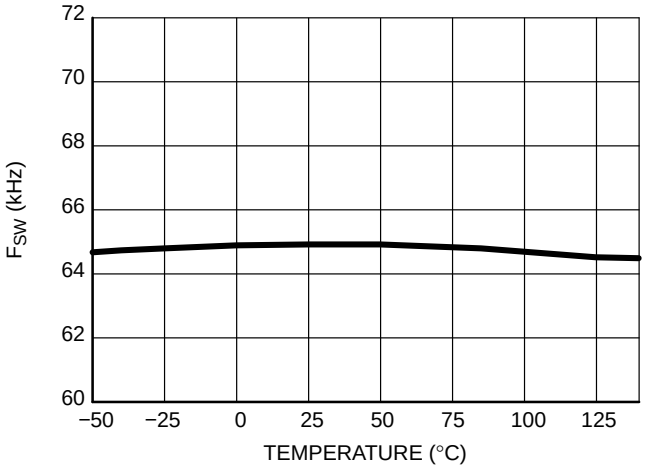


Figure 4.

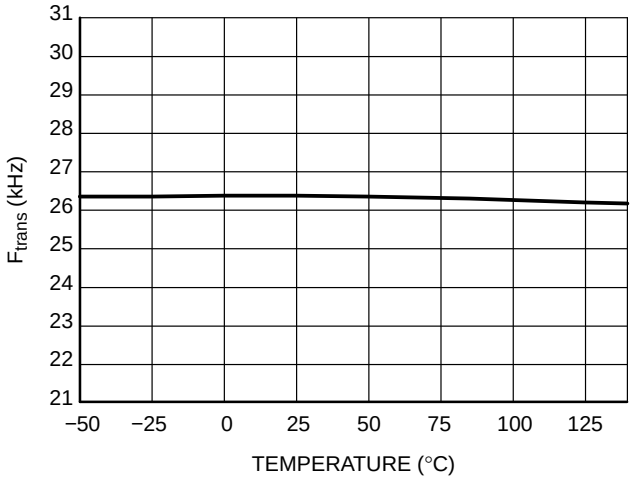


Figure 5.

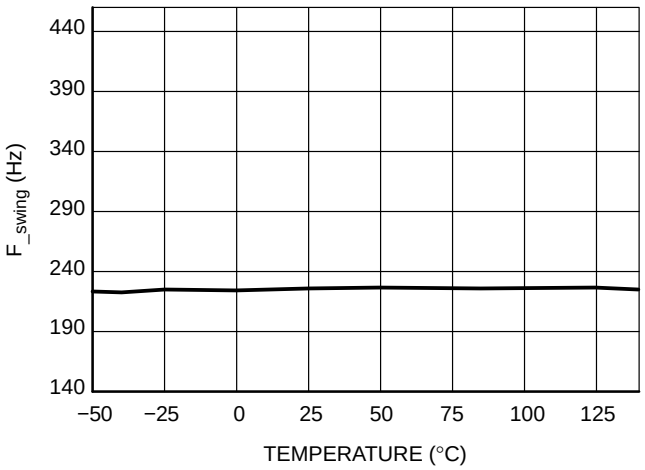


Figure 6.

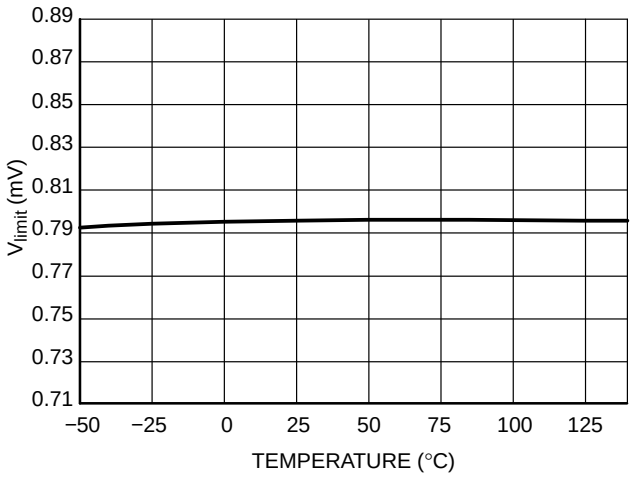


Figure 7.

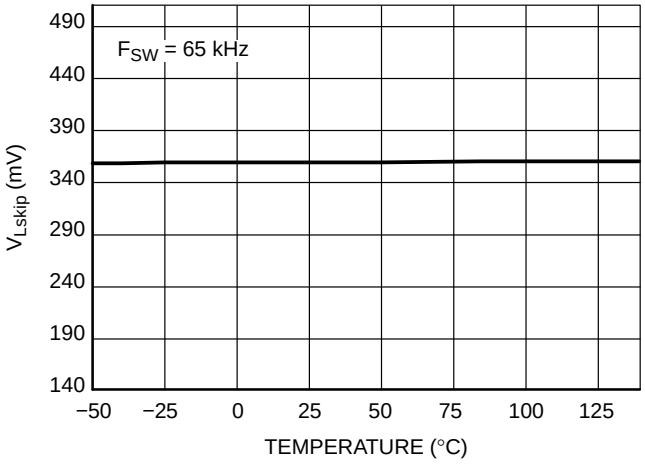


Figure 8.

TYPICAL CHARACTERISTICS

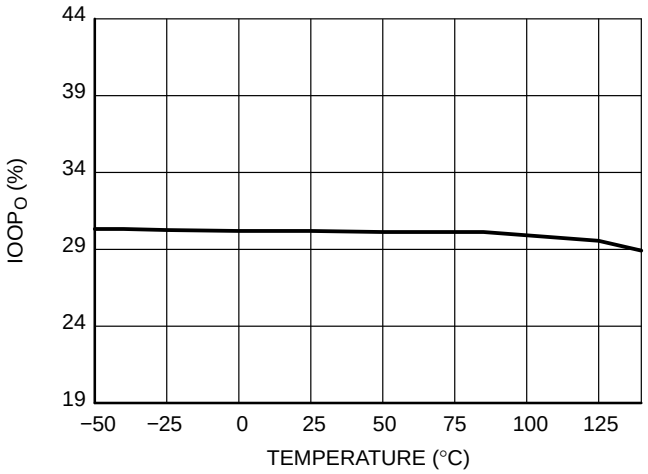


Figure 9.

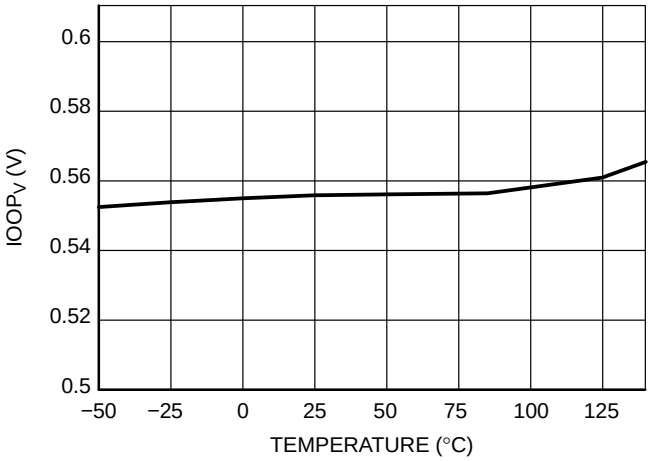


Figure 10.

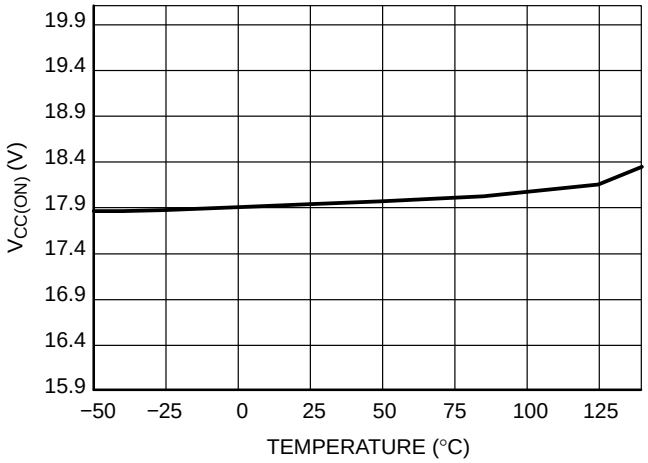


Figure 11.

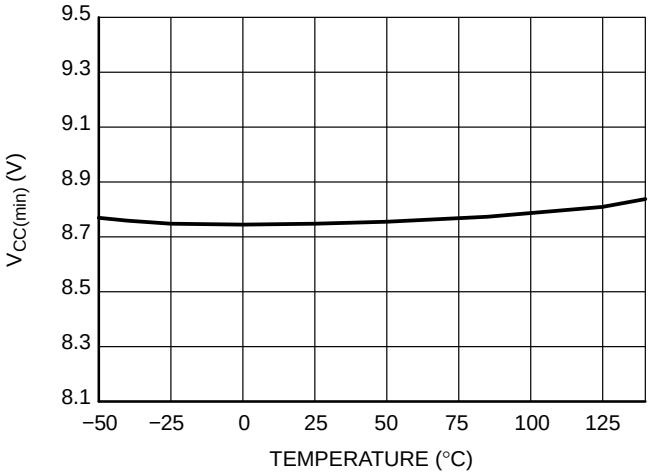


Figure 12.

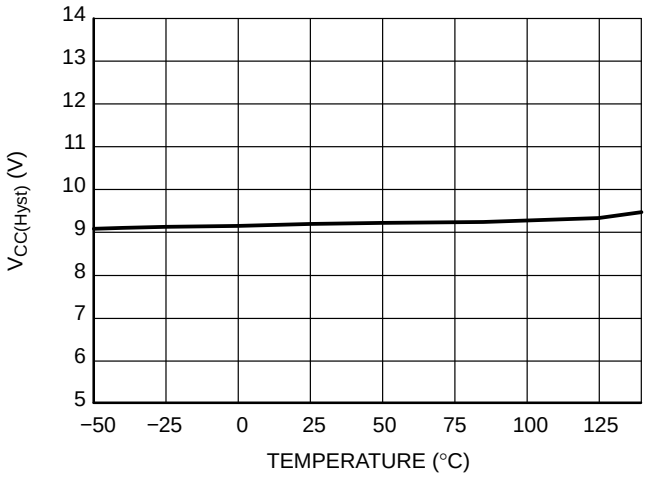


Figure 13.

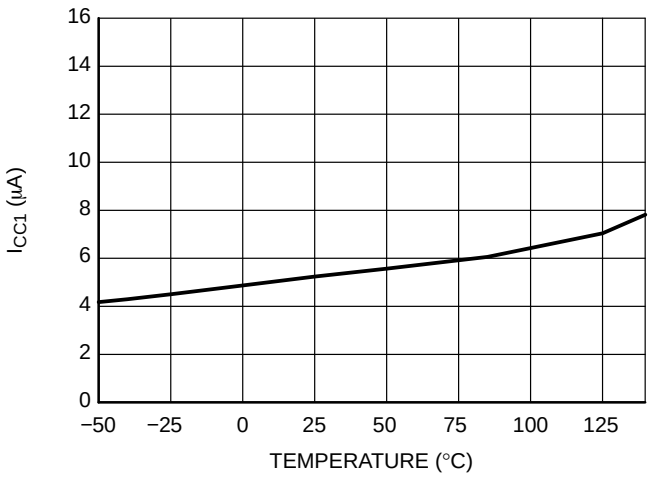


Figure 14.

TYPICAL CHARACTERISTICS

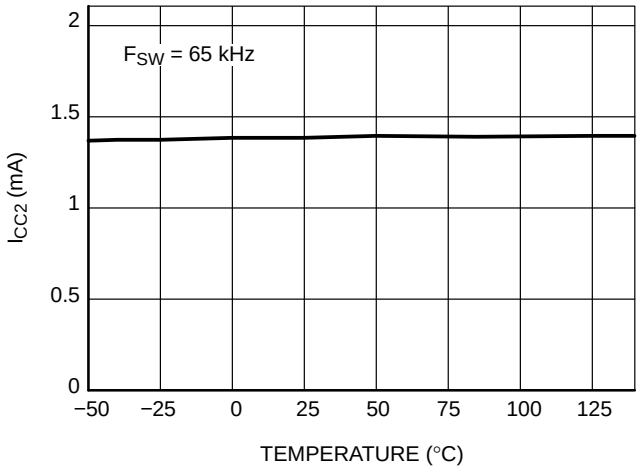


Figure 15.

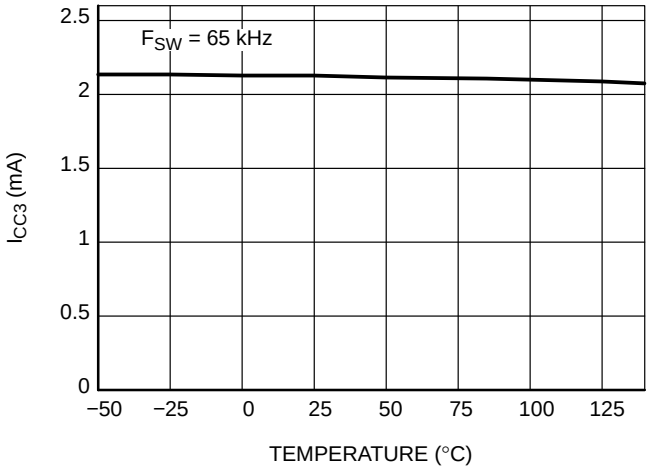


Figure 16.

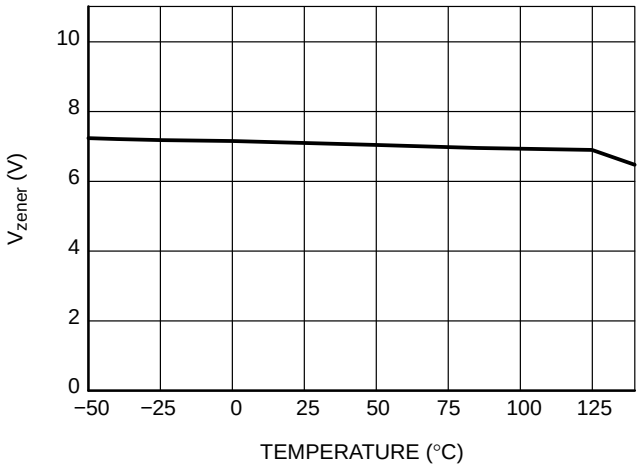


Figure 17.

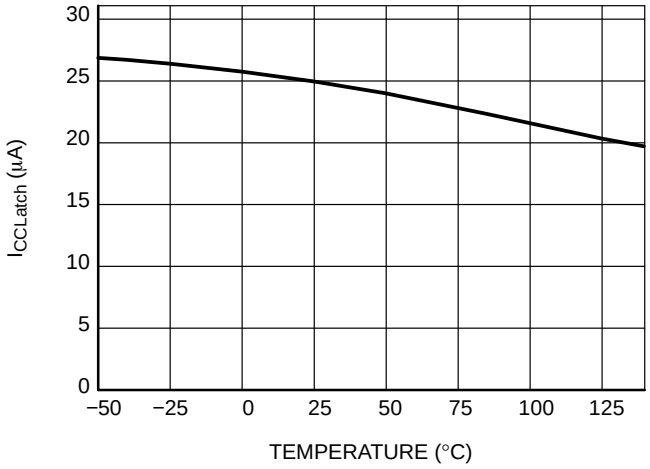


Figure 18.

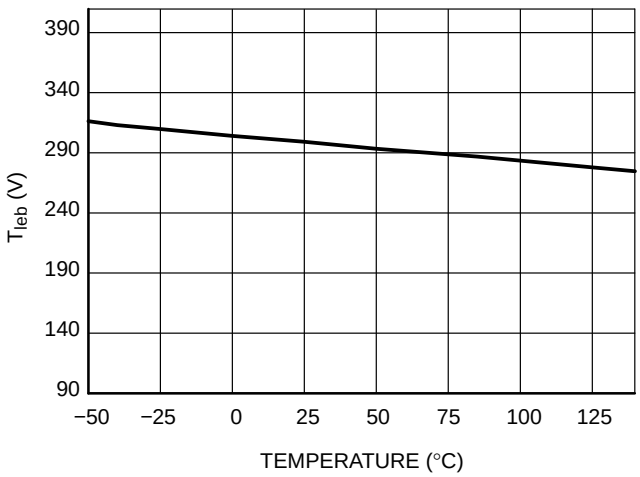


Figure 19.

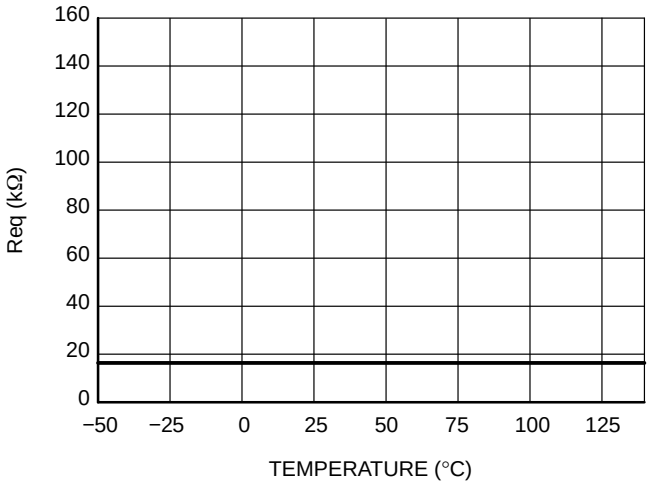


Figure 20.

TYPICAL CHARACTERISTICS

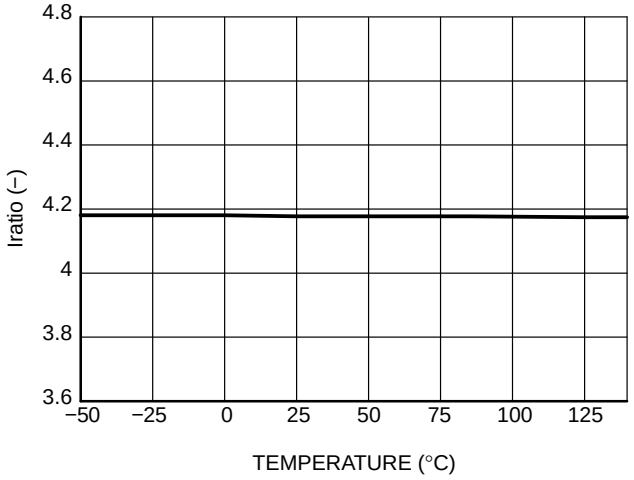


Figure 21.

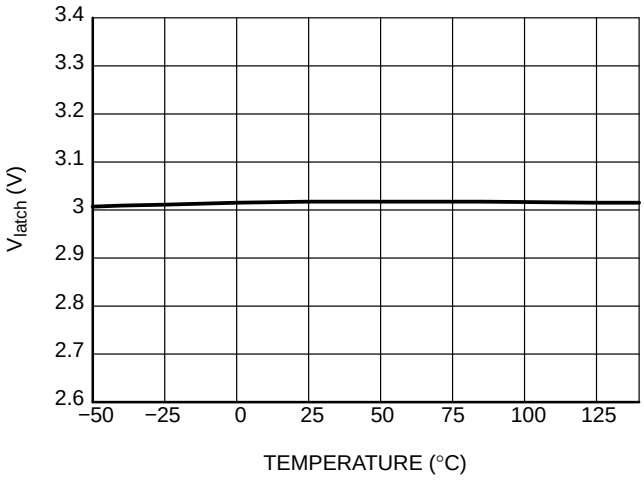


Figure 22.

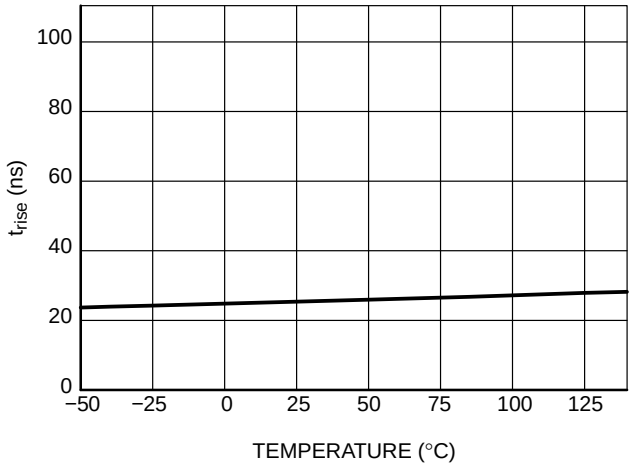


Figure 23.

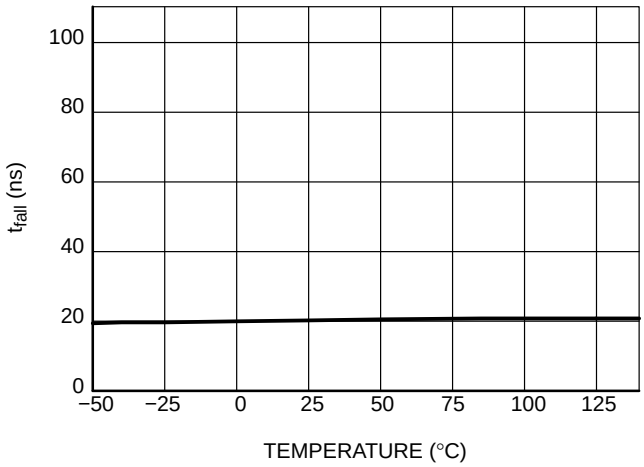


Figure 24.

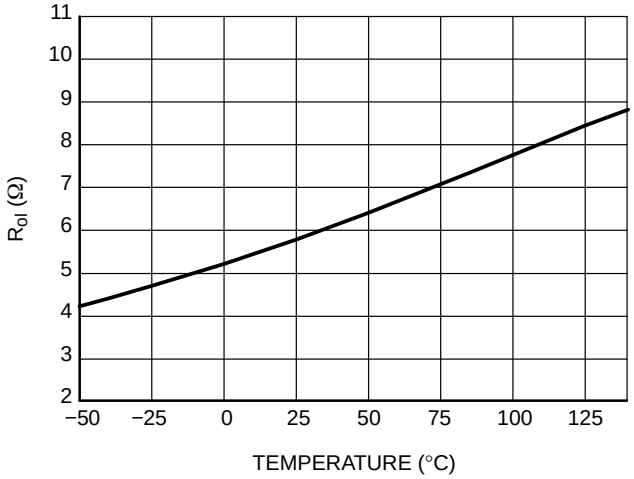


Figure 25.

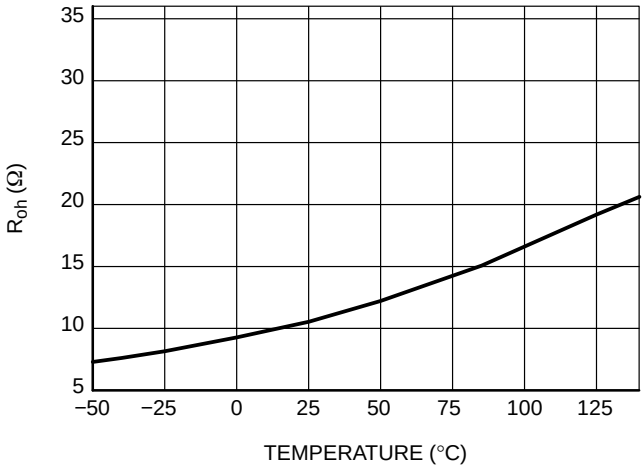


Figure 26.

TYPICAL CHARACTERISTICS

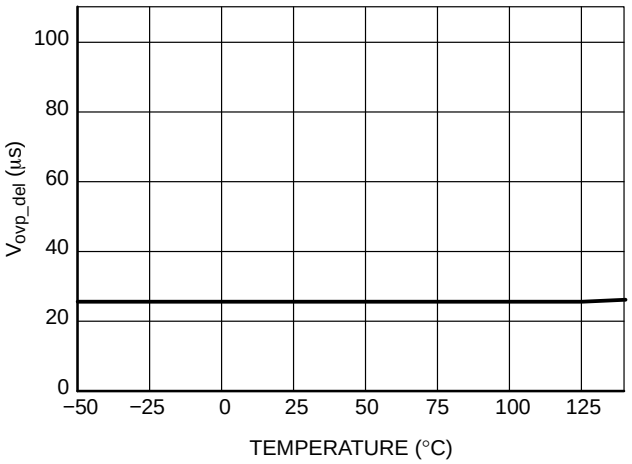


Figure 27.

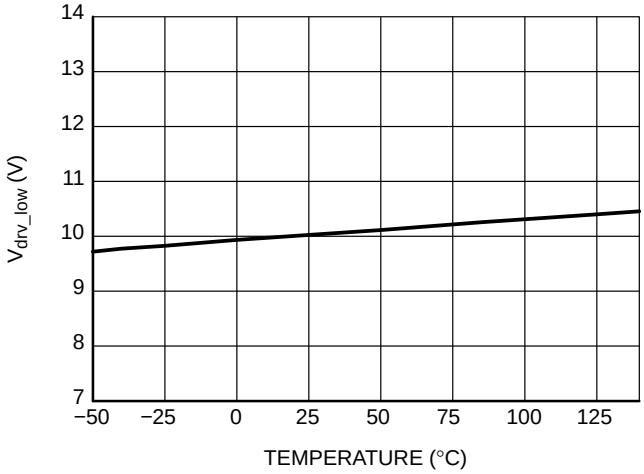


Figure 28.

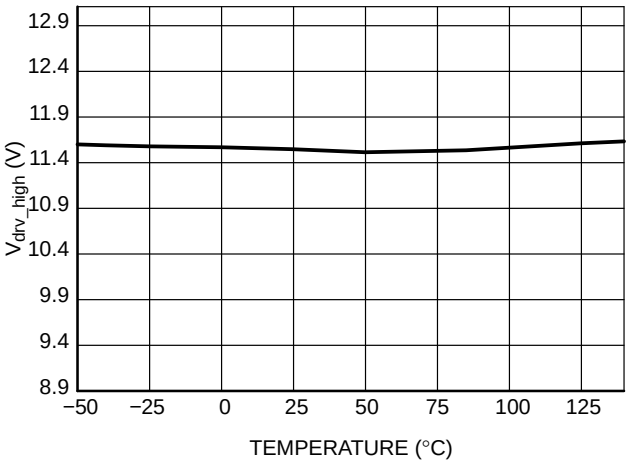


Figure 29.

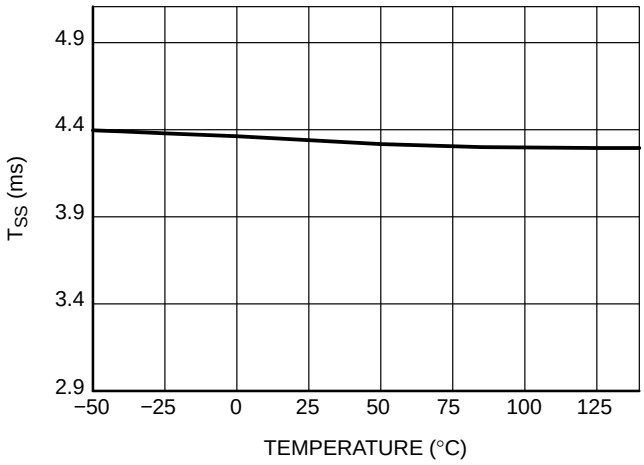


Figure 30.

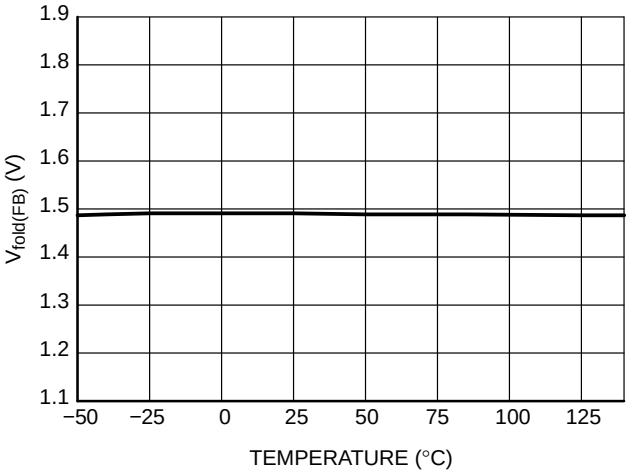


Figure 31.

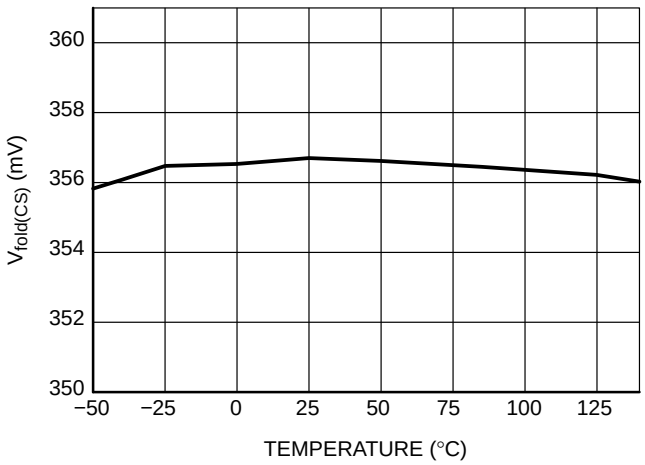


Figure 32.

TYPICAL CHARACTERISTICS

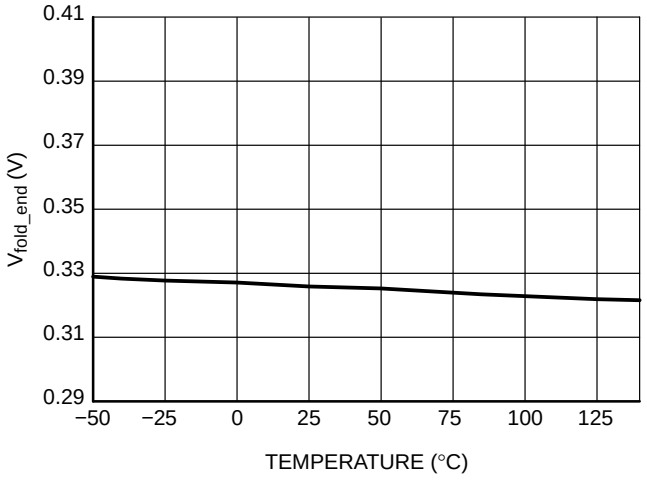


Figure 33.

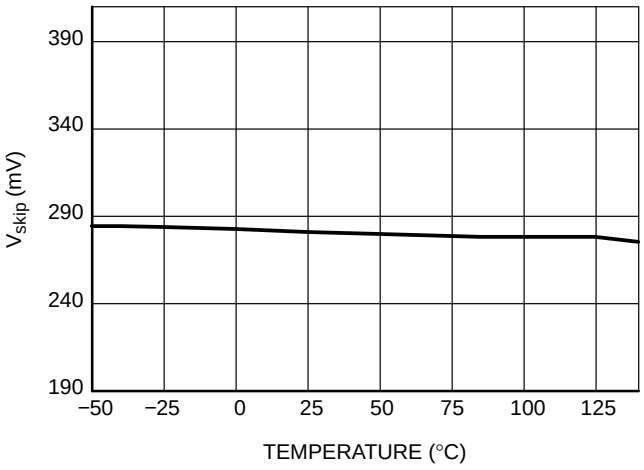


Figure 34.

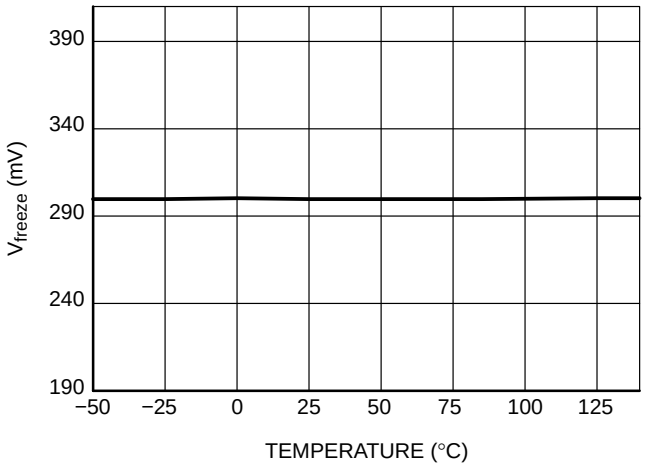


Figure 35.

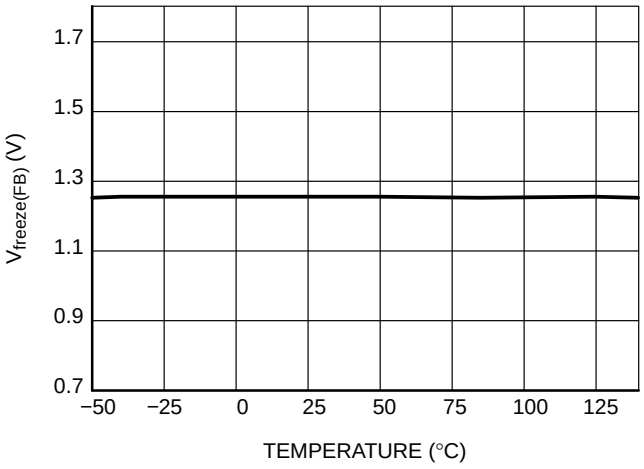


Figure 36.

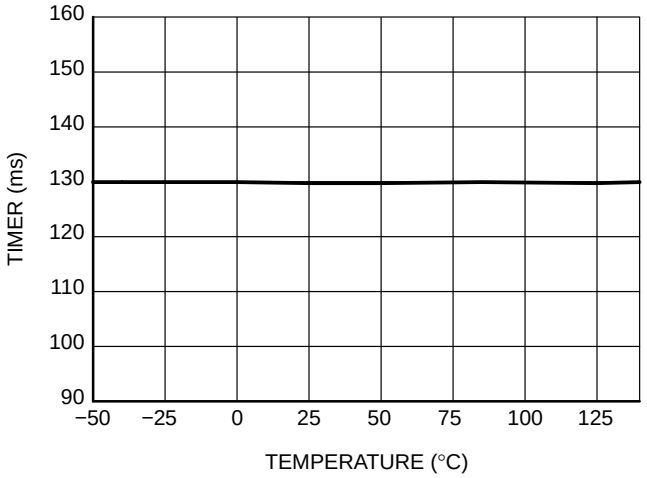


Figure 37.

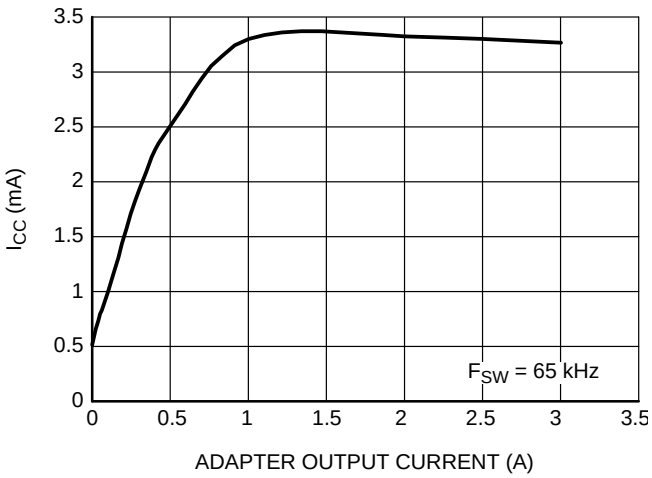


Figure 38. Controller Consumption vs. Adapter Output Current

TYPICAL CHARACTERISTICS

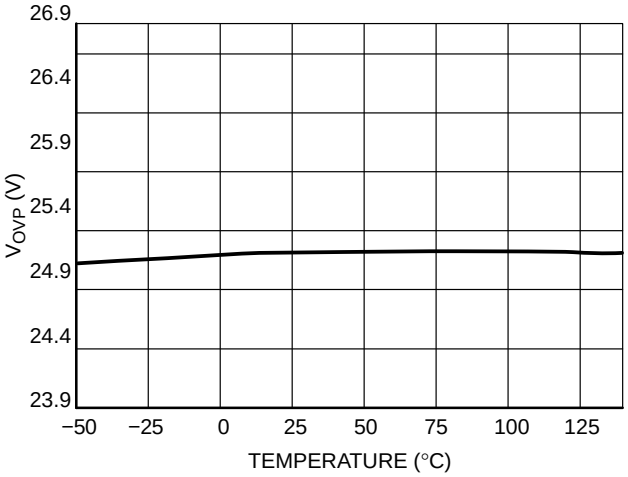


Figure 39.

APPLICATION INFORMATION

Introduction

The NCP1251 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. Capitalizing on the NCP120X series success, the NCP1251 packs all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a non−dissipative OPP.

- **Current−mode operation with internal ramp compensation**: Implementing peak current mode control at a fixed 65 kHz or 100 kHz, the NCP1251 offers an internal ramp compensation signal that can easily by summed with the sensed current. Sub harmonic oscillations are eliminated via the inclusion of a single resistor in series with the current−sense information.
- **Internal OPP**: By routing a portion of the negative voltage present during the on−time on the auxiliary winding to the dedicated OPP pin (pin 3), the user has a simple and non−dissipative means to alter the maximum peak current setpoint as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage down to –250 mV, then a peak current reduction down to 31.3% typical can be achieved. For an improved performance, the maximum voltage excursion on the sense resistor is limited to 0.8 V.
- **Low startup current**: Achieving a low no−load standby power always represents a difficult exercise when the controller draws a significant amount of current during start−up. Due to its proprietary architecture, the NCP1251 is guaranteed to draw less than 15 μA typical, easing the design of low standby power adapters.
- **EMI jittering**: An internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps by spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering remains active in frequency foldback mode.
- **Frequency foldback capability**: A continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of 1.5 V, the oscillator then starts to reduce its switching frequency as the feedback level continues to decrease. When the feedback pin reaches 1.05 V, the peak current setpoint is internally frozen and the frequency continues to decrease. It can go down to 26 kHz (typical) reached for a feedback level of roughly 350 mV. At this point, if the power continues to drop, the controller enters classical skip−cycle mode.
- **Internal soft−start**: A soft−start precludes the main power switch from being stressed upon start−up. In this controller, the soft−start is internally fixed to 4 ms. The soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- **OVP input**: The NCP1251 includes a latch input (pin 3) that can be used to sense an overvoltage condition on the adapter. If this pin is brought higher than the internal reference voltage V_{latch}, then the circuit permanently latches off. The V_{CC} pin is pulled down to a fixed level, keeping the controller latched. The latch reset occurs when the user disconnects the adapter from the mains and lets the V_{CC} falls below the V_{CC} reset.
- **Latched OVP on V_{CC}**: It is sometimes interesting to implement a circuit protection by sensing the V_{CC} level. This is what the NCP1251 does by monitoring its V_{CC} pin. When the voltage on this pin exceeds 25 V typical, the pulses are immediately stopped and the part latches off. The Vcc is maintained to 7 V typical and remains in this state until the user unplugs the power supply.
- **Short−circuit protection**: Short−circuit and especially over−load protections are difficult to implement for transformers with high leakage inductance between auxiliary and power windings (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8 V maximum peak current limit is activated (or less when OPP is used), an error flag is asserted and a time period starts, thanks to an internal timer. If the timer reaches completion while the error flag is still present, the controller stops the pulses and goes into a latch−off phase, operating in a low−frequency burst−mode. When the fault is cleared, the SMPS resumes operation. Please note that some versions offer an auto−recovery mode as described and some latch off in case of a short circuit.

Start−up Sequence

The NCP1251 start−up voltage is made purposely high to permit a large energy storage in a small V_{CC} capacitor value. This helps to operate with a small start−up current which, together with a small V_{CC} capacitor, will not hamper the start−up time. To further reduce the standby power, the start−up current of the controller is extremely low, below 15 μA maximum. The start−up resistor can therefore be connected to the bulk capacitor or directly to the mains input voltage to further reduce the power dissipation.

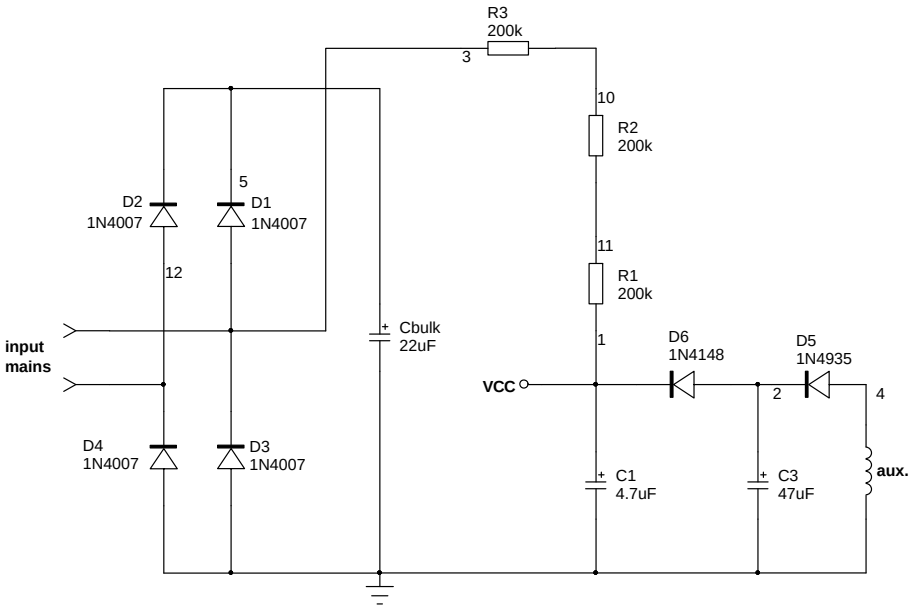


Figure 40. The Startup Resistor Can Be Connected to the Input Mains for Further Power Dissipation Reduction

The first step starts with the calculation of the V_{CC} capacitor which will supply the controller when it operates until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 ms and 20 ms. If we consider we need at least an energy reservoir for a t_1 time of 10 ms, the V_{CC} capacitor must be larger than:

$$CV_{CC} \geq \frac{I_{CC}t_1}{VCC_{on} - VCC_{min}} \geq \frac{3m \times 10m}{9} \geq 3.3\ \mu F \quad \text{(eq. 1)}$$

Let us select a 4.7 μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for the time t_1. The V_{CC} capacitor being known, we can now evaluate the charging current we need to bring the V_{CC} voltage from 0 to the VCC_{on} of the IC, 18 V typical. This current has to be selected to ensure a start−up at the lowest mains (85 V rms) to be less than 3 s (2.5 s for design margin):

$$I_{charge} \geq \frac{VCC_{on}C_{VCC}}{2.5} \geq \frac{18 \times 4.7\mu}{2.5} \geq 34\ \mu A \quad \text{(eq. 2)}$$

If we account for the 15 μA that will flow inside the controller, then the total charging current delivered by the start−up resistor must be 49 μA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when V_{CC} reaches the VCC_{on} of the controller:

$$I_{CVCC,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 49 μA, then the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{I_{CVCC,min}} \leq \frac{\frac{85 \times 1.414}{\pi} - 18}{49\mu} \leq 413.5\ k\Omega \quad \text{(eq. 4)}$$

This calculation is purely theoretical, and assumes a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the V_{CC} capacitor. Hence, a decrease in charging current and an increase of the start−up resistor, thus reducing the standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 413 kΩ resistor as suggested by Equation 4, the dissipated power at high line amounts to:

$$P_{Rstart-up} = \frac{V_{ac,peak}{}^2}{4R_{start-up}} = \frac{\left(230 \times \sqrt{2}\right)^2}{4 \times 413k} \quad \text{(eq. 5)}$$

$$= \frac{230^2}{0.827Meg} = 64\ mW$$

Now that the first V_{CC} capacitor has been selected, we must ensure that the self−supply does not disappear when in no−load conditions. In this mode, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the V_{CC} capacitor. If this ripple is too large, chances exist to touch the VCC_{min} and reset the controller into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 40 elegantly solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the V_{CC} pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the controller without jeopardizing the start−up time and standby power. A capacitor ranging from 22 to 47 μF is the typical value for this device.

One note on the start-up current. If reducing it helps to improve the standby power, its value cannot fall below a certain level at the minimum input voltage. Failure to inject

enough current (30 μA) at low line will turn a converter in fault into an auto-recovery mode since the SCR won't remain latched. To build a sufficient design margin, we recommend to keep at least 60 μA flowing at the lowest input line (80 V rms for 85 V minimum for instance). An excellent solution is to actually combine X2 discharge and start-up networks as proposed in Figure 13 of application note AND8488/D.

Internal Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the power switch on−time, this point dips to $-NV_{in}$, *N* being the turns ratio between the primary winding and the auxiliary winding. The negative plateau observed on Figure 42 will have an amplitude dependant on the input voltage. The idea implemented in this chip is to sum a portion of this negative swing with the 0.8 V internal reference level. For instance, if the voltage swings down to −150 mV during the on time, then the internal peak current set point will be fixed to 0.8 − 0.150 = 650 mV. The adopted principle appears in Figure 42 and shows how the final peak current set point is constructed.

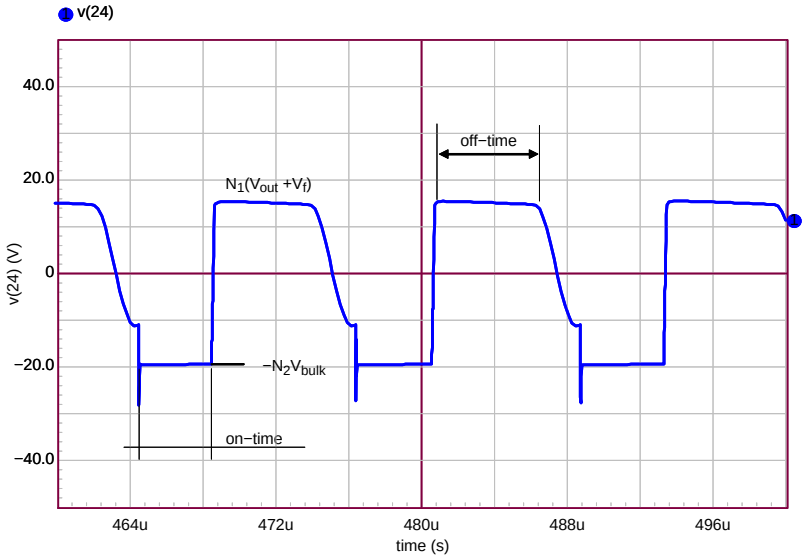


Figure 41. The Signal Obtained on the Auxiliary Winding Swings Negative During the On−time

Let's assume we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to a 20% reduction or a set point voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 640m - 800m = -160\ mV \qquad \text{(eq. 6)}$$

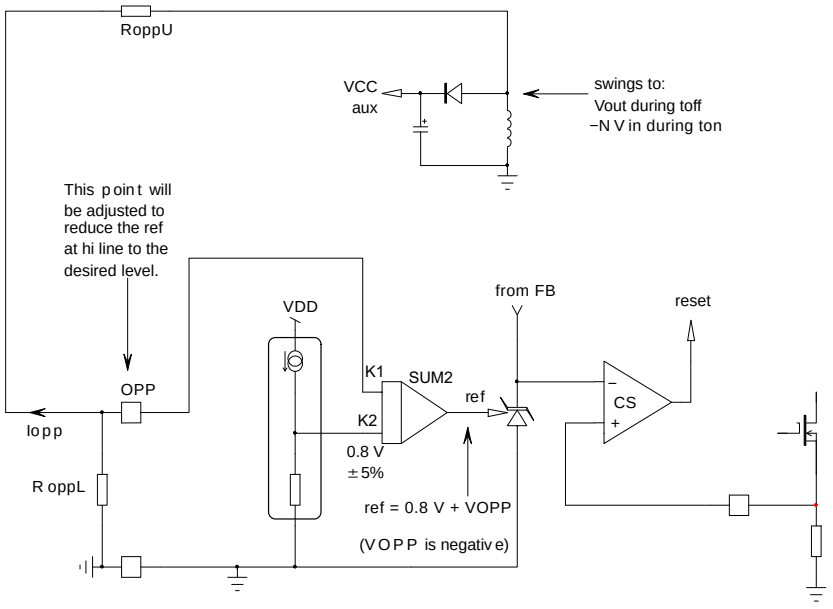


Figure 42. The OPP Circuitry Affects the Maximum Peak Current Set Point by Summing a Negative Voltage to the Internal Voltage Reference

Let us assume that we have the following converter characteristics:

V_{out} = 19 V
V_{in} = 85 to 265 V_{rms}
$N_1 = N_p:N_s$ = 1:0.25
$N_2 = N_p:N_{aux}$ = 1:0.18

Given the turns ratio between the primary and the auxiliary windings, the on−time voltage at high line (265 Vac) on the auxiliary winding swings down to:

$$V_{aux} = -N_2 V_{in,max} = -0.18 \times 375 = -67.5\ V \qquad \text{(eq. 7)}$$

To obtain a level as imposed by Equation 6, we need to install a divider featuring the following ratio:

$$Div = \frac{0.16}{67.5} \approx 2.4m \qquad \text{(eq. 8)}$$

If we arbitrarily fix the pull−down resistor R_{OPPL} to 1 kΩ, then the upper resistor can be obtained by:

$$R_{OPPU} = \frac{67.5 - 0.16}{0.16/1k} \approx 421\ k\Omega \qquad \text{(eq. 9)}$$

If we now plot the peak current set point obtained by implementing the recommended resistor values, we obtain the following curve (Figure 43):

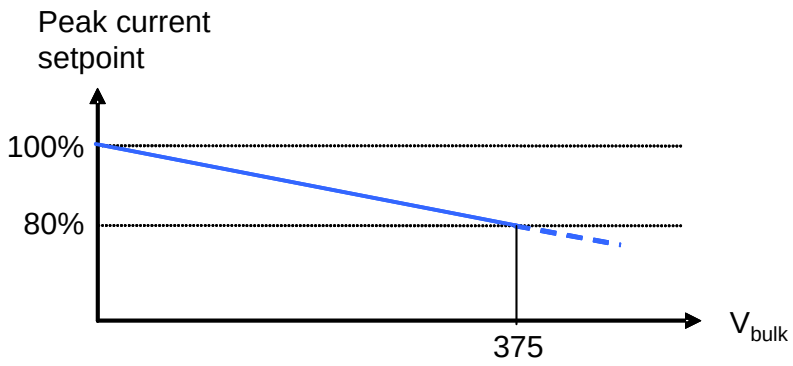


Figure 43. The Peak Current Regularly Reduces Down to 20% at 375 Vdc

The OPP pin is surrounded by Zener diodes stacked to protect the pin against ESD pulses. These diodes accept some peak current in the avalanche mode and are designed to sustain a certain amount of energy. On the other side, negative injection into these diodes (or forward bias) can cause substrate injection which can lead to an erratic circuit behavior. To avoid this problem, the pin is internally clamped slightly below –300 mV which means that if more current is injected before reaching the ESD forward drop, then the maximum peak reduction is kept to 40%. If the voltage finally forward biases the internal zener diode, then care must be taken to avoid injecting a current beyond –2 mA. Given the value of R_{OPPU}, there is no risk in the present example.

Finally, please note that another comparator internally fixes the maximum peak current set point to 0.8 V even if the OPP pin is inadvertently biased above 0 V.

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change to the traditional fixed−frequency type of operation. This controller implements a switching frequency foldback when the feedback voltage passes below a certain level, V_{fold}, set around 1.5 V. At this point, the oscillator enters frequency foldback and reduces its switching frequency. The peak current setpoint follows the feedback pin until its level reaches 1.05 V. Below this value, the peak current freezes to V_{fold}/4.2 (250 mV or 31% of the maximum 0.8 V setpoint) and the only way to further reduce the transmitted power is to reduce the operating frequency down to 26 kHz. This value is reached at a voltage feedback level of 350 mV typically. Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise−free performance in no−load conditions. Figure 44 depicts the adopted scheme for the part.

The NCP1251F version offers a means to improve light−load efficiency by folding the switching frequency sooner compared to the other versions. With the 1251 A, B and C versions, the minimum frequency is reached for V_{FB} equals 350 mV. With the 1251F, this minimum frequency will be obtained at a feedback voltage equal to 1.5 V, naturally offering a better efficiency for lighter load conditions. Figure 45 portrays the specific foldback scheme implemented in the NCP1251F.

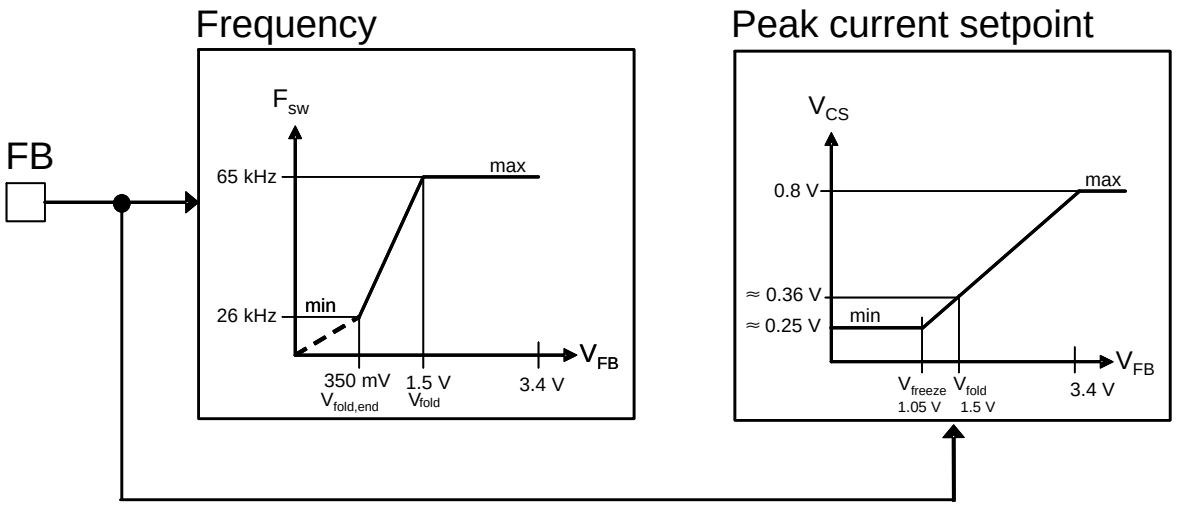


Figure 44. By Observing the Voltage on the Feedback Pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

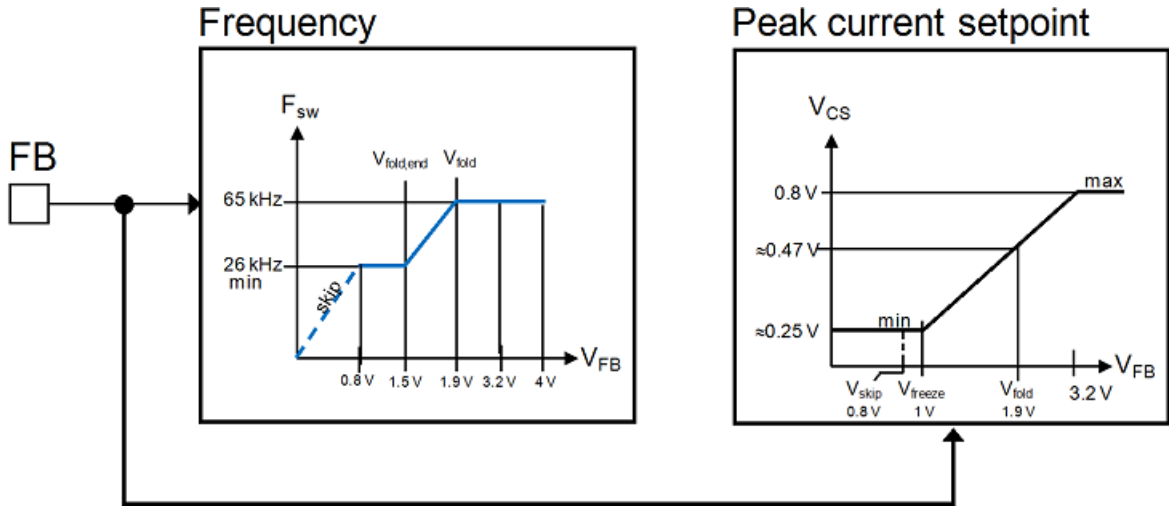


Figure 45. with NCP1251F, the frequency foldback occurs sooner as the load gets lighter.

Auto−Recovery Short−Circuit Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than 100 ms, the driving pulses are stopped and the V_{CC} pin slowly goes down to around 7 V. At this point, the controller wakes−up and the V_{CC} builds up again due to the resistive starting network. When V_{CC} reaches VCC_{ON}, the controller attempts to re−start, checking for the absence of the fault. If the fault is still there, the supply enters another cycle of so−called hiccup mode. If the fault has cleared, the power supply resumes normal operation. Please note that the soft−start is activated during each of the re−start sequence.

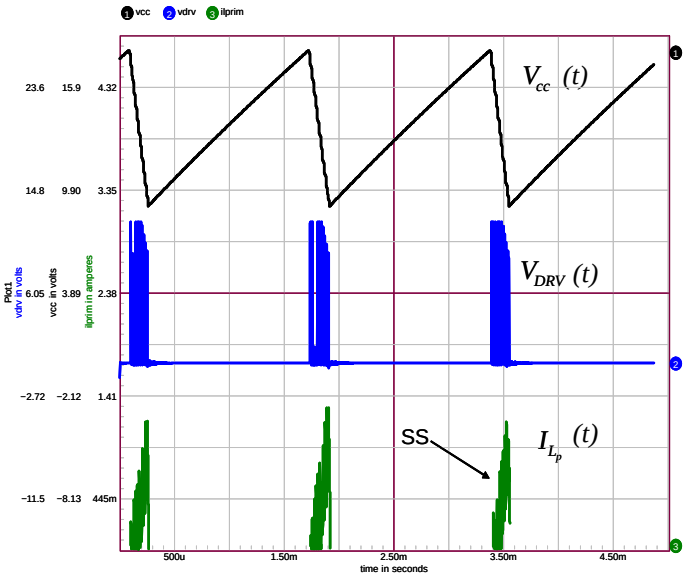


Figure 46. An Auto−Recovery Hiccup Mode is Activated for Faults Longer than 100 ms

Slope Compensation

The NCP1251 includes an internal ramp compensation signal. This is the buffered oscillator clock delivered only during the on time. Its amplitude is around 2.5 V at the maximum duty−cycle. Ramp compensation is a known means used to cure sub harmonic oscillations in Continuous Conduction Mode (CCM) operated current−mode converters. These oscillations take place at half the switching frequency and occur only during CCM with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50% and 100% of the inductor downslope. Figure 47 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the off time.

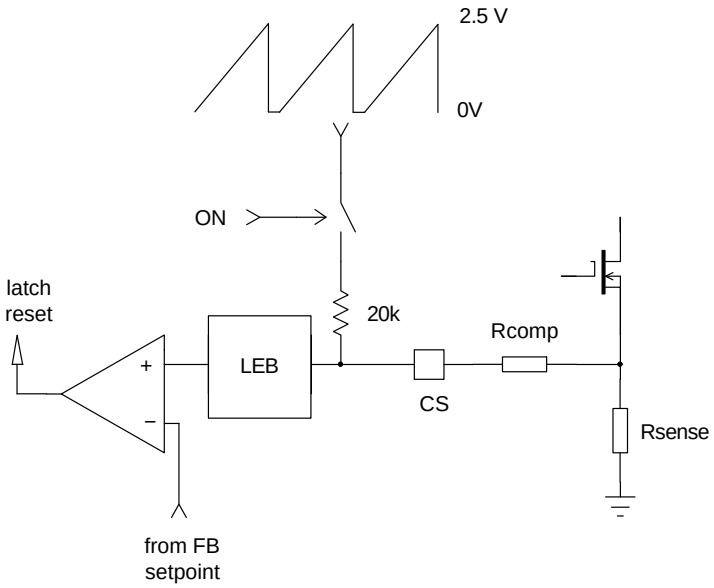


Figure 47. Inserting a Resistor in Series with the Current Sense Information Brings Ramp Compensation and Stabilizes the Converter in CCM Operation.

In the NCP1251 controller, the oscillator ramp features a 2.5 V swing reached at a 80% duty−ratio. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak}}{D_{max}T_{SW}} = \frac{2.5}{0.8 \times 15\mu} \quad \text{(eq. 10)}$$

$$= 208\ \text{kV/s or } 208\ \text{mV/}\mu\text{s}$$

In our flyback design, let's assume that our primary inductance L_p is 770 μH, and the SMPS delivers 19 V with a N_p:N_s ratio of 1:0.25. The off−time primary current slope S_p is thus given by:

$$S_p = \frac{\left(V_{out} + V_f\right)\frac{N_p}{N_s}}{L_p} = \frac{(19 + 0.8) \times 4}{770\mu} = 103\ \text{kA/s} \quad \text{(eq. 11)}$$

Given a sense resistor of 330 mΩ, the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} = 103\text{k} \times 0.33 \quad \text{(eq. 12)}$$

$$= 34\ \text{kV/s or } 34\ \text{mV/}\mu\text{s}$$

If we select 50% of the downslope as the required amount of ramp compensation, then we shall inject a ramp whose slope is 17 mV/μs. Our internal compensation being of 208 mV/μs, the divider ratio (*divratio*) between R_{comp} and the internal 20 kΩ resistor is:

$$\text{divratio} = \frac{17\text{m}}{208\text{m}} = 0.082 \quad \text{(eq. 13)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp} \cdot \text{divratio} = 20\text{k} \times 0.082 \approx 1.6\ \text{k}\Omega \quad \text{(eq. 14)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small capacitor of 100 pF, from the current sense pin to the controller ground for an improved immunity to the noise. Please make sure both components are located very close to the controller.

Latching Off the Controller

The OPP pin not only allows a reduction of the peak current set point in relationship to the line voltage, it also offers a means to permanently latch−off the part. When the part is latched−off, the V_{CC} pin is internally pulled down to around 7 V and the part stays in this state until the user cycles the V_{CC} down and up again, e.g. by un−plugging the converter from the mains outlet. It is important to note that the SCR maintains its latched state as long as the injected current stays above the minimum value of 30 μA. As the SCR delatches for an injected current below this value, it is the designer duty to make sure the injected current is high enough at the lowest input voltage. Failure to maintain a sufficiently high current would make the device auto recover. A good design practice is to ensure at least 60 μA at the lowest input voltage. The latch detection is made by observing the OPP pin by a comparator featuring a 3 V reference voltage. However, for noise reasons and in particular to avoid the leakage inductance contribution at turn off, a 1 μs blanking delay is introduced before the output of the OVP comparator is checked. Then, the OVP comparator output is validated only if its high−state duration lasts a minimum of 600 ns. Below this value, the event is ignored. Then, a counter ensures that 4 successive OVP events have occurred before actually latching the part. There are several possible implementations, depending on the needed precision and the parameters you want to control.

The first and easiest solution is the additional resistive divider on top of the OPP one. This solution is simple and inexpensive but requires the insertion of a diode to prevent disturbing the OPP divider during the on time.

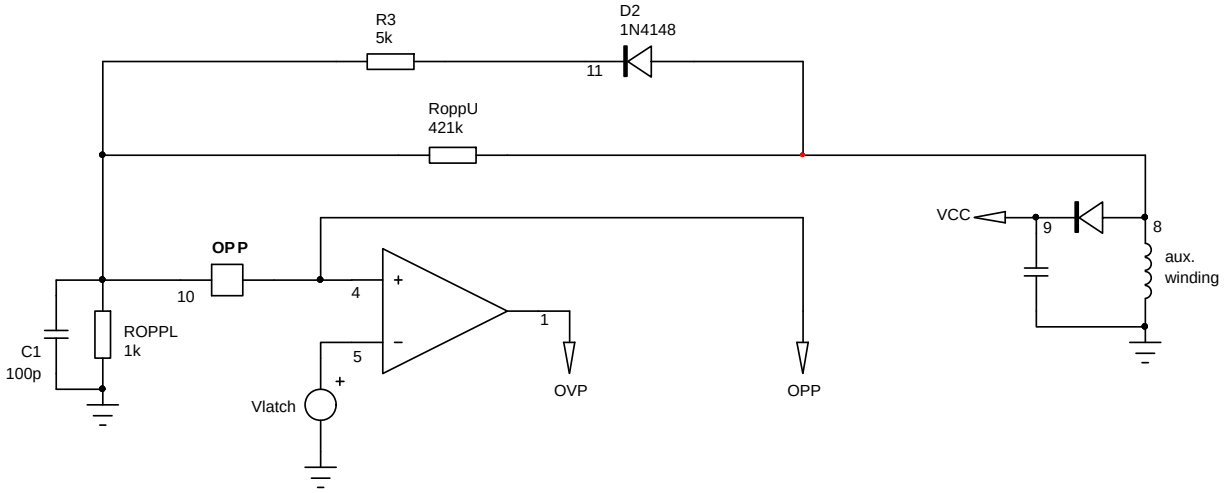


Figure 48. A Simple Resistive Divider Brings the OPP Pin Above 3 V in Case of a V_{CC} Voltage Runaway above 18 V

First, calculate the OPP network with the above equations. Then, suppose we want to latch off our controller when V_{out} exceeds 25 V. On the auxiliary winding, the plateau reflects the output voltage by the turns ratio between the power and the auxiliary winding. In case of voltage runaway for our 19 V adapter, the plateau will go up to:

$$V_{aux,OVP} = 25 \times \frac{0.18}{0.25} = 18\ V \qquad \text{(eq. 15)}$$

Since our OVP comparator trips at a 3 V level, across the 1 kΩ selected OPP pulldown resistor, it implies a 3 mA current. From 3 V to go up to 18 V, we need an additional 15 V. Under 3 mA and neglecting the series diode forward drop, it requires a series resistor of:

$$R_{OVP} = \frac{V_{latch} - V_{VOP}}{V_{OVP}/R_{OPPL}} = \frac{18 - 3}{3/1k} = \frac{15}{3m} = 5\ k\Omega \quad \text{(eq. 16)}$$

In nominal conditions, the plateau establishes to around 14 V. Given the divide−by−6 ratio, the OPP pin will swing to 14/6 = 2.3 V during normal conditions, leaving 700 mV margin. A 100 pF capacitor can be added between the OPP pin and GND to improve noise immunity and avoid erratic trips in presence of external surges. Do not increase this capacitor too much otherwise the OPP signal will be affected by the integrating time constant.

A second solution for the OVP detection alone, is to use a Zener diode wired as recommended by.

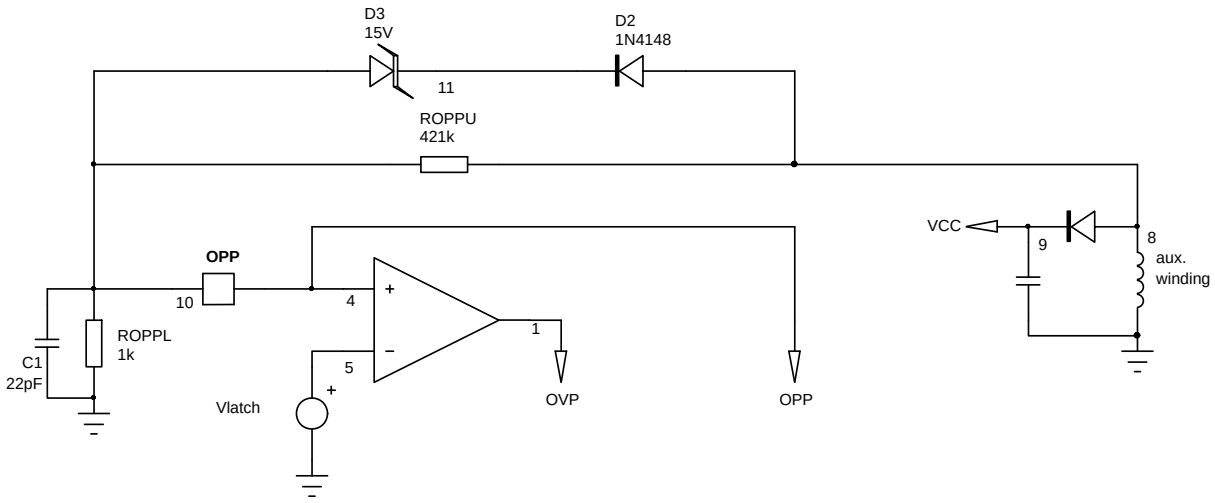


Figure 49. A Zener Diode in Series with a Diode Helps to Improve the Noise Immunity of the System

For this configuration to maintain an 18 V level, we have selected a 15 V Zener diode. In nominal conditions, the voltage on the OPP pin is almost 0 V during the off time as the Zener is fully blocked. This technique clearly improves the noise immunity of the system compared to that obtained from a resistive string as in Figure 48. Please note the reduction of the capacitor on the OPP pin to 10 pF − 22 pF. This capacitor is necessary because of the potential spike coupling through the Zener parasitic capacitance from the bias winding due to the leakage inductance. Despite the 1 μs blanking delay at turn off. This spike is energetic enough to charge the added capacitor C_1 and given the time constant, could make it discharge slower, potentially disturbing the blanking circuit. When implementing the Zener option, it is important to carefully observe the OPP pin voltage (short probe connections!) and check that enough margin exists to that respect.

Over Temperature Protection

In a lot of designs, the adapter must be protected against thermal runaways, e.g. when the temperature inside the adapter box increases above a certain value. Figure 50 shows how to implement a simple OTP using an external NTC and a series diode. The principle remains the same: make sure the OPP network is not affected by the additional NTC hence the presence of this isolation diode. When the NTC resistance decreases as the temperature increases, the voltage on the OPP pin during the off time will slowly increase and, once it passes 3 V for 4 consecutive clock cycles, the controller will permanently latch off.

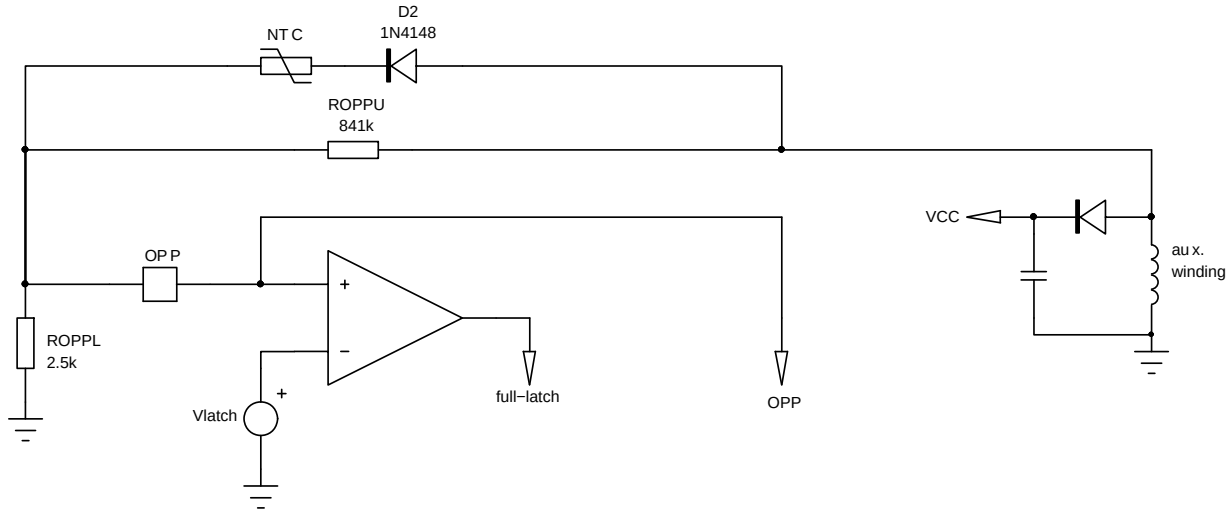


Figure 50. The Internal Circuitry Hooked to Pin 3 Can Be Used to Implement Over Temperature Protection (OTP)

Back to our 19 V adapter, we have found that the plateau voltage on the auxiliary diode was 13 V in nominal conditions. We have selected an NTC which offers a resistance of 470 kΩ at 25°C and drops to 8.8 kΩ at 110°C. If our auxiliary winding plateau is 14 V and we consider a 0.6 V forward drop for the diode, then the voltage across the NTC in fault mode must be:

$$V_{NTC} = 14 - 3 - 0.6 = 10.4\ V \qquad \text{(eq. 17)}$$

Based on the 8.8 kΩ NTC resistor at 110 °C, the current through the device must be:

$$I_{NTC} = \frac{10.4}{8.8k} \approx 1.2\ mA \qquad \text{(eq. 18)}$$

As such, the bottom resistor R_{OPPL}, can easily be calculated:

$$R_{OPPL} = \frac{3}{1.2m} = 2.5\ k\Omega \qquad \text{(eq. 19)}$$

Now that the pulldown OPP resistor is known, we can calculate the upper resistor value R_{OPPU} to adjust the power limit at the chosen output power level. Suppose we need a 200 mV decrease from the 0.8 V set point and the on−time swing on the auxiliary anode is −67.5 V, then we need to drop over R_{OPPU} a voltage of:

$$V_{ROPPU} = 67.5 - 0.2 = 67.3\ V \qquad \text{(eq. 20)}$$

The current flowing in the pulldown resistor R_{OPPL} in this condition will be:

$$I_{ROPPU} = \frac{200m}{2.5k} = 80\ \mu A \qquad \text{(eq. 21)}$$

The R_{OPPU} value is therefore easily derived:

$$R_{OPPU} = \frac{67.3}{80\mu} = 841\ k\Omega \qquad \text{(eq. 22)}$$

Combining OVP and OTP

The OTP and Zener−based OVP can be combined together as illustrated by Figure 51.

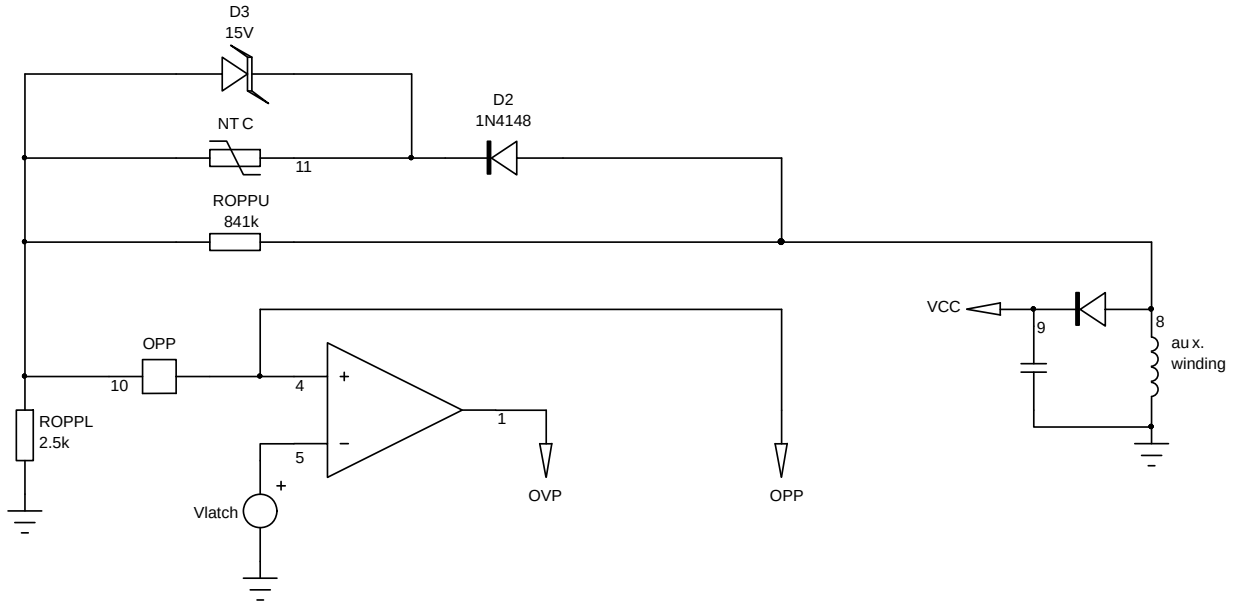


Figure 51. With the NTC Back in Place, the Circuit Nicely Combines OVP, OTP and OPP on the Same Pin

In nominal V_{CC} / output conditions, when the Zener is not activated, the NTC can drive the OPP pin and trigger the adapter in case of an over temperature. During nominal temperature if the loop is broken, the voltage runaway will be detected and the controller will shut down the converter.

In case the OPP pin is not used for either OPP or OVP, it can simply be grounded.

Filtering the Spikes

The auxiliary winding is the seat of spikes that can couple to the OPP pin via the parasitic capacitances exhibited by the Zener diode and the series diode. To prevent an adverse triggering of the Over Voltage Protection circuitry, it is possible to install a small *RC* filter before the detection network. Typical values are those given in Figure 52 and must be selected to provide the adequate filtering function without degrading the stand−by power by an excessive current circulation.

Latched OVP on V_{CC}

The V_{CC} pin is permanently monitored by a comparator. When the V_{CC} exceeds 25.5 V (typical), all pulses are immediately stopped and the V_{CC} falls to the SCR latched-level around 7 V typical. The controller remains in this state as long as a sufficient current flows in the SCR, at least 30 μA. We recommend to put a design margin there, with a minimum current around 60 μA at the lowest input line. With the C version, the OVP on V_{CC} is autorecovery.

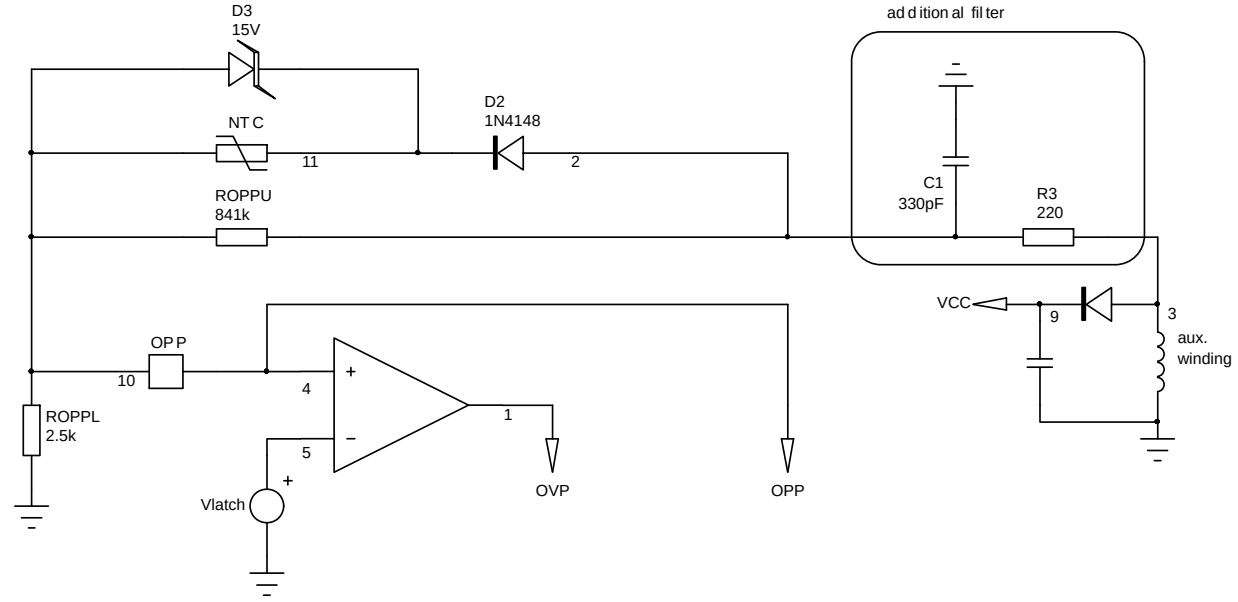


Figure 52. A Small *RC* Filter Avoids the Fast Rising Spikes from Reaching the Protection Pin of the NCP1251 in Presence of Energetic Perturbations Superimposed on the Input Line

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

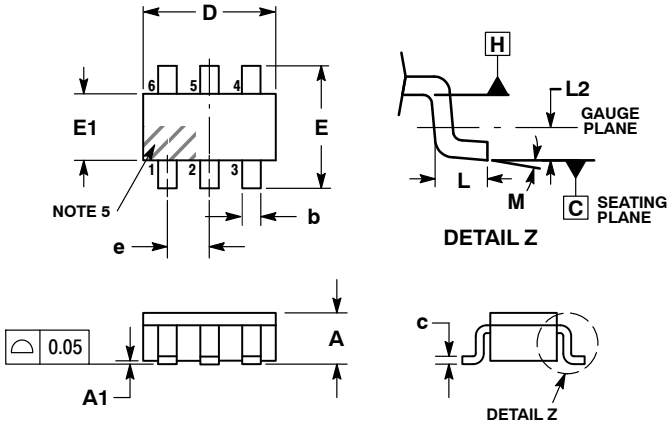
ON Semiconductor®



SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

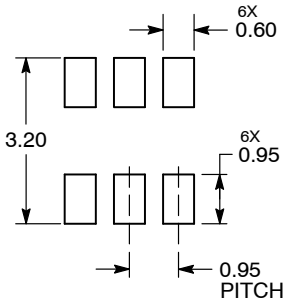
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

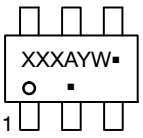
RECOMMENDED SOLDERING FOOTPRINT*



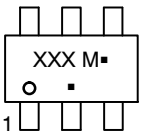
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

DOCUMENT NUMBER:	**98ASB14888C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOP−6**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊