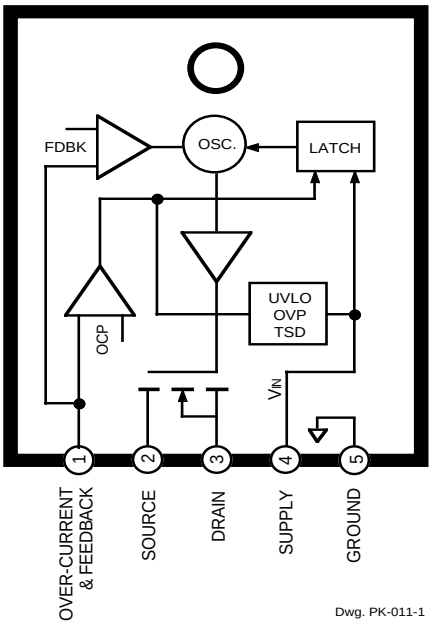
Series STR-F6600

Data Sheet
28102.8

INTERIM DATA SHEET
(Subject to change without notice)
February 22, 2000

OFF-LINE QUASI-RESONANT FLYBACK SWITCHING REGULATORS



ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Control Supply Voltage, V_{IN} . . . . . **35 V**
Drain-Source Voltage, V_{DS}
- Series STR-F6620 . . . . . **450 V**
- Series STR-F6630 . . . . . **500 V**
- Series STR-F6650 . . . . . **650 V**
- Series STR-F6670 . . . . . **900 V**

Drain Switching Current, I_D . . . **See Table**
Peak Drain Current, I_{DM} . . . . . **See Table**
Avalanche Energy, E_{AS} . . . . . **See Table**
OCP/FB Voltage Range,
V_{OCP} . . . . . **-0.3 V to +6 V**
Package Power Dissipation, P_D
- control (V_{IN} x $I_{IN(ON)}$) . . . . . **0.8 W**
- total . . . . . **See Graph**

FET Channel Temperature, T_J . . . **+150°C**
Internal Frame Temperature, T_F . . **+125°C**
Operating Temperature Range,
T_A . . . . . **-20°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-40°C to +125°C**

The Series STR-F6600 is specifically designed to satisfy the requirements for increased integration and reliability in off-line quasi-resonant flyback converters. The series incorporates a primary control and drive circuit with discrete avalanche-rated power MOSFETs.

Covering the power range from below 25 watts up to 300 watts for 100/115/230 VAC inputs, and up to 150 watts for 85 to 265 VAC universal input, these devices can be used in a range of applications, from battery chargers and set top boxes, to televisions, monitors, and industrial power supply units.

Cycle-by-cycle current limiting, under-voltage lockout with hysteresis, over-voltage protection, and thermal shutdown protects the power supply during the normal overload and fault conditions. Over-voltage protection and thermal shutdown are latched after a short delay. The latch may be reset by cycling the input supply. Low-current startup and a low-power standby mode selected from the secondary circuit completes a comprehensive suite of features. The series is provided in a five-pin overmolded TO-3P style package, affording dielectric isolation without compromising thermal characteristics.

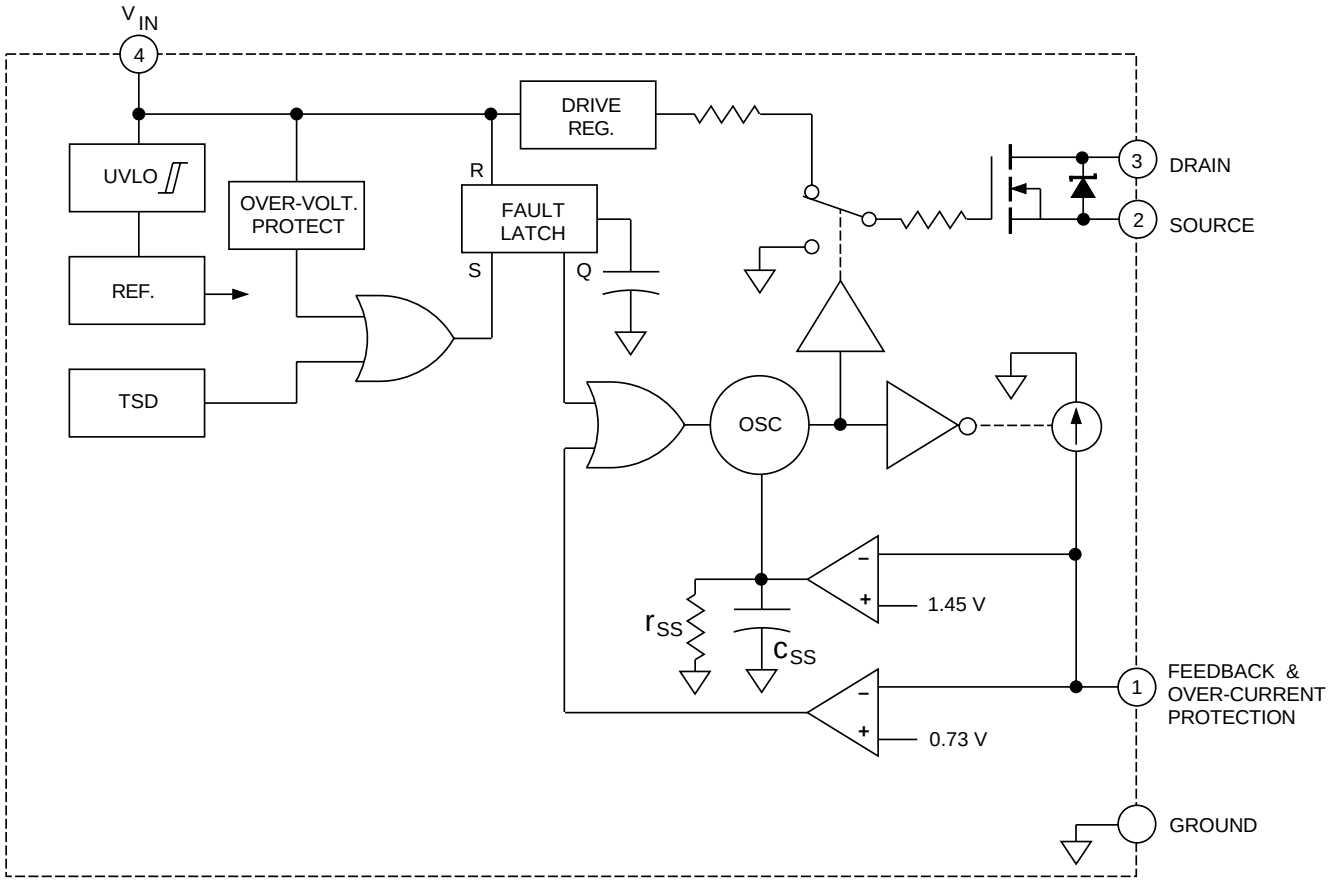
FEATURES

- Flyback Operation with Quasi-Resonant Soft Switching for Low Power Dissipation and EMI
- Rugged Avalanche-Rated MOSFET
- Choice of MOSFET Voltage and $r_{DS(on)}$
- Full Over-Current Protection (no blanking)
- Under-Voltage Lockout with Hysteresis
- Over-Voltage Protection
- Direct Voltage Feedback
- Low Start-up Current (<400 µA)
- Low-Frequency, Low-Power Standby Operation
- Overmolded 5-Pin Package

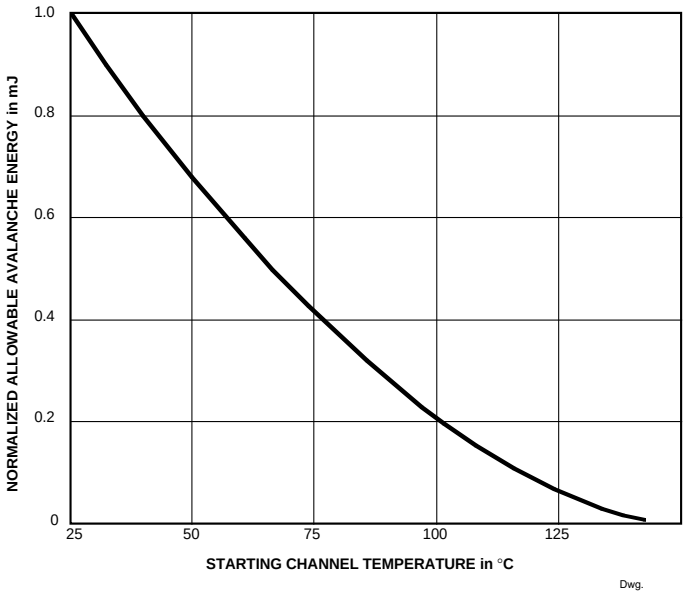
Always order by complete part number, e.g., **STR-F6652** .

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FUNCTIONAL BLOCK DIAGRAM



Dwg. FK-002-6



Dwg.

Allowable package power dissipation curves are shown on page 10.

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OUTPUT MAXIMUM RATINGS at T_A = +25°C

Part Number	V_{DSS} (V)	$r_{DS(on)}$ (Ω)	E_{AS} (mJ)*	I_D (A)†	I_{DM} (A)	P_{OUT} (W)	at V_{IN} (V rms)
STR-F6624	450	0.92	204	16	19	98 130	100 120
STR-F6626	450	0.58	327	16	26	145 190	100 120
STR-F6628	450	0.35	647	22	36	225 290	100 120
STR-F6632	500	2.54	7.4	9.0	11.2	36 50	100 120
STR-F6652	650	2.8	126	7.9	10	40 86	85-265 220
STR-F6653	650	1.95	260	5.6	14	58 120	85-265 220
STR-F6654	650	1.15	399	9.7	18	92 190	85-265 220
STR-F6656	650	0.71	521	16	25	150 300	85-265 220
STR-F6672	900	7.7	163	4.6	6.4	25 (no heatsink) 50 (with heat sink)	220 220
STR-F6674	900	4.49	242	6.0	9.2	28 76	85-265 220
STR-F6676	900	2.81	275	7.8	12	44 115	85-265 220

* Derate per graph, page 2

† Derate per graph, page 12

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{IN} = 18 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
On-State Voltage	V_{INT}	Turn-on, increasing V_{IN}	14.4	16	17.6	V
Under-Voltage Lockout	V_{INQ}	Turn-off, decreasing V_{IN}	9.0	10	11	V
Over-Voltage Threshold	$V_{OVP(th)}$	Turn-off, increasing V_{IN}	20.5	22.5	24.5	V
Drain-Source Breakdown Voltage	$V_{BR(DSS)}$	I_D = 300 µA	V_{DS} max	–	–	V
Drain Leakage Current	I_{DSS}	At V_{DS} max	–	–	300	µA
On-State Resistance	$r_{DS(ON)}$	V_S = 10 V, I_D = 0.9 A, T_J = +25°C	–	–	see table	Ω
Maximum Off Time	t_{off}	Drain waveform high	45	–	55	µs
Minimum Pulse Duration for Input of Quasi-Resonant Signals	$t_{w(th)}$	Drain waveform high[1]	–	–	1.0	µs
Minimum Off Time	t_{off}	Drain waveform high[1]	–	–	1.5	µs
Feedback Threshold Voltage	V_{FDBK}	Drain waveform low to high[1]	0.68	0.73	0.78	V
		Oscillation synchronized[2]	1.3	1.45	1.6	V
Over-Current Protection/Feedback Sink Current	$I_{OCP/FB}$	$V_{OCP/FB}$ = 1.0 V	1.2	1.35	1.5	mA
Latch Holding Current	$I_{IN(OVP)}$	V_{IN} reduced from 24.5 V to 8.5 V	–	–	400	µA
Latch Release Voltage	V_{IN}	$I_{IN} \leq$ 20 µA, V_{IN} reduced from 24.5 V	6.6	–	8.4	V
Switching Time	t_f	V_{DD} = 200 V, I_D = 0.9 A	–	–	250	ns
Supply Current	$I_{IN(ON)}$	Operating[3]	–	–	30	mA
	$I_{IN(OFF)}$	Increasing V_{IN} prior to oscillation	–	–	100	µA
Insulation RMS Voltage	$V_{WM(RMS)}$	All terminals simultaneous reference to a metal plate against the backside	2000	–	–	V
Thermal Resistance	$R_{\theta JM}$	Output channel to mounting frame	–	–	1.75	°C/W
Thermal Shutdown	T_J		140	–	–	°C

Notes: Typical Data is for design information only.

1. Feedback is square wave, V_{IM} = 2.2 V, t_h = 1 µs, t_l = 35 µs.
2. For quasi-resonant operation, the input signal must be longer than $t_{w(th)}$ and greater than V_{FDBK}.
3. Feedback is square wave, V_{IM} = 2.2 V, t_h = 4 µs, t_l = 1 µs.

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Functional Description and Operation

The voltage on the V_{IN} terminal (pin 4) controls startup and shutdown of the Series STR-F6600 devices.

Figure 1 shows a typical start up circuit. The V_{IN} terminal voltage during startup is shown in figure 2.

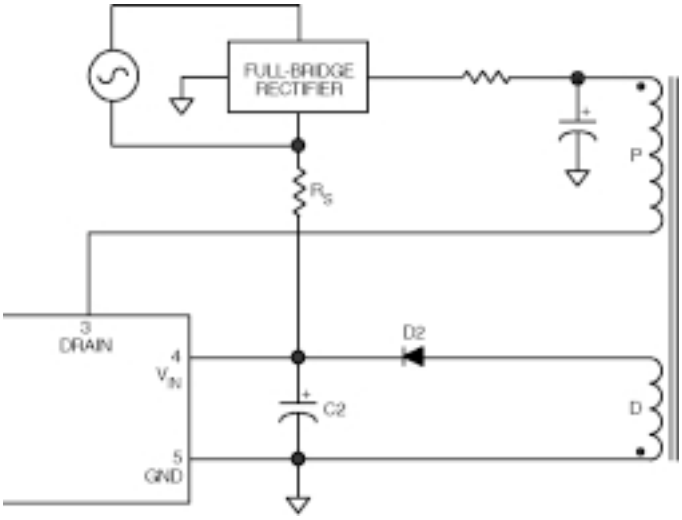


Figure 1 – Start-Up Circuit

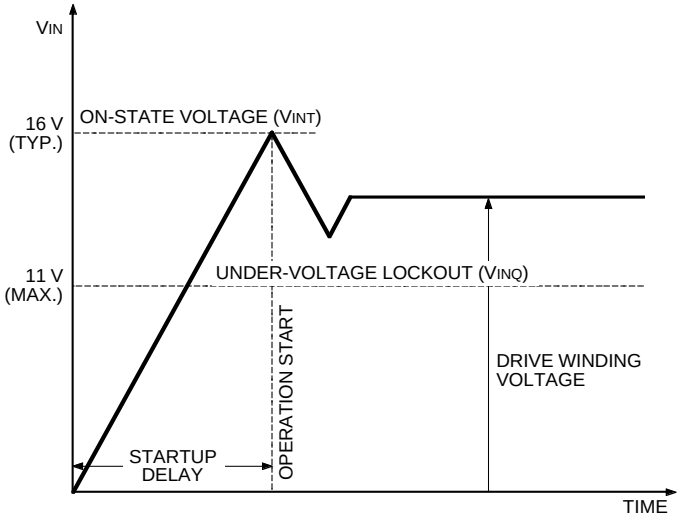


Figure 2 – Waveform of V_{IN} Terminal Voltage at Startup

At startup, C2 is charged through the startup resistor R_S. When the V_{IN} terminal voltage reaches 16 V (typ.), the control circuit enables regulator operation. Once the regulator starts, it draws up to 30 mA from C2 causing the voltage on C2 to fall momentarily. Once the regulator output voltage is established, the drive winding D starts to charge C2 via D2. The voltage on C2 thus recovers to the nominal drive voltage (18 V).

As shown in figure 3, the input current is below 100 µA (at $T_M = 25^{\circ}C$) prior to control circuit turn on. The latch circuit holding current is 400 µA (max.). To ensure latch operation, the current in R_S at the lowest ac input voltage should be at least 500 µA.

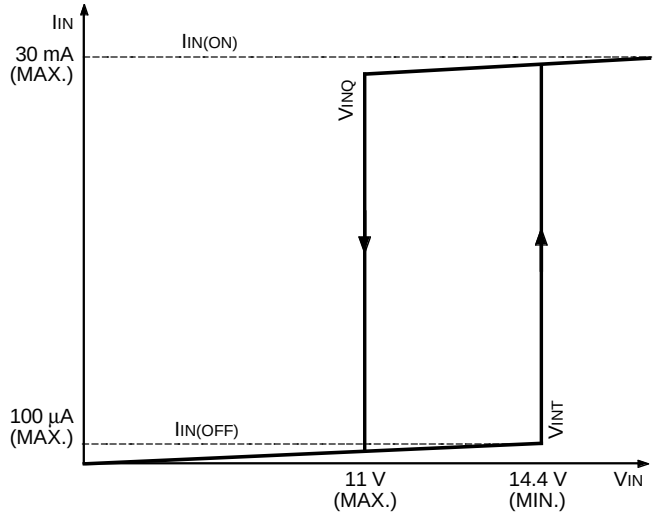


Figure 3 – Supply Terminal Current, I_{IN}

The value of R_S thus determines the charge time of C2 and thus the startup delay. R_S is typicaly 68 kΩ for wide operation (90 V ac to 265 V ac) and 100 kΩ for 220 volt ac operation.

The choice of C2 is a compromise between an acceptable startup delay (in conjunction with R_S) and a hold-up time sufficient to keep pin 4 above its under-voltage shutdown threshold of 11 V. Typically C2 is in the range of 47 µF to 100 µF.

continued, next page...

Functional Description and Operation (cont'd)

The drive winding voltage is set such that in normal operation the C2 voltage is above the specified maximum shutdown voltage (11 V) and below the specified minimum over-voltage threshold (20.5 V).

In applications where there is a significant variation in load current, the V_{IN} terminal voltage may vary, as shown in figure 4. This is due to peak charging of C2. In this case, adding a resistor in the range of a few ohms to tens of ohms in series with the rectifier diode D2 will bring the voltage variation within limits.

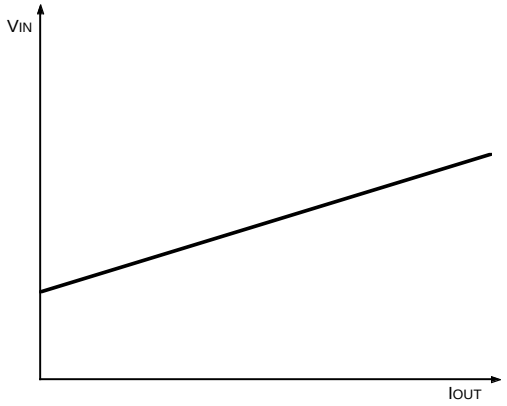


Figure 4 – Output Current I_{OUT} – Terminal Voltage V_{IN}

Soft Start, Quasi Resonant and Voltage Regulation

Refer to the Functional Block Diagram and the Typical Application Diagram (figure 6). The internal oscillator uses the charge/discharge of an internal 4700 pF capacitor (c_{SS}) to generate the MOSFET drive signals.

The regulator has two modes of operation:

1. fixed 50 µs off time (soft start) and

2. demagnetization sensing quasi-resonant mode — normal operation.

In both cases, voltage regulation is achieved by taking the composite optocoupled voltage error and superimposed drain current ramp (current-mode control) and comparing this to an internal 0.73 V reference. The FBK/OCP comparator output pre-terminates the oscillator, which turns off the MOSFET drive signal.

The MOSFET is turned on again when either c_{SS} discharges or a quasi-resonance signal is detected on pin 1.

Fixed 50 µs Off-Time: Soft-Start Mode

This is the mode of operation in the absence of a quasi-resonance signal on pin 1 (see figure 5), and occurs at

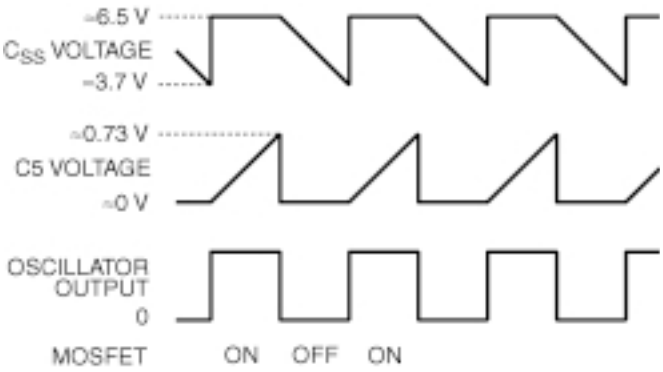


Figure 5 – Soft-Start Operation

startup and in overload. It also can be commanded externally to provide low-power standby operation.

In the absence of a feedback signal (such as at startup, or a short circuit) the drain current ramp, sensed across R5 and noise filtered by R4/C5 appears on pin 1. When the ramp voltage on C5 exceeds the 0.73 V reference signal, the FBK/OCP comparator changes state, shutting down the oscillator and turning off the MOSFET. Thus the voltage on c_{SS} is held high (6.5 V) by the comparator. When the comparator changes state, c_{SS} discharges via r_{SS}; the voltage on c_{SS} ramps down until it reaches 3.7 V. The oscillator turns on the MOSFET. This ramp-down time is internally trimmed to 50 µs. The comparator changes state again and the cycle repeats. Thus in the absence of feedback, the current-sense resistor R5 accurately controls the MOSFET maximum current.

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Functional Description and Operation (cont'd)

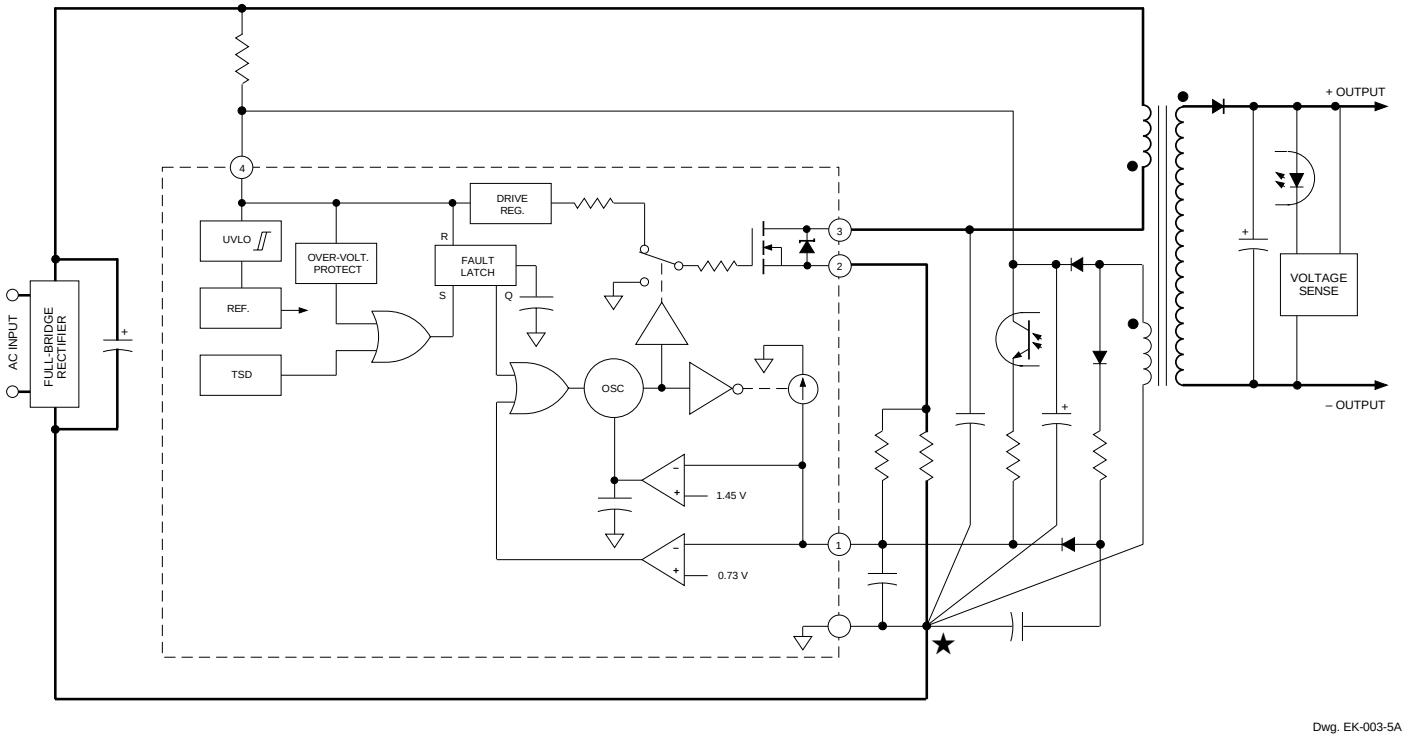


Figure 6 – Series STR-F6600 Typical Application

WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

Soft Start with Voltage Feedback (refer to figure 7)

Output voltage control is achieved by sensing the opto-coupled feedback current (proportional to the output voltage error signal) across resistor R4 and summing this with the drain current ramp on R5. The signal on pin 1 is therefore the opposite of the output voltage error signal and the drain current ramp. The dc bias signal across R4 is thus a function of the load. Consequently at light load, the bias signal on R4 is closer to the threshold voltage of the comparator.

To eliminate the possibility of false shutdown at MOSFET turn on (when there is a current spike due to the discharge of primary capacitance), a constant-current sink of 1.35 mA is turned on, effectively lowering the input impedance on pin 1, and momentarily increasing the shutdown threshold.

Functional Description and Operation (cont'd)

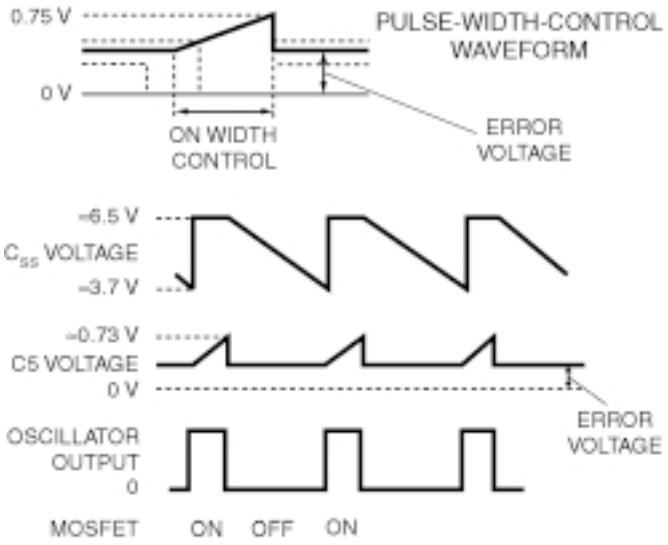


Figure 7 - Voltage Regulation Waveforms

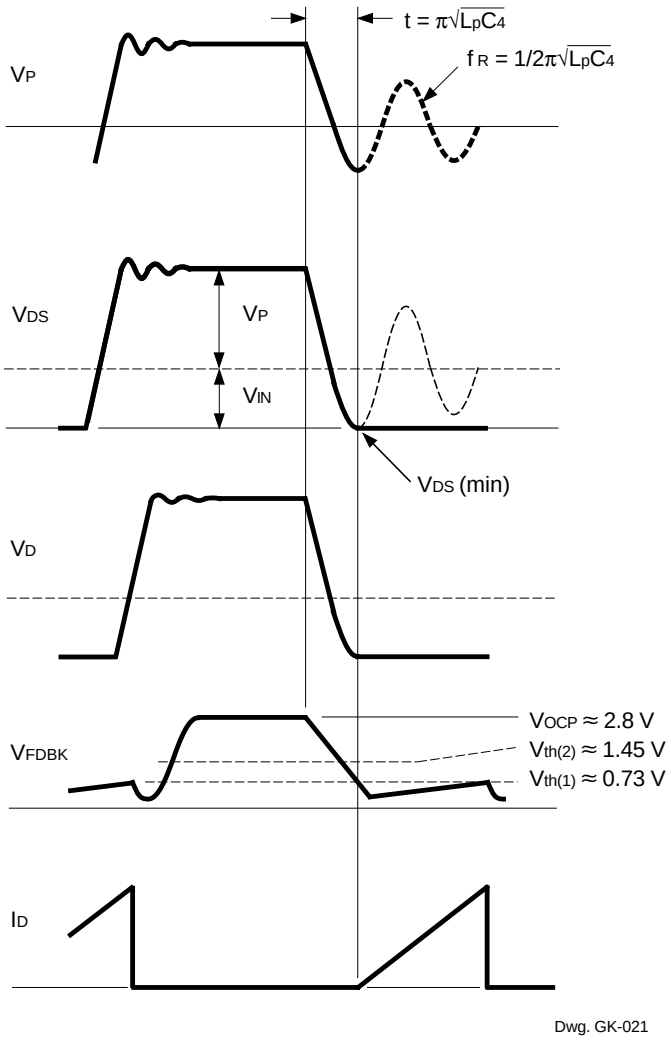


Figure 8 – Quasi-Resonance Waveforms

Normal Operation (Quasi-Resonant) Mode

Refer to the Functional Block Diagram, Typical Application diagram (figure 6), and Quasi-Resonance Waveforms (figure 8).

Regulation is achieved as in fixed off-time mode but instead of having a fixed off-time, the demagnetization of the transformer is sensed by a second comparator. This comparator threshold, $V_{th(2)}$ is nominally 1.45 V. Quasi-resonance sensing makes use of the natural magnetizing and leakage inductances and self-capacitances of the power circuit.

Figure 8 shows the drain voltage waveform, (V_{DS}), on pin 3 of the STR-F66xx, as well as V_P, the voltage on the primary of the transformer.

Once the current in the output diode stops flowing, the primary stored energy 'rings' as shown by V_P and V_{DS}.

The resonant frequency (f_r) is determined by the magnetizing inductance of the transformer and the capacitor C4.

The addition of this capacitor sets the ringing frequency and reduces the harmonic content in the V_{DS} waveform, lowering EMI. Also since V_{DS} falls to a minimum during the first half-cycle of the ring this point can be sensed and used to turn on the MOSFET with minimum voltage across it. Thus the MOSFET is low voltage and zero current switched (LVS/ZCS).

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Functional Description and Operation (cont'd)

The voltage V_{OCP} (pin 1) has the same form as the V_{DS} waveform. The condition for quasi-resonant operation is given by:

$$2.0\ V < V_{OCP} > 5.5\ V \text{ for } >1\ \mu s$$

Transformer design is exactly as for any other discontinuous-mode type flyback.

For optimum EMI/efficiency performance, quasi-resonance turn off is achieved when the MOSFET is at zero voltage and zero current; that is, at one half cycle of the quasi-resonance frequency, f_r.

Over-Current Protection (OCP) Functions

Refer to the Functional Block diagram and Typical Application diagram (figure 6).

The regulator implements pulse-by-pulse over-current protection, which limits the maximum drain current in the MOSFET on every pulse by switching off the internal drive to the MOSFET, and the MOSFET drain current is detected across R5.

Drive Circuit

Refer to the Functional Block Diagram.

This circuit is driven from the oscillator and provides the current drive to charge and discharge the MOSFET gate-source capacitance, thereby switching the device on and off. The basic circuit configuration is totem-pole type with an additional limiting resistor in the gate circuit at turn on. This limits the turn on speed of the MOSFET, thereby reducing EMI due to the discharge of primary capacitance. This is possible because of the low-voltage switching, zero-current switching nature of the turn on.

The value of the turn-off resistance is lower, allowing the device turn-off current to be increased. This reduces the turn-off loss in the MOSFET.

The gate drive voltage (8.3 V) is such that even with 0.73 V across R5 (drain current sense resistor), the MOSFET is fully enhanced, allowing full use to be made of its high current handling capacity.

Latch Circuit

The latch circuit keeps the oscillator output low to inhibit operation of the regulator when over-voltage protection (OVP) and thermal shutdown (TSD) circuits are in operation. As long as the latch hold-in current is 400 µA (max., supplied via R_S) with V_{IN} at 8.5 V (pin 4), the regulator will stay in the off state.

An internal noise filter provides 10 µs of noise immunity to prevent spurious operation of the over-voltage protection or thermal shutdown.

With the latch 'on', the voltage on pin 4 cycles between 16 V and 10 V as shown in figure 9. This is due to the higher current drawn when the pin 4 is at 16 V compared to that drawn close to shutdown (10 V).

Pulling V_{IN} (pin 4) below 6.5 V will reset the latch circuit, re-enabling the regulator.

Thermal Shutdown

This internal feature triggers the latch if the internal frame temperature exceeds 140°C (typ.).

The temperature is sensed on the control IC, but also protects against overheating of the MOSFET as the MOSFET and the control IC are mounted on the same lead frame. Additionally, protection is provided for other on-board components.

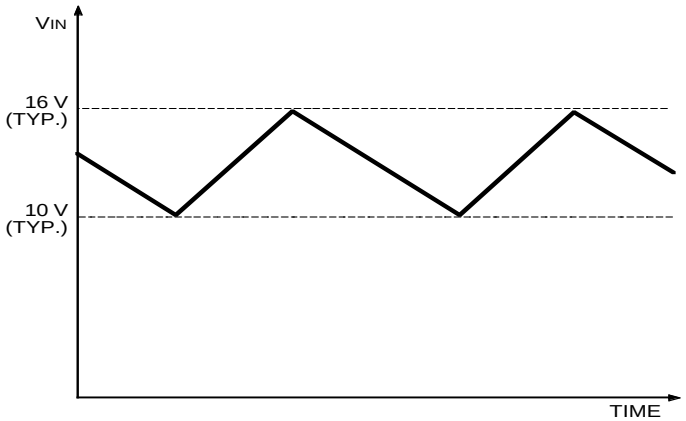


Figure 9 – Example of V_{IN} Terminal Voltage Waveform at Latch Circuit On

Functional Description and Operation (cont'd)

Over-Voltage Protection Circuit

This feature of the STR-F66xx triggers the latch circuit when the V_{IN} voltage (pin 4) exceeds 22.5 V (typ.). Because the voltage on pin 4 is proportional to the output voltage (they are linked by the transformer turns ratio), the regulator protects the output against over-voltage. This function is entirely independant of the output-voltage regulation loop and indeed will protect against output over-voltage should the voltage error signal be lost. The measure of over-voltage is given by:

$$V_{OUT(OVP)} = V_{OUT(NOM)} \times V_{IN(OVP)}/V_{IN(NOM)}$$

where $V_{IN(OVP)}$ is the drive voltage on pin 4.

In an over-voltage sensitive application, the drive voltage can be set to close to 20 V and thus will protect the output, if it rises more than 10% above nominal.

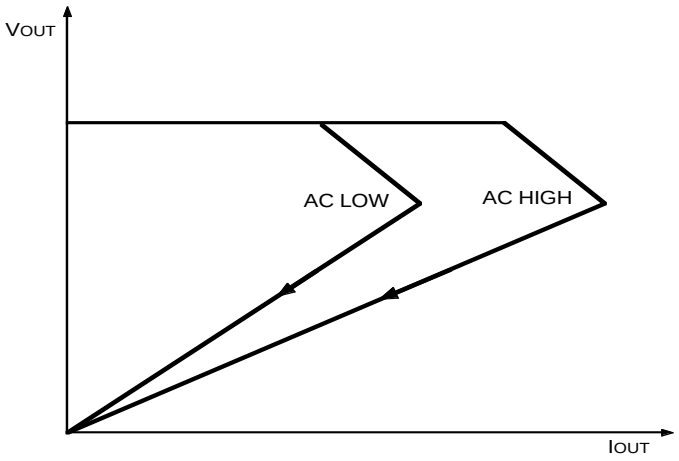
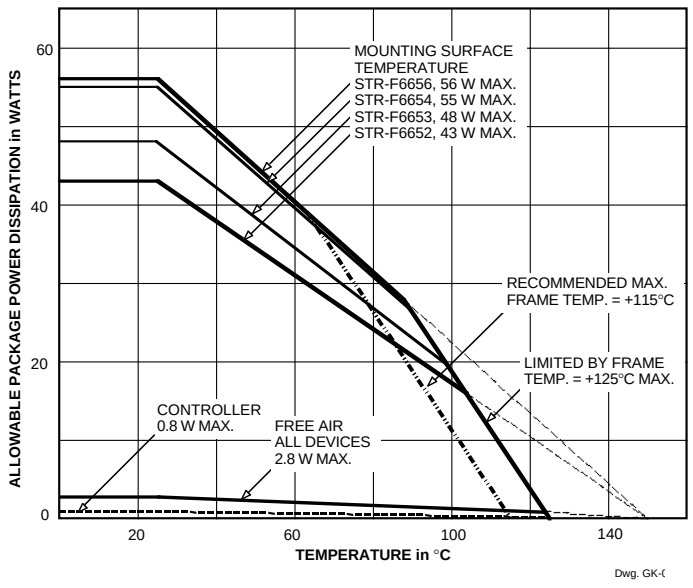


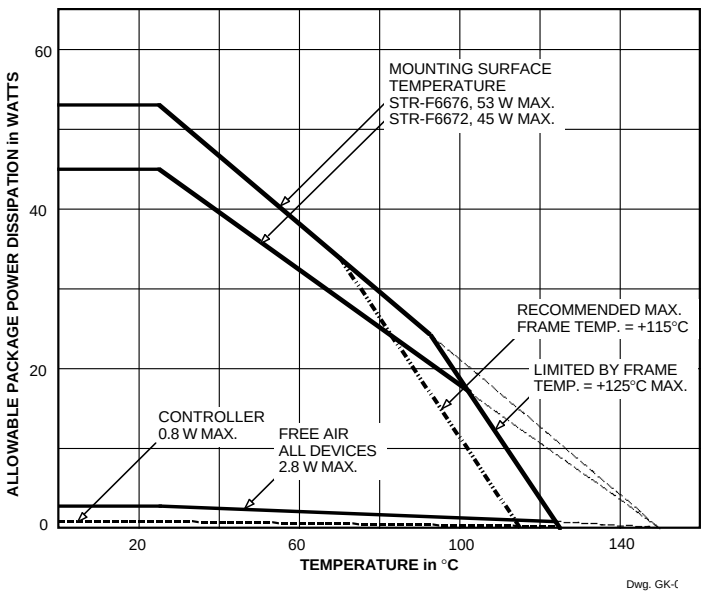
Figure 10 – Power Supply Output Overload Characteristics

ALLOWABLE PACKAGE POWER DISSIPATION

STR-F665x



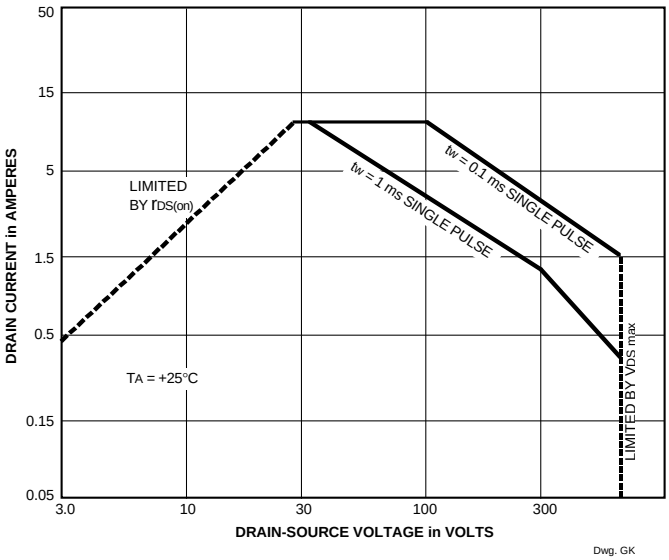
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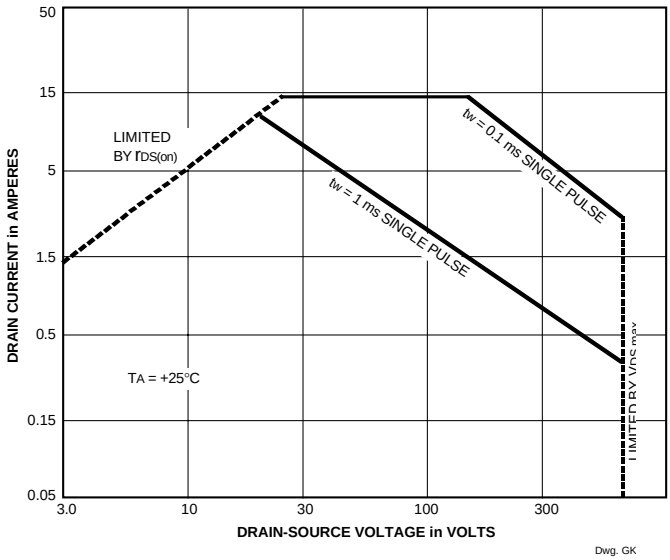
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MOSFET Safe Operating Areas
(single pulse at T_A = +25°C)

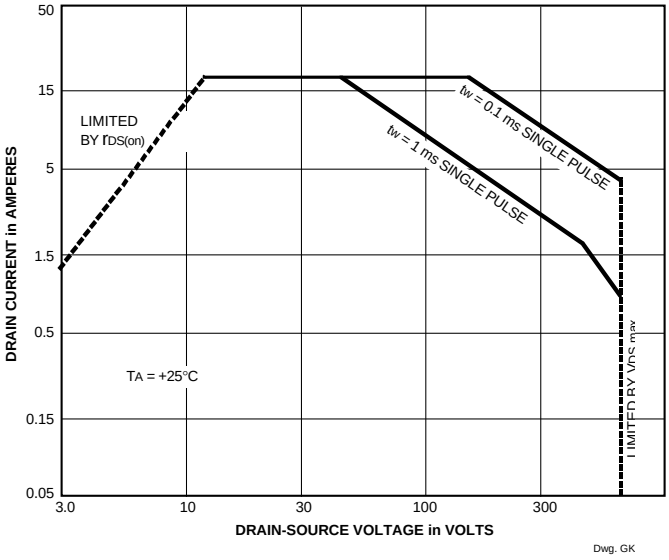
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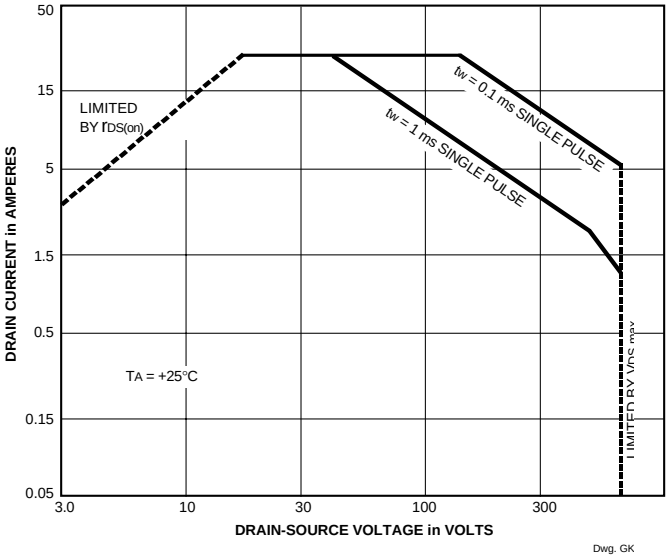
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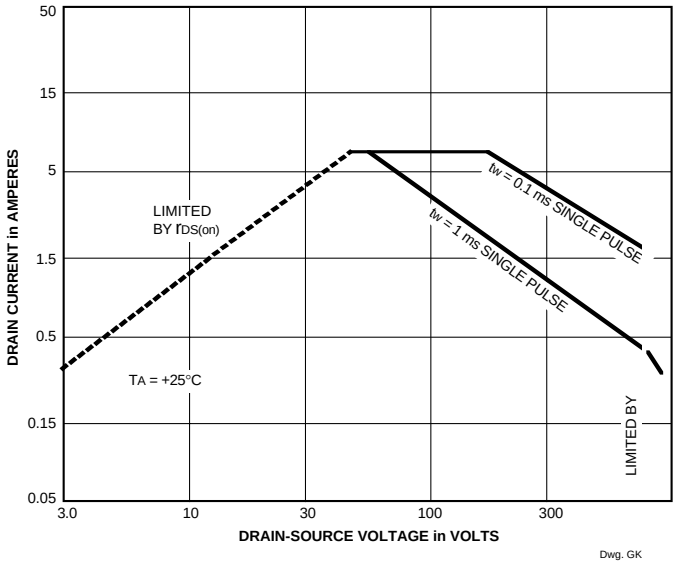


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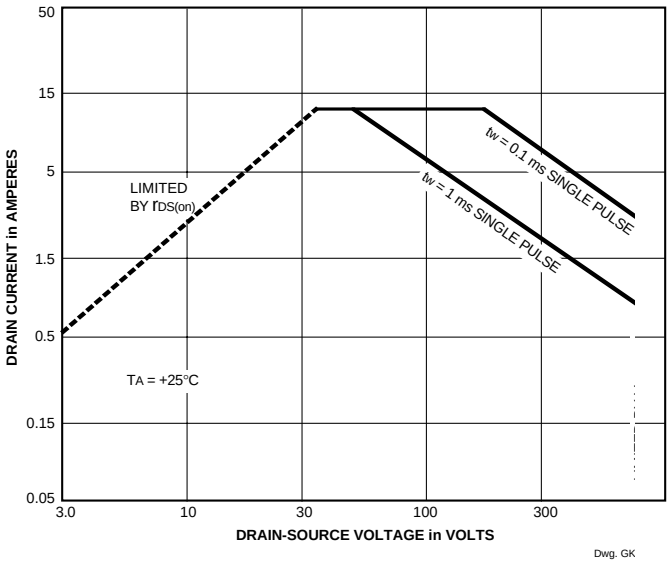


MOSFET Safe Operating Areas (cont)
(single pulse at T_A = +25°C)

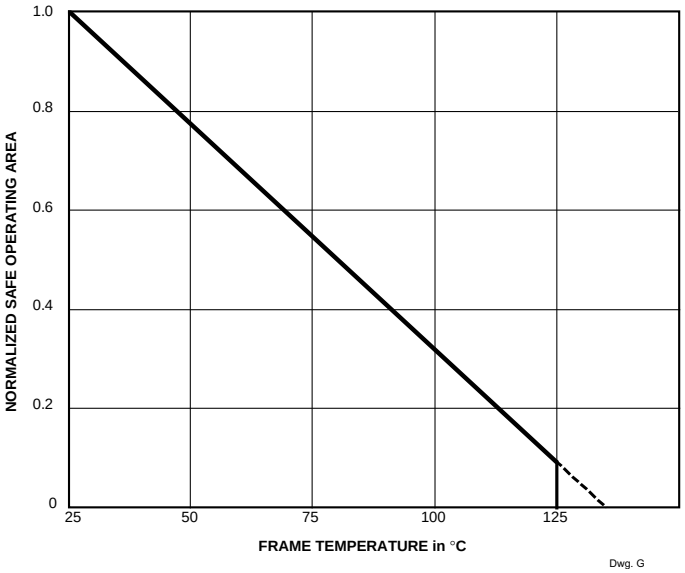
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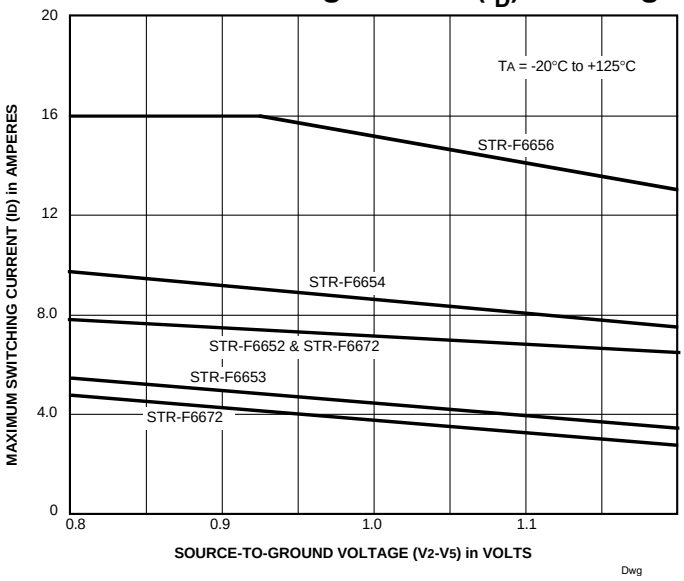
STR-F6676



S.O.A. Derating



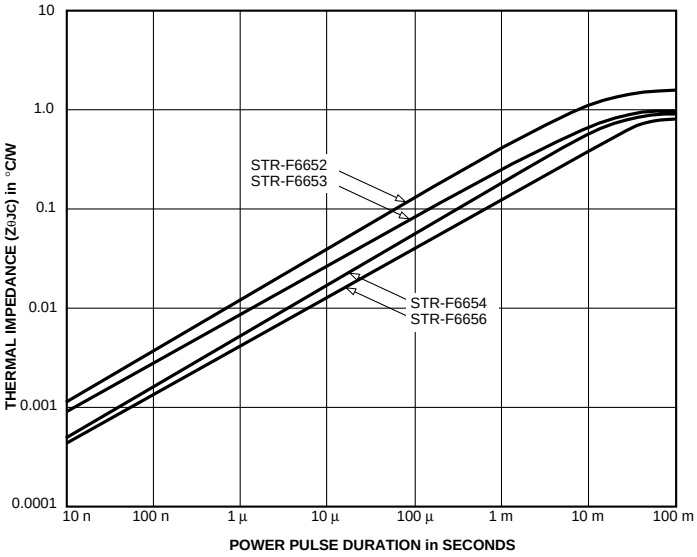
Drain Switching Current (I_D) Derating



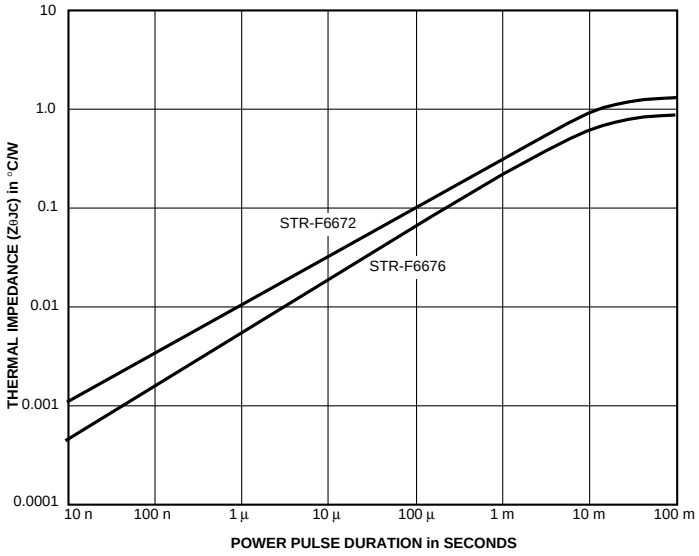
Allegro® MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000
SanKen™

Transient Thermal Impedance

STR-F665x



STR-F667x



Applications Information

Capacitors

Electrolytic capacitors carrying large switching frequency ripple currents (C1 and the output capacitors) should be capable of handling the high rms currents involved. Capacitors with low ESR are suitable. The quasi-resonance capacitor C4 should be a high-voltage ceramic type suitable for pulsed current operation.

The safety critical nature of the off-line application must be considered when selecting both X and Y capacitors for common- and differential-mode noise filtering. Use of the low-noise quasi-resonant Series STR-F6600 will allow optimization of these capacitor values.

C5, the 470 pF filtering capacitor should be a 50 V temperature-stable (COG) ceramic type.

Resistors

Resistor R5 carries high-frequency current, and so a low internal inductance type of 1 W rating should be used.

Resistor R9 (R_S) should be 2 W metal oxide.

All other resistors can be 1/4 watt or 1/2 watt metal film.

Diodes

Diodes carrying the high-frequency flyback currents (such as the transformer rectifier diodes) should have a fast or ultrafast reverse-recovery characteristic, adequate current handing and peak reverse-voltage rating. Allegro/Sanken supplies a range of suitable diodes, and these are described in the Allegro/Sanken short-form catalogue (AMS-127) or latest issue of Bulletin D01EC0.

Optocoupler

Both Toshiba TLP 621 and Siemens SFH 610A2 or 615A2 are suitable. A current-transfer ratio of 50% to 200% is acceptable.

Error Amplifier

A standard TL431 transconductance amplifier or an Allegro/Sanken Series SE error-amplifier IC can be used. The Series SE is particularly well-suited to high-voltage (70 V to 140 V) power outputs.

If a Series SE error-amplifier IC is used, normally phase compensation is not required. Should additional high-frequency attenuation be required, a capacitor (0.022 µF or less) can be connected across the primary side (collector-emitter) of the optocoupler, a diode to maintain quasi-resonant operation should be added in series with the phototransistor emitter.

The products described here are manufactured in Japan by Sanken Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

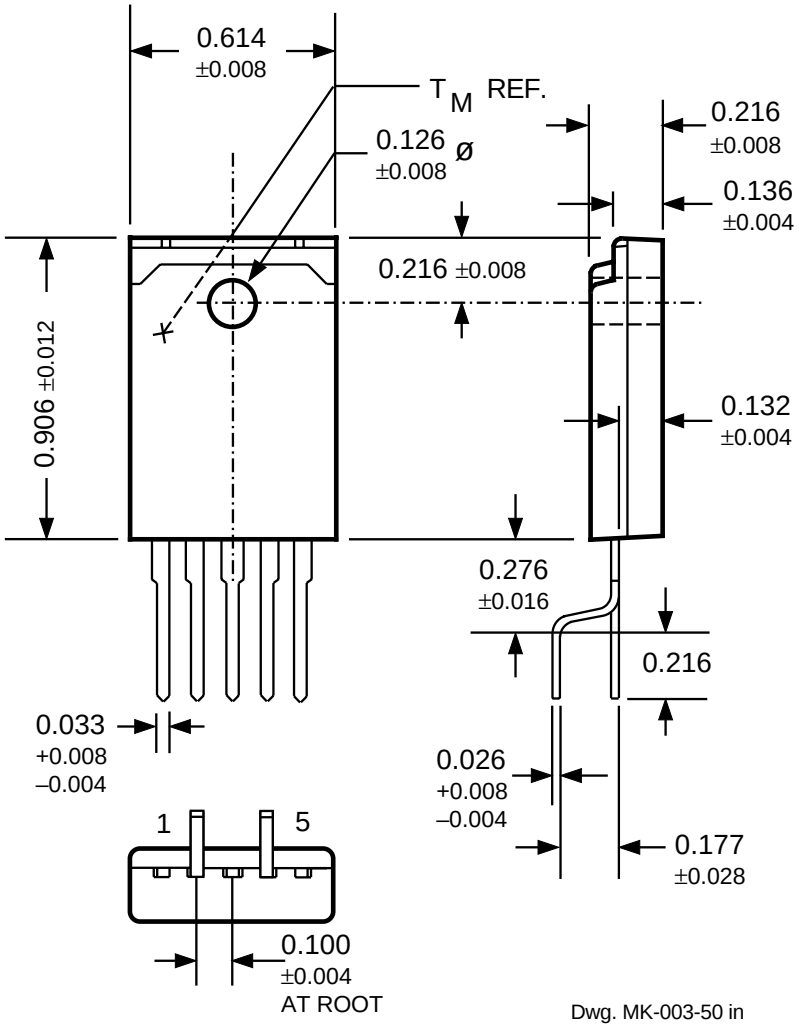
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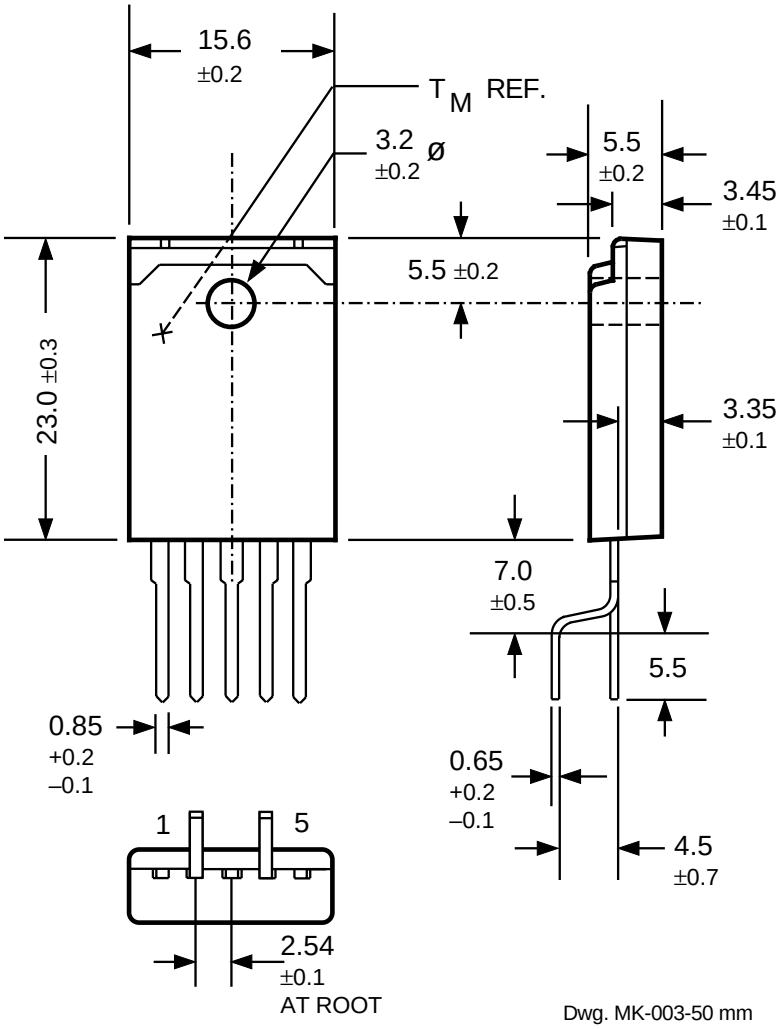
Dimensions in Inches
(for reference only)



Dwg. MK-003-50 in

Recommended mounting hardware torque: 4.34 – 5.79 lbf•ft.
Recommended silicone grease: Dow Corning SC102, Toshiba YG6260, Shin-Etsu G746., or equivalent

Dimensions in Millimeters
(controlling dimensions)



Dwg. MK-003-50 mm

Recommended mounting hardware torque: 6 – 8 kg•cm or 0.588 – 0.784 Nm.
Recommended silicone grease: Dow Corning SC102, Toshiba YG6260, Shin-Etsu G746., or equivalent

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