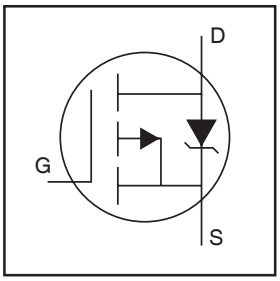
International
IOR Rectifier

PD - 94980

IRF9530NPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead-Free



V_{DSS} = -100V

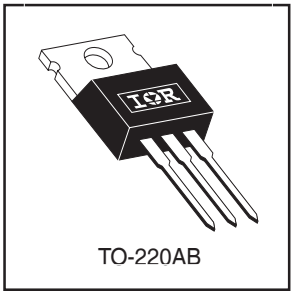
$R_{DS(on)}$ = 0.20Ω

I_D = -14A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

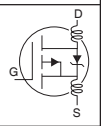
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-14	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-10	
I_{DM}	Pulsed Drain Current ①	-56	
P_D @T_C = 25°C	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	250	mJ
I_{AR}	Avalanche Current①	-8.4	A
E_{AR}	Repetitive Avalanche Energy①	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	1.9	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient	–––	62	

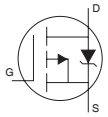
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	–––	–––	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	-0.11	–––	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.20	Ω	V_{GS} = -10V, I_D = -8.4A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	–––	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	3.2	–––	–––	S	V_{DS} = -50V, I_D = -8.4A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	-25	µA	V_{DS} = -100V, V_{GS} = 0V
		–––	–––	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
Q_g	Total Gate Charge	–––	–––	58	nC	I_D = -8.4A
Q_{gs}	Gate-to-Source Charge	–––	–––	8.3		V_{DS} = -80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	32		V_{GS} = -10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	–––	15	–––	ns	V_{DD} = -50V
t_r	Rise Time	–––	58	–––		I_D = -8.4A
$t_{d(off)}$	Turn-Off Delay Time	–––	45	–––		R_G = 9.1Ω
t_f	Fall Time	–––	46	–––		R_D = 6.2Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	–––	7.5	–––		
C_{iss}	Input Capacitance	–––	760	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	260	–––		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	–––	170	–––		f = 1.0MHz, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	-14	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	-56		
V_{SD}	Diode Forward Voltage	–––	–––	-1.6	V	T_J = 25°C, I_S = -8.4A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	130	190	ns	T_J = 25°C, I_F = -8.4A
Q_{rr}	Reverse RecoveryCharge	–––	650	970	nC	di/dt = -100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 7.0mH
R_G = 25Ω, I_{AS} = -8.4A. (See Figure 12)

③ I_{SD} ≤ -8.4A, di/dt ≤ -490A/µs, V_{DD} ≤ $V_{(BR)DSS}$,
T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

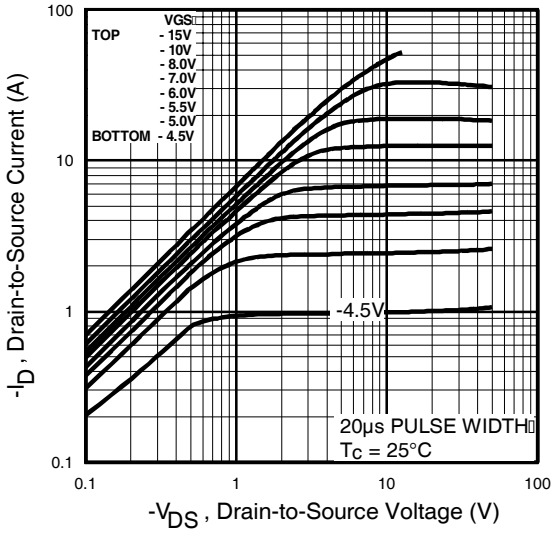


Fig 1. Typical Output Characteristics

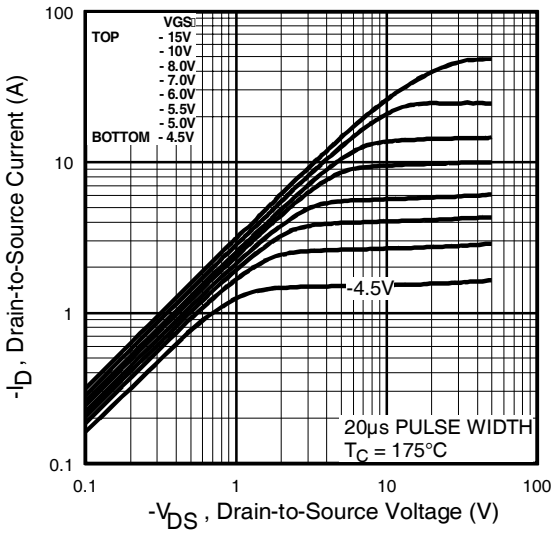


Fig 2. Typical Output Characteristics

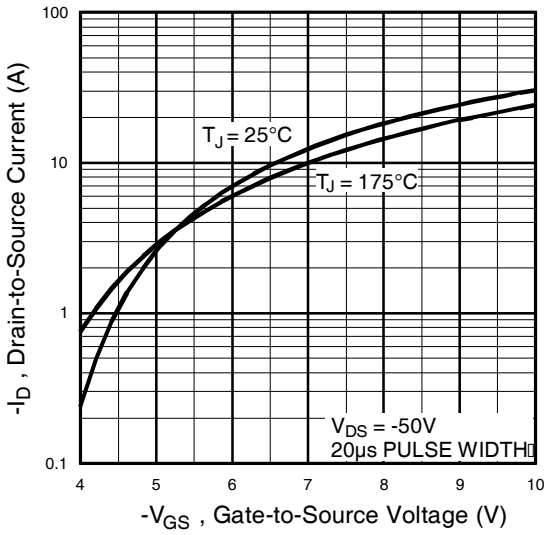


Fig 3. Typical Transfer Characteristics

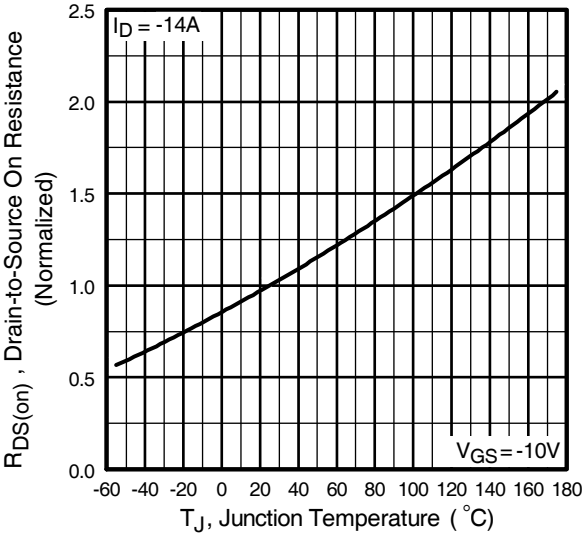


Fig 4. Normalized On-Resistance Vs. Temperature

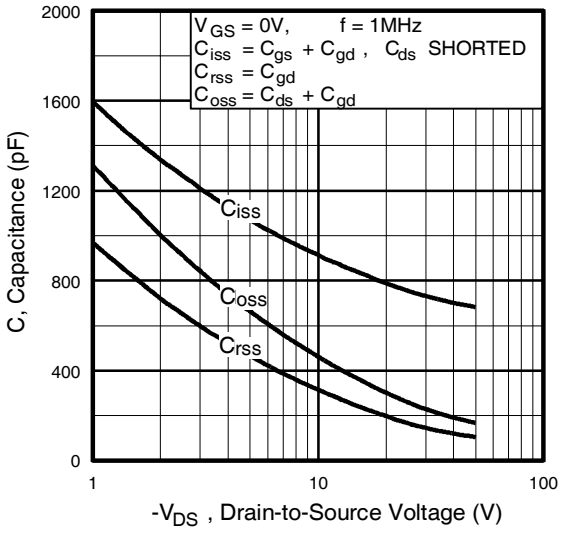


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

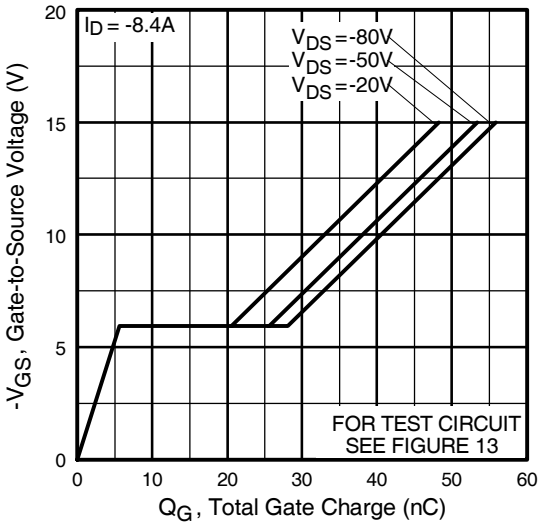


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

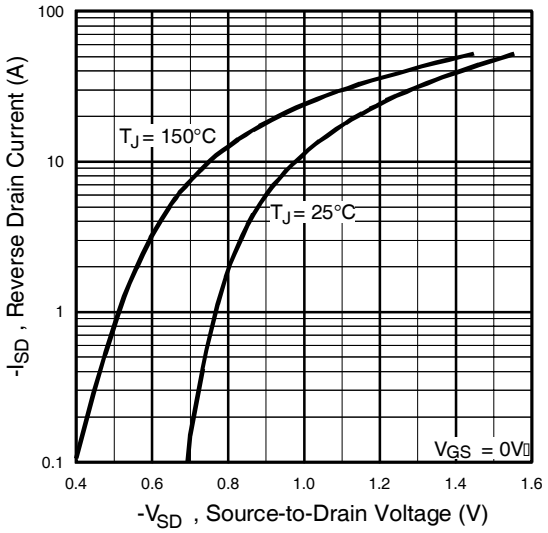


Fig 7. Typical Source-Drain Diode Forward Voltage

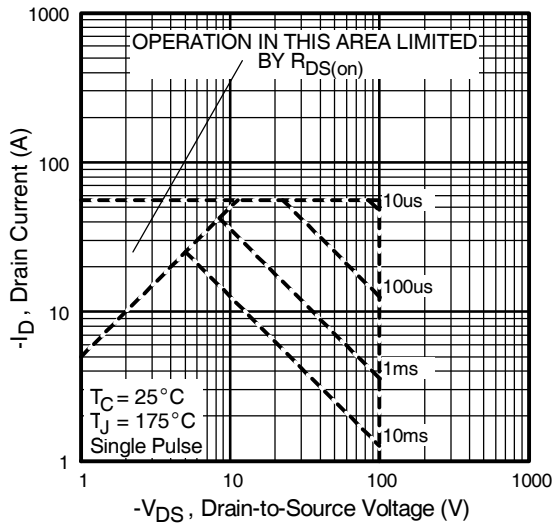


Fig 8. Maximum Safe Operating Area

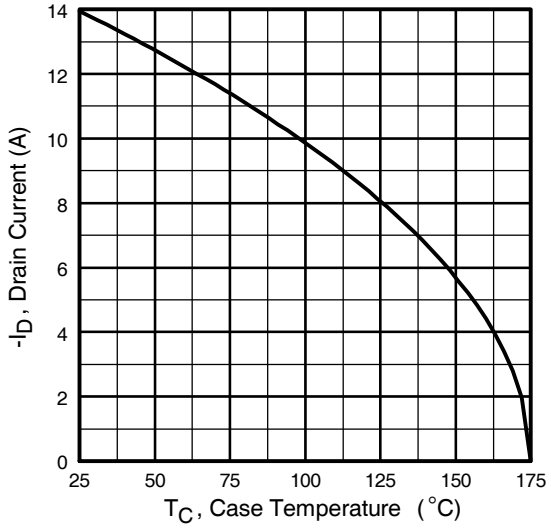


Fig 9. Maximum Drain Current Vs. Case Temperature

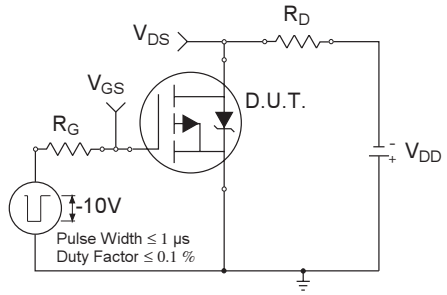


Fig 10a. Switching Time Test Circuit

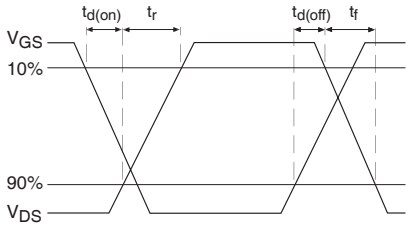


Fig 10b. Switching Time Waveforms

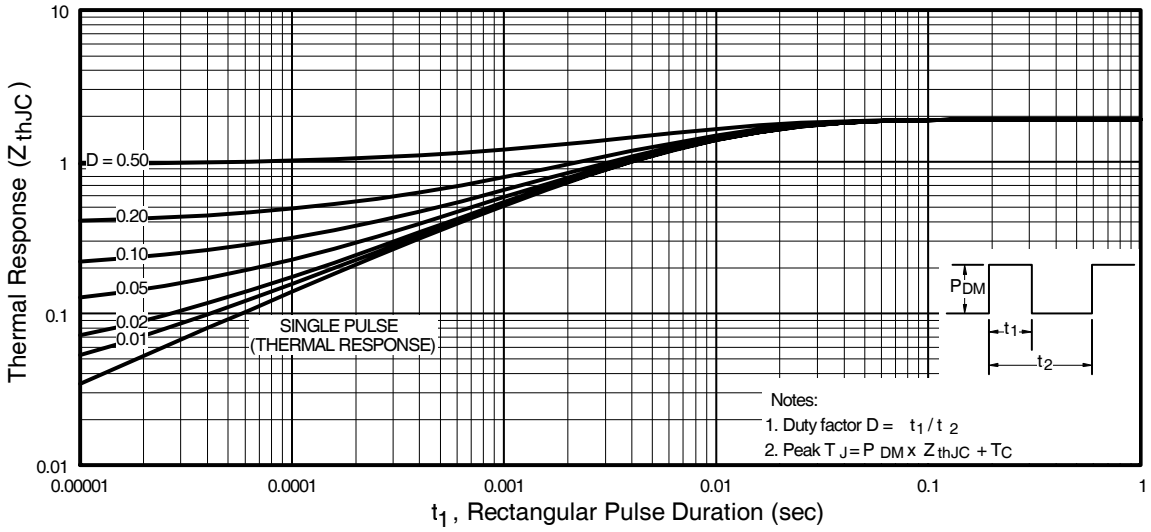


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

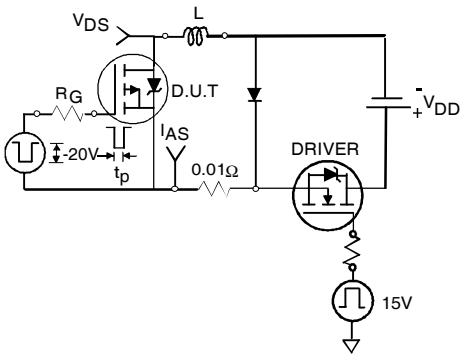


Fig 12a. Unclamped Inductive Test Circuit

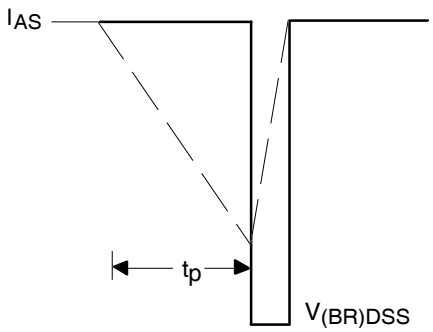


Fig 12b. Unclamped Inductive Waveforms

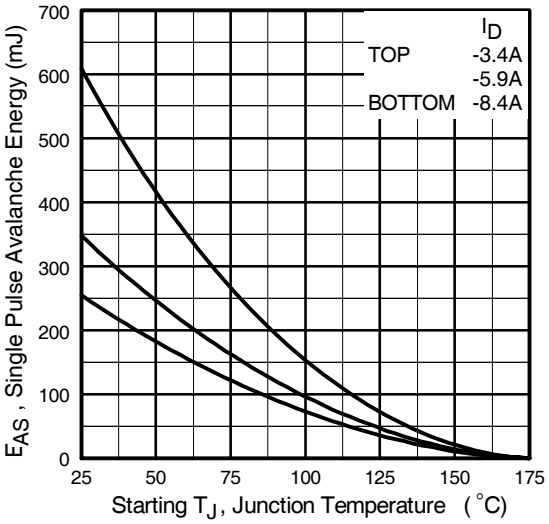


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

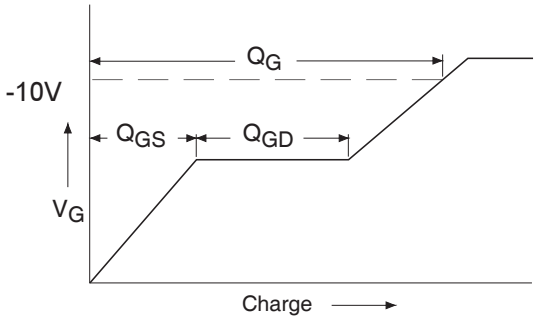


Fig 13a. Basic Gate Charge Waveform

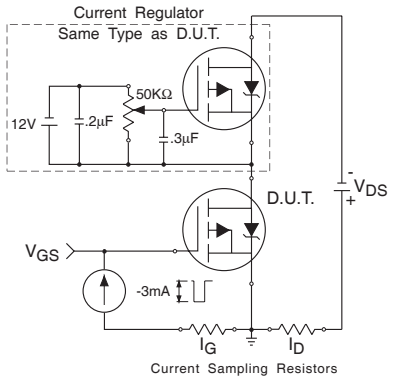
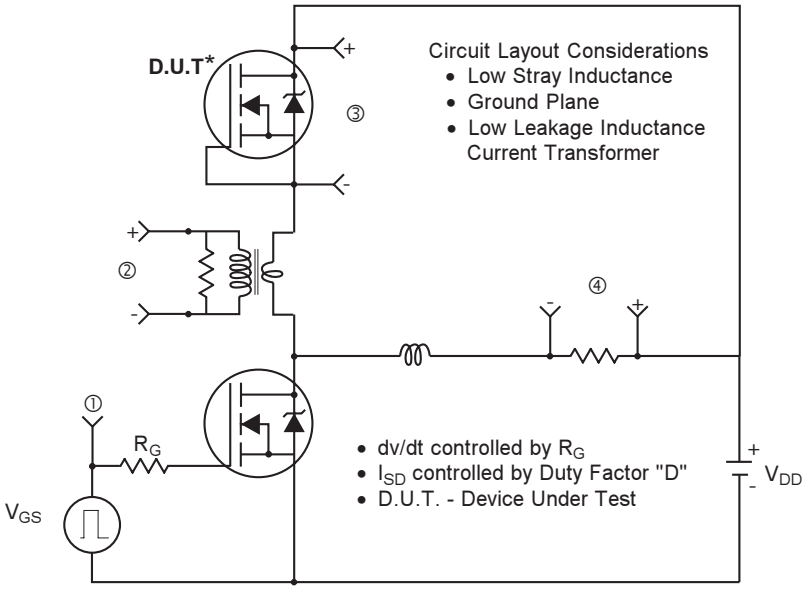
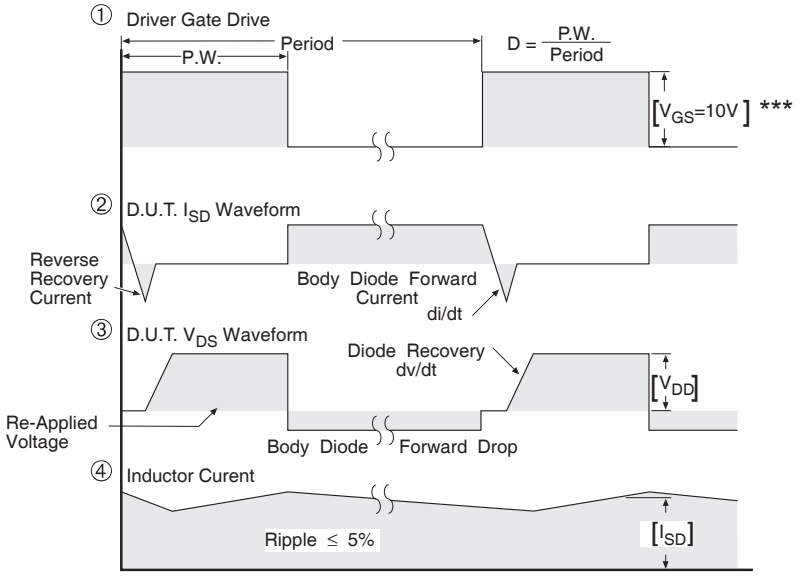


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

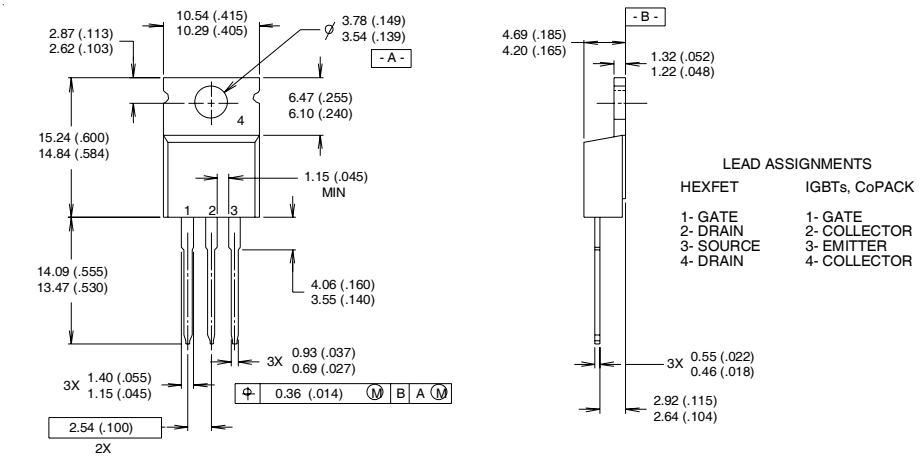


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

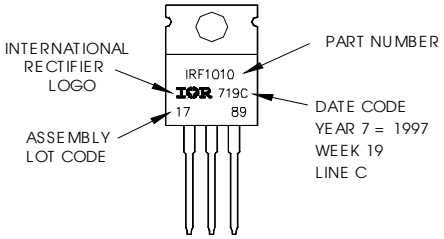
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

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