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FAIRCHILD SEMICONDUCTOR®

August 2013

FQPF7N65C

N-Channel QFET® MOSFET

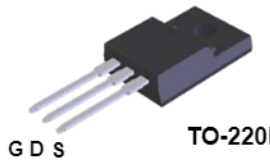
650 V, 7 A, 1.4 Ω

Description

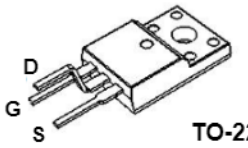
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

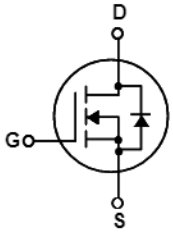
- 7 A, 650 V, $R_{DS(on)}$ = 1.4 Ω (Max.) @ V_{GS} = 10 V, I_D = 3.5 A
- Low Gate Charge (Typ. 28 nC)
- Low C_{rss} (Typ. 12 pF)
- 100% Avalanche Tested



TO-220F



TO-220F
Y-formed



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQPF7N65C / FQPF7N65CYDTU	Unit
V_{DSS}	Drain-Source Voltage		650	V
I_D	Drain Current - Continuous (T_C = 25°C)		7 *	A
	- Continuous (T_C = 100°C)		4.2 *	A
I_{DM}	Drain Current - Pulsed	(Note 1)	28 *	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	212	mJ
I_{AR}	Avalanche Current	(Note 1)	7	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	1.6	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		52	W
	- Derate above 25°C		0.42	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FQPF7N65C / FQPF7N65CYDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

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Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQPF7N65C	FQPF7N65C	TO-220F	-	-	50
FQPF7N65C	FQPF7N65CYDTU	TO-220F (Y-formed)	-	-	50

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	650	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.8	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 520 V, T_C = 125°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A	--	1.2	1.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 3.5 A	--	8	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	955	1245	pF
C_{oss}	Output Capacitance		--	100	130	pF
C_{rss}	Reverse Transfer Capacitance		--	12	16	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 325 V, I_D = 7A, R_G = 25 Ω (Note 4)	--	20	50	ns
t_r	Turn-On Rise Time		--	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		--	90	190	ns
t_f	Turn-Off Fall Time		--	55	120	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 7A, V_{GS} = 10 V (Note 4)	--	28	36	nC
Q_{gs}	Gate-Source Charge		--	4.5	--	nC
Q_{gd}	Gate-Drain Charge		--	12	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	28	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 7A, dI_F / dt = 100 A/µs	--	400	--	ns
Q_{rr}	Reverse Recovery Charge		--	3.3	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 8mH, I_{AS} = 7A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 7A, di/dt ≤ 200A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Essentially independent of operating temperature

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Typical Characteristics

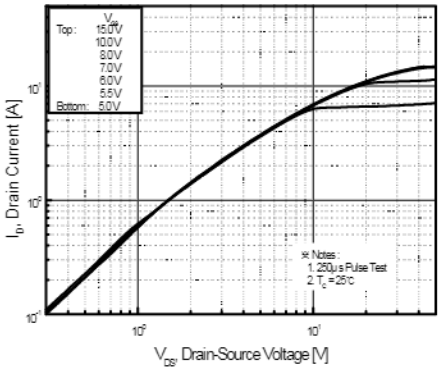


Figure 1. On-Region Characteristics

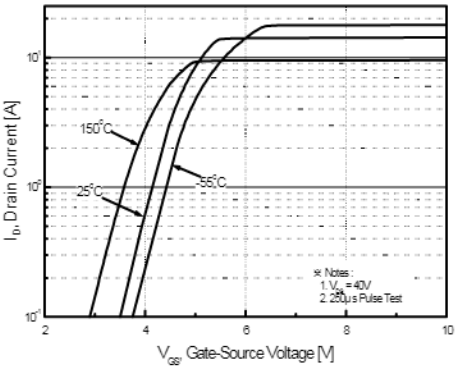


Figure 2. Transfer Characteristics

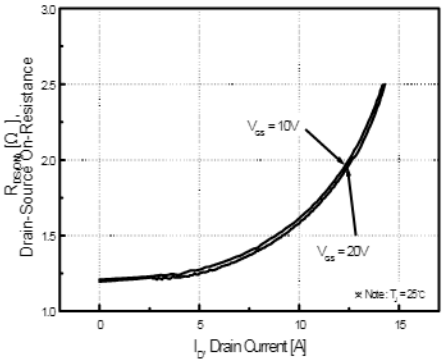


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

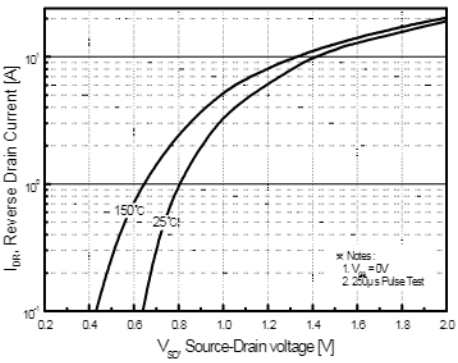


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

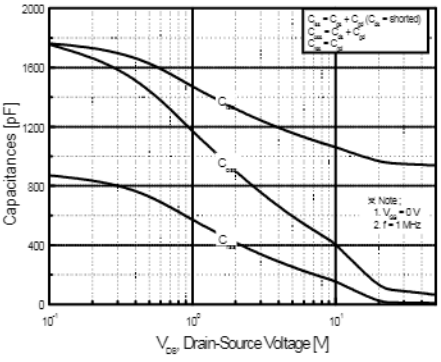


Figure 5. Capacitance Characteristics

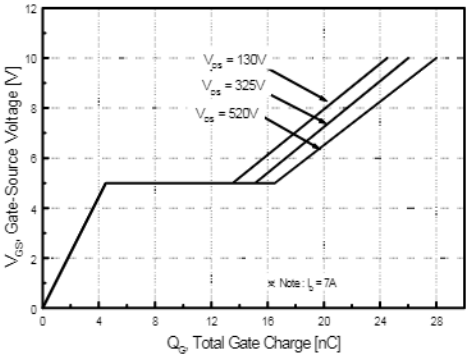


Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

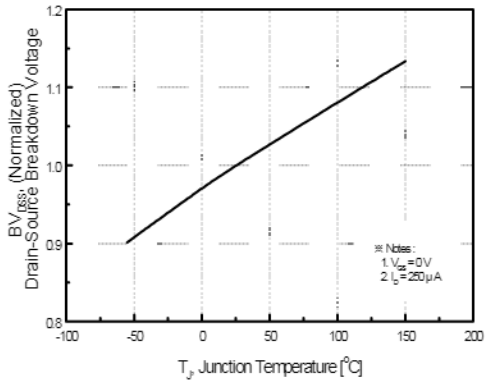


Figure 7. Breakdown Voltage Variation vs Temperature

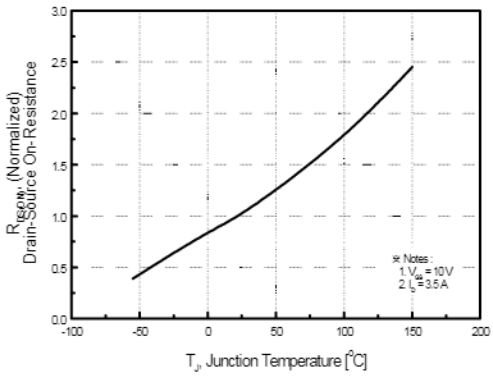


Figure 8. On-Resistance Variation vs Temperature

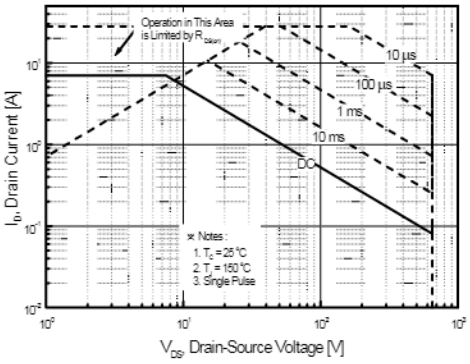


Figure 9. Maximum Safe Operating Area

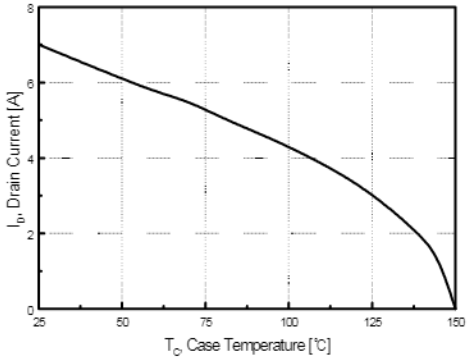


Figure 10. Maximum Drain Current vs Case Temperature

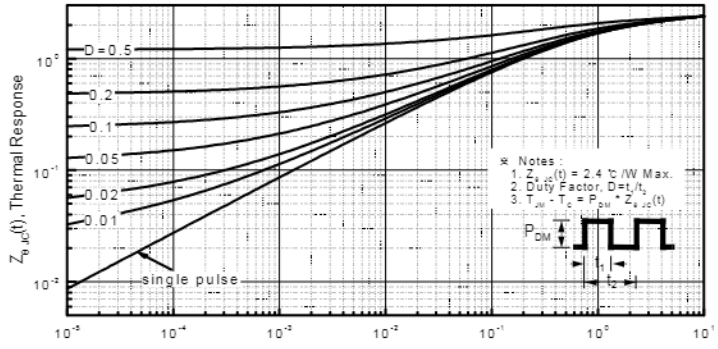


Figure 11 . Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

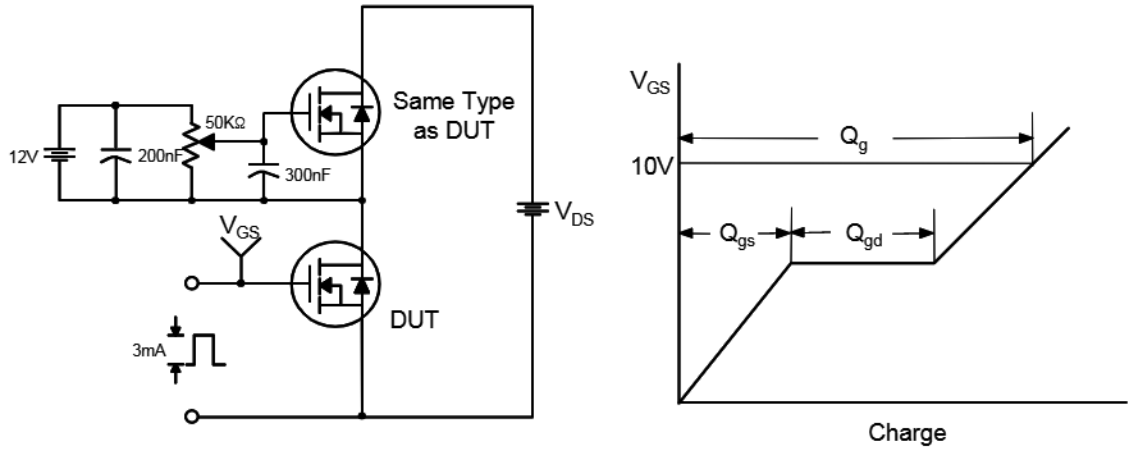


Figure 13. Resistive Switching Test Circuit & Waveforms

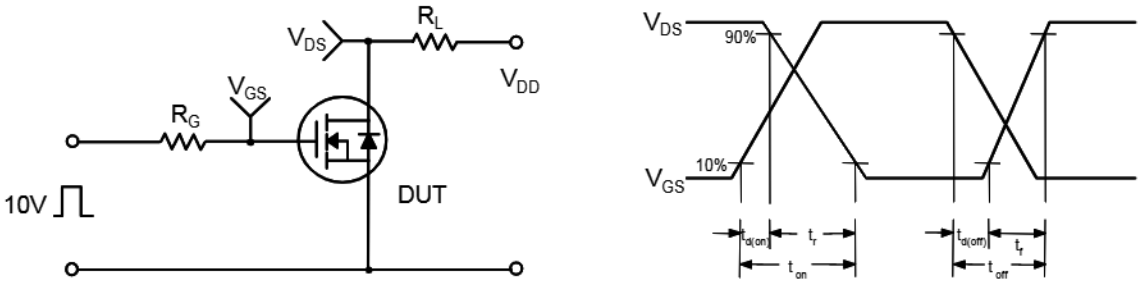
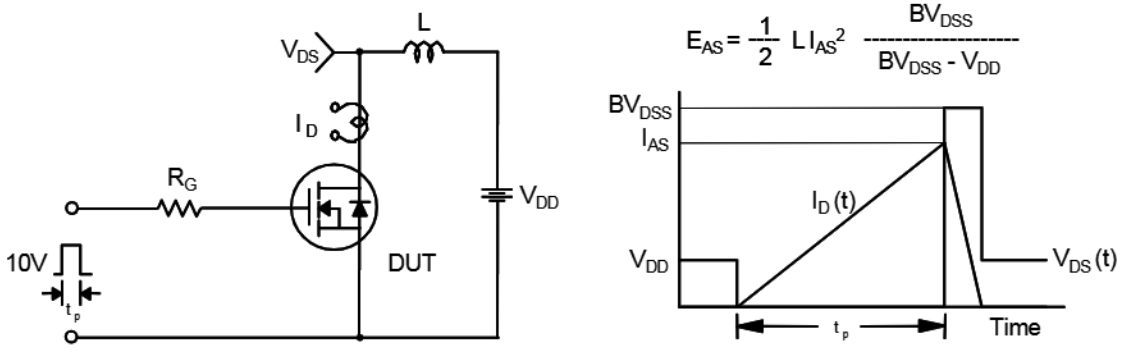
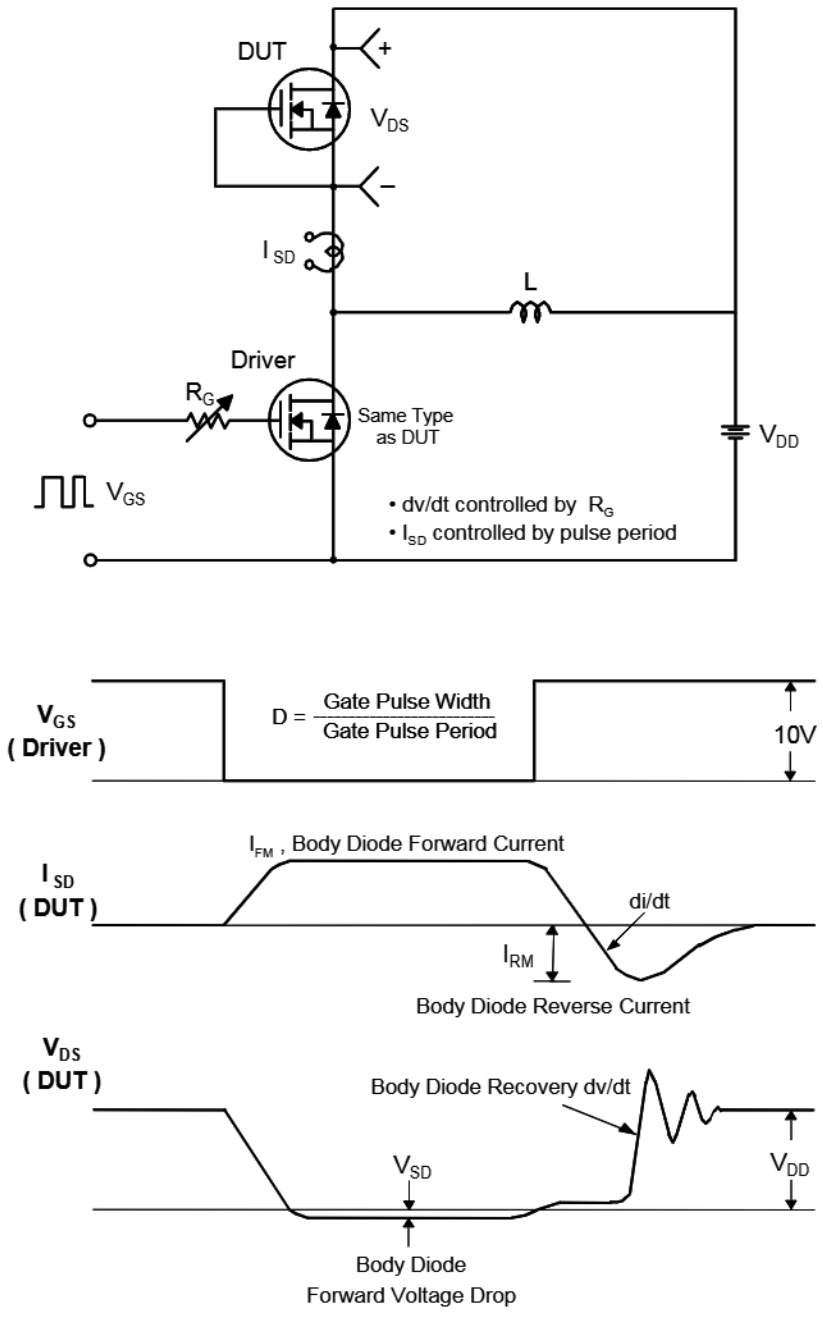


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



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Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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Mechanical Dimensions

TO-220F

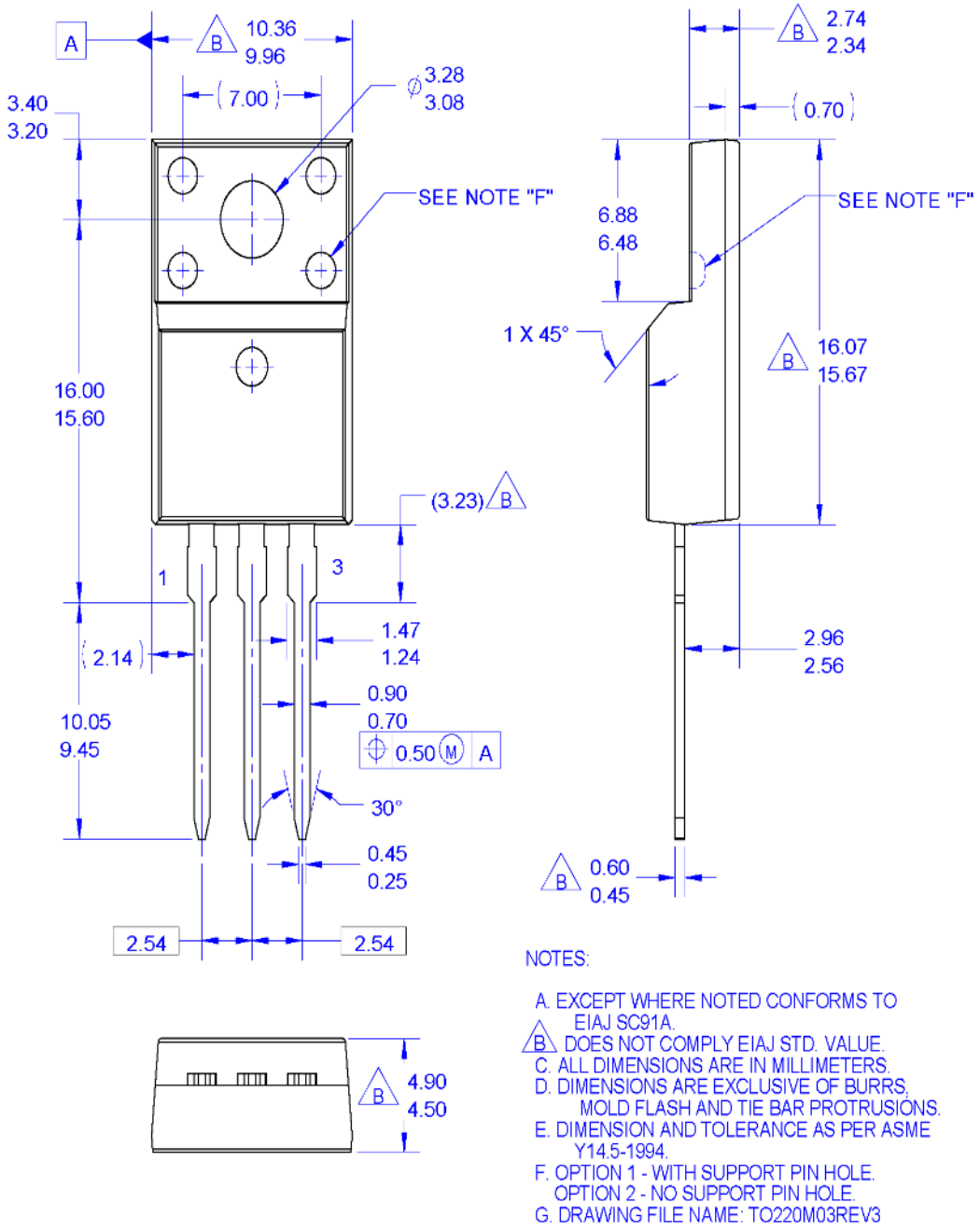


Figure 16. TO-220F 3L - TO220, Molded, 3LD, Full Pack, EIAJ SC91, Straight lead

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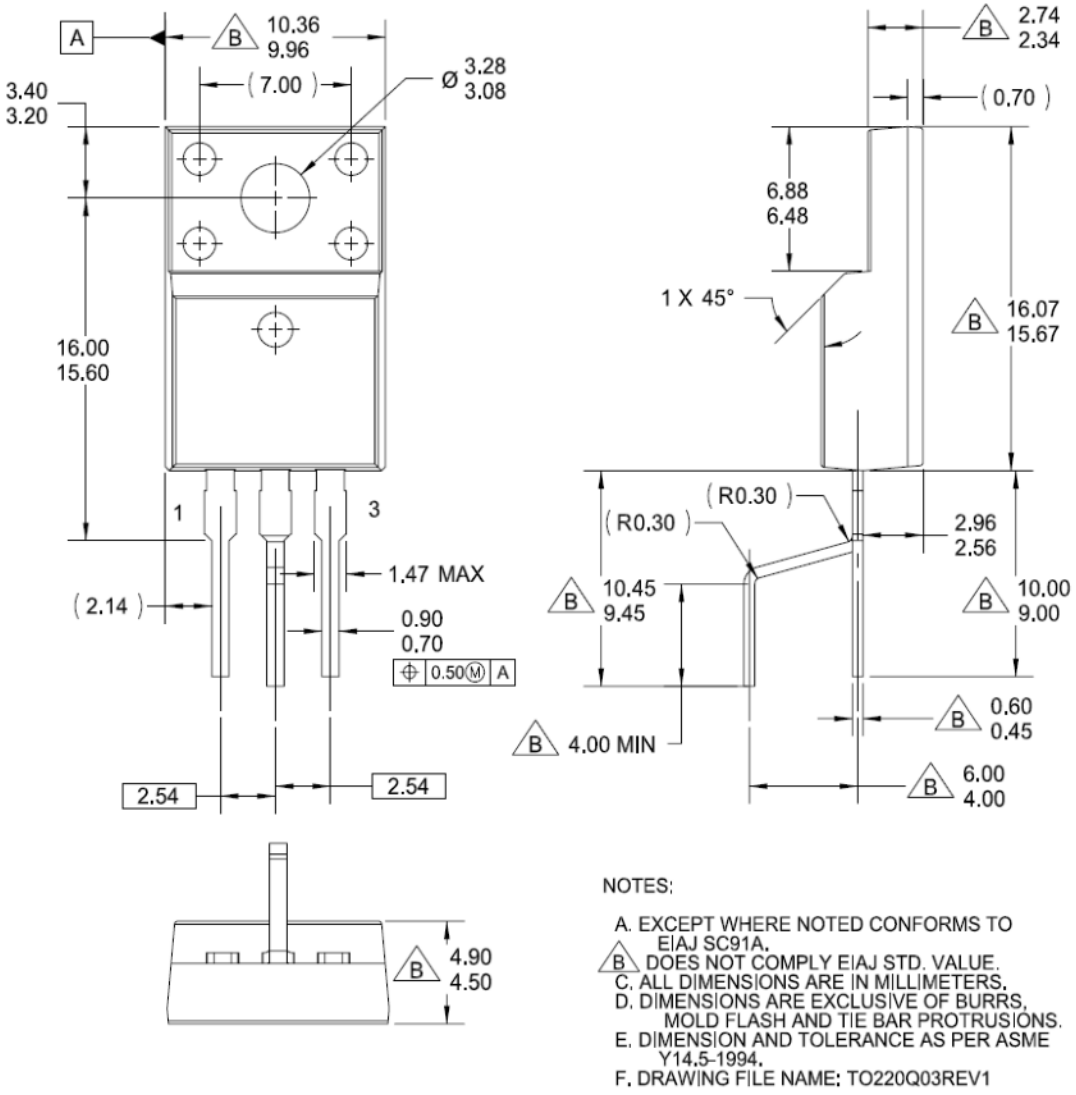
http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TF220-003

Dimensions in Millimeters

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Mechanical Dimensions

TO-220F (Y-formed)



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. DRAWING FILE NAME: TO220Q03REV1

Figure 17. TO-220F 3L - TO220, Molded, 3LD, Full Pack, EIAJ SC91, Y formed lead

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Dimensions in Millimeters

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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