TRINNO TECHNOLOGY

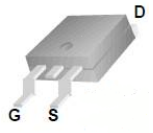
TMD5N50/TMU5N50
TMD5N50G/TMU5N50G

Features

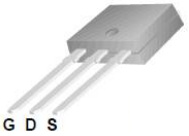
- Low gate charge
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant
- Halogen free package
- JEDEC Qualification
- Fast reverse recovery

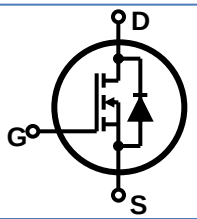
V_{DSS} = 550 V @T_{jmax}
I_D = 4.5A
$R_{DS(ON)}$ = 1.65 Ω(max) @ V_{GS}= 10 V

D-PAK



I-PAK





Device	Package	Marking	Remark
TMD5N50/TMU5N50	D-PAK/I-PAK	TMD5N50/TMU5N50	RoHS
TMD5N50G/TMU5N50G	D-PAK/I-PAK	TMD5N50G/TMU5N50G	Halogen Free

Absolute Maximum Ratings

Parameter		Symbol	TMD5N50(G)/TMU5N50(G)	Unit
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 ℃	I_D	4.5	A
	T_C = 100 ℃		2.86	A
Pulsed Drain Current (Note 1)		I_{DM}	18	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	240	mJ
Repetitive Avalanche Current (Note 1)		I_{AR}	4.5	A
Repetitive Avalanche Energy (Note 1)		E_{AR}	9.25	mJ
Power Dissipation	T_C = 25 ℃	P_D	92.5	W
	Derate above 25 ℃		0.74	W/℃
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300	℃

* Limited only by maximum junction temperature

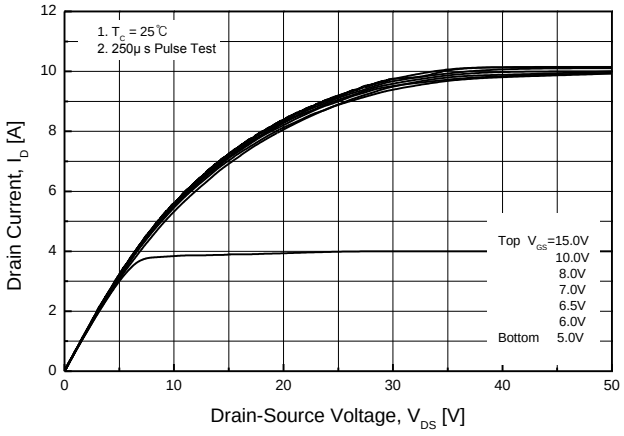
Thermal Characteristics

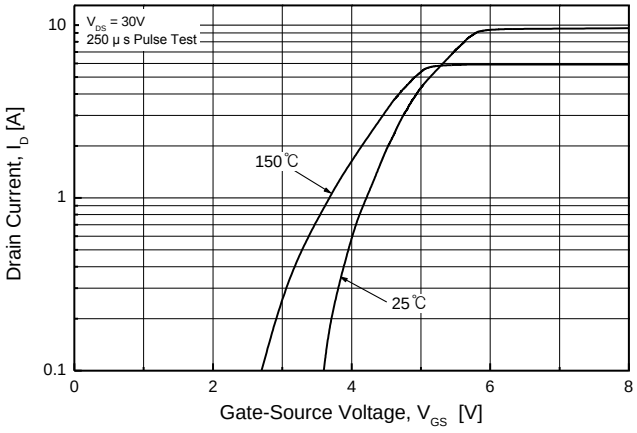
Parameter	Symbol	TMD5N50(G)/TMU5N50(G)	Unit
Maximum Thermal resistance, Junction-to-Case	$R_{\theta JC}$	1.35	℃/W
Maximum Thermal resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	℃/W

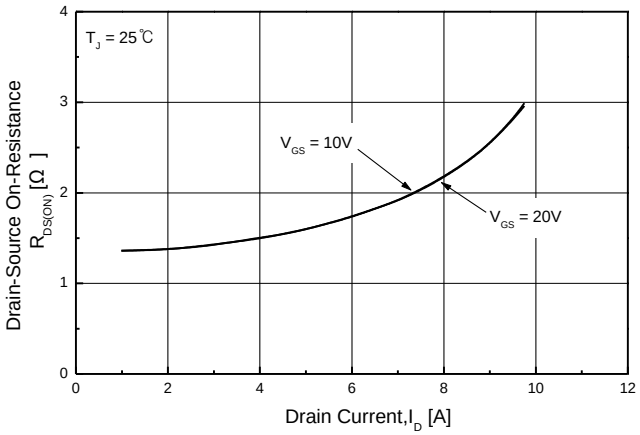
Electrical Characteristics : T_C=25℃, unless otherwise noted

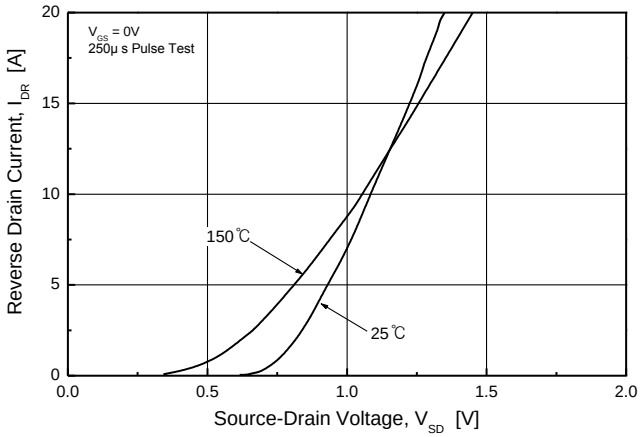
Parameter	Symbol	Test condition	Min	Typ	Max	Units
OFF						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	500	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	µA
Forward Gate-Source Leakage Current	I_{GSSF}	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
Reverse Gate-Source Leakage Current	I_{GSSR}	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
ON						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2.25 A	--	1.4	1.65	Ω
Forward Transconductance (Note 4)	g_{FS}	V_{DS} = 30 V, I_D = 2.25 A	--	6	--	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	627	--	pF
Output Capacitance	C_{oss}		--	61	--	pF
Reverse Transfer Capacitance	C_{rss}		--	4.4	--	pF
SWITCHING						
Turn-On Delay Time (Note 4,5)	$t_{d(on)}$	V_{DD} = 250 V, I_D = 4.5 A, R_G = 25 Ω	--	42	--	ns
Turn-On Rise Time (Note 4,5)	t_r		--	32	--	ns
Turn-Off Delay Time (Note 4,5)	$t_{d(off)}$		--	68	--	ns
Turn-Off Fall Time (Note 4,5)	t_f		--	30	--	ns
Total Gate Charge (Note 4,5)	Q_g	V_{DS} = 400V, I_D = 4.5 A, V_{GS} = 10 V	--	11	--	nC
Gate-Source Charge (Note 4,5)	Q_{gs}		--	3.2	--	nC
Gate-Drain Charge (Note 4,5)	Q_{gd}		--	2.7	--	nC
SOURCE DRAIN DIODE						
Maximum Continuous Drain-Source Diode Forward Current	I_S	----	--	--	4.5	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	----	--	--	18	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 4.5 A	--	--	1.5	V
Reverse Recovery Time (Note 4)	t_{rr}	V_{GS} = 0 V, I_S = 4.5 A	--	255	--	ns
Reverse Recovery Charge (Note 4)	Q_{rr}	dI_F / dt = 100 A/µs	--	1.43	--	µC

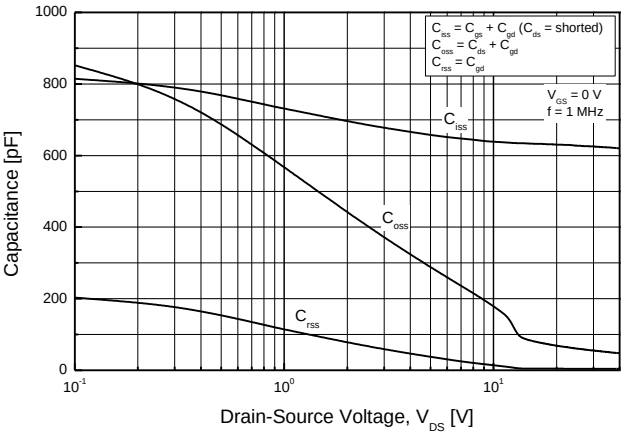
Note :
1. Repeated rating : Pulse width limited by safe operating area
2. L=21mH, I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J= 25 ℃
3 I_{SD} ≤ 4.5A, di/dt ≤ 200A/µs , V_{DD} ≤ BV_{DS}, Starting T_J= 25 ℃
4. Pulse Test :Pulse width ≤ 300µs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

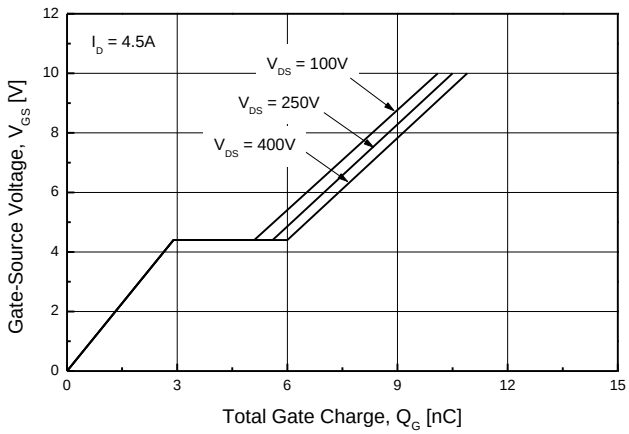

1. T_C = 25℃
2. 250μ s Pulse Test
Top V_GS=15.0V
10.0V
8.0V
7.0V
6.5V
6.0V
Bottom 5.0V
Drain Current, I_D [A]
Drain-Source Voltage, V_DS [V]

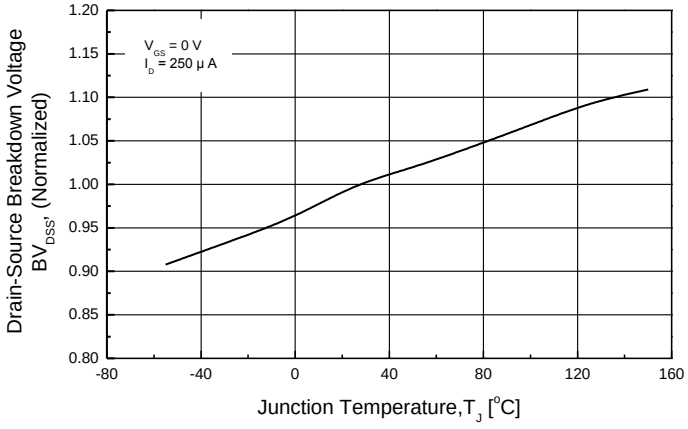

V_DS = 30V
250 μ s Pulse Test
150℃
25℃
Drain Current, I_D [A]
Gate-Source Voltage, V_GS [V]

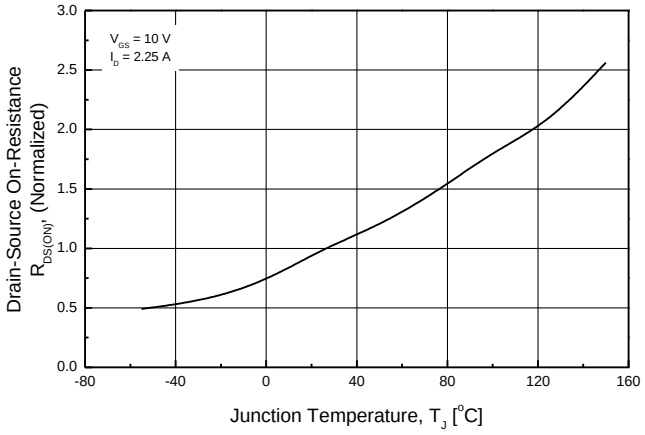

T_J = 25℃
V_GS = 10V
V_GS = 20V
Drain-Source On-Resistance
R_DS(ON) [Ω]
Drain Current,I_D [A]

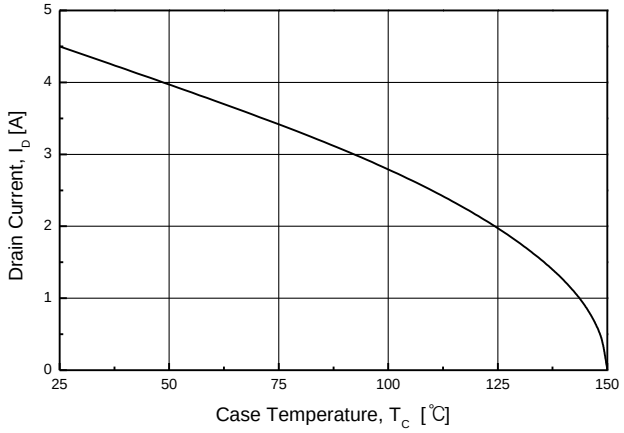

V_GS = 0V
250μ s Pulse Test
150℃
25℃
Reverse Drain Current, I_DR [A]
Source-Drain Voltage, V_SD [V]

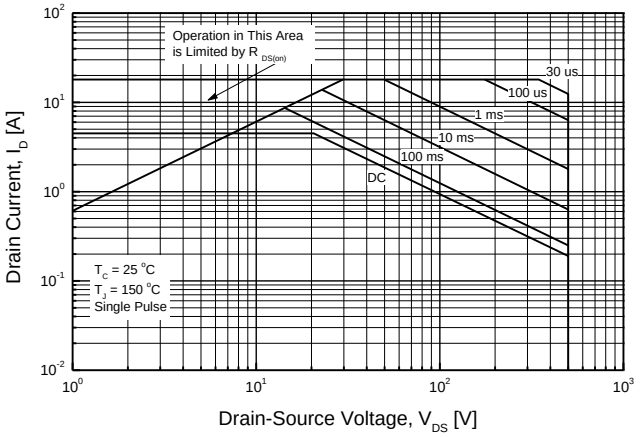

C_iss = C_gs + C_gd (C_ds = shorted)
C_oss = C_ds + C_gd
C_rss = C_gd
V_GS = 0 V
f = 1 MHz
C_iss
C_oss
C_rss
Capacitance [pF]
Drain-Source Voltage, V_DS [V]

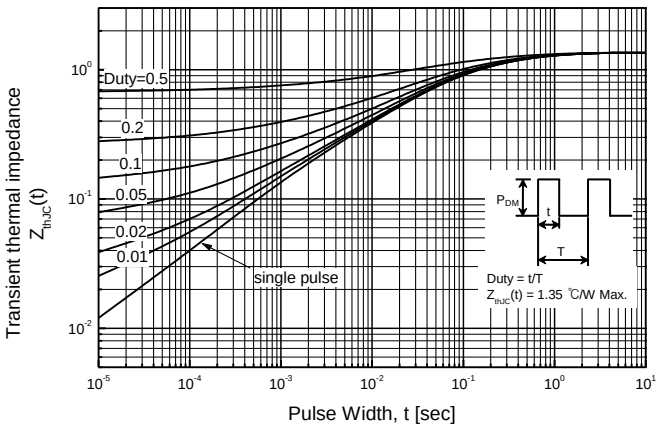

I_D = 4.5A
V_DS = 100V
V_DS = 250V
V_DS = 400V
Gate-Source Voltage, V_GS [V]
Total Gate Charge, Q_G [nC]


Drain-Source Breakdown Voltage
BV_DSS, (Normalized)
V_GS = 0 V
I_D = 250 μ A
1.20
1.15
1.10
1.05
1.00
0.95
0.90
0.85
0.80
-80
-40
0
40
80
120
160
Junction Temperature,T_J [°C]


Drain-Source On-Resistance
R_DS(ON), (Normalized)
V_GS = 10 V
I_D = 2.25 A
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-80
-40
0
40
80
120
160
Junction Temperature, T_J [°C]


Drain Current, I_D [A]
5
4
3
2
1
0
25
50
75
100
125
150
Case Temperature, T_C [℃]


Drain Current, I_D [A]
Operation in This Area
is Limited by R DS(on)
30 us
100 us
1 ms
10 ms
100 ms
DC
T_C = 25 °C
T_J = 150 °C
Single Pulse
10^2
10^1
10^0
10^-1
10^-2
10^0
10^1
10^2
10^3
Drain-Source Voltage, V_DS [V]


Transient thermal impedance
Z_thJC (t)
Duty=0.5
0.2
0.1
0.05
0.02
0.01
single pulse
P_DM
t
T
Duty = t/T
Z_thJC(t) = 1.35 ℃/W Max.
10^0
10^-1
10^-2
10^-5
10^-4
10^-3
10^-2
10^-1
10^0
10^1
Pulse Width, t [sec]