SNx4LVC14A Hex Schmitt-Trigger Inverters

1 Features

- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)
  - 1000-V charged-device model (C101)
- Operate from 1.65 V to 3.6 V V_{CC}
- Specified from –40°C to +85°C, –40°C to 125°C, and –55°C to 125°C
- Inputs accept voltages to 5.5 V
- Max t_{pd} of 6.4 ns at 3.3 V
- Typical V_{OLP} (output ground bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Barcode scanner
- Cable solutions
- E-books
- Embedded PCs
- Field transmitter: temperature or pressure sensors
- Fingerprint biometrics
- HVAC: heating, ventilating, and air conditioning
- Network attached storage (NAS)
- Server motherboard and PSU
- Software defined radio (SDR)
- TV: High-definition (HDTV), LCD, and digital
- Video communications systems
- Wireless data access cards, headsets, keyboards, mice, and LAN cards

3 Description

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

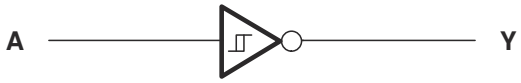
The devices contain six independent inverters and perform the Boolean function $Y = \overline{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54LVC14AFK	LCCC (20)	8.90 mm × 8.90 mm
SN54LVC14AJ	CDIP (14)	20.00 mm × 7.00 mm
SN54LVC14AW	CFP (14)	9.21 mm × 6.30 mm
SN74LVC14ANS	SO (14)	10.20 mm × 5.30 mm
SN74LVC14AD	SOIC (14)	8.65 mm × 6.00 mm
SN74LVC14ADB	SSOP (14)	6.20 mm × 5.30 mm
SN74LVC14APW	TSSOP (14)	5.00 mm × 4.40 mm
SN74LVC14ADGV	TVSOP (14)	4.40 mm × 3.60 mm
SN74LVC14ARGY	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision AB (June 2015) to Revision AC (April 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Removed the *Standard CMOS Inputs* section	11
• Added the *CMOS Schmitt-Trigger Inputs* section	11
• Removed *Δt/Δv* specifications throughout the data sheet	14

Changes from Revision AA (June 2015) to Revision AB (January 2019)	Page
• Changed order of the 'Features' list	1
• Deleted "I_{off} Support Live Insertion, Partial-Power-Down Mode and Back Drive protection" from Features list.	1
• Deleted *Device Options* table, see *Mechanical, Packaging, and Orderable Information* at the end of the data sheet	1
• Added $V_O > V_{CC}$ to Output clamp current in *Absolute Maximum Ratings*	5
• Changed MAX value for Output clamp current, I_{OK} from: –50 to: ±50	5
• Changed values in the *Thermal Information* table to align with JEDEC standards	6
• Added *Feature Description sections for Balanced High-Drive CMOS Push-Pull Outputs*, *Standard CMOS Inputs*, *Clamp Diodes*, and *Over-Voltage Tolerant Inputs*	11
• Added *Related Documentation* and *Receiving Notification of Documentation Updates* sections	16

Changes from Revision Z (January 2014) to Revision AA (June 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Moved T_{stg} to *Absolute Maximum Ratings* table	5

Changes from Revision Y (October 2010) to Revision Z (January 2014)	Page
• Updated document to new TI data sheet format	1
• Updated *Features*	1

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- Added Military Disclaimer to *Features* list.....1

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5 Pin Configuration and Functions

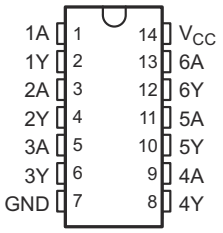


Figure 5-1. D, DB, DGV, NS, J, W, or PW Package, 14-Pin SOIC, SSOP, TVSOP, SO, CDIP, CFP, or TSSOP (Top View)

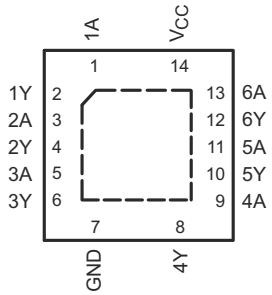


Figure 5-2. RGY Package, 14-Pin VQFN (Top View)

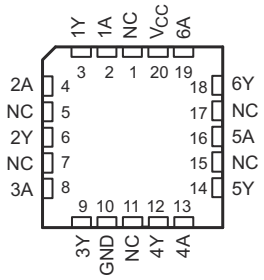


Figure 5-3. FK Package, 20-Pin LCCC (Top View)

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, SO, CDIP, CFP, TSSOP, VQFN	LCCC		
1A	1	2	I	Data input
2A	3	4	I	Data input
3A	5	8	I	Data input
4A	9	13	I	Data input
5A	11	16	I	Data input
6A	13	19	I	Data input
GND	7	10	—	Ground
V_{CC}	14	20	—	Positive supply
1Y	2	3	O	Data output
2Y	4	6	O	Data output
3Y	6	9	O	Data output
4Y	8	12	O	Data output
5Y	10	14	O	Data output
6Y	12	18	O	Data output
NC	—	1	—	No connection
		5		
		7		
		11		
		15		
		17		

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Output voltage(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
P_{tot}	Power dissipation	T_A = –40°C to +125°C(4) (5)		500	mW
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.
(4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
(5) For the DB, DGV, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+1000	
		Machine Model	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions: SN54LVC14A

See (1)

			SN54LVC14A –55 TO +125°C		UNIT
			MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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6.4 Recommended Operating Conditions: SN74LVC14A

See (1)

			SN74LVC14A						UNIT
			T_A = 25°C		–40 TO +85°C		–40 TO +125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4		–4		–4	mA
		V_{CC} = 2.3 V		–8		–8		–8	
		V_{CC} = 2.7 V		–12		–12		–12	
		V_{CC} = 3 V		–24		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4		4		4	mA
		V_{CC} = 2.3 V		8		8		8	
		V_{CC} = 2.7 V		12		12		12	
		V_{CC} = 3 V		24		24		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.5 Thermal Information

THERMAL METRIC(1)		SN74LVC14A						UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SO)	PW (TSSOP)	RGY (LCCC)	
		14 PINS					20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.6	131.8	153.5	115.7	145.9	93.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.2	83.9	75.2	72.2	73.4	106.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.9	79.2	86.6	74.4	87.7	69.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	39.3	41.7	19.9	33.7	18.9	22.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.6	78.6	85.9	74.1	87.1	70.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	49.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics, SN54LVC14A

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54LVC14A			UNIT
				–55 TO +125°C			
				MIN	TYP	MAX	
V_{T+}	Positive-going threshold		2.7 V	0.8		2	V
			3 V	0.9		2	
			3.6 V	1.1		2	
V_{T-}	Negative-going threshold		2.7 V	0.4		1.4	V
			3 V	0.6		1.5	
			3.6 V	0.8		1.7	

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6.6 Electrical Characteristics, SN54LVC14A (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54LVC14A			UNIT
				–55 TO +125°C			
				MIN	TYP	MAX	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		2.7 V	0.3		1.1	V
			3 V	0.3		1.2	
			3.6 V	0.3		1.2	
V_{OH}		I_{OH} = –100 µA	2.7 V to 3.6 V	V_{CC} – 0.2			V
		V_{OL}	2.7 V	2.2			
			I_I	2.4			
		I_{CC}	3 V	2.2			
ΔI_{CC}		I_{OL} = 100 µA	2.7 V to 3.6 V			0.2	V
		C_i	2.7 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
		V_I = 5.5 V or GND	3.6 V			±5	µA
		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V			10	µA
		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	µA
		$V_I = V_{CC}$ or GND	3.3 V		5[1]		pF

(1) T_A = 25°C

6.7 Electrical Characteristics, SN74LVC14A

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN74LVC14A						UNIT
				T_A = 25°C			–40 TO +85°C		–40 TO +125°C	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+}	Positive-going threshold		1.65 V	0.4		1.3	0.4	1.3	0.4	1.3	V
			1.95 V	0.6		1.5	0.6	1.5	0.6	1.5	
			2.3 V	0.8		1.7	0.8	1.7	0.8	1.7	
			2.5 V	0.8		1.7	0.8	1.7	0.8	1.7	
			2.7 V	0.8		2	0.8	2	0.8	2	
			3 V	0.9		2	0.9	2	0.9	2	
			3.6 V	1.1		2	1.1	2	1.1	2	
$V_{T–}$	Negative-going threshold		1.65 V	0.15		0.85	0.15	0.85	0.15	0.85	V
			1.95 V	0.25		0.95	0.25	0.95	0.25	0.95	
			2.3 V	0.4		1.2	0.4	1.2	0.4	1.2	
			2.5 V	0.4		1.2	0.4	1.2	0.4	1.2	
			2.7 V	0.4		1.4	0.4	1.4	0.4	1.4	
			3 V	0.6		1.5	0.6	1.5	0.6	1.5	
			3.6 V	0.8		1.7	0.8	1.7	0.8	1.7	

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6.7 Electrical Characteristics, SN74LVC14A (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LVC14A							UNIT
			T_A = 25°C			–40 TO +85°C		–40 TO +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		1.65 V	0.1		1.15	0.1	1.15	0.1	1.15	V
		1.95 V	0.15		1.25	0.15	1.25	0.15	1.25	
		2.3 V	0.25		1.3	0.25	1.3	0.25	1.3	
		2.5 V	0.25		1.3	0.25	1.3	0.25	1.3	
		2.7 V	0.3		1.1	0.3	1.1	0.3	1.1	
		3 V	0.3		1.2	0.3	1.2	0.3	1.2	
		3.6 V	0.3		1.2	0.3	1.2	0.3	1.2	
V_{OH}	I_{OH} = –100 µA	1.65 V to 3.6 V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.3		V
	I_{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I_{OH} = –8 mA	2.3 V	1.9			1.7		1.65		
	I_{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
	I_{OH} = –24 mA	3 V	2.3			2.2		2		
V_{OL}	I_{OL} = 100 µA	1.65 V to 3.6 V			0.1		0.2		0.3	V
	I_{OL} = 4 mA	1.65 V			0.24		0.45		0.6	
	I_{OL} = 8 mA	2.3 V			0.3		0.7		0.75	
	I_{OL} = 12 mA	2.7 V			0.4		0.4		0.6	
	I_{OL} = 24 mA	3 V			0.55		0.55		0.8	
I_I	V_I = 5.5 V or GND	3.6 V			±1		±5		±20	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			1		10		40	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500		500		5000	µA
C_i	V_I = V_{CC} or GND	3.3 V		5						pF

6.8 Switching Characteristics, SN54LVC14A

over operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54LVC14A		UNIT
				–55 TO +125°C		
				MIN	MAX	
t_{pd}	A	Y	2.7 V		7.5	ns
			3.3 V ± 0.3 V	1	6.4	

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6.9 Switching Characteristics, SN74LVC14A

over operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74LVC14A							UNIT
				T_A = 25°C			–40 TO +85°C		–40 TO +125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.8 V ± 0.15 V	1	5	10.5	1	11	1	13	ns
			2.5 V ± 0.2 V	1	3.4	7.3	1	7.8	1	10	
			2.7 V	1	3.6	7.3	1	7.5	1	9.5	
			3.3 V ± 0.3 V	1	3.2	6.2	1	6.4	1	8	
$t_{sk(o)}$			3.3 V ± 0.3 V			1		1		1.5	ns

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	11	12	15	pF

6.11 Typical Characteristics

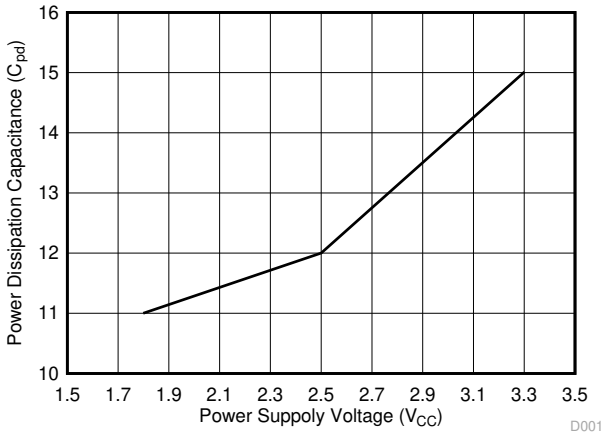
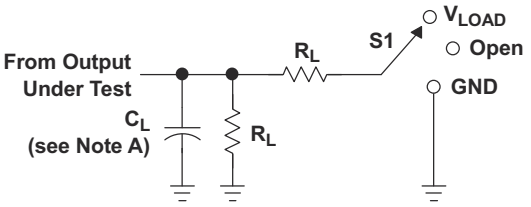


Figure 6-1. Power Dissipation Capacitance vs. Power Supply Voltage

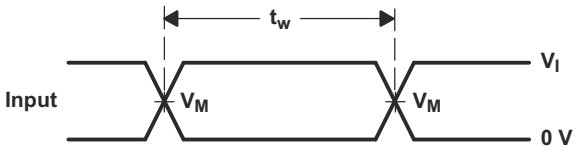
7 Parameter Measurement Information



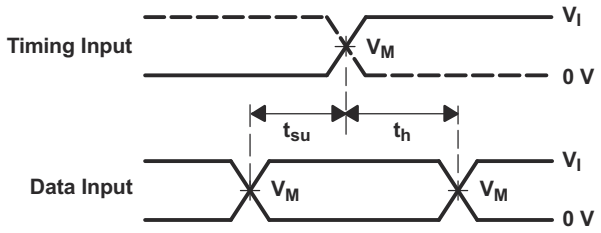
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

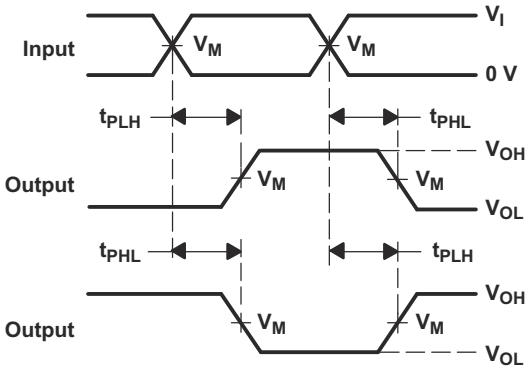
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kW	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 W	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V



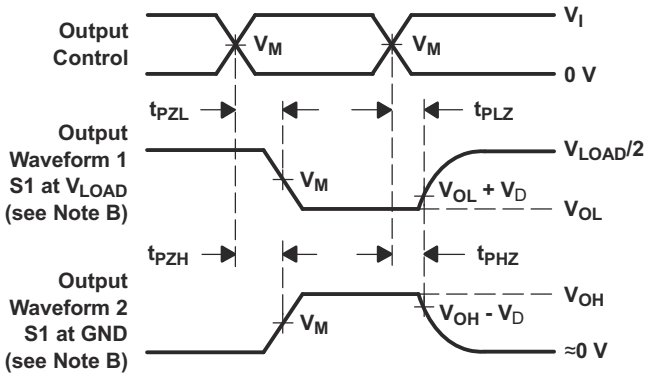
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 W.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

The devices contain six independent inverters and perform the Boolean function $Y = \overline{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

8.2 Functional Block Diagram

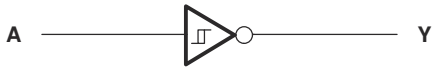


Figure 8-1. Logic Diagram, Each Inverter (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* section must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

8.3.3 Clamp Diodes

The inputs to this device have negative clamping diodes. The outputs to this device have both positive and negative clamping diodes as shown in Figure 8-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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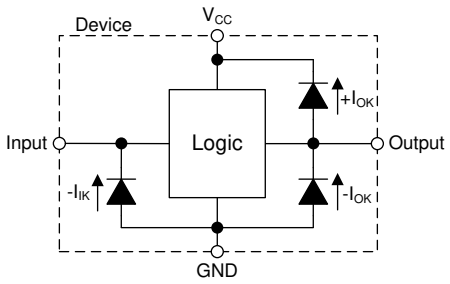


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings table*.

8.4 Device Functional Modes

Table 8-1 lists the functional modes for the SN54LVC14A and SN74LVC14A devices.

Table 8-1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

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9 Application and Implementation

Note

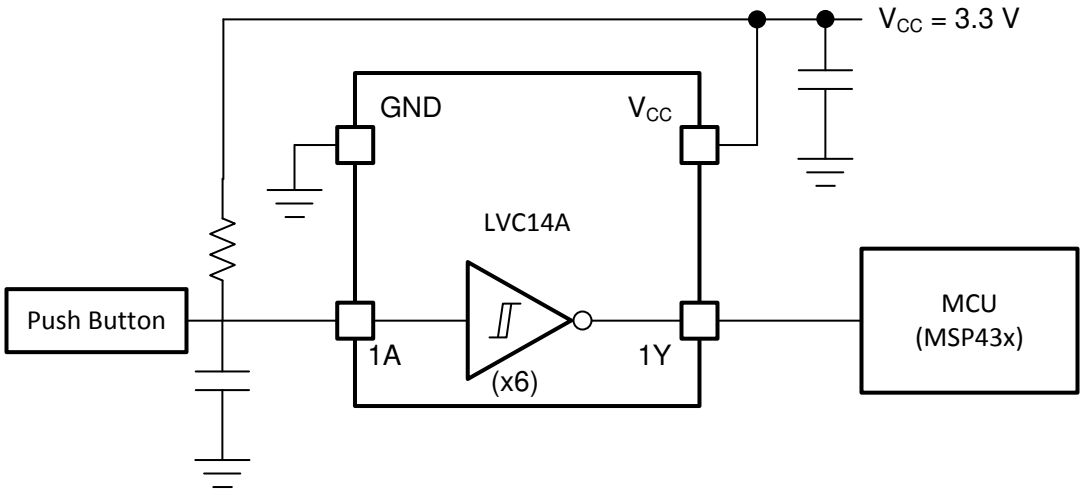
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Physically interactive interface elements like push buttons or rotary knobs offer simple and easy ways to interact with an electronic system. Many of these physical interface elements often have issues with bouncing, or where the physical conductive contact can connect and disconnect multiple times during a button push or release. This bouncing can cause one or more faulty transient signals to be passed during this transitional period. These faulty signals can be observed in many common applications: for example, a television remote with bouncing error can adjust the TV channel multiple times despite the button being pushed only once. To mitigate these faulty signals, use a Schmitt-trigger, or a device with hysteresis, to remove these faulty signals. Hysteresis allows a device to *remember* its history, and in this case, the LVC14A uses this memory to debounce the physical element's signal, or filter the faulty transient signals and pass only the valid signal each time the element is used. In this example, we show a push button signal passed through an LVC14A that is debounced and inverted to the MCU for push detection.

9.2 Typical Application

The signal effects of the debounce circuit can be seen when comparing Figure 9-2 and Figure 9-3. In Figure 9-2, the input is a very poor quality signal due to the error in the physical push button. If the MCU attempts to sample this input to detect a push, there is high probability that multiple push events will be falsely detected. Once the debounce circuit has been implemented, the input is cleaned up, and the MCU can perform push detection without any error, as seen in Figure 9-3.



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Figure 9-1. Debouncer Application Diagram

9.2.1 Design Requirements

The SN74LVC14A device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

The SN74LVC14A allows for performing logical Boolean functions with hysteresis using digital signals. All input signals should remain as close as possible to either 0 V or V_{CC} for optimal operation.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions: SN74LVC14A* table.
   - Inputs and outputs are overvoltage tolerant and can therefore go as high as 3.6 V at any valid V_{CC}.
2. Recommended output conditions:
   - Load currents should not exceed ±50 mA.
3. Frequency selection criterion:
   - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the *Layout* section

9.2.3 Application Curves

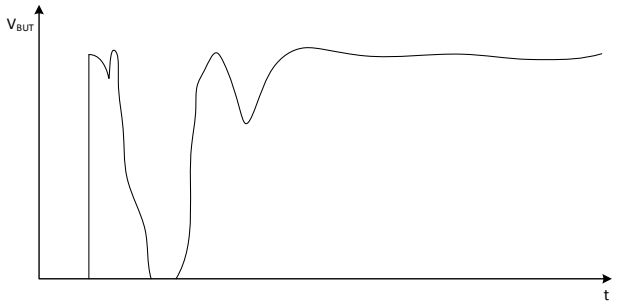


Figure 9-2. Input Response Without Debounce Circuit

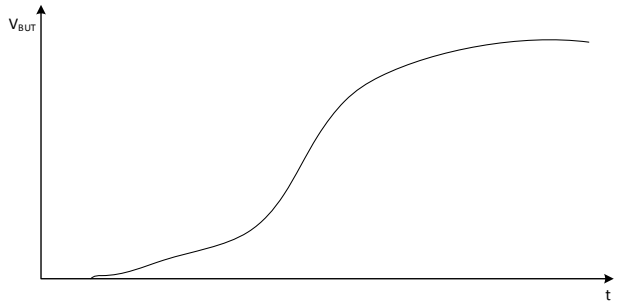


Figure 9-3. Input Response With Debounce Circuit

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Absolute Maximum Ratings* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

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11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. Figure 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

11.2 Layout Examples

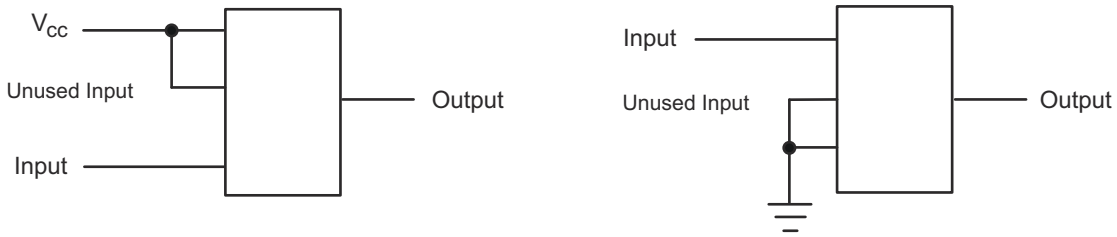


Figure 11-1. Layout Diagrams

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9761501Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501Q2A SNJ54LVC 14AFK	Samples
5962-9761501QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501QCA SNJ54LVC14AJ	Samples
5962-9761501QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501QDA SNJ54LVC14AW	Samples
5962-9761501V2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501V2A SNV54LVC 14AFK	Samples
5962-9761501VCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501VCA SNV54LVC14AJ	Samples
5962-9761501VDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501VDA SNV54LVC14AW	Samples
SN74LVC14AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14ADBRE4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14ADE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14ADRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC14ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC14A	Samples
SN74LVC14APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14APWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14APWTG4	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC14A	Samples
SN74LVC14ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC14A	Samples
SN74LVC14ARGYRG4	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC14A	Samples
SNJ54LVC14AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501Q2A SNJ54LVC 14AFK	Samples
SNJ54LVC14AJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501QC A SNJ54LVC14AJ	Samples
SNJ54LVC14AW	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761501QD A SNJ54LVC14AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LVC14A, SN54LVC14A-SP, SN74LVC14A :

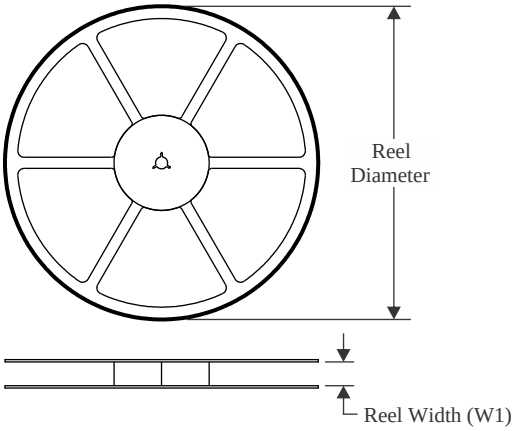
- Catalog : SN74LVC14A, SN54LVC14A
- Automotive : SN74LVC14A-Q1, SN74LVC14A-Q1
- Enhanced Product : SN74LVC14A-EP, SN74LVC14A-EP
- Military : SN54LVC14A
- Space : SN54LVC14A-SP

NOTE: Qualified Version Definitions:

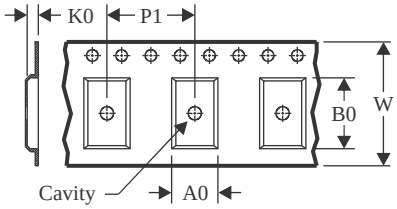
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

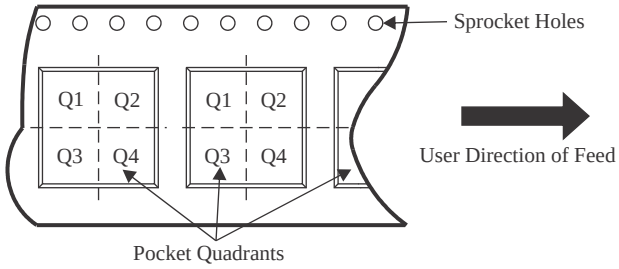


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

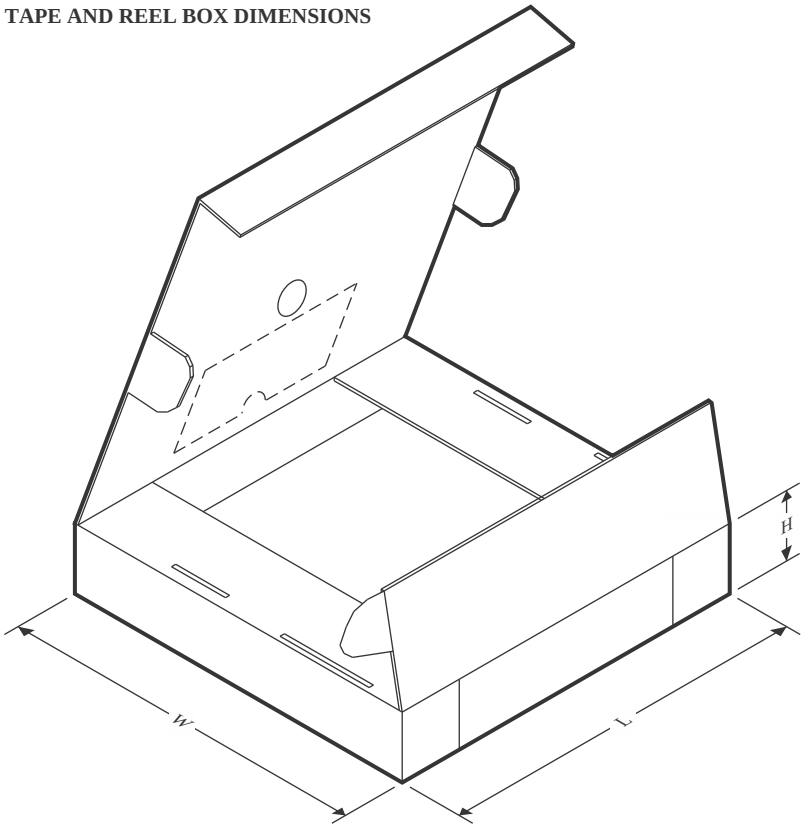
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC14ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC14ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74LVC14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74LVC14ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

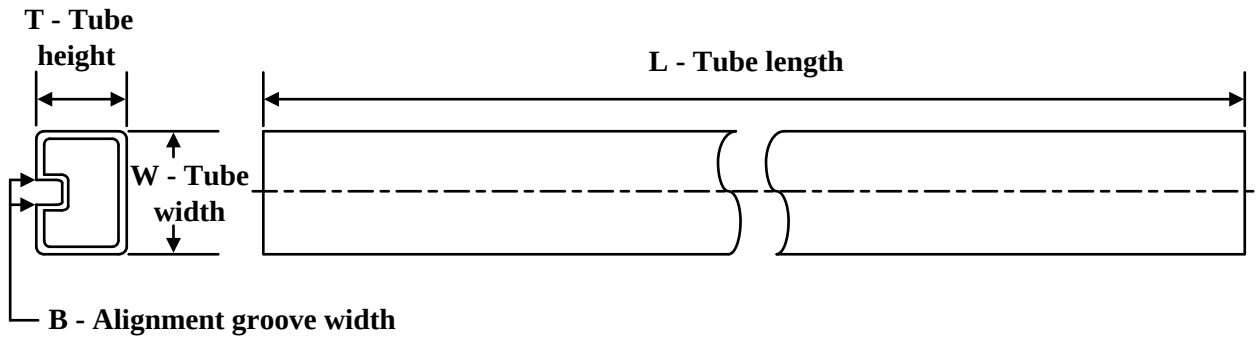
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC14ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC14ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LVC14ADR	SOIC	D	14	2500	340.5	336.1	32.0
SN74LVC14ADR	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC14ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC14ADRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC14ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74LVC14ADRG4	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC14ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC14ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC14APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC14APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC14APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC14APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC14APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC14ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE

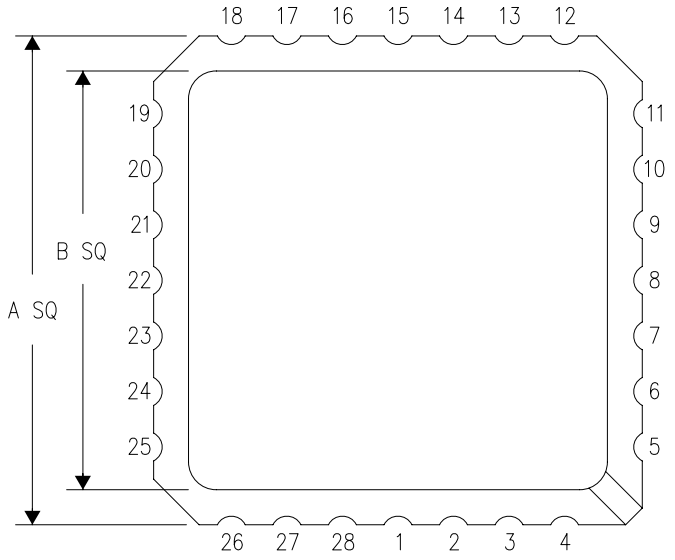


*All dimensions are nominal

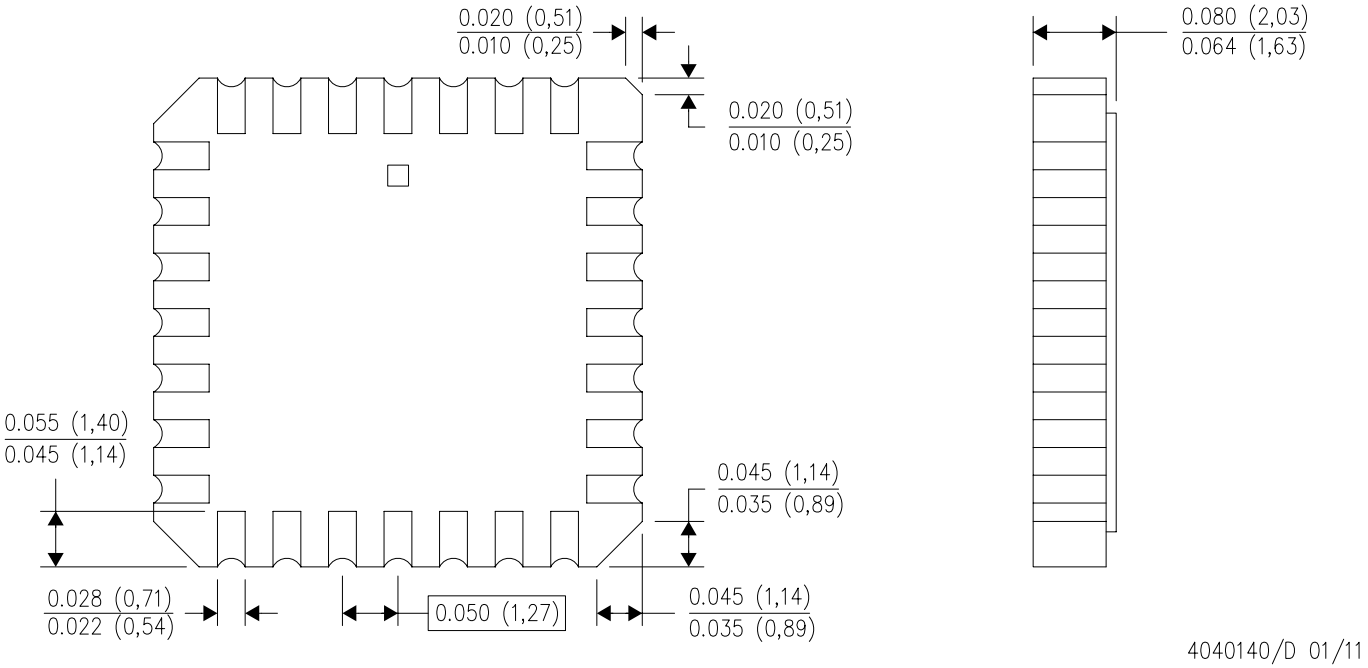
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9761501Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9761501QDA	W	CFP	14	1	506.98	26.16	6220	NA
5962-9761501V2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9761501VDA	W	CFP	14	1	506.98	26.16	6220	NA
SN74LVC14AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC14ADE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC14ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC14APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC14APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC14AFK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54LVC14AW	W	CFP	14	1	506.98	26.16	6220	NA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



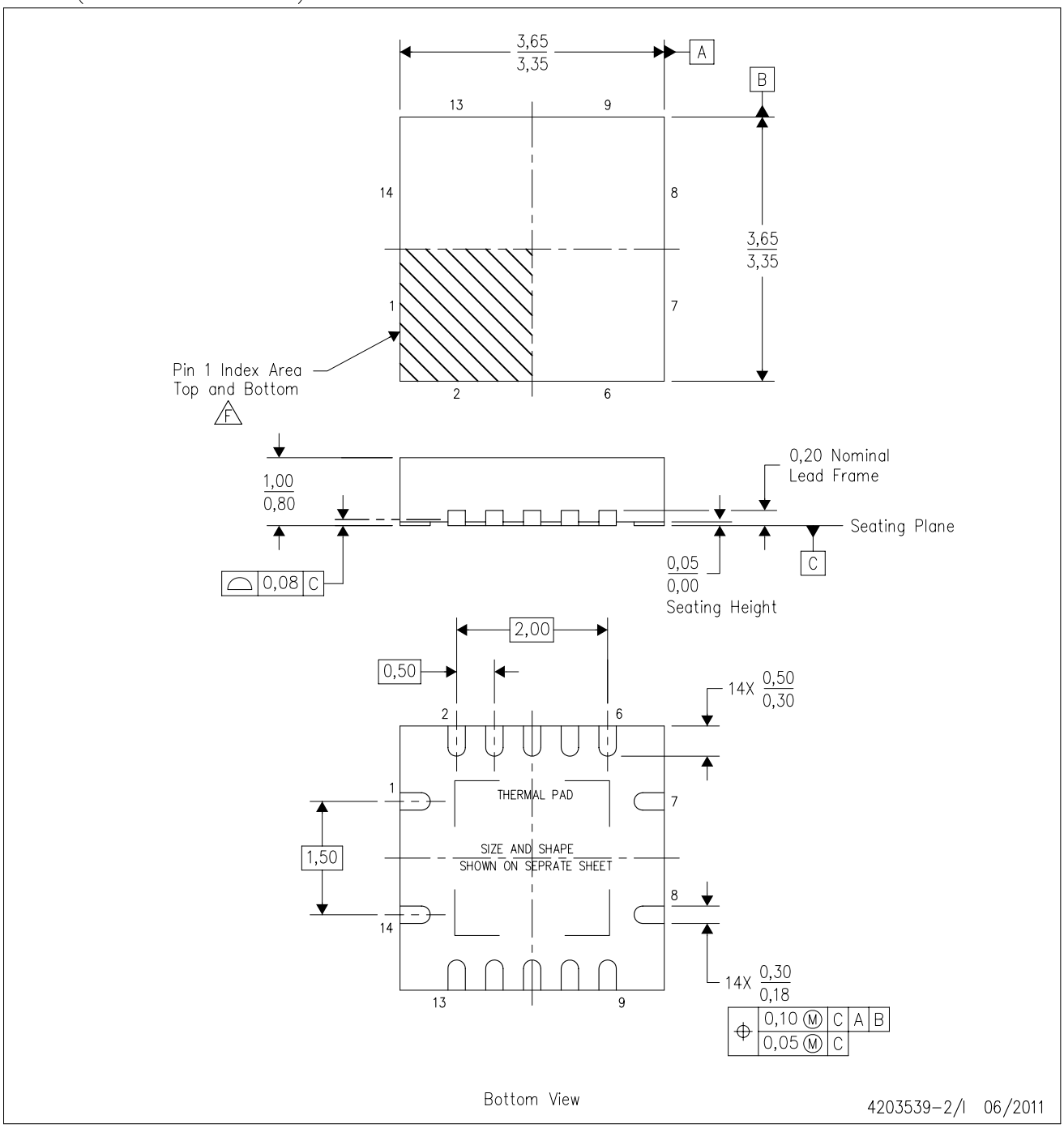
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

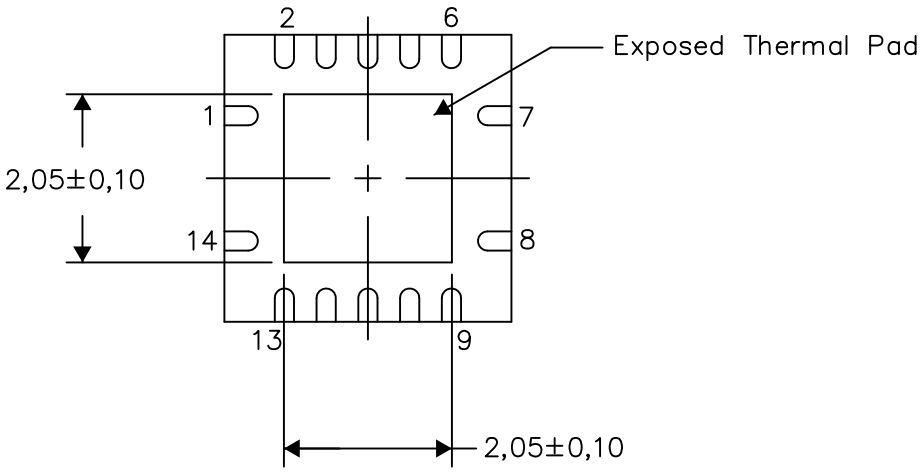
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



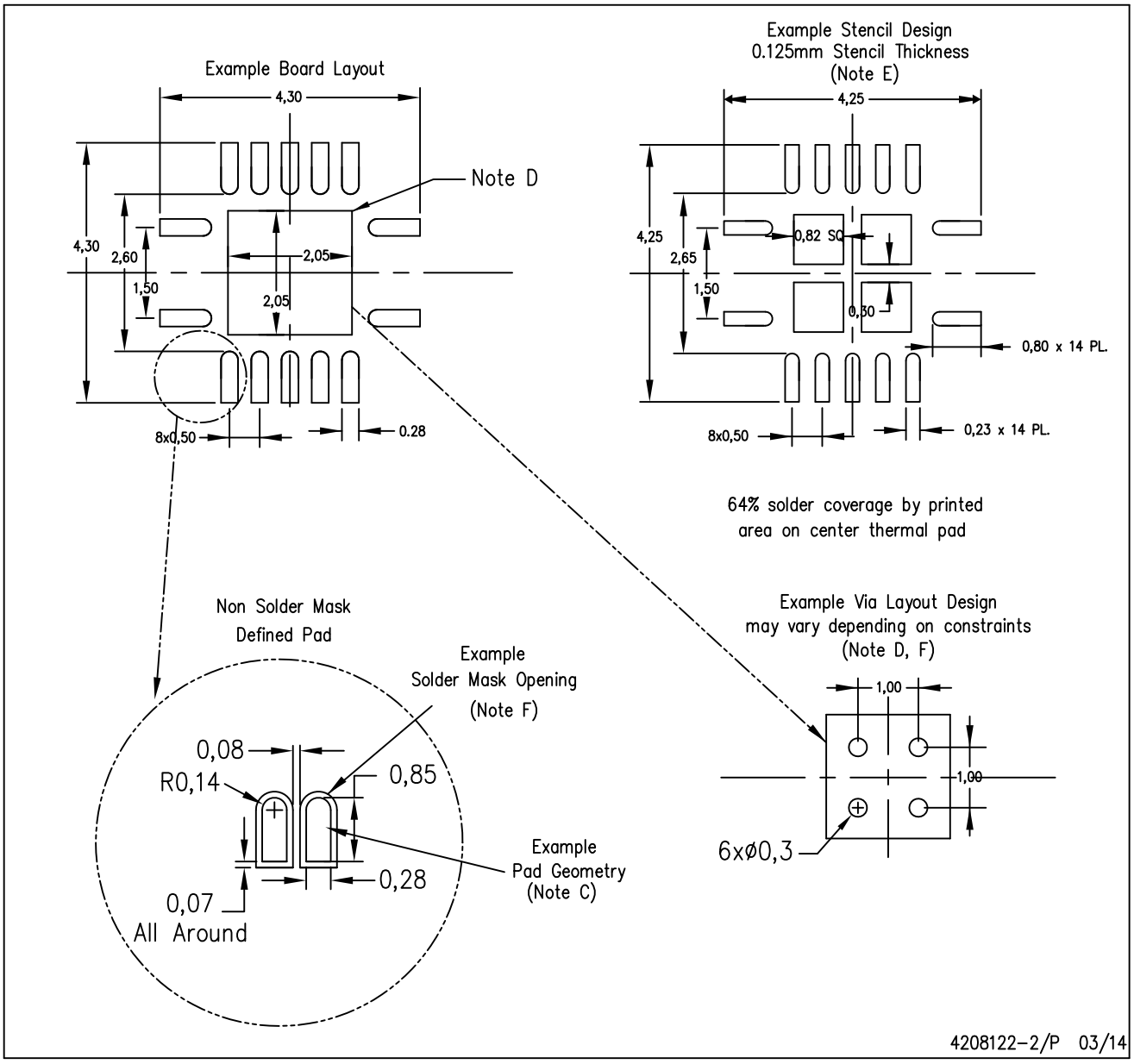
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

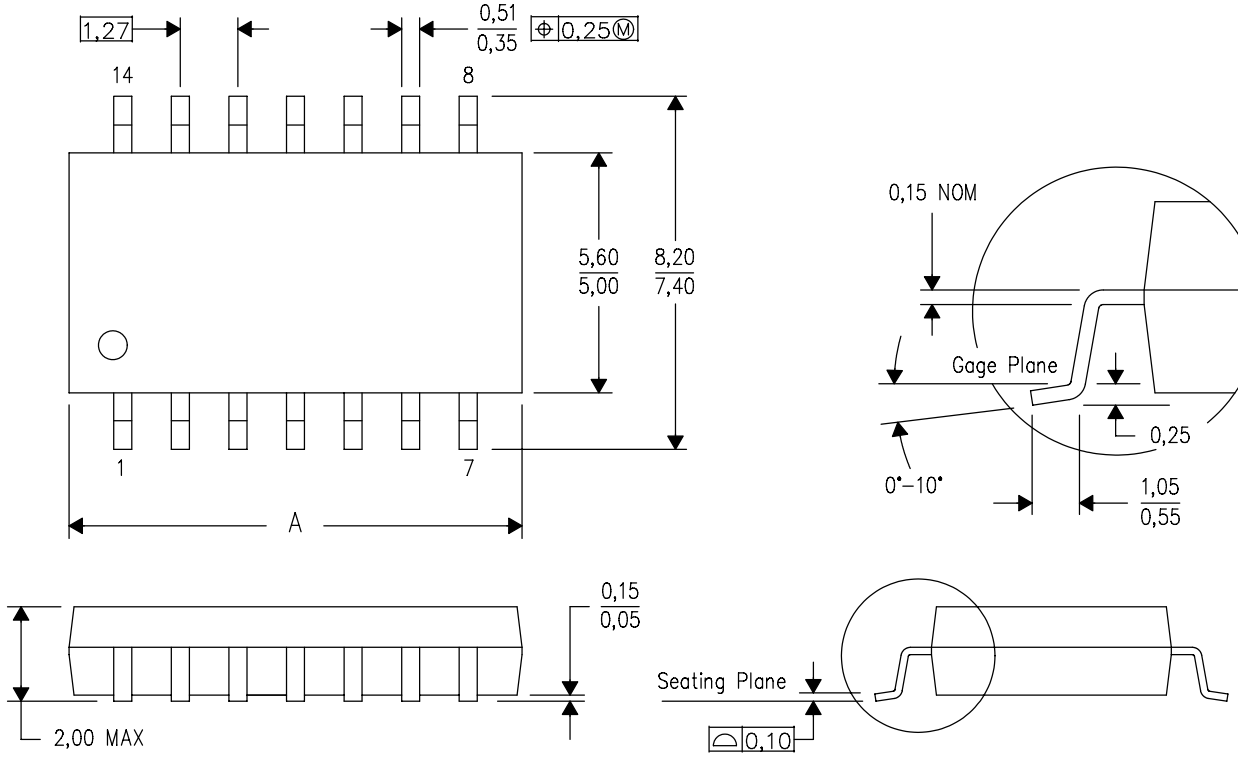


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

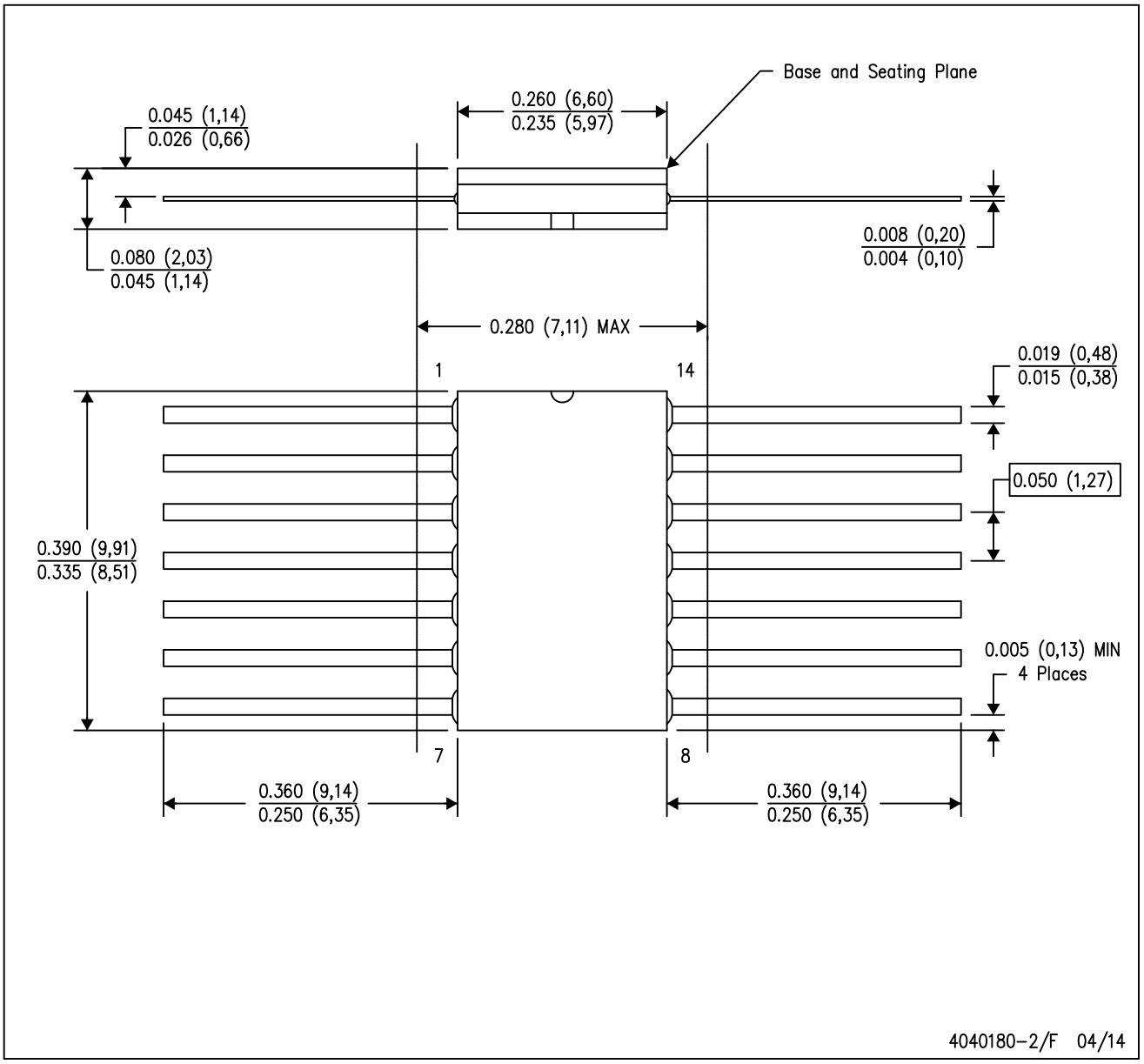


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

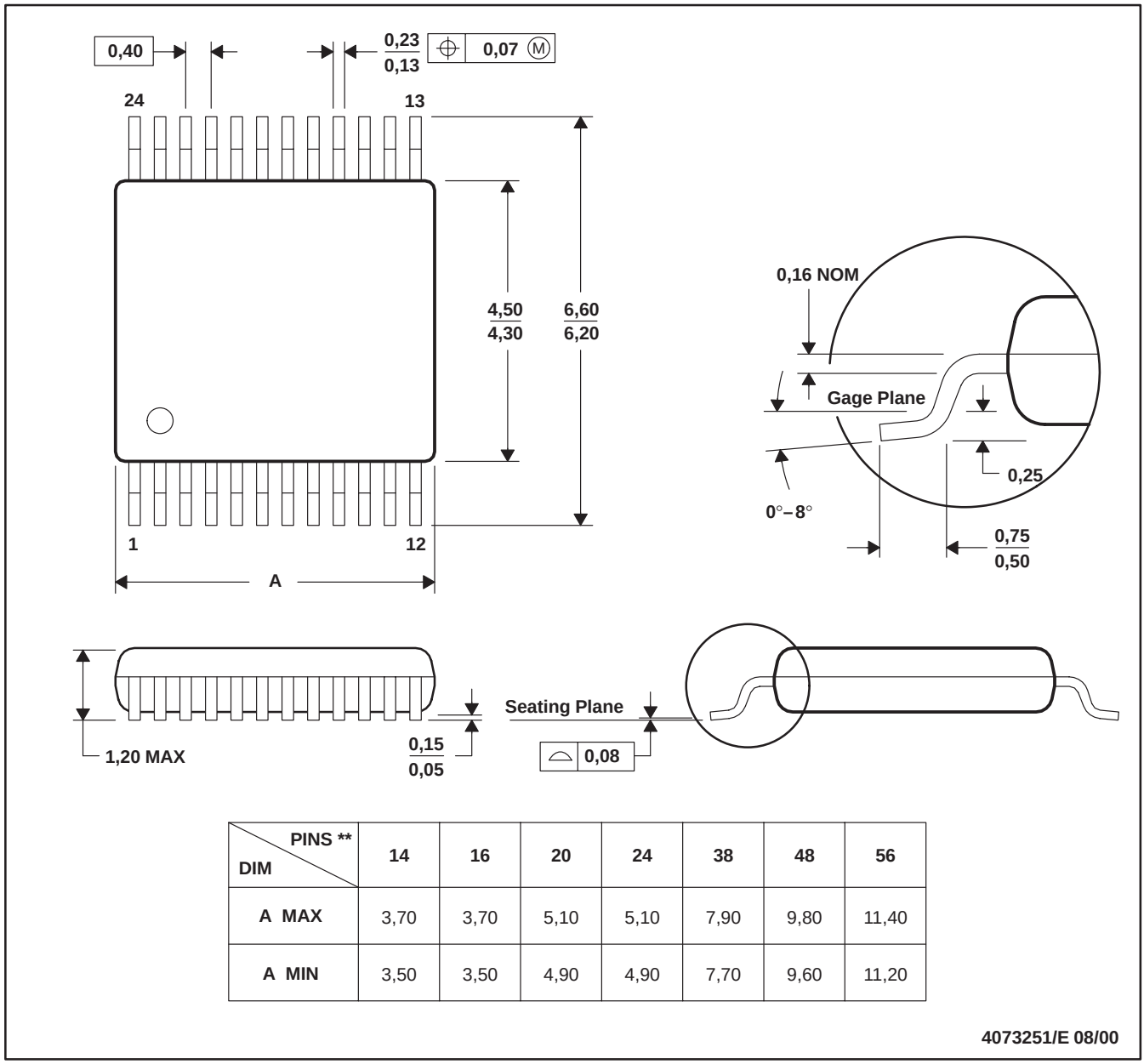
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

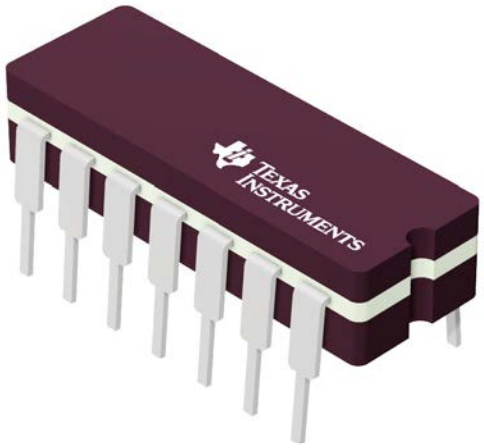
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

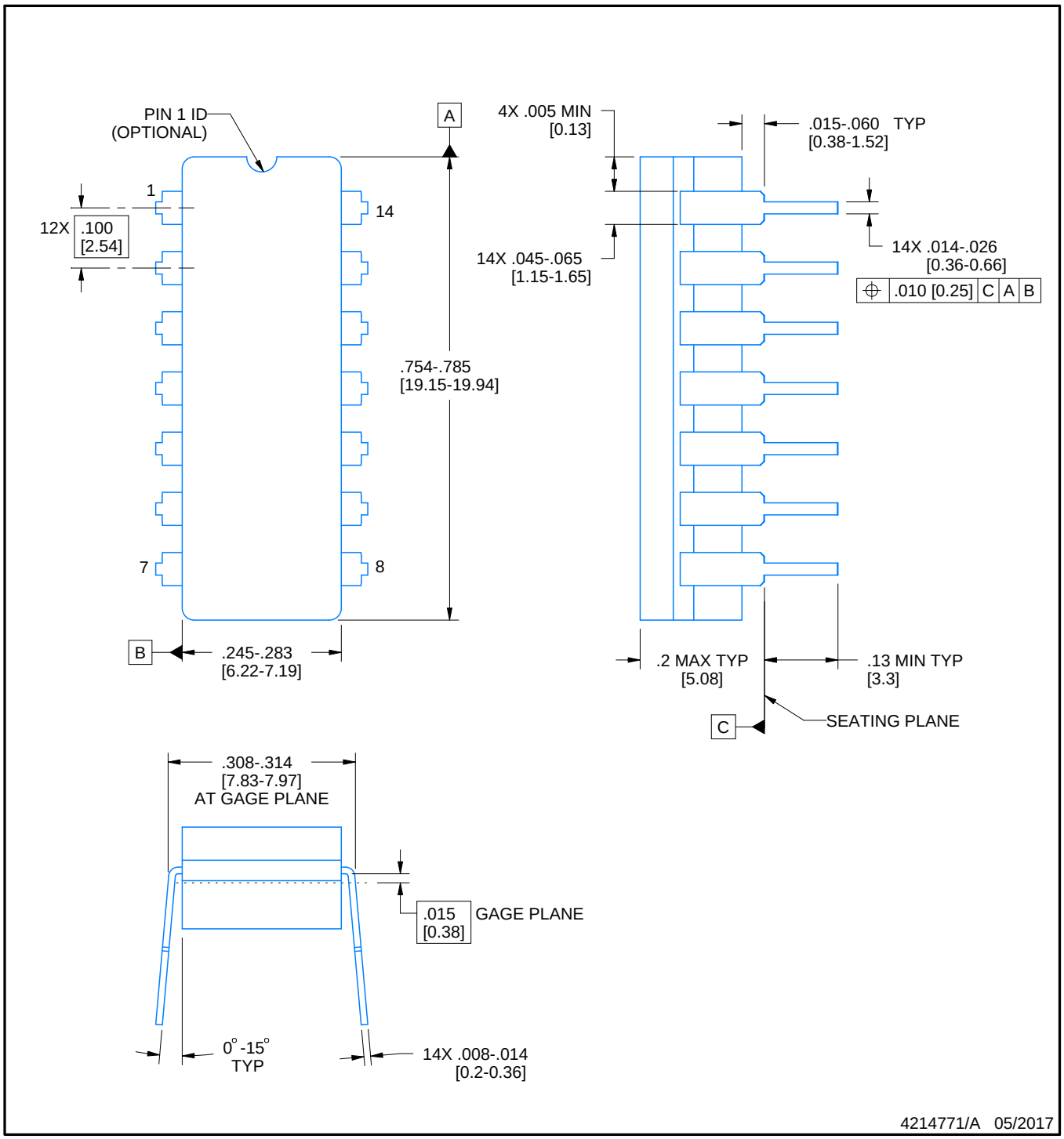


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

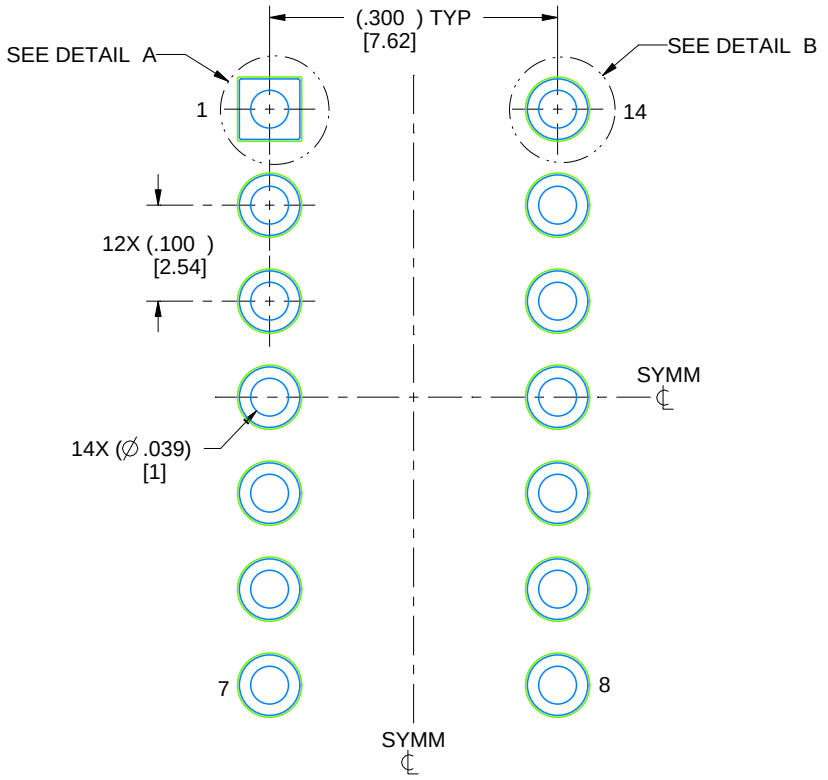
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

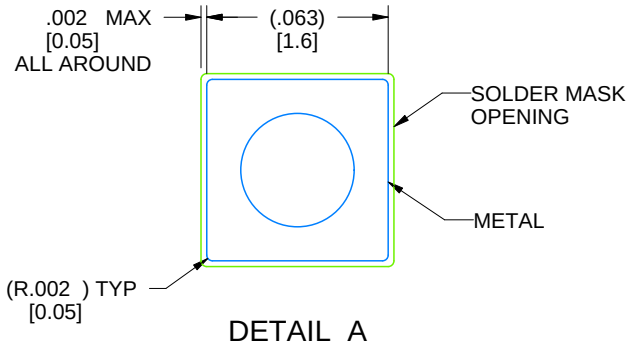
J0014A

CDIP - 5.08 mm max height

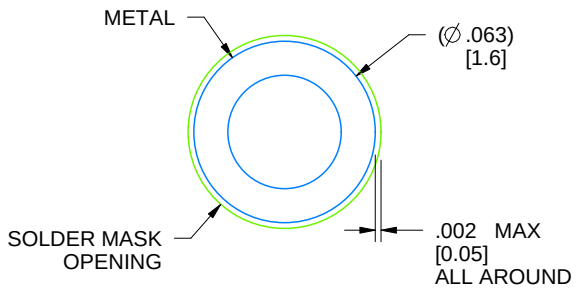
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



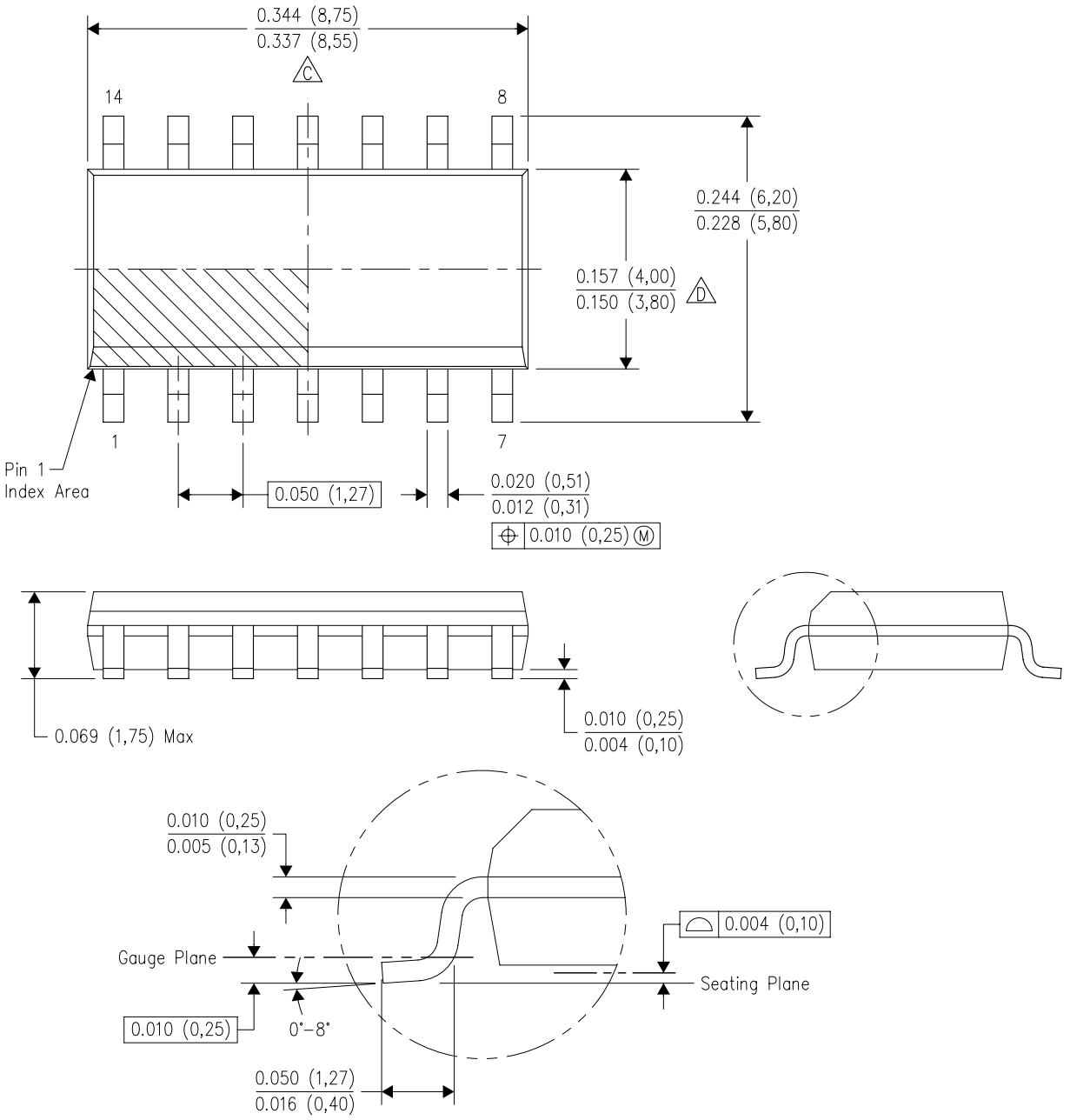
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

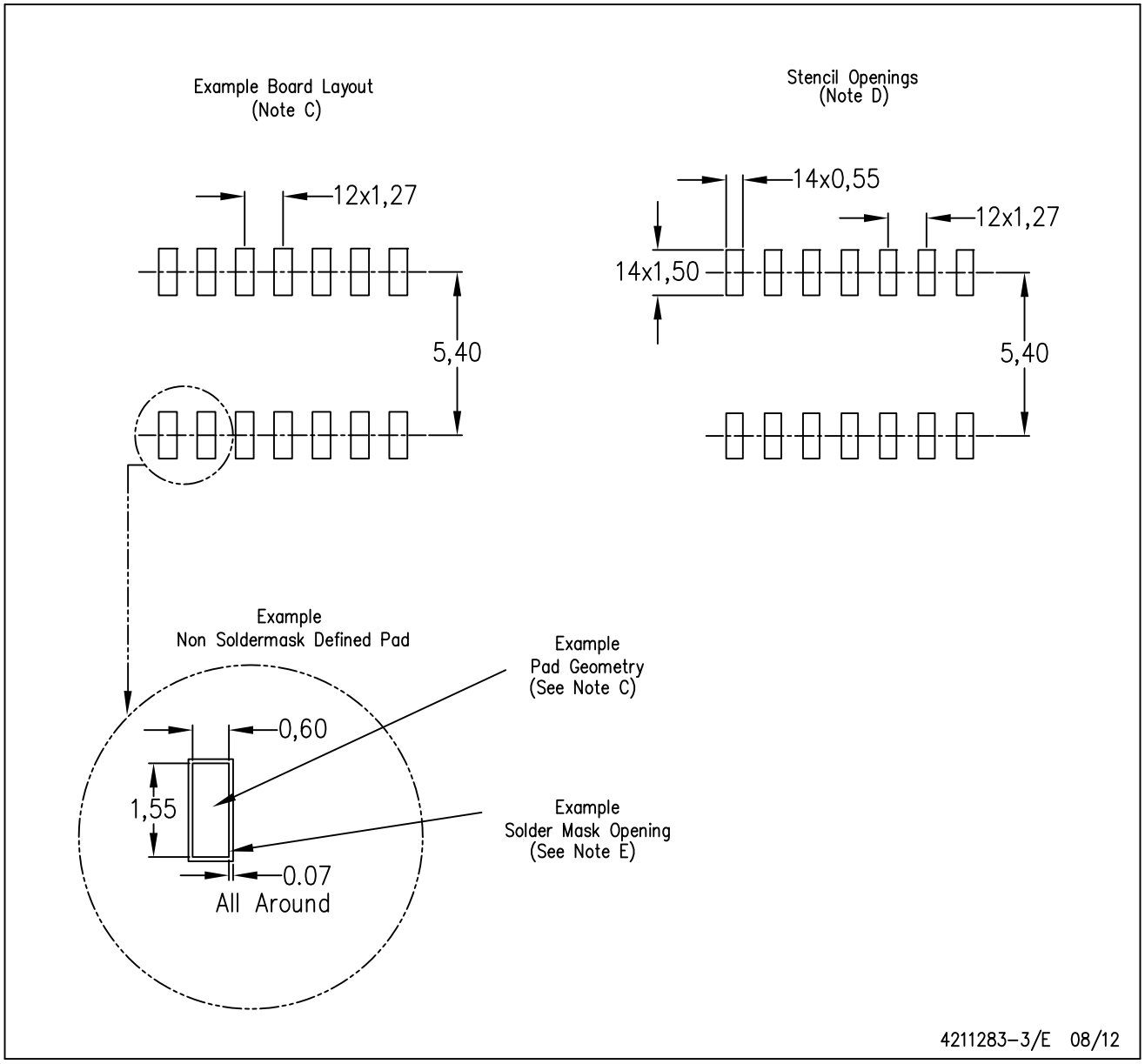
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

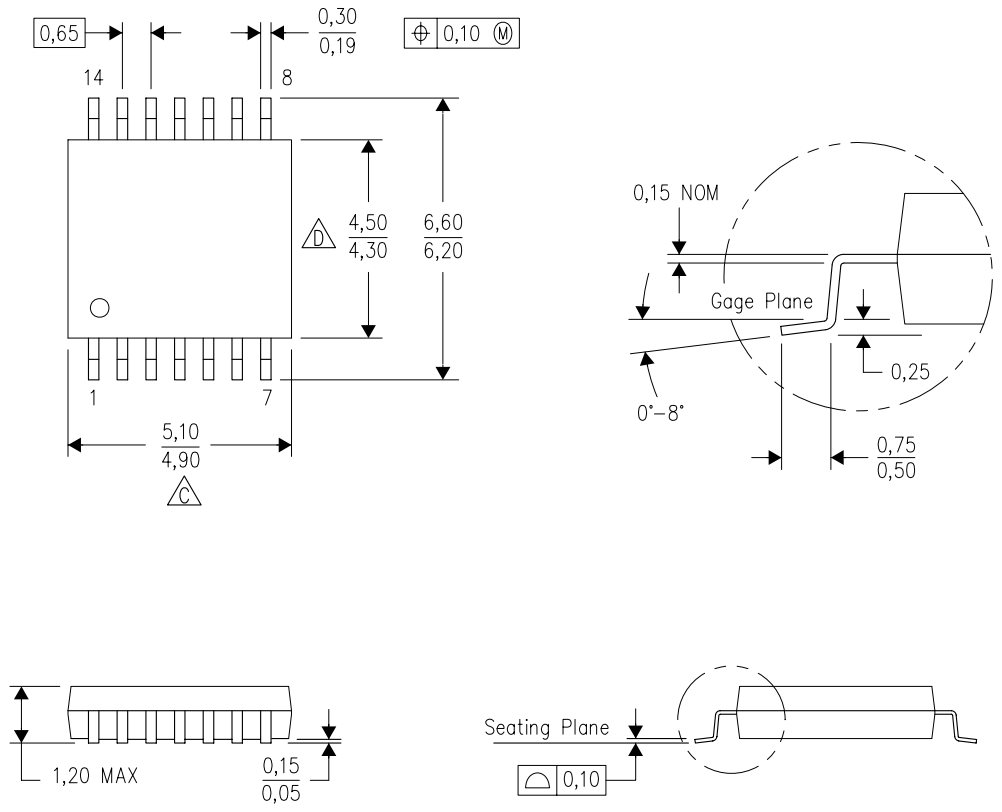
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

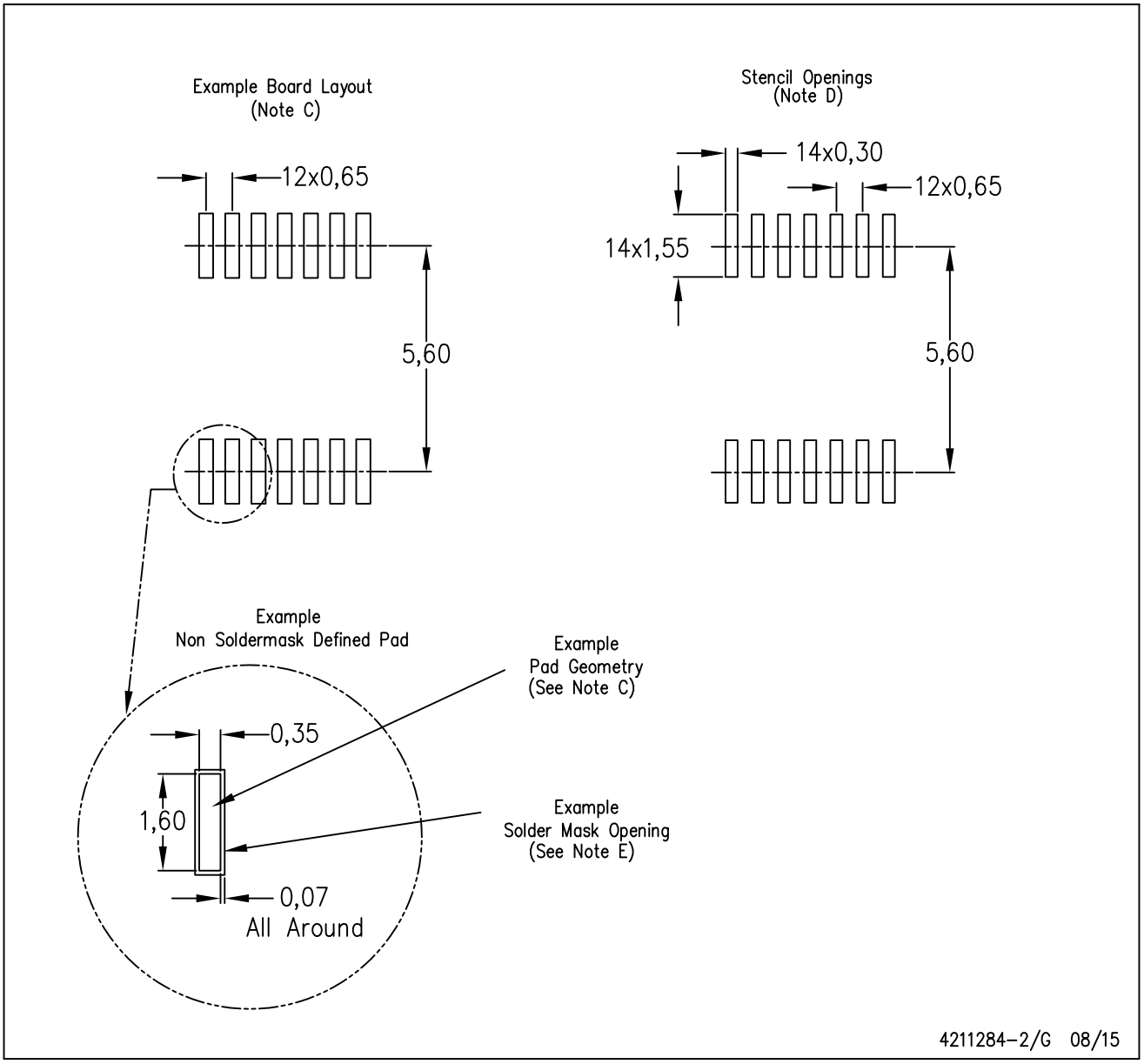
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

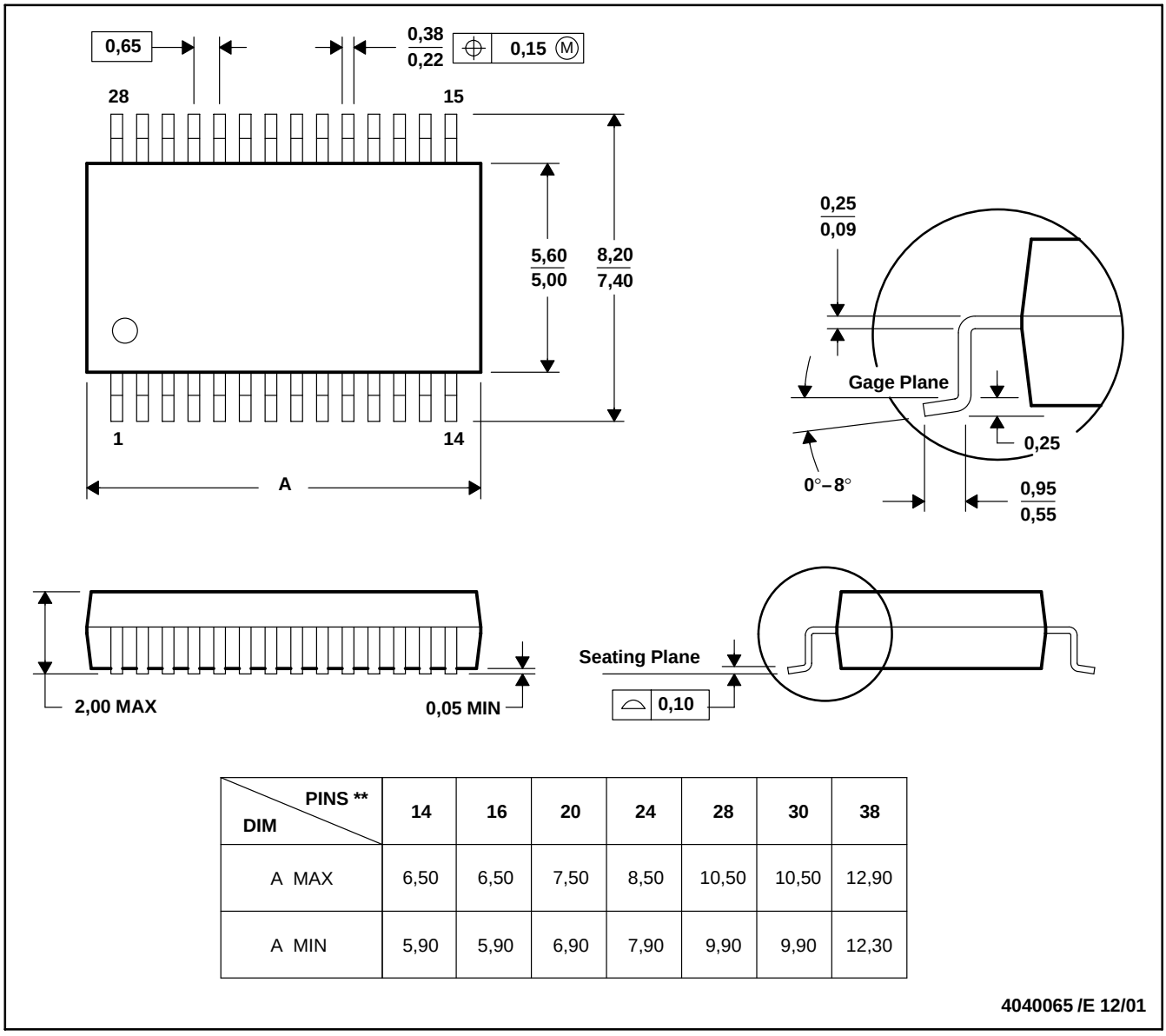


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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