

PDTD113ZT

NPN 500 mA, 50 V resistor-equipped transistor; R1 = 1 kΩ, R2 = 10 kΩ

Rev. 02 — 23 March 2009 Product data sheet

1. Product profile

1.1 General description

NPN 500 mA Resistor-Equipped Transistor (RET) in a small Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTB113ZT.

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- 500 mA output current capability
- Reduces component count
- Reduces pick and place costs
- ±10 % resistor ratio tolerance

1.3 Applications

- Digital application in automotive and industrial segments
- Controlling IC inputs
- Cost-saving alternative for BC817 series in digital applications
- Switching loads

1.4 Quick reference data

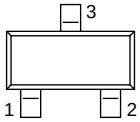
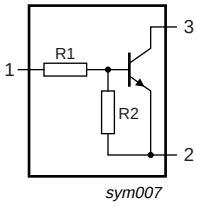
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	500	mA
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		9	10	11	

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2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	input (base)		
2	GND (emitter)		
3	output (collector)		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTD113ZT	-	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTD113ZT	*7V

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	5	V
V_I	input voltage				
	positive		-	+10	V
	negative		-	–5	V
I_O	output current		-	500	mA

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Table 5. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	250	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

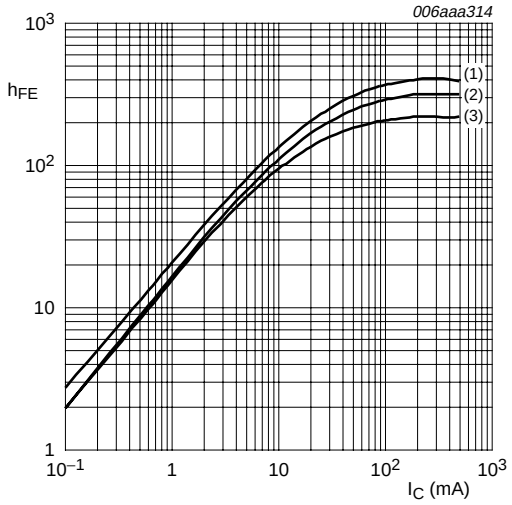
7. Characteristics

Table 7. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = 40 V; I_E = 0 A	-	-	100	nA
		V_{CB} = 50 V; I_E = 0 A	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 50 V; I_B = 0 A	-	-	0.5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	-	-	0.8	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 50 mA	70	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 50 mA; I_B = 2.5 mA	-	-	0.3	V
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA	0.3	0.6	1	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 20 mA	0.4	0.8	1.4	V
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		9	10	11	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 100 MHz	-	7	-	pF

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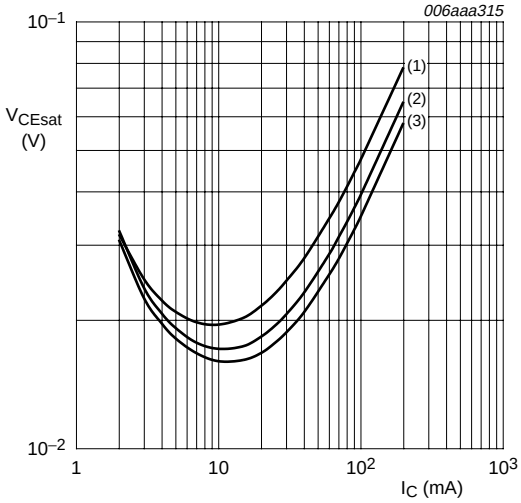
V_{CE} = 5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 1. DC current gain as a function of collector current; typical values



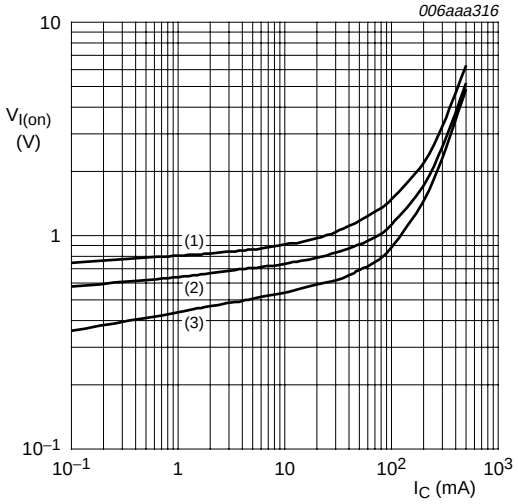
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values



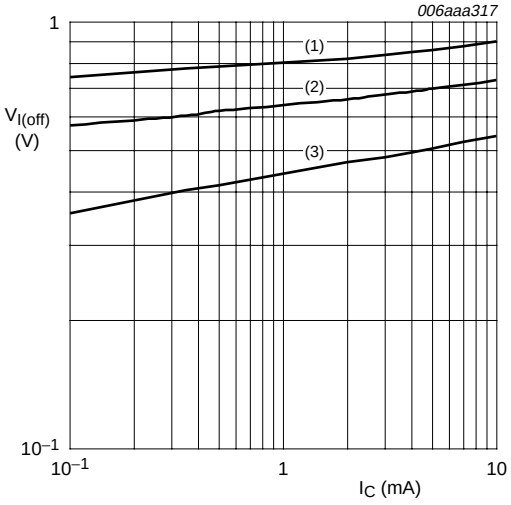
V_{CE} = 0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 3. On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 4. Off-state input voltage as a function of collector current; typical values

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8. Package outline

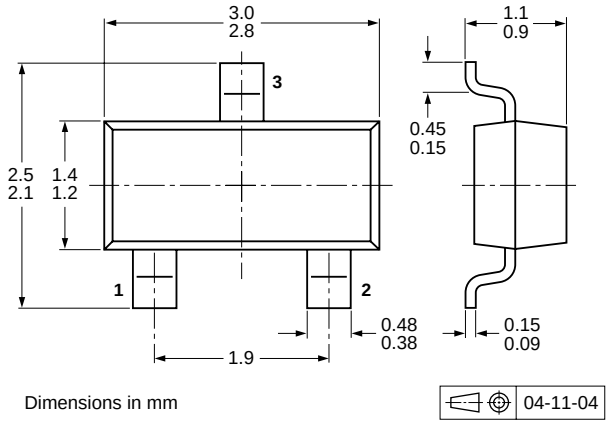


Fig 5. Package outline SOT23 (TO-236AB)

9. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PDTD113ZT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235

[1] For further information and the availability of packing methods, see Section 13.

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10. Soldering

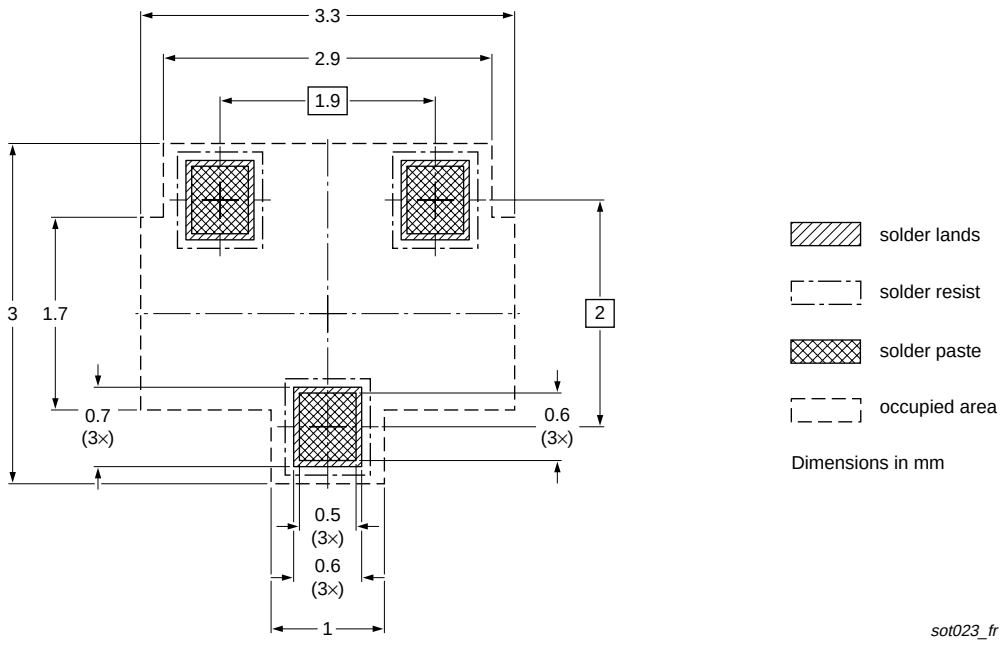


Fig 6. Reflow soldering footprint SOT23 (TO-236AB)

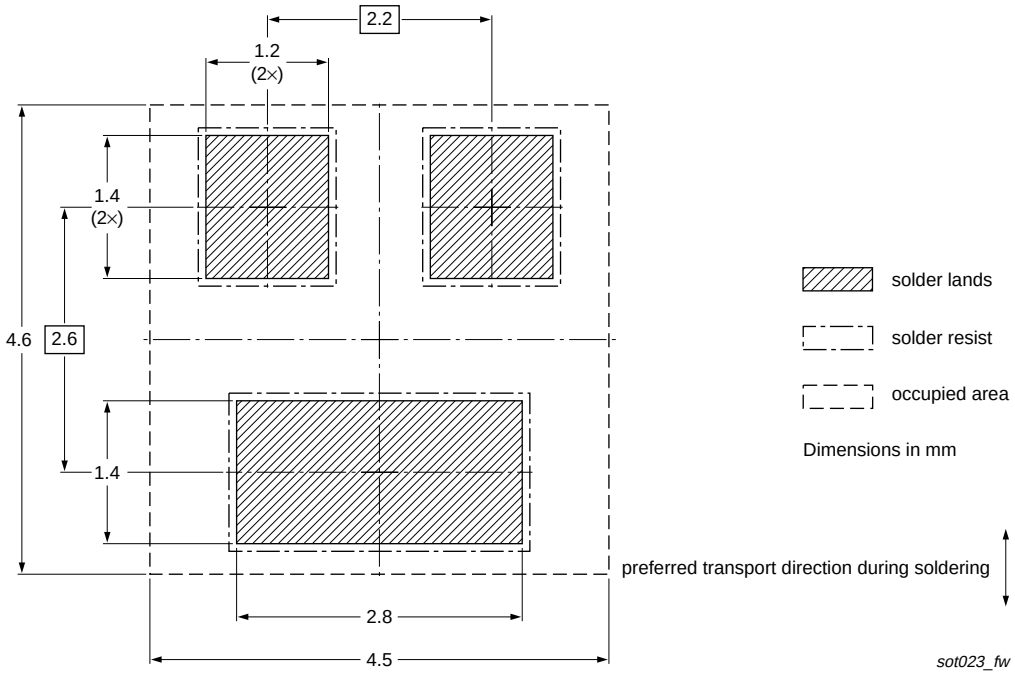


Fig 7. Wave soldering footprint SOT23 (TO-236AB)

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11. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTD113ZT_2	20090323	Product data sheet	-	PDTD113Z_SER_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers PDTD113ZK and PDTD113ZS removed • Table 5 “Limiting values”: typo for maximum value of V_I positive corrected • Section 10 “Soldering”: added • Section 12 “Legal information”: updated			
PDTD113Z_SER_1	20050405	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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