OptiMOS®3 Power-Transistor

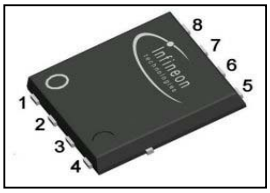
Features

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC[1] for target applications
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% Avalanche tested
- Pb-free plating; RoHS compliant

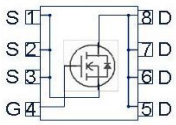
Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	9.3	mΩ
I_D	49	A

PG-TDSON-8



Type	Package	Marking
BSC093N04LS G	PG-TDSON-8	093N04LS



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	49	A
		V_{GS}=10 V, T_C=100 °C	31	
		V_{GS}=4.5 V, T_C=25 °C	40	
		V_{GS}=4.5 V, T_C=100 °C	26	
		V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[2]	13	
Pulsed drain current[3]	$I_{D,pulse}$	T_C=25 °C	196	
Avalanche current, single pulse[4]	I_{AS}	T_C=25 °C	40	
Avalanche energy, single pulse	E_{AS}	I_D=40 A, R_{GS}=25 Ω	10	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	35	W
		T_A=25 °C, R_{thJA}=50 K/W[2)]	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	3.6	K/W
Device on PCB	R_{thJA}	6 cm^2 cooling area[2)]	-	-	50	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=14 µA	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=20 A	-	11.0	13.7	mΩ
		V_{GS}=10 V, I_D=40 A	-	7.8	9.3	
Gate resistance	R_G		-	1	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=40 A	34	67	-	S

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3)] See figure 3 for more detailed information

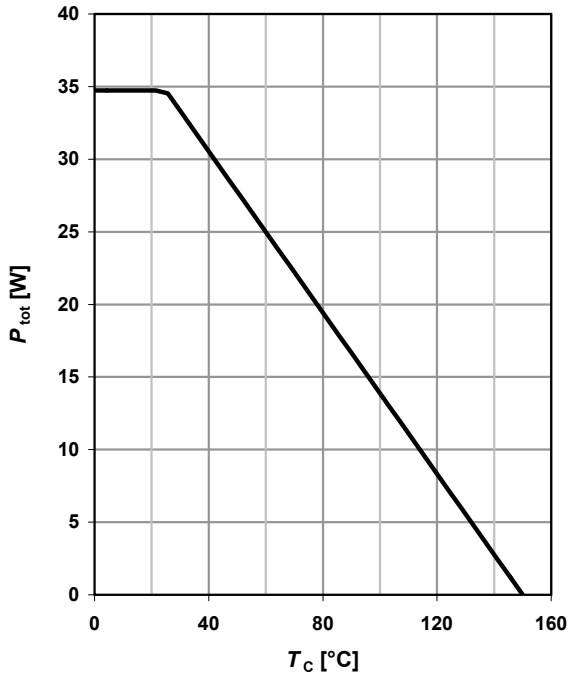
[4)] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz	-	1400	1900	pF
Output capacitance	C_{oss}		-	340	450	
Reverse transfer capacitance	C_{rss}		-	16	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω	-	3.6	-	ns
Rise time	t_r		-	2.4	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	t_f		-	2.8	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=20 V, I_D=30 A, V_{GS}=0 to 10 V	-	4.9	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	2.3	-	
Gate to drain charge	Q_{gd}		-	2.0	-	
Switching charge	Q_{sw}		-	4.6	-	
Gate charge total	Q_g		-	18	24	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V
Gate charge total	Q_g	V_{DD}=20 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	8.6	11.4	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 10 V	-	17	-	
Output charge	Q_{oss}	V_{DD}=20 V, V_{GS}=0 V	-	13	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	29	A
Diode pulse current	$I_{S,pulse}$		-	-	196	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=40 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery charge	Q_{rr}	V_R=20 V, I_F=I_S, di_F/dt=400 A/µs	-	15	-	nC

[5)] See figure 16 for gate charge parameter definition

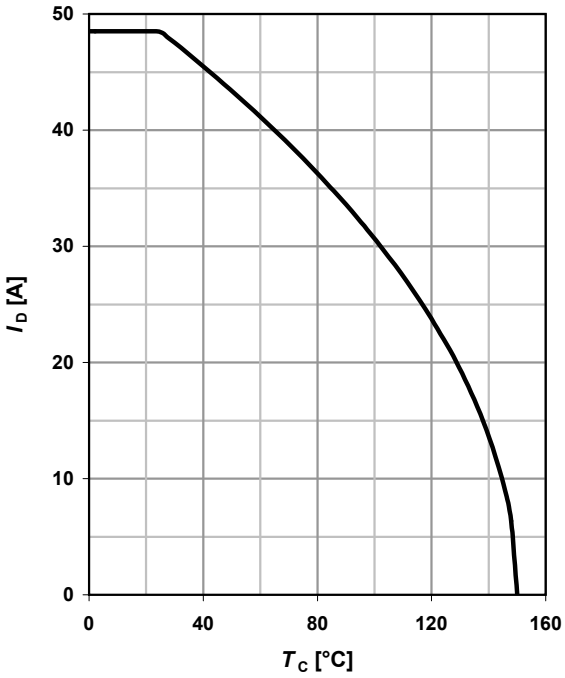
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

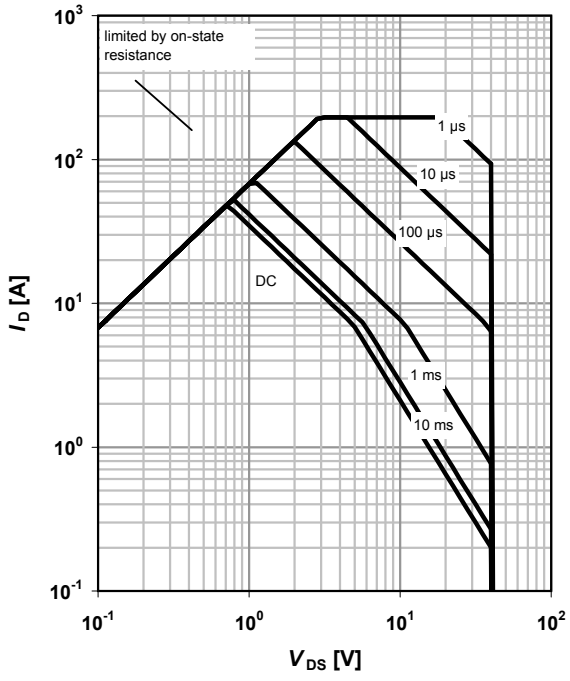
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

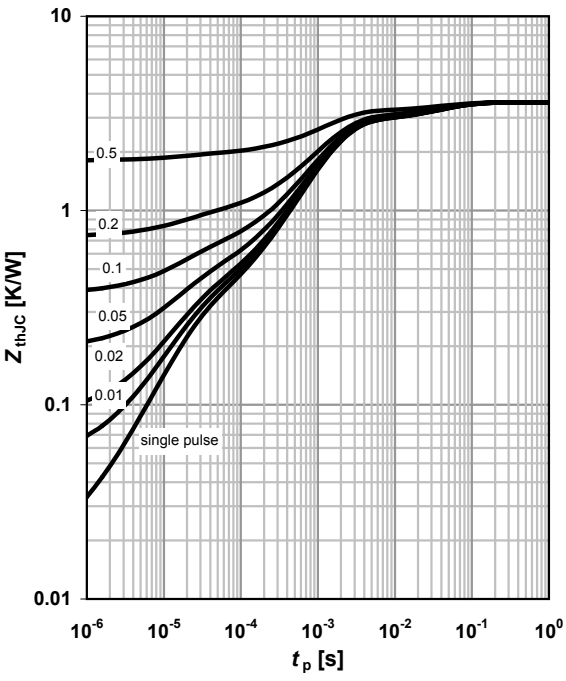
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

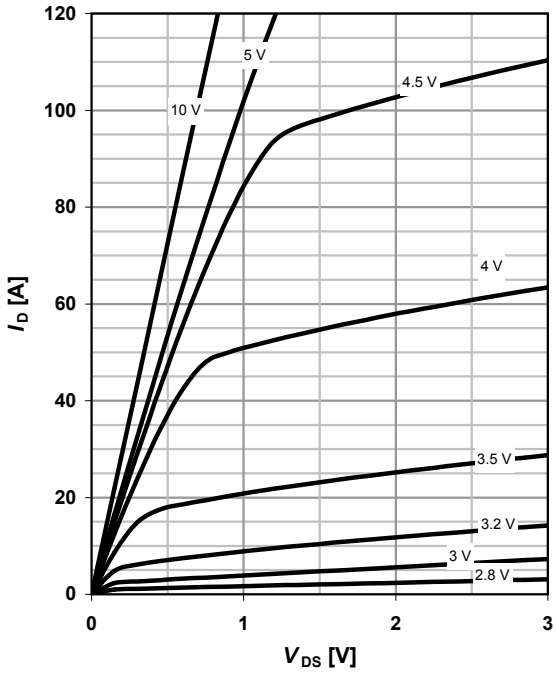
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

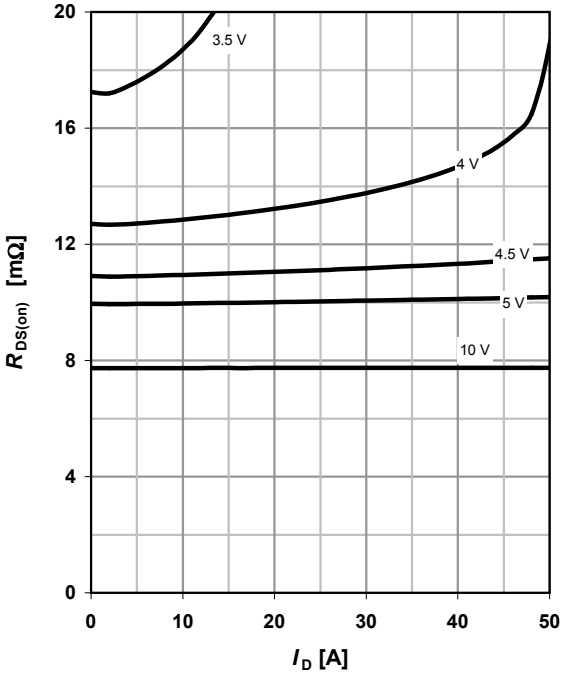
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

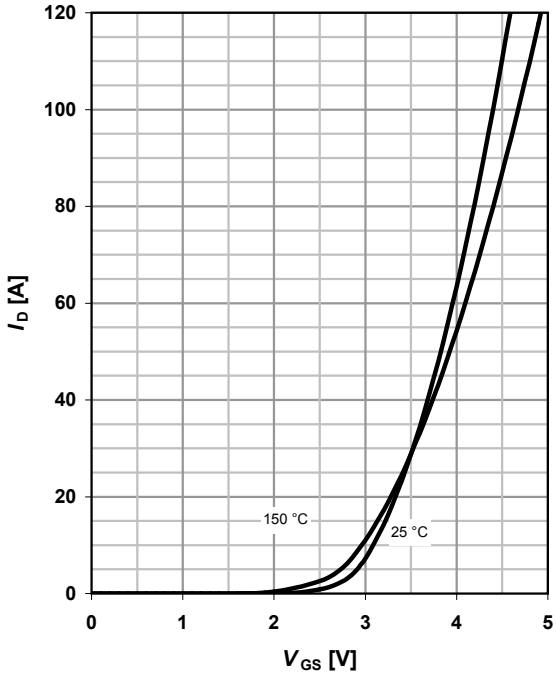
parameter: V_{GS}



7 Typ. transfer characteristics

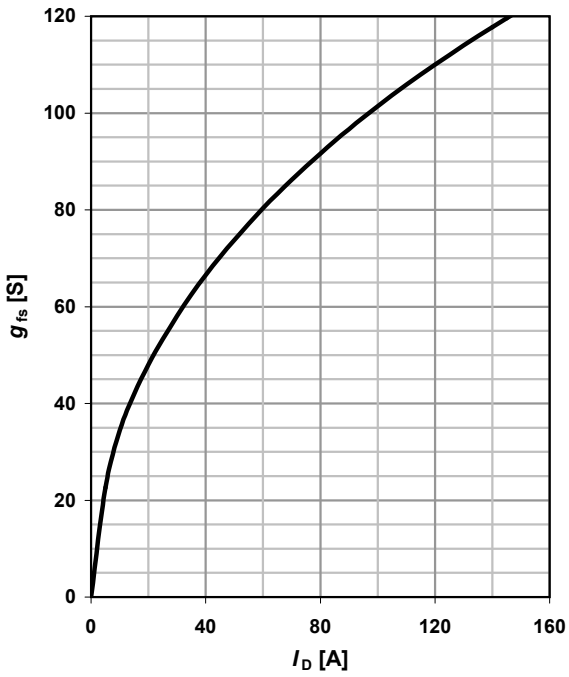
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



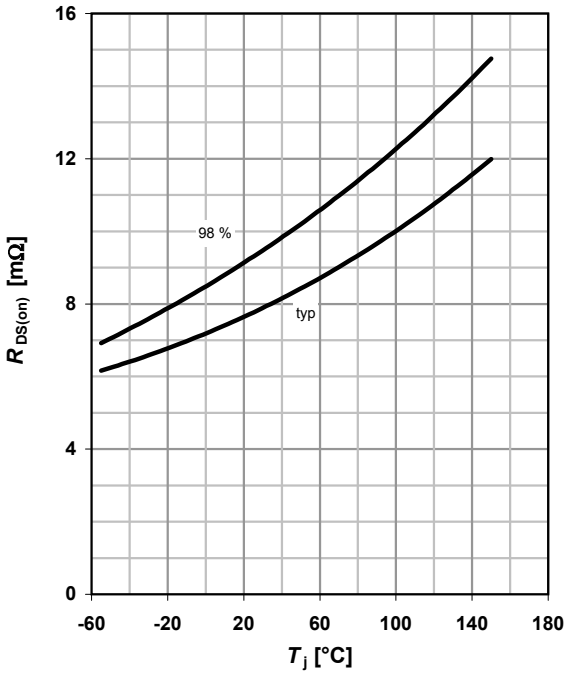
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



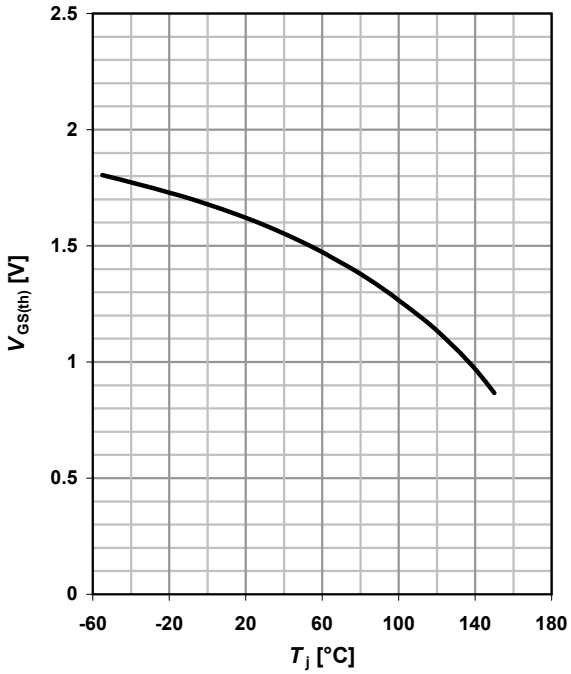
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=40 A; V_{GS}=10 V



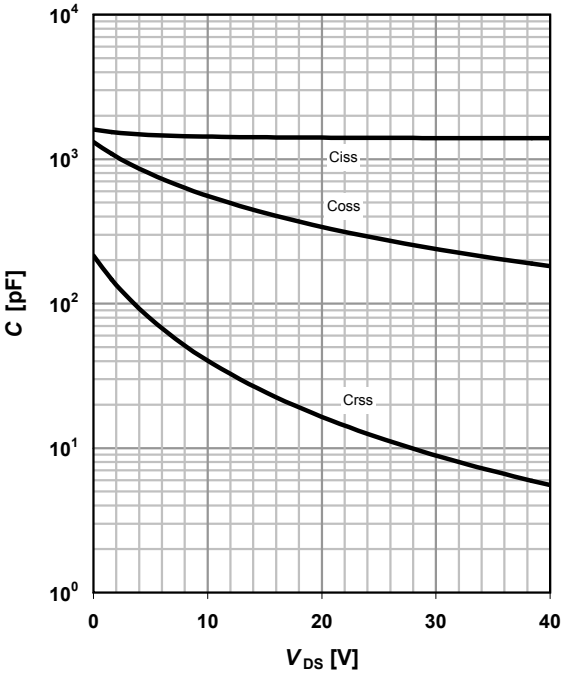
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=14 µA



11 Typ. capacitances

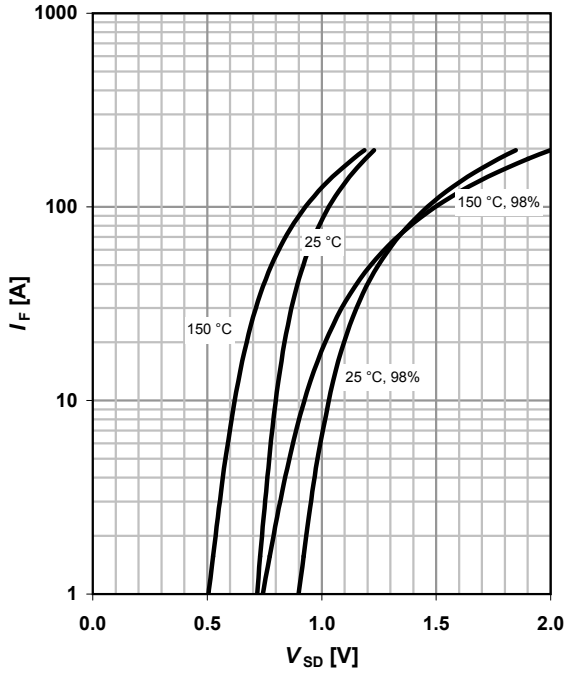
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

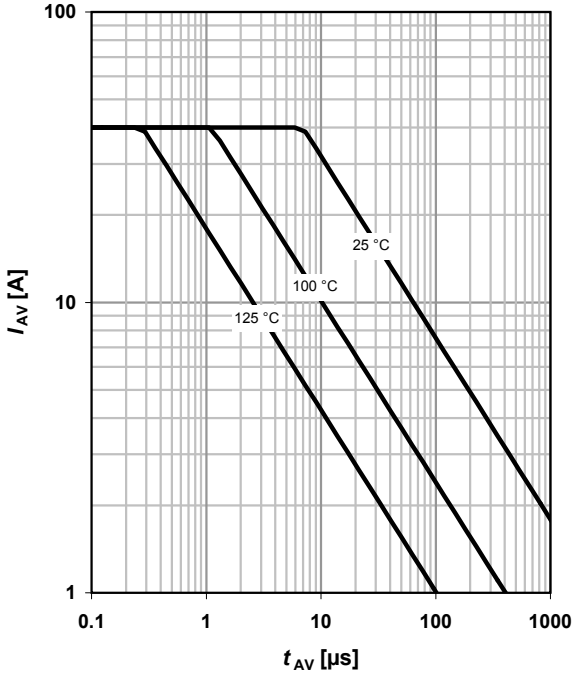
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

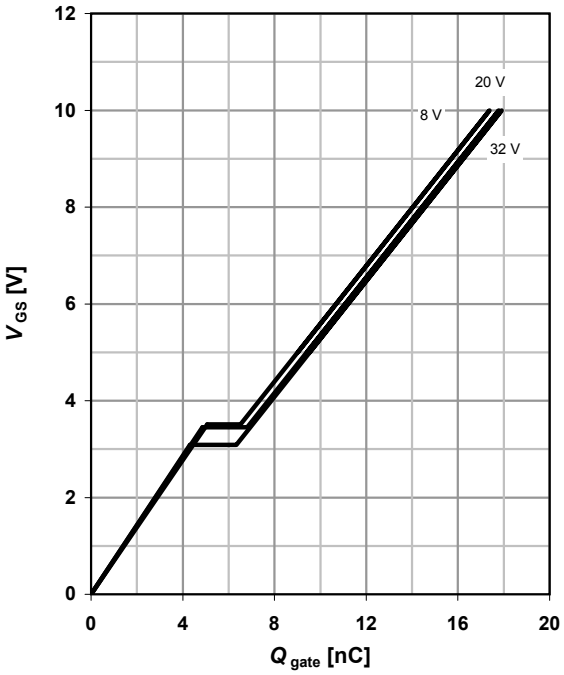
parameter: $T_{j(start)}$



14 Typ. gate charge

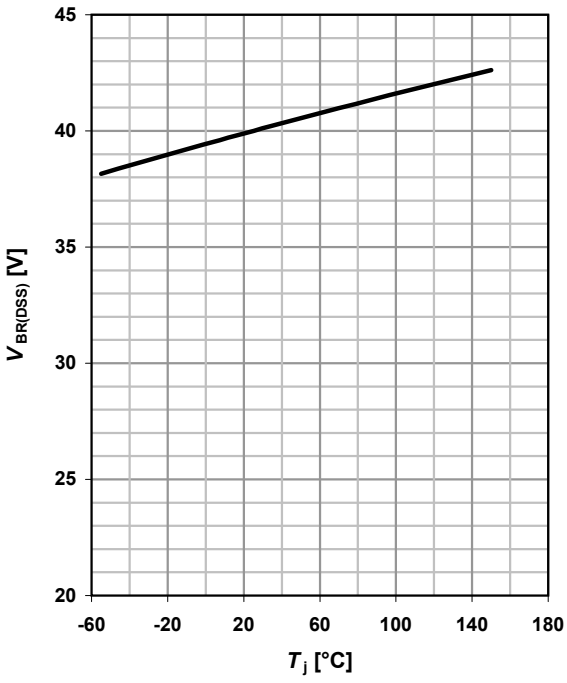
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

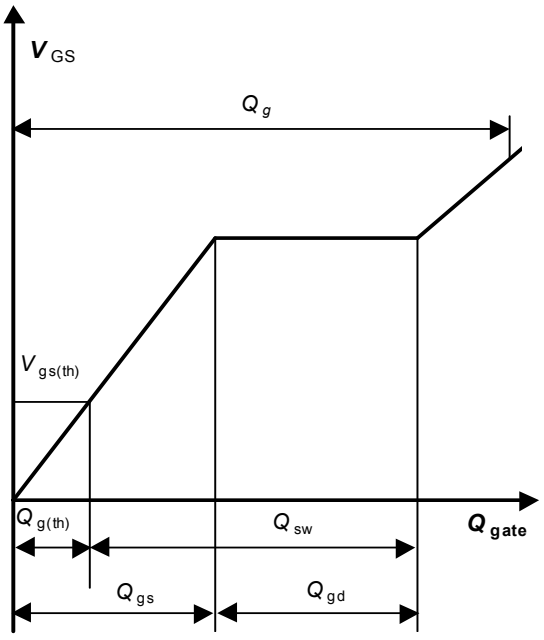


15 Drain-source breakdown voltage

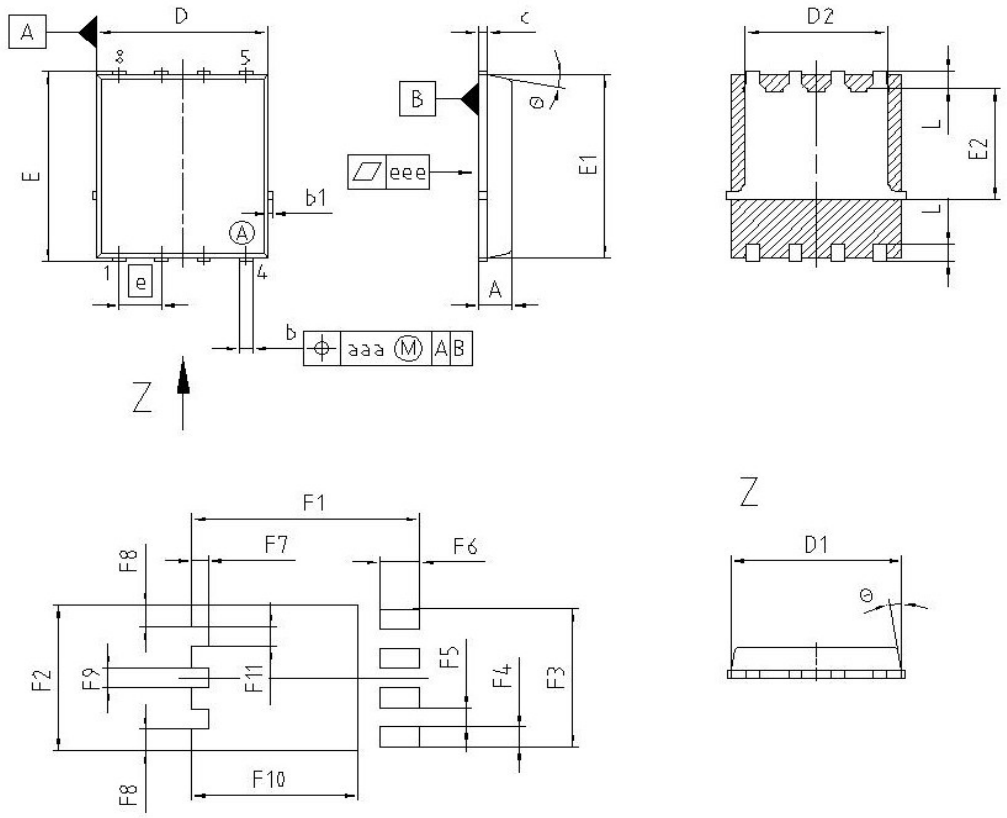
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



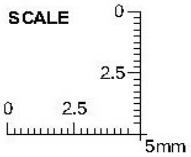
Package Outline **PG-TDSON-8**



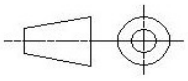
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.900	1.100	0.035	0.043
b	0.340	0.540	0.013	0.021
b1	0.000	0.120	0.000	0.005
c	0.150	0.350	0.006	0.014
D=D1	4.950	5.350	0.195	0.211
D2	4.200	4.400	0.165	0.173
E	5.950	6.350	0.234	0.250
E1	5.700	6.100	0.224	0.240
E2	3.400	3.800	0.134	0.150
e	1.270		0.050	
N	8		8	
L	0.450	0.650	0.018	0.026
Θ	9°	11°	9°	11°
aaa	0.250		0.010	
eee	0.050		0.002	
F1	6.750	6.950	0.266	0.274
F2	4.600	4.800	0.181	0.189
F3	4.360	4.560	0.172	0.180
F4	0.550	0.750	0.022	0.030
F5	0.520	0.720	0.020	0.028
F6	1.100	1.300	0.043	0.051
F7	0.400	0.600	0.016	0.024
F8	0.600	0.800	0.024	0.031
F9	0.530	0.730	0.021	0.029
F10	4.900	5.100	0.193	0.201
F11	0.535	0.735	0.021	0.029

REFERENCE
JEDEC / MO-240

SCALE



EUROPEAN PROJECTION

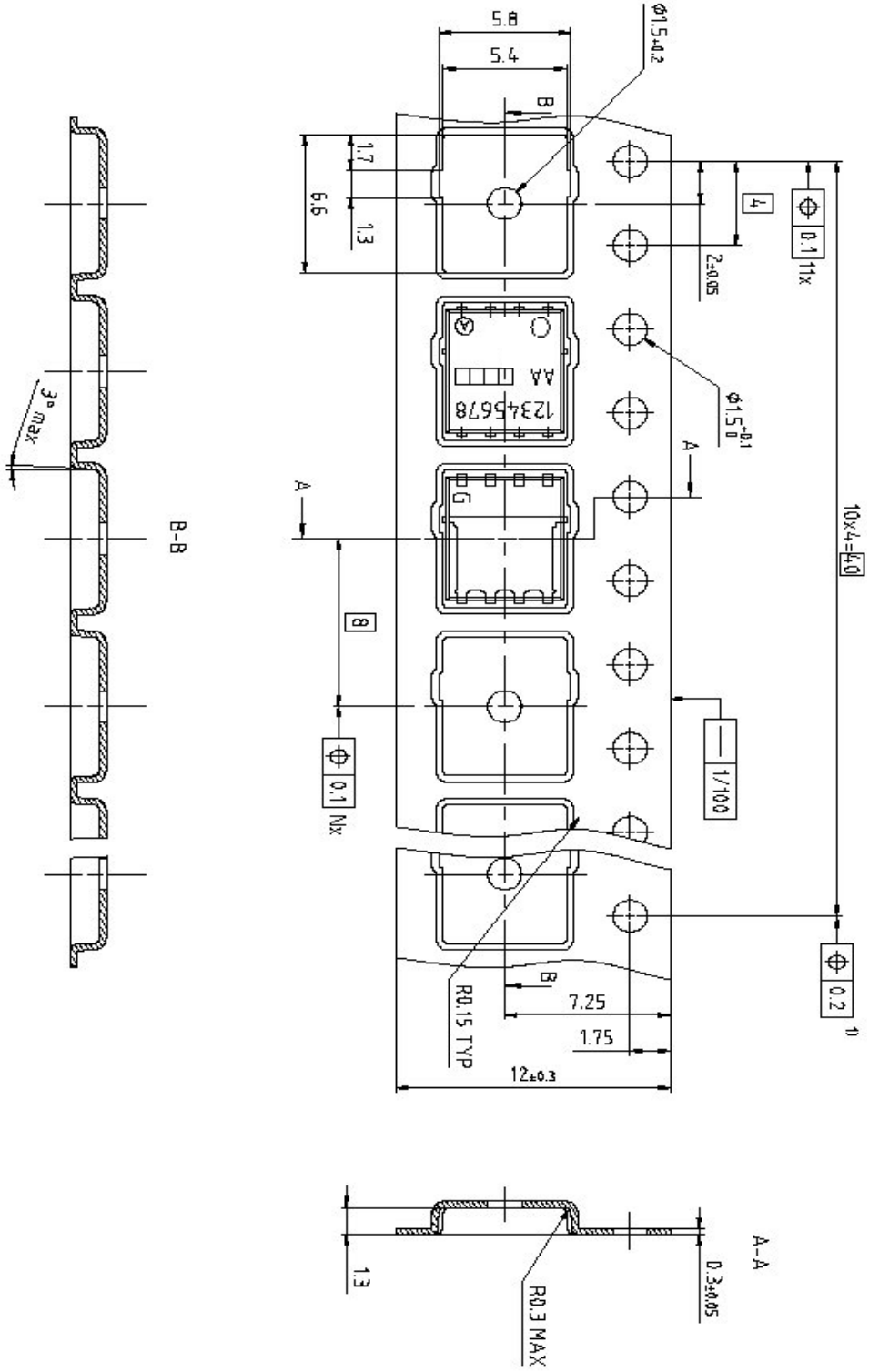


ISSUE DATE
23-08-2006

FILE
TDSON_1

Package Outline

PG-TDSON-8: Tape



Dimensions in mm

Published by
Infineon Technologies AG
81726 Munich, Germany
© 2007 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.