Multi-Phase PWM Controller with PWM-VID Reference

General Description

The RT8813A is a 3/2/1 phase synchronous Buck PWM controller which is optimized for high performance graphic microprocessor and computer applications. The IC integrates a Constant-On-Time (COT) PWM controller, two MOSFET drivers with internal bootstrap diodes, as well as channel current balance and protection functions including Over Voltage Protection (OVP), Under Voltage Protection (UVP), current limit, and thermal shutdown into the WQFN-24L 4x4 package.

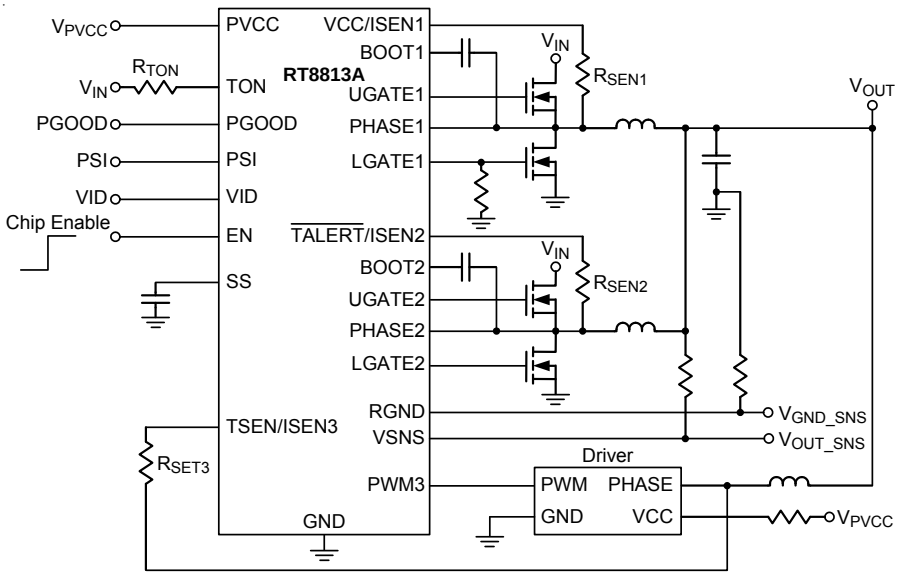
The RT8813A adopts $R_{DS(ON)}$ current sensing technique. Current limit is accomplished through continuous inductor-current-sense, while $R_{DS(ON)}$ current sensing is used for accurate channel current balance. Using the method of current sampling utilizes the best advantages of each technique.

The RT8813A features external reference input and PWM-VID dynamic output voltage control, in which the feedback voltage is regulated and tracks external input reference voltage. Other features include adjustable switching frequency, dynamic phase number control, internal/external soft-start, power good indicator, and enable functions.

Features

- **Multi-Phase PWM Controller**
- **Two Embedded MOSFET Drivers and Embedded Switching Boot Diode**
- **External Reference Input Control**
- **PWM-VID Dynamic Voltage Control**
- **Dynamic Phase Number Control**
- **Lossless $R_{DS(ON)}$ Current Sensing for Current Balance**
- **Internal Fixed and External Adjustable Soft-Start**
- **Adjustable Current Limit Threshold**
- **Adjustable Switching Frequency**
- **UVP/OVP Protection**
- **Shoot Through Protection and Short Pulse Free Technology**
- **Support an Ultra-Low Output Voltage as Standby Voltage**
- **Thermal Alert Indicator in 2/1 Active Phase Application**
- **Thermal Shutdown**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit

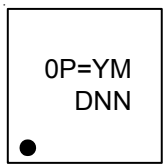


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Applications

- CPU/GPU Core Power Supply
- Notebook PC Memory Power Supply
- Chipset/RAM Power Supply
- Generic DC/DC Power Regulator

Marking Information



0P= : Product Code

YMDNN : Date Code

Ordering Information

RT8813A□□

Package Type
QW : WQFN-24L 4x4 (W-Type)
(Exposed Pad-Option 1)

Lead Plating System
G : Green (Halogen Free and Pb Free)

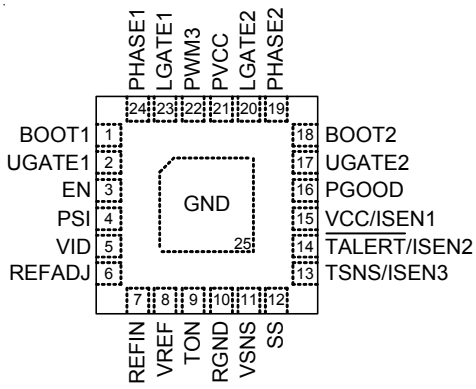
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



WQFN-24L 4x4

Function Pin Description

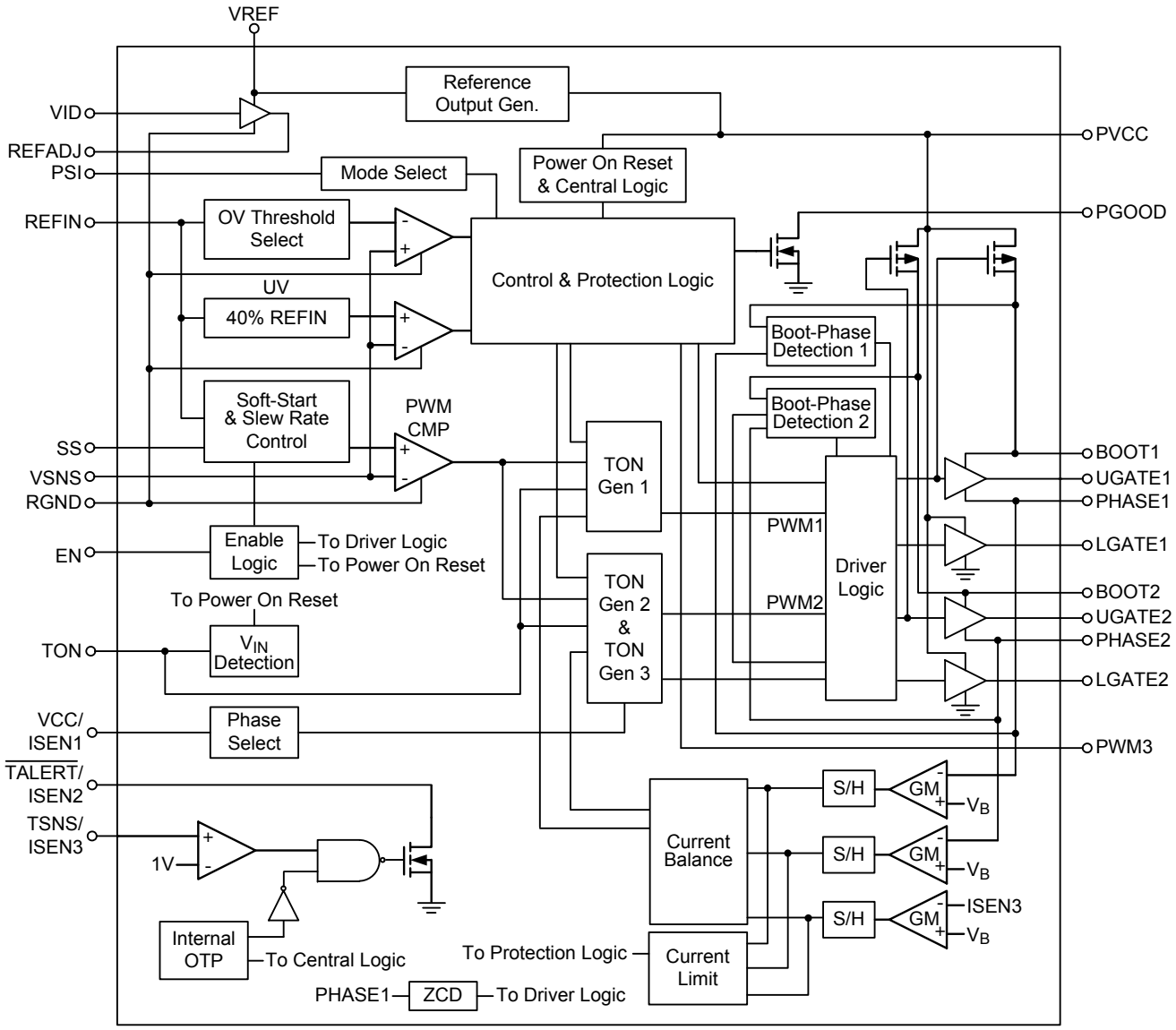
Pin No.	Pin Name	Pin Function
1	BOOT1	Bootstrap Supply for PWM 1. This pin powers the high side MOSFET driver.
2	UGATE1	High Side Gate Driver of PWM 1. This pin provides the gate drive for the converter's high side MOSFET. Connect this pin to the Gate of high side MOSFET.
3	EN	Enable Control Input. Active high input.
4	PSI	Power Saving Interface. When the voltage is pulled below 0.8V, the device will operate into 1 phase DEM. When the voltage is between 1.2V to 1.8V, the device will operate into 1 phase force CCM. When the voltage is between 2.4V to 5.5V, the device will operate into active phase force CCM (only for 2 or 3 phase).
5	VID	Programming Output Voltage Control Input. Refer to PWM-VID Dynamic Voltage Control.
6	REFADJ	Reference Adjustment Output. Refer to PWM-VID Dynamic Voltage Control.
7	REFIN	External Reference Input.
8	VREF	Reference Voltage Output. This is a high precision voltage reference (2V) from VREF pin to RGND pin.
9	TON	On-Time/Switching Frequency Adjustment Input. Connect a 100pF capacitor between C_{TON} and ground is optional for noise immunity enhancement.
10	RGND	Negative Remote Sense Input. Connect this pin to the ground of output load.
11	VSNS	Positive Remote Sense Input. Connect this pin to the positive terminal of output load.
12	SS	Soft-Start Time Setting. Connect an external capacitor to adjust soft-start time. When the external capacitor is removed, the internal soft-start function will be chose.
13	TSNS	Temperature Sensing Input for 2/1 Phase Operation.
	ISEN3	Phase 3 Current Sense Input for 3 Phase Operation.

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Pin No.	Pin Name	Pin Function
14	$\overline{\text{TALERT}}$	Thermal Alert. Active low open drain output for 2/1 Phase Operation.
	ISEN2	Phase 2 Current Sense Input for 3 Phase Operation.
15	VCC	Supply Voltage Input for 2/1 Phase Operation. (Connect to PVCC)
	ISEN1	Phase 1 Current Sense Input for 3 Phase Operation. (Connect to PHASE1)
16	PGOOD	Power Good Indicator Output. Active high open drain output.
17	UGATE2	High Side Gate Driver of PWM 2. This pin provides the gate drive for the converter's high side MOSFET. Connect this pin to the Gate of high side MOSFET.
18	BOOT2	Bootstrap Supply for of PWM 2. This pin powers the high side MOSFET driver.
19	PHASE2	Switch Node for PWM2. This pin is return node of the high side driver of PWM 2. Connect this pin to the Source of high side MOSFET together with the Drain of low side MOSFET and the inductor.
20	LGATE2	Low Side Gate Driver of PWM 2. This pin provides the gate drive for the converter's low side MOSFET. Connect this pin to the Gate of low side MOSFET.
21	PVCC	Supply Voltage Input. Connect this pin to a 5V bias supply. Place a high quality bypass capacitor from this pin to GND.
22	PWM3	Third Phase PWM Control Signal Output to Driver for 3 Phase Operation. In 2/1 Phase Operation, this pin is high impedance.
23	LGATE1	Low Side Gate Driver of PWM 1. This pin provides the gate drive for the converter's low side MOSFET. Connect this pin to the Gate of low side MOSFET.
24	PHASE1	Switch Node for PWM1. This pin is return node of the high side driver of PWM 1. Connect this pin to the Source of high side MOSFET together with the Drain of low side MOSFET and the inductor.
25 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.

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Function Block Diagram



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Operation

The RT8813A is a 3/2/1 phase synchronous Buck PWM controller with integrated drivers which are optimized for high performance graphic microprocessor and computer applications. The IC integrates a COT (Constant-On-Time) PWM controller with two MOSFET drivers, as well as output current monitoring and protection functions. Referring to the function block diagram of TON Genx, the synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one-shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range and output voltage. Another one-shot sets a minimum off-time.

The RT8813A also features a PWM-VID dynamic voltage control circuit driven by the pulse width modulation method. This circuit reduces the device pin count and enables a wide dynamic voltage range.

Soft-Start (SS)

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval. For external soft-start function, an additional capacitor connected from SS to the GND will be charged by a current source and determines the soft-start time.

PGOOD

The power good output is an open drain architecture.

When the soft-start is finished, the PGOOD open drain output will be high impedance.

Current Balance

The RT8813A implements internal current balance mechanism in the current loop. The RT8813A senses per phase current and compares it with the average current. If the sensed current of any particular phase is higher than average current, the on-time of this phase will be adjusted to be shorter.

Current Limit

The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the under voltage protection threshold, inducing IC shutdown.

Over Voltage Protection (OVP) & Under Voltage Protection (UVP)

The output voltage is continuously monitored for over voltage and under voltage protection. When the output voltage exceeds its set voltage threshold (If $V_{REFIN} \leq 1.33V$, OV = 2V, or $V_{REFIN} > 1.33V$, OV = 1.5 x V_{REFIN}), UGATE goes low and LGATE is forced high; when it is less than 40% of its set voltage, under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until PVCC is re-supplied and exceeds the POR rising threshold voltage or EN is reset.

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Absolute Maximum Ratings (Note 1)

- TON to GND ---------- –0.3V to 30V
- RGND to GND ---------- –0.7V to 0.7V
- BOOTx to PHASEx ---------- –0.3V to 6V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - <20ns ---------- –8V to 36V
- UGATEx to PHASEx
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –2.5V to 7.5V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-24L 4x4 ---------- 3.57W
- Package Thermal Resistance (Note 2)
  - WQFN-24L 4x4, θ_{JA} ---------- 28°C/W
  - WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 7V to 26V
- Supply Voltage, V_{PVCC} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
PVCC Supply Voltage	V_{PVCC}		4.5	--	5.5	V
PVCC Supply Current	I_{SUPPLY}	EN = 3.3V, Not Switching	--	1.5	2	mA
PVCC Shutdown Current	I_{SHDN}	EN = 0V	--	--	10	μA
PVCC POR Threshold			3.8	4.1	4.4	V
POR Hysteresis			--	0.3	--	V

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency		f_{SW}	R_{TON} = 500kΩ (Note 5)	270	300	330	kHz
Minimum On-Time		$t_{ON(MIN)}$		--	70	--	ns
Minimum Off-Time		$t_{OFF(MIN)}$		--	300	--	ns
EN Threshold							
EN Input Voltage	Logic-High	V_{ENH}		1.6	--	--	V
	Logic-Low	V_{ENL}		--	--	0.8	V
Mode Decision							
PSI High Threshold		V_{PSIH}	Enables Two Phases with FCCM	2.4	--	--	V
PSI Intermediate Threshold		V_{PSIM}	Enables One Phases with FCCM	1.2	--	1.8	V
PSI Low Threshold		V_{PSIL}	Enables One Phases with DEM	--	--	0.8	V
VID Input Voltage	Logic-High	V_{VIDH}		2	--	--	V
	Logic-Low	V_{VIDL}		--	--	1	V
Protection Function							
Zero Current Crossing Threshold				–8	--	8	mV
Current Limit Setting Current		I_{OCSET}		9	10	11	μA
Current Limit Setting Current Temperature Coefficient		I_{OCSET_TC}		--	6300	--	ppm/°C
Current Limit Threshold			R_{OCSET} = 10k	--	60	--	mV
Absolute Over Voltage Protection Threshold		$V_{OVP, Absolute}$	$V_{REFIN} \leq$ 1.33V	1.9	2	2.1	V
Relative Over Voltage Protection Threshold		$V_{OVP, Relative}$	V_{REFIN} > 1.33V	145	150	155	%
OV Fault Delay			FB forced above OV threshold	--	5	--	μs
Relative Under Voltage Protection Threshold		V_{UVP}	UVP	35	40	45	%
UV Fault Delay			FB forced above UV threshold	--	3	--	μs
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Minimum TM Threshold		V_{TSEN}	(No Shutting Down)	0.98	1	1.02	V
PGOOD Blanking Time (Internal)			From EN = high to PGOOD = high with VSNS within regulation point	--	2.5	--	ms
VSNS Soft-Start (Internal)			From first UGATE to VSNS regulation point, V_{REFIN} = 1V and VSNS initial = 0V	--	0.7	--	ms
Soft-Start Current Source		I_{SS}		--	5	--	μA
Error Amplifier							
VSNS Error Comparator Threshold (Valley)			V_{REFIN} = 1V	–17.5	–12.5	–7.5	mV

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference						
Reference Voltage	V_{VREF}	Sourcing Current = 1mA, VID no Switching	1.98	2	2.02	V
Driver On-Resistance						
UGATE Driver Source	$R_{UGATEsr}$	BOOTx – PHASEx Forced to 5V	--	2	4	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOTx – PHASEx Forced to 5V	--	1	2	Ω
LGATE Driver Source	$R_{LGATEsr}$	LGATEx, High State	--	1.5	3	Ω
LGATE Driver Sink	$R_{LGATEsk}$	LGATEx, Low State	--	0.7	1.5	Ω
Dead-Time		From LGATE Falling to UGATE Rising	--	30	--	ns
		From UGATE Falling to LGATE Rising	--	20	--	
Internal Boost Charging Switch On-Resistance	R_{BOOT}	PVCC to BOOTx, I_{BOOT} = 10mA	--	40	80	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Not production tested. Test condition is V_{IN} = 8V, V_{OUT} = 1V, I_{OUT} = 20A using application circuit.

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Typical Application Circuit

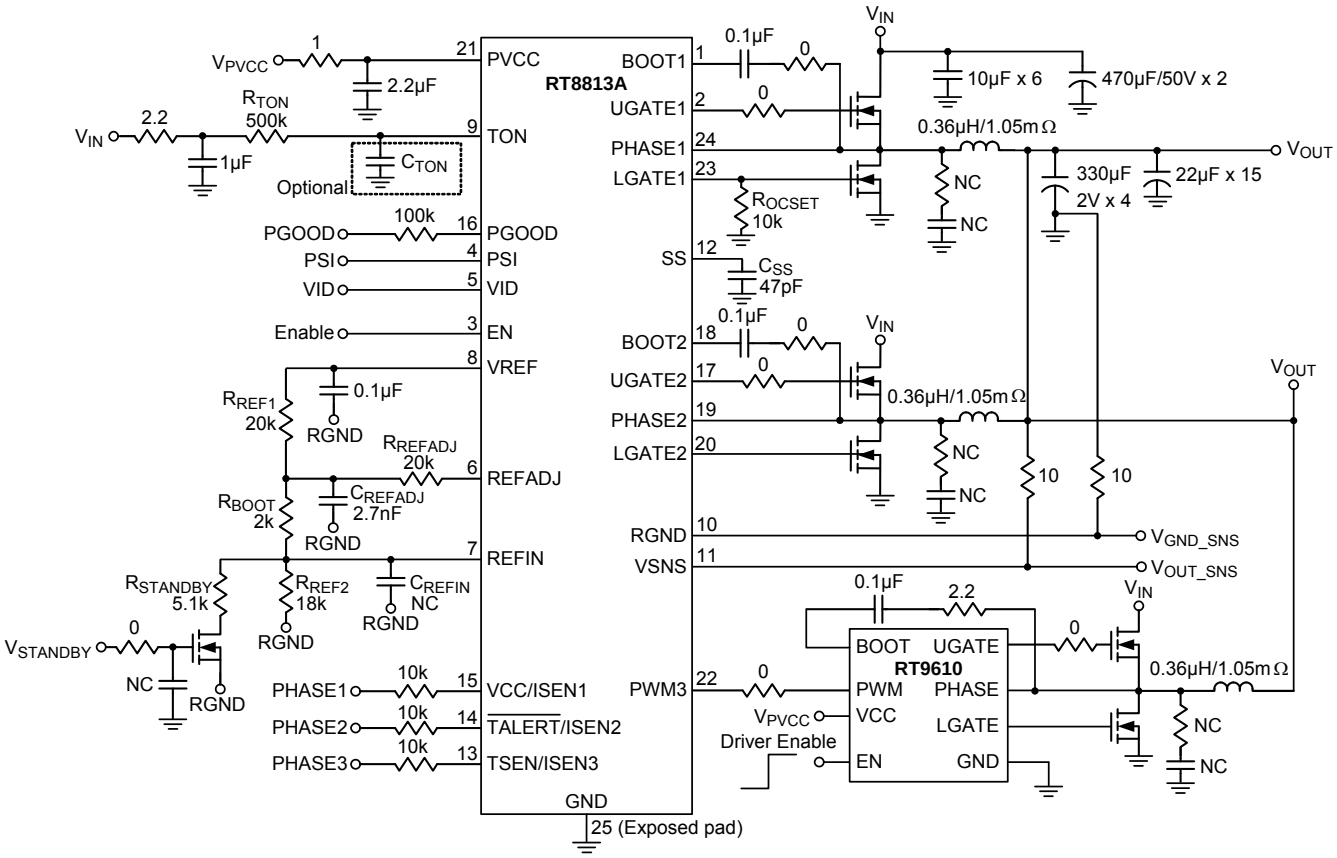


Figure 1. 3 Active Phase Configuration

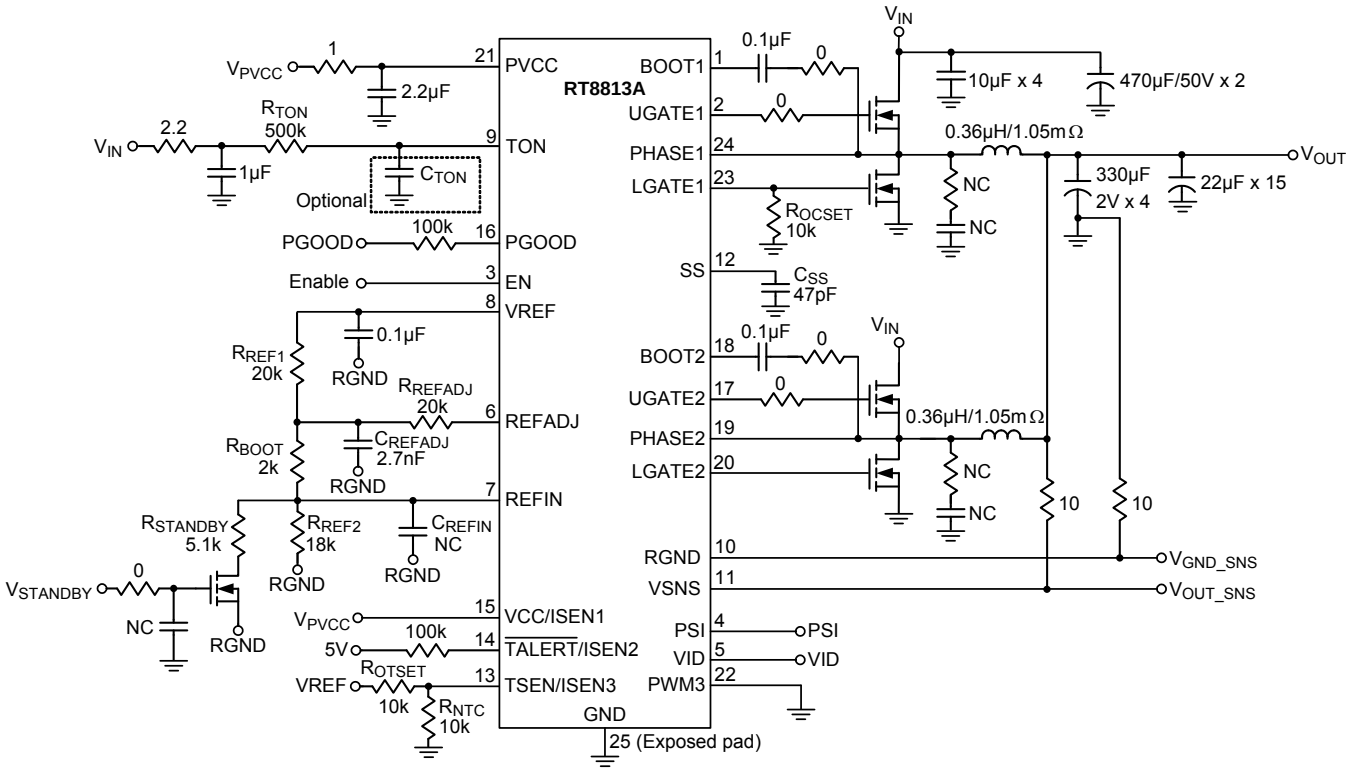


Figure 2. 2 Active Phase Configuration

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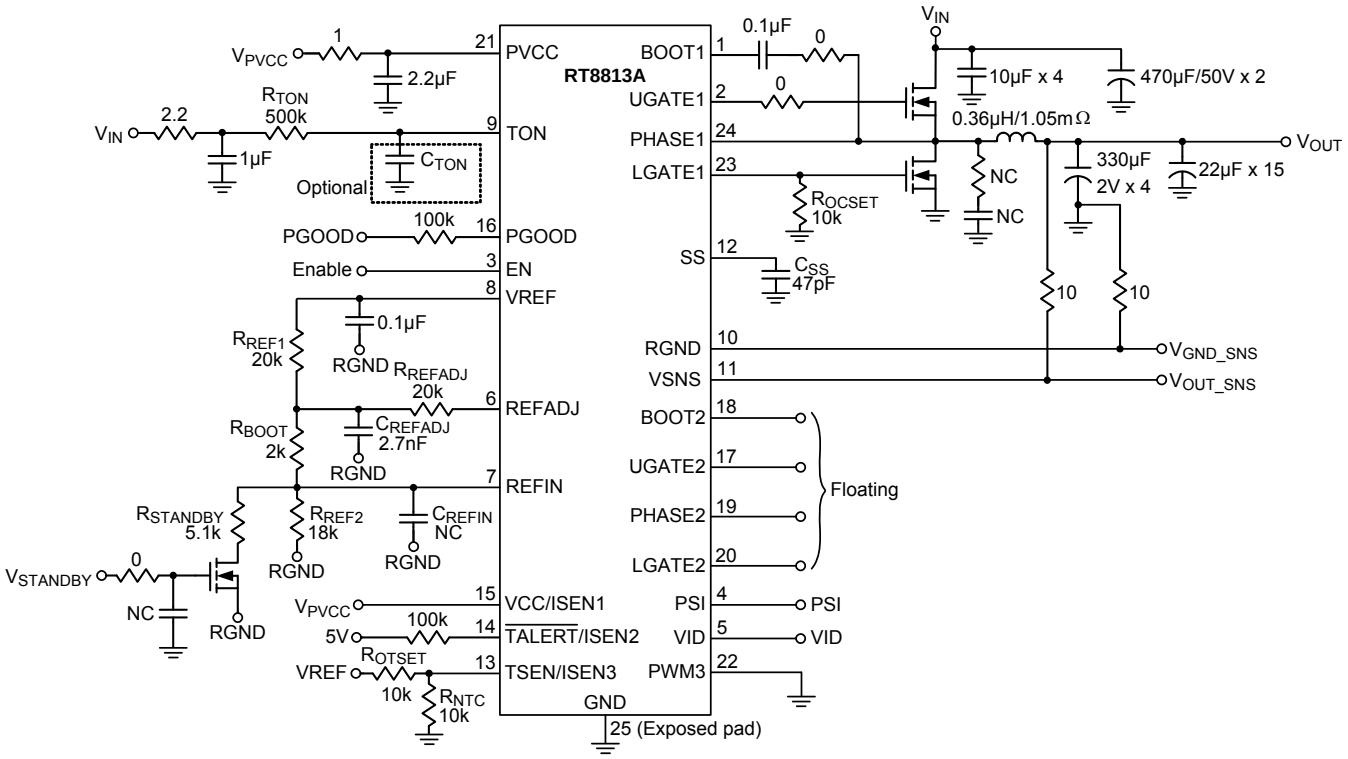
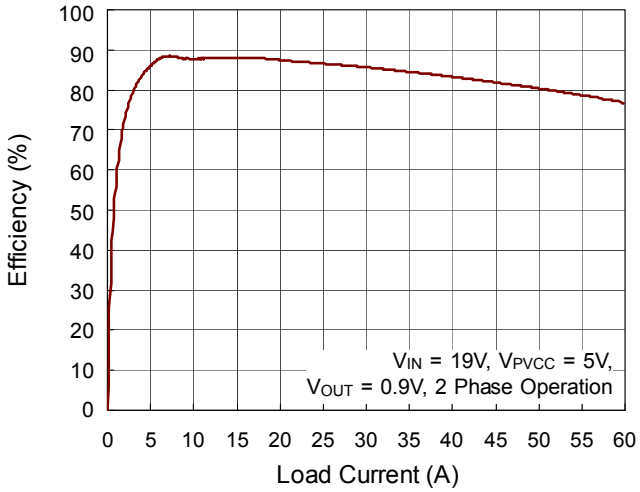


Figure 3. 1 Active Phase Configuration

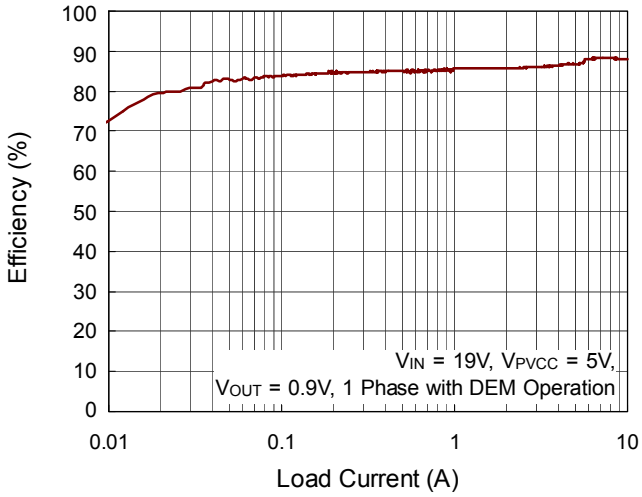
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Typical Operating Characteristics

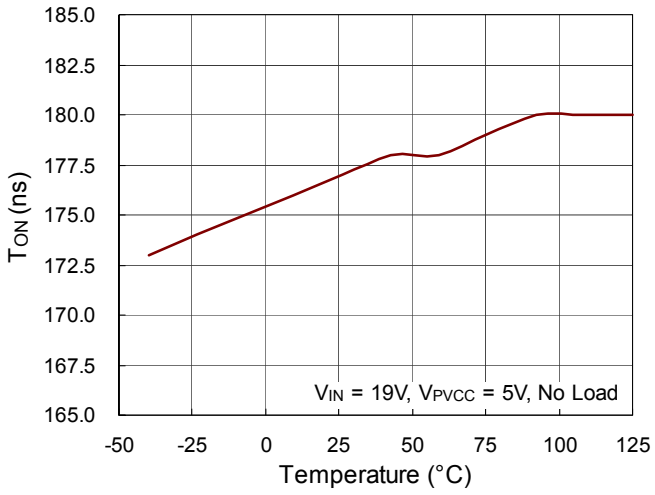
Efficiency vs. Load Current



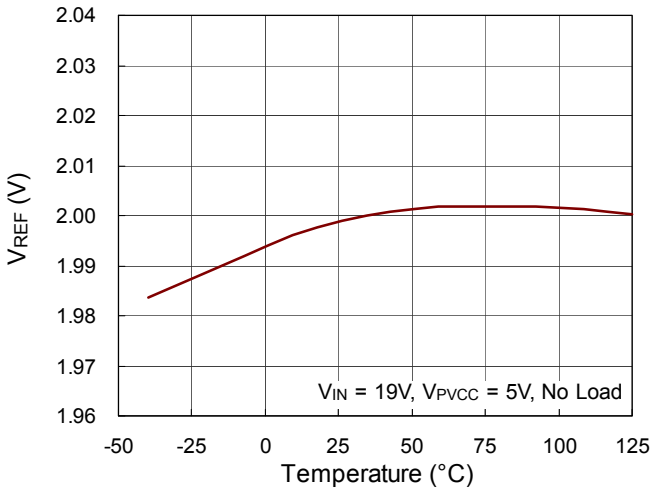
Efficiency vs. Load Current



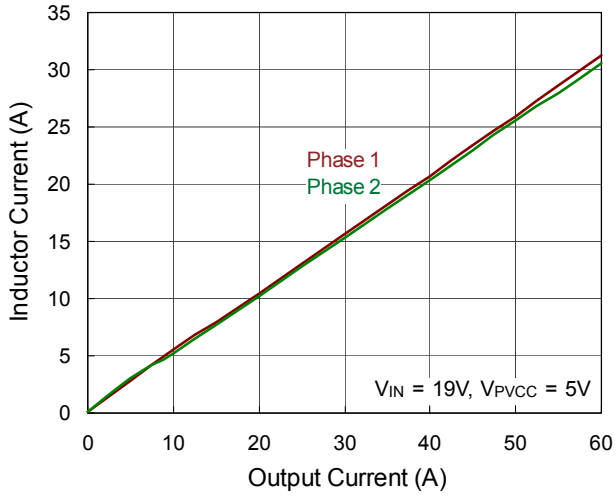
T_{ON} vs. Temperature



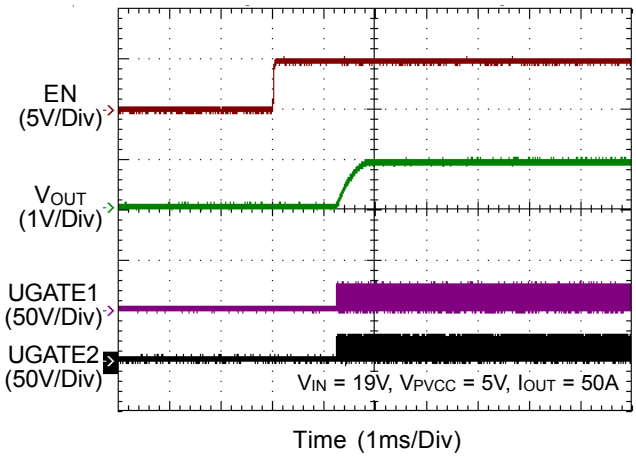
V_{REF} vs. Temperature



Inductor Current vs. Output Current

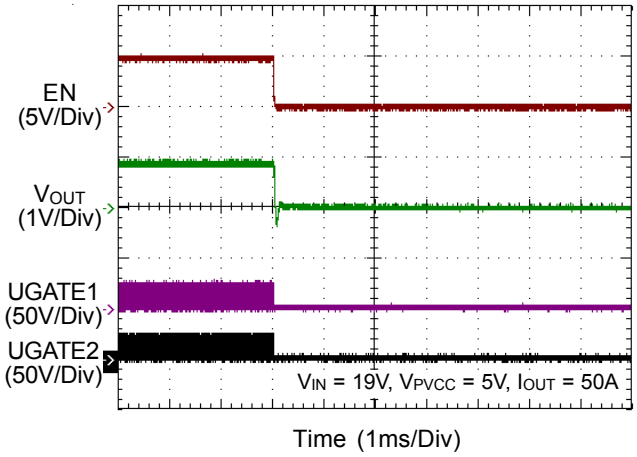


Power On from EN

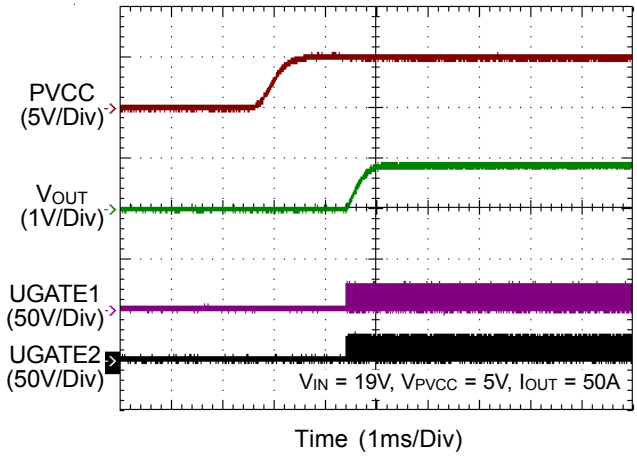


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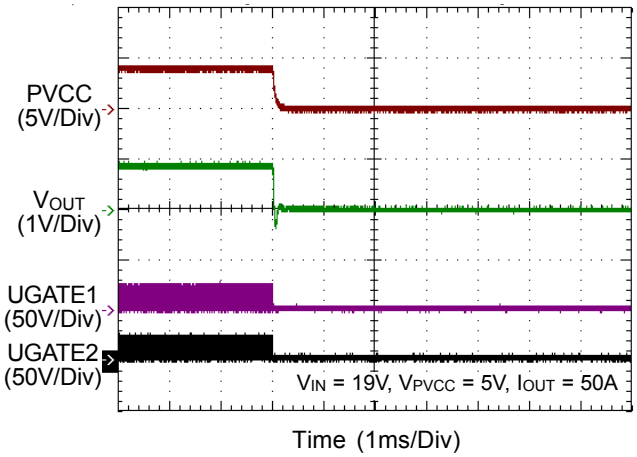
Power Off from EN



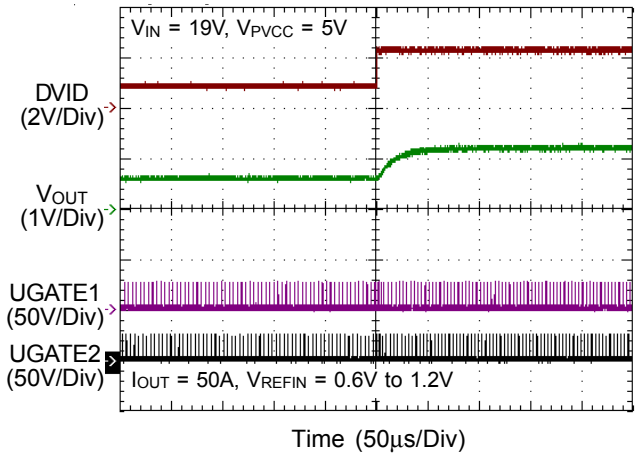
Power On from VCC



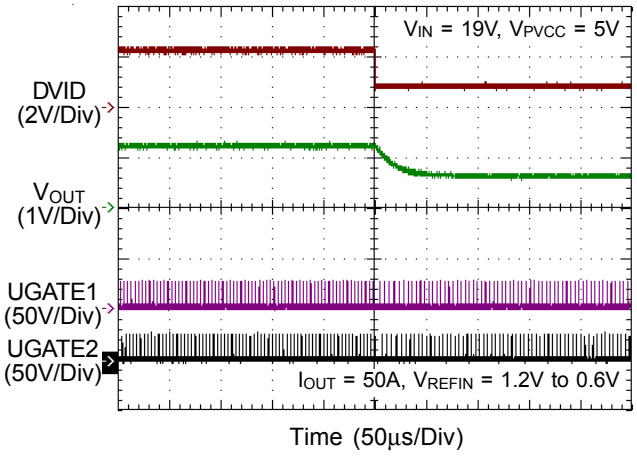
Power Off from VCC



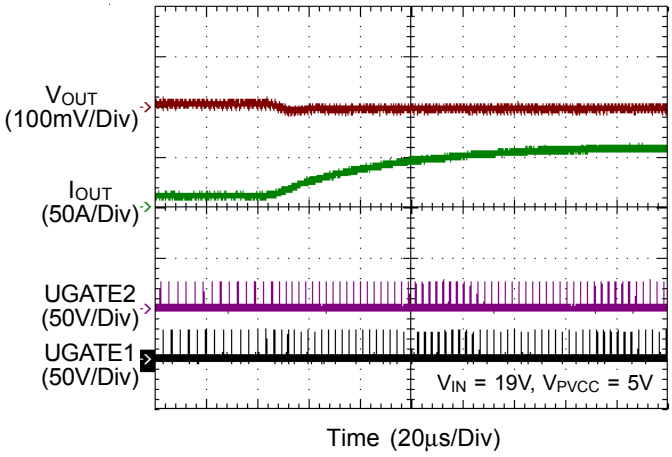
Dynamic Output Voltage Control



Dynamic Output Voltage Control

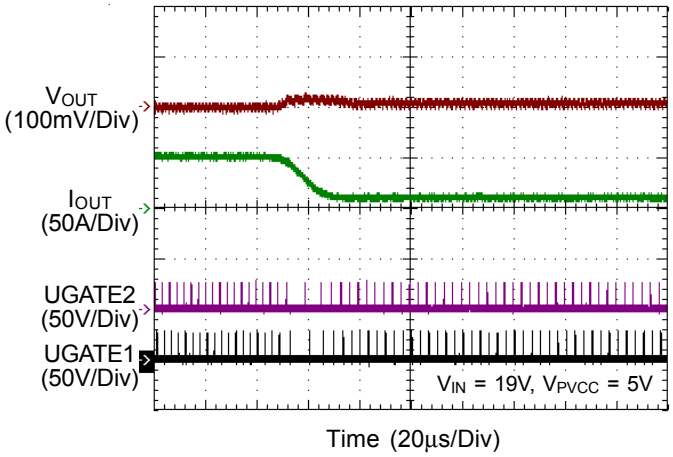


Load Transient Response

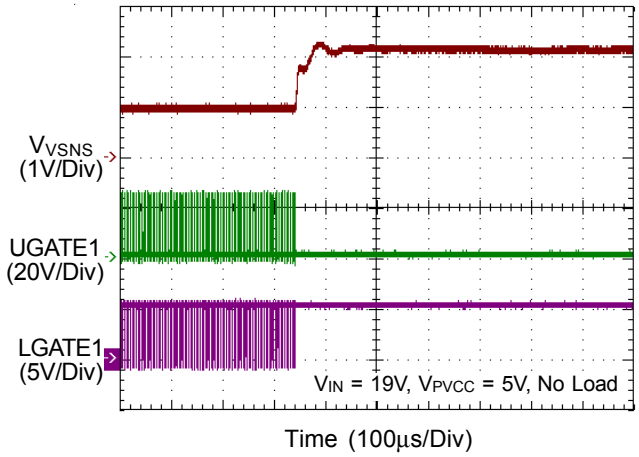


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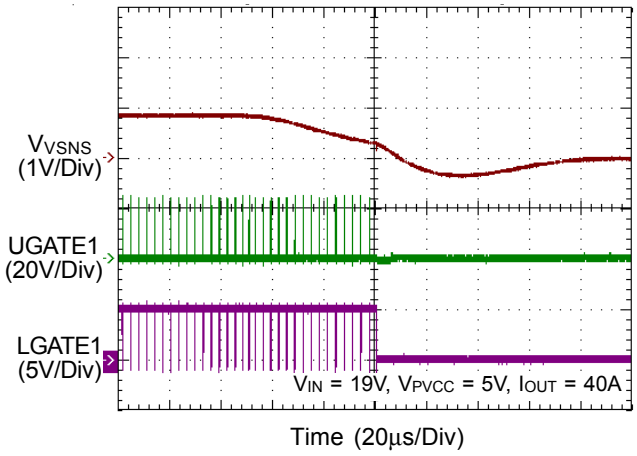
Load Transient Response



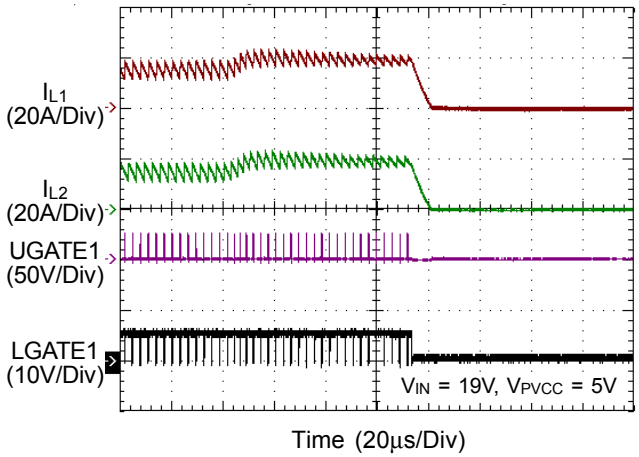
OVP



UVP



OCP



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Application Information

The RT8813A is a multi-phase synchronous Buck PWM controller with integrated drivers which is optimized for high-performance graphic microprocessor and computer applications. A COT (Constant-On-Time) PWM controller and two MOSFET drivers with internal bootstrap diodes are integrated so that the external circuit can be easily designed and the number of component is reduced.

The topology solves the poor load transient response timing problems of fixed-frequency mode PWM and avoids the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes.

The IC supports dynamic mode transition function with various operating states, which include multi-phase with CCM operation and single phase with diode emulation mode. These different operating states make the system efficiency as high as possible.

The RT8813A provides a PWM-VID dynamic control operation in which the feedback voltage is regulated and tracks external input reference voltage. It also features complete fault protection functions including over voltage, under voltage and current limit.

Remote Sense

The RT8813A uses the remote sense path (VSNS and RGND) to overcome voltage drops in the power lines by sensing the voltage directly at the end of GPU. Normally, to protect remote sense path disconnecting, there are two resistors (R_{Local}) connecting between local sense path and remote sense path. That is, in application with remote sense, the R_{Local} is recommended to be 10Ω to 100Ω. If no need of remote sense, the R_{Local} is recommended to be 0Ω.

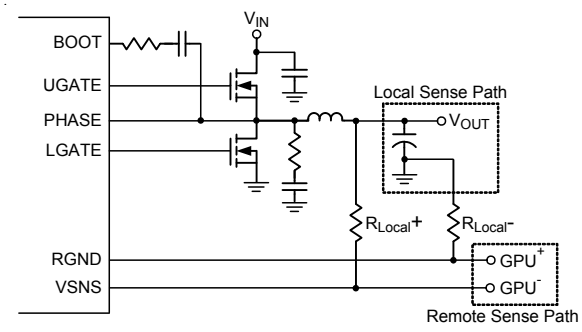


Figure 4. Output Voltage Sensing

PWM Operation

The RT8813A integrates a Constant-On-Time (COT) PWM controller, and the controller provides the PWM signal which relies on the output ripple voltage comparing with internal reference voltage as shown in Figure 5. Referring to the function block diagram of TON Genx, the synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one-shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage and output voltage range. Another one-shot sets a minimum off-time.

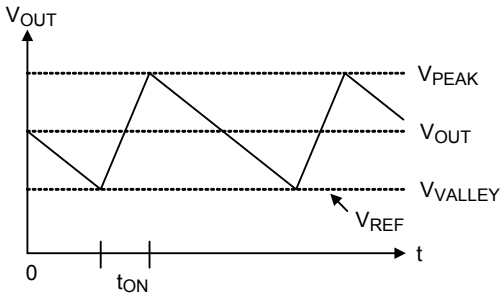


Figure 5. Constant On-Time PWM Control

On-Time Control

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need for a clock generator.

$$T_{ON} = \frac{2 \times V_{OUT} \times 3.2p}{V_{IN} - 0.5} \times R_{TON}$$

And then the switching frequency F_S is :

$$F_S = V_{OUT} / (V_{IN} \times T_{ON})$$

R_{TON} is a resistor connected from the V_{IN} to TON pin. The value of R_{TON} can be selected according to Figure 6.

The recommend operation frequency range is 150kHz to 600kHz.

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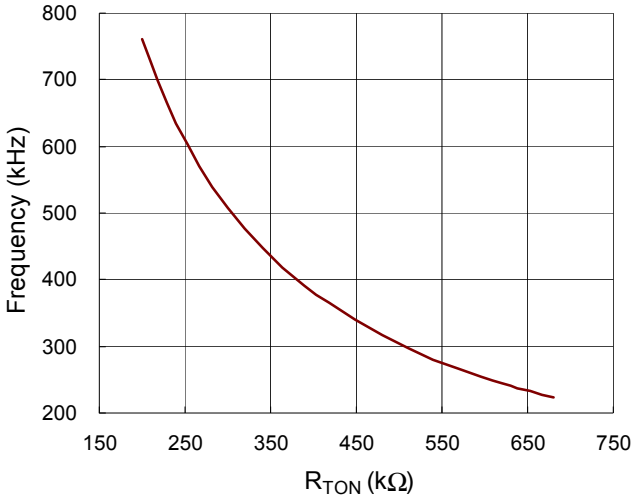


Figure 6. Frequency vs. R_{TON}

Active Phase Circuit setting : Before POR

The RT8813A can operate in 3/2/1 phase. When PVCC is higher than POR threshold and EN is higher than logic-high level, the RT8813A will detect the VCC/ISEN1 pin to determine how many phases should be active. For three phases operation, the VCC/ISEN1 pin is connected to PHASE1, the $\overline{\text{TALERT}}$/ISEN2 pin is connected to PHASE2, the TSNS/ISEN3 pin is connected to PHASE3, and external MOSEFT driver's PWM pin is connected to PWM3. For two phases operation, the VCC/ISEN1 pin is connected to PVCC, the $\overline{\text{TALERT}}$/ISEN2 pin is connected to $\overline{\text{TALERT}}$ signal, the TSNS/ISEN3 pin is connected to TSNS signal, and the PWM3 pin is connected to GND. For one phase operation, the VCC/ISEN1 pin is connected to PVCC, $\overline{\text{TALERT}}$/ISEN2 pin is connected to $\overline{\text{TALERT}}$ signal, the TSNS/ISEN3 pin is connected to TSNS signal, the PWM3 pin is connected to GND, and UGATE2, BOOT2, PHASE2, and LGATE 2 pins are floating. The voltage setting at PSI pin can't higher than 1.8V.

Mode Selection

The RT8813A can operate in 3 phases or 2 phases with force CCM, 1 phase with force CCM, and 1 phase with DEM according to PSI voltage setting. If PSI voltage is pulled below 0.8V, the controller will operate into 1 phase with DEM. In DEM operation, the RT8813A automatically reduces the operation frequency at light load conditions for saving power loss. If PSI voltage is pulled between 1.2V to 1.8V, the controller will switch operation into 1 phase with force CCM. If PSI voltage is pulled between 2.4V to 5.5V, the controller will switch operation into active phase (only for 2 or 3 phase). The operation mode is summarized in Table 1. Moreover, the PSI pin is valid after POR of VR.

Table 1

Operation Phase Number	PSI Voltage Setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

Diode-Emulation Mode

In diode-emulation mode, the RT8813A automatically reduces switching frequency at light-load conditions to maintain high efficiency. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial of negative current when the inductor freewheeling current reaches negative value. As the load current is further decreased, it takes a longer time to discharge the output capacitor to the level that requires the next "ON" cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction condition. The transition load point to the light load operation is shown in Figure 7 and can be calculated as follows :

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is on-time.

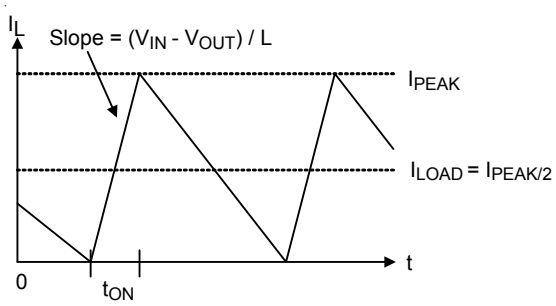


Figure 7. Boundary condition of CCM/DEM

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The switching waveforms may be noisy and asynchronous in light loading diode-emulation operation condition, but this is a normal operating condition that results in high light-load efficiency. Trade-off in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broad high efficiency range vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

Forced-CCM Mode

The low noise, forced-CCM mode disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate drive waveform to be the complement of the high side gate drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant.

Enable and Disable

The EN pin is a high impedance input that allows power sequencing between the controller bias voltage and another voltage rail. The RT8813A remains in shutdown if the EN pin is lower than 800mV. When the EN voltage rises above the 1.6V high level threshold, the RT8813A will begin a new initialization and soft-start cycle.

Power On Reset (POR), UVLO

Power On Reset (POR) occurs when V_{PVCC} rises above to approximately 4.1V (typical), the RT8813A will reset the fault latch circuit and prepare for PWM operation. When the V_{PVCC} is lower than 3.8V (typical), the Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low.

Soft-Start

The RT8813A provides both internal soft-start function and external soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered-up. The soft-start function automatically begins once the chip is enabled. There is a delay time around 1.1ms from EN goes high to V_{OUT} begins to ramp-up.

If the external capacitor between the SS pin and ground is removed, the internal soft-start function will be chosen. An internal current source charges the internal soft-start capacitor so that the internal soft-start voltage ramps up linearly. The output voltage will track the internal soft-start voltage during the soft-start interval. After the internal soft-start voltage exceeds the REFIN voltage, the output voltage no longer tracks the internal soft-start voltage but follows the REFIN voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited. The soft-start process is finished until both the single internal SSOK and external SSOK go high and protection is not triggered. Figure 8 shows the internal soft-start sequence.

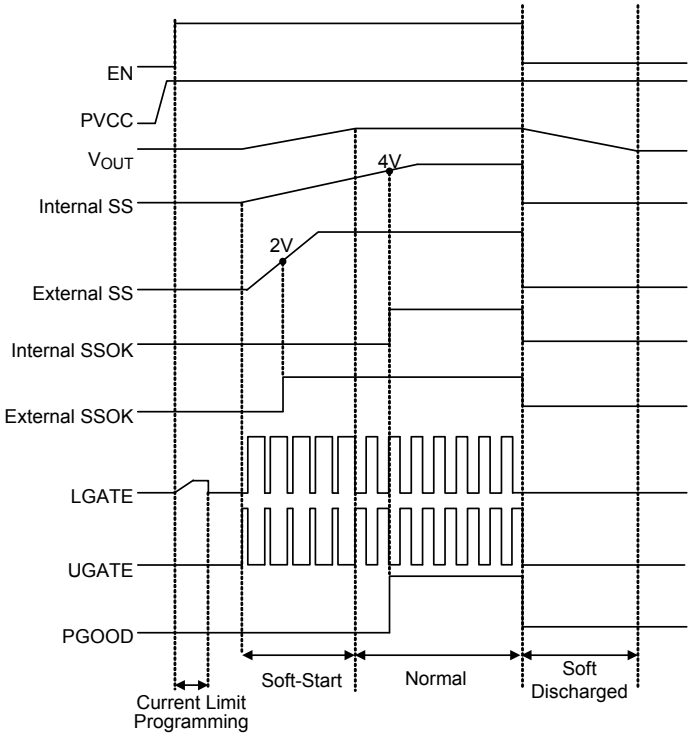


Figure 8. Internal Soft-Start Sequence

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The RT8813A also provides an external soft-start function, and the external soft-start sequence is shown in Figure 9. The external capacitor connected from SS pin to GND is charged by a 5μA current source to build a soft-start voltage ramp. If the external soft-start function is chosen, the external soft-start time should be set longer than internal soft-start time to avoid output voltage tracking the internal soft-start ramp. The recommended external soft-start slew rate is from 0.1V/ms to 0.4V/ms.

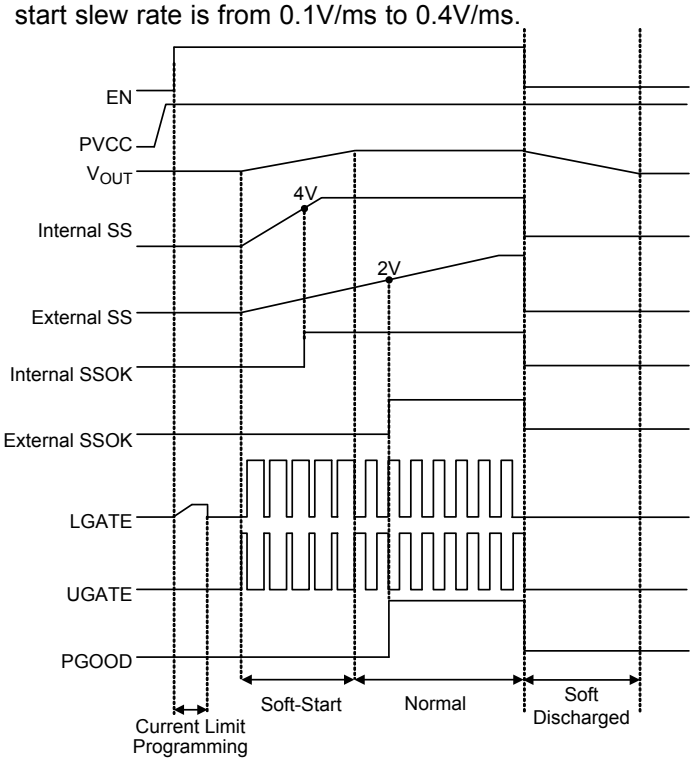


Figure 9. External Soft-Start Sequence

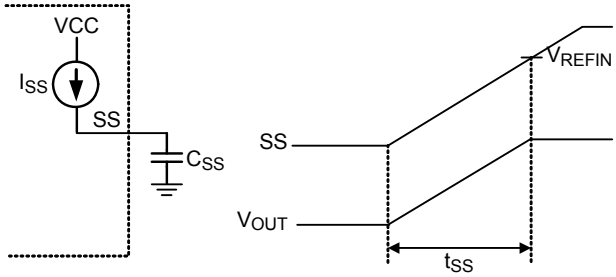


Figure 10. External Soft-Start Time Setting

The soft-start time can be calculated as :

$$t_{SS} = \frac{(C_{SS} \times V_{REFIN})}{I_{SS}}$$

Where I_{SS} = 5μA (typ.), V_{REFIN} is the voltage of REFIN pin, and C_{SS} is the external capacitor placed from SS to GND.

Power Good Output (PGOOD)

The PGOOD pin is an open drain output, and it requires a pull-up resistor. During soft-start, the PGOOD is held low and is allowed to be pulled high after V_{OUT} achieved over UVP threshold and under OVP threshold. In additional, if any protection is triggered during operation, the PGOOD will be pulled low immediately.

PWM VID and Dynamic Output Voltage Control

The RT8813A features a PWM VID input for dynamic output voltage control as shown in Figure 11, which reduces the number of device pin and enables a wide dynamic voltage range. The output voltage is determined by the applied voltage on the REFIN pin. The PWM duty cycle determines the variable output voltage at REFIN.

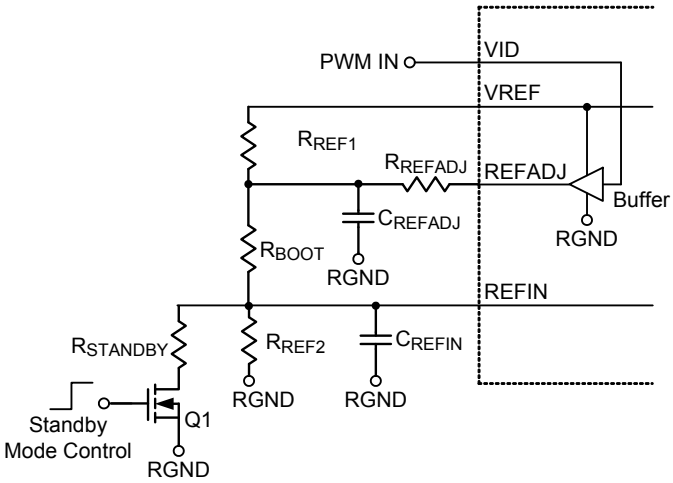


Figure 11. PWM VID Analog Circuit Diagram

With the external circuit and VID control signal, the controller provides three operation modes shown as Figure 12.

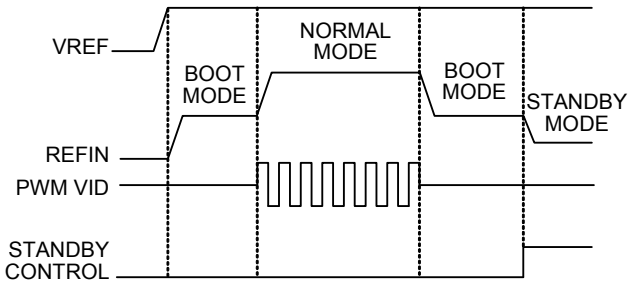


Figure 12. PWM VID Time Diagram

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Boot Mode

VID is not driven, and the buffer output is tri-state. At this time, turn off the switch Q1 and connect a resistor divider as shown in Figure 11 that can set the REFIN voltage to be V_{BOOT} as the following equation :

$$V_{BOOT} = V_{VREF} \times \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2} + R_{BOOT}} \right)$$

Where V_{VREF} = 2V (typ.)

Choose R_{REF2} to be approximately 10kΩ, and the R_{REF1} and R_{BOOT} can be calculated by the following equations :

$$R_{REF1} + R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}}$$

$$R_{REF1} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{BOOT}$$

$$R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{REF1}$$

Standby Mode

An external control can provide a very low voltage to meet V_{OUT} operating in standby mode. If the VID pin is floating and switch Q1 is enabled as shown in Figure 11, the REFIN pin can be set for standby voltage according to the calculation below :

$$V_{STANDBY} = V_{VREF} \times \frac{R_{REF2} \;//\; R_{STANDBY}}{R_{REF1} + R_{BOOT} + (R_{REF2} \;//\; R_{STANDBY})}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the $R_{STANDBY}$ can be calculated by the following equation :

$$R_{STANDBY} = \frac{R_{REF2} \times (R_{REF1} + R_{BOOT}) \times V_{STANDBY}}{R_{REF2} \times V_{REF} - V_{STANDBY} \times (R_{REF1} + R_{REF2} + R_{BOOT})} - R_{REF1}$$

Normal Mode

If the VID pin is driven by a PWM signal and switch Q1 is disabled as shown in Figure 11, the V_{REFIN} can be adjusted from V_{min} to V_{max}, where V_{min} is the voltage at zero percent PWM duty cycle and V_{max} is the voltage at one hundred percent PWM duty cycle. The V_{min} and V_{max} can be set by the following equations :

$$V_{min} = V_{VREF} \times \frac{R_{REF2}}{R_{REF2} + R_{BOOT}} \times \frac{R_{REFADJ} \;//\; (R_{BOOT} + R_{REF2})}{R_{REF1} + [R_{REFADJ} \;//\; (R_{BOOT} + R_{REF2})]}$$

$$V_{max} = V_{VREF} \times \frac{R_{REF2}}{(R_{REF1} \;//\; R_{REFADJ}) + R_{BOOT} + R_{REF2}}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the R_{REFADJ} can be calculated by the following equation :

$$R_{REFADJ} = \frac{R_{REF1} \times V_{min}}{V_{max} - V_{min}}$$

The relationship between VID duty and V_{REFIN} is shown in Figure 13, and V_{OUT} can be set according to the calculation below :

$$V_{OUT} = V_{min} + N \times V_{STEP}$$

where V_{STEP} is the resolution of each voltage step 1.

$$V_{STEP} = \frac{(V_{max} - V_{min})}{N_{max}}$$

where N_{max} is the number of total available voltage steps and N is the number of step at a specific V_{OUT}. The dynamic voltage VID period ($T_{vid} = T_u \times N_{max}$) is determined by the unit pulse width (T_u) and the available step number (N_{max}). The recommended T_u is 27ns.

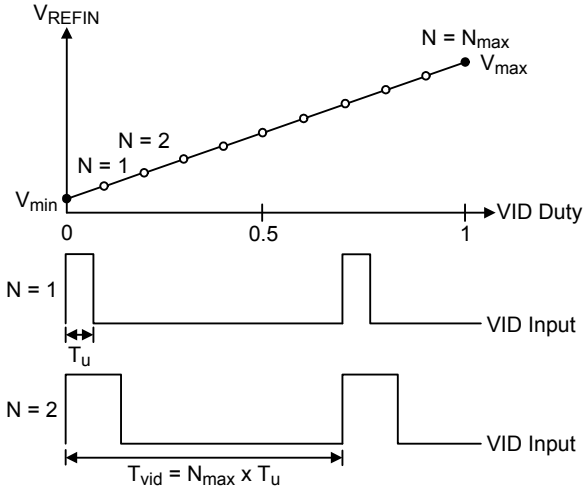


Figure 13. PWM VID Analog Output

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VID Slew Rate Control

In RT8813A, the V_{REFIN} slew rate is proportional to PWM VID duty, the rising time and falling time is the same because the voltage of REFIN pin traveling is the same. In normal mode, the V_{REFIN} slew rate SR can be estimated by C_{REFADJ} or C_{REFIN} as the following equation :

When choose C_{REFADJ} :

$$SR = \frac{(V_{REFIN_Final} - V_{REFIN_initial}) \times 80\%}{2.2 R_{SR} C_{REFADJ}}$$

$$R_{SR} = [(R_{REF1} // R_{REFADJ})] // (R_{BOOT} + R_{REF2})$$

When choose C_{REFIN} :

$$SR = \frac{(V_{REFIN_Final} - V_{REFIN_initial}) \times 80\%}{2.2 R_{SR} C_{REFIN}}$$

$$R_{SR} = \left[(R_{REF1} // R_{REFADJ}) + R_{BOOT}\right] // R_{REF2}$$

The recommend SR is estimated by C_{REFADJ}.

Current limit

The RT8813A provides cycle-by-cycle current limit control by detecting the PHASE voltage drop across the low side MOSFET when it is turned on. The current limit circuit employs a unique "valley" current sensing algorithm as shown in Figure 14. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle.

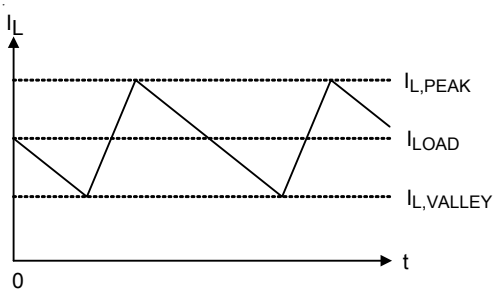


Figure 14. "Valley" Current Limit

In order to provide both good accuracy and a cost effective solution, the RT8813A supports temperature compensated MOSFET $R_{DS(ON)}$ sensing.

In an over current condition, the current to the load exceeds the average output inductor current. Thus, the output voltage falls and eventually crosses the under voltage protection threshold, inducing IC shutdown.

Current Limit Setting

Current limit threshold can be set by a resistor (R_{OCSET}) between LGATE1 and GND. Once PVCC exceeds the POR threshold and chip is enabled, an internal current source I_{OCSET} flows through R_{OCSET}. The voltage across R_{OCSET} is stored as the current limit protection threshold V_{OCSET}. The threshold range of V_{OCSET} is 50mV to 400mV. After that, the current source is switched off.

R_{OCSET} can be determined using the following equation :

$$R_{OCSET} = \frac{(I_{VALLEY} \times R_{LGDS(ON)}) + 40mV}{I_{OCSET}}$$

where I_{VALLEY} represents the desired inductor limit current (valley inductor current) and I_{OCSET} is current limit setting current which has a temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$.

If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the current limit threshold. In this situation, the current limit threshold is internally preset to 400mV (typical).

Negative Current Limit

The RT8813A supports cycle-by-cycle negative current limiting. The absolute value of negative current limiting threshold is the same with the positive current limit threshold. If negative inductor current is rising to trigger negative current limit, the low side MOSFET will be turned off and the current will flow to input side through the body diode of the high side MOSFET. At this time, output voltage tends to rise because this protection limits current to discharge the output capacitor. In order to prevent shutdown because of over voltage protection, the low side MOSFET is turned on again 400ns after it is turned off. If the device hits the negative over current threshold again before output voltage is discharged to the target level, the low side MOSFET is turned off and process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output is discharged to the target level before negative current threshold is reached, the low side MOSFET is turned off, the high side MOSFET is then turned on, and the device keeps normal operation.

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Current Balance

The RT8813A implements current balance mechanism in the current loop. The RT8813A senses per phase current signal and compares it with the average current. If the sensed current of any particular phase is higher than the average current, the on-time of this phase will be decreased.

The current balance accuracy is major related with on-resistance of low side MOSFET ($R_{LG,DS(ON)}$). That is, in practical application, using lower $R_{LG,DS(ON)}$ will reduce the current balance accuracy.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. If REFIN voltage is lower than 1.33V, the over voltage threshold follows to absolute over voltage 2V. If REFIN voltage is higher than 1.33V, the over voltage threshold follows relative over voltage 1.5 x V_{REFIN}. When OVP is triggered, UGATE goes low and LGATE is forced high. The RT8813A is latched once OVP is triggered and can only be released by PVCC or EN power on reset. A 5μs delay is used in OVP detection circuit to prevent false trigger.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 40% of its set voltage, under voltage protection is triggered and then all UGATEx and LGATEx gate drivers are forced low. There is a 3μs delay built in the UVP circuit to prevent false transitions. During soft-start, the UVP blanking time is equal to PGOOD blanking time.

Thermal Monitoring and Temperature Reporting

The RT8813A provides thermal monitoring function in 2/1 phase operation via sensing the TSNS pin voltage, and which can indicate ambient temperature through the voltage divider R_{OTSET} and R_{NTC} shown in Figure 15. The voltage of V_{TSNS} is typically set to be higher than 1V. When ambient temperature rises, V_{TSNS} will fall and the $\overline{TALERT}$ signal will be pulled to low level if TSNS voltage drops below 1V.

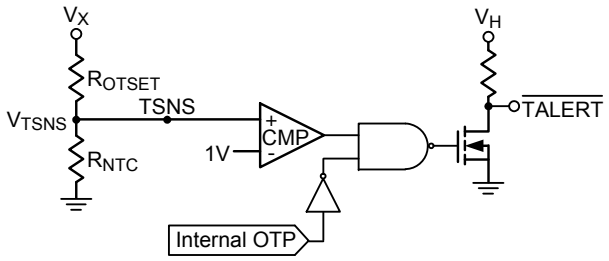


Figure 15. External OTP Setting

R_{OTSET} can be determined using the following equation :

$$R_{OTSET} = R_{NTC,T°C}\left(V_X - 1\right)$$

where $R_{NTC,T°C}$ is the thermistor's resistance at OTP trigger temperature.

The standard formula for the resistance of the NTC thermistor as a function of temperature is given by :

$$R_{NTC,T°C} = R_{25°C} \times e^{\left\{\beta\left[\left(\frac{1}{T+273}\right)-\left(\frac{1}{298}\right)\right]\right\}}$$

where $R_{25°C}$ is the thermistor's nominal resistance at room temperature 25°C, β (beta) is the thermistor's material constant in Kelvins, and T is the thermistor's actual temperature in Celsius.

MOSFET Gate Driver

The RT8813A integrates high current gate drivers for the MOSFETs to obtain high efficiency power conversion in synchronous Buck topology. A dead-time is used to prevent the crossover conduction for high side and low side MOSFETs. Because both the two gate signals are off during the dead-time, the inductor current freewheels through the body diode of the low side MOSFET. The freewheeling current and the forward voltage of the body diode contribute power losses to the converter. The RT8813A employs adaptive dead-time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent cross conduction. For high output current applications, two power MOSFETs are usually paralleled to reduce $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/sink current capability results in longer rising/falling time in gate signals and higher switching loss. The RT8813A embeds high current gate drivers to obtain high efficiency power conversion.

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Inductor Selection

Inductor plays an importance role in step-down converters because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of inductor should be as small as possible to minimize the copper loss. In additional, the inductor occupies most of the board space so the size of it is important. Low profile inductors can save board space especially when the height is limited. However, low DCR and low profile inductors are usually not cost effective.

Additionally, higher inductance results in lower ripple current, which means the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is designed to let the ripple current ranges between 20% to 40% of full load current. The inductance can be calculated using the following equation :

$$L_{min} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times k \times I_{OUT_rated}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting input capacitor. Generally, input capacitor has a voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select proper capacitor for RMS current rating. Use more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Besides, placing ceramic capacitor close to the drain of the high side MOSFET is helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full load to no load condition without tripping the OVP circuit. Organic semiconductor capacitor(s) or special polymer capacitor(s) are recommended.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high side MOSFET is small. Therefore, the switching loss of the high side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application.

However, the small duty cycle means the low side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, the MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low side MOSFET driver capability and the budget.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

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For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-24L 4x4 package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 3.57W for WQFN-24L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 16 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

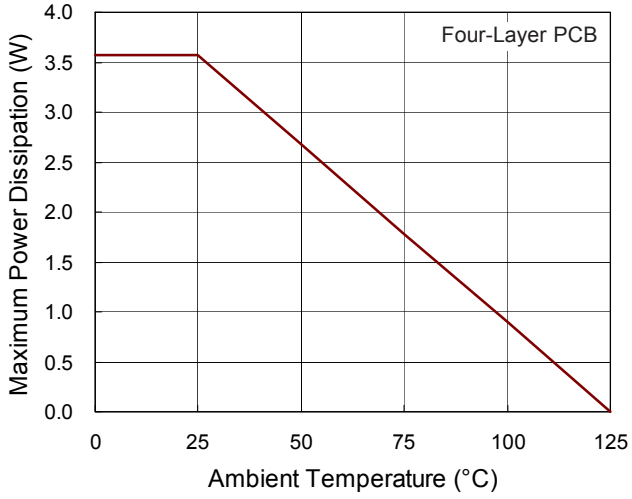


Figure 16. Derating Curve of Maximum Power Dissipation

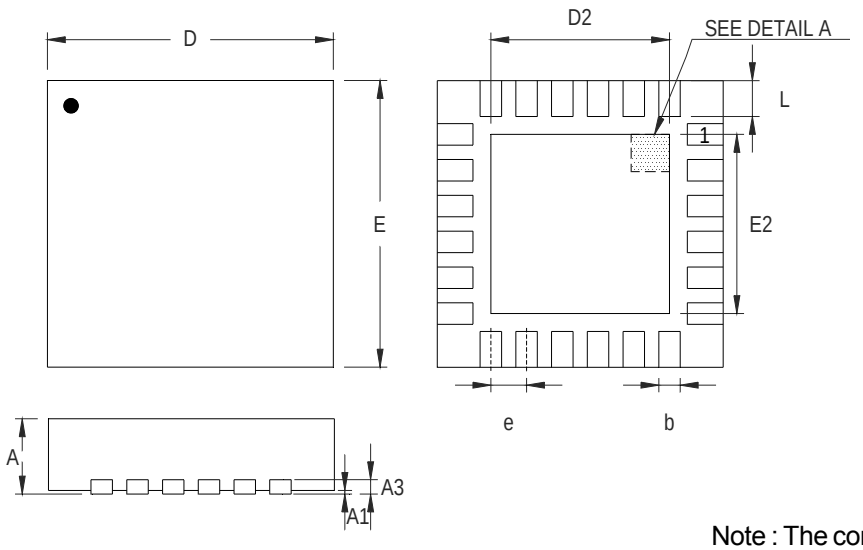
Layout Considerations

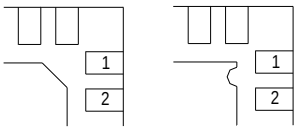
Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Following layout guidelines must be considered before starting a layout for RT8813A.

- Place the RC filter as close as possible to the PVCC pin.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VSNS, RGND, EN, PSI, VID, PGOOD, VREF, TON VREFADJ, VREFIN and TSNS should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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