TPS51206 2-A Peak Sink / Source DDR Termination Regulator With VTTREF Buffered Reference for DDR2, DDR3 and DDR3L

1 Features

- Supply Input Voltage: Supports 3.3-V Rail and 5-V Rail
- VLDOIN Input Voltage Range: VTT+0.4 V to 3.5 V
- VTT Termination Regulator
  - Output Voltage Range: 0.5 V to 0.9 V
  - 2-A Peak Sink and Source Current
  - Requires Only 10-µF MLCC Output Capacitor
  - ±20 mV Accuracy
- VTTREF Buffered Reference
  - VDDQ/2 ± 1% Accuracy
  - 10-mA Sink / Source Current
- Supports High-Z in S3 and Soft-Stop in S4/S5 with S3/S5 Inputs
- Overtemperature Protection
- 10-Pin 2-mm × 2-mm SON (DSQ) Package

2 Applications

- DDR2/DDR3/DDR3L Memory Power Supplies
- SSTL_18, SSTL_15, SSTL_135 and HSTL Termination

3 Description

The TPS51206 is a sink / source double date rate (DDR) termination regulator with VTTREF buffered reference output. It is specifically designed for low-input voltage, low-cost, low-external component count systems where space is a key consideration. The TPS51206 maintains fast transient response and only requires 1 × 10-µF of ceramic output capacitance. The TPS51206 supports a remote sensing function and all power requirements for DDR2, DDR3 and Low-Power DDR3 (DDR3L) VTT bus. The VTT current capability is ±2-A peak. The TPS51206 supports all of the DDR power states, putting VTT to High-Z in S3 state (suspend to RAM) and discharging VTT and VTTREF in S4/S5 state (suspend to disk).

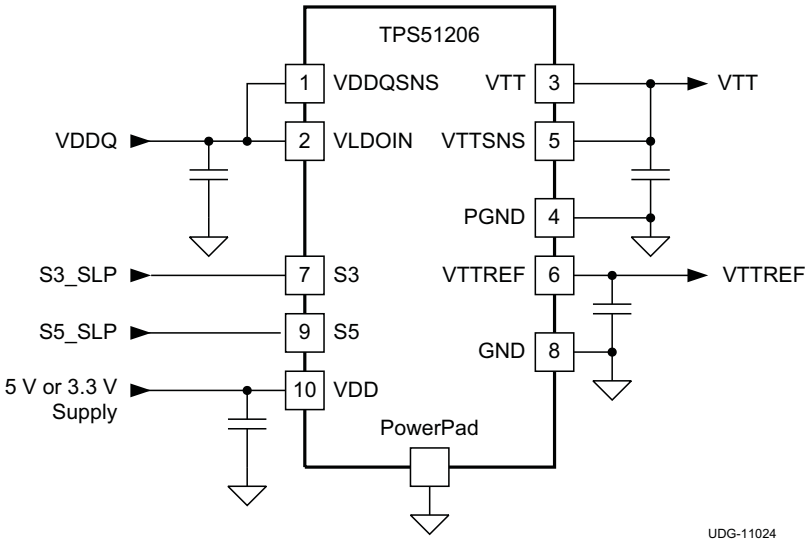
The TPS51206 is available in 10-pin, 2 × 2, SON (DSQ) PowerPAD™ package and specified from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51206	WSON (10)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 11
8 Application and Implementation ... 12
8.1 Application Information ... 12
8.2 Typical Applications ... 12
9 Power Supply Recommendations ... 16
10 Layout ... 16
10.1 Layout Guidelines ... 16
10.2 Layout Example ... 17
10.3 Thermal Considerations ... 17
11 Device and Documentation Support ... 18
11.1 Device Support ... 18
11.2 Trademarks ... 18
11.3 Electrostatic Discharge Caution ... 18
11.4 Glossary ... 18
12 Mechanical, Packaging, and Orderable Information ... 18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2013) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

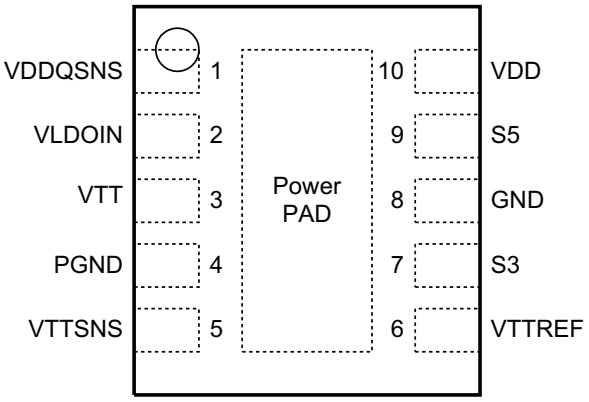
Changes from Original (MAY 2011) to Revision A **Page**

- Added minimum and maximum values to the wake up condition of the VDD UVLO threshold voltage specification ... 5

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5 Pin Configuration and Functions

10-Pins
DSQ Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	8	–	Signal ground
PGND	4	–	Power GND for VTT LDO
S3	7	I	S3 signal input
S5	9	I	S5 signal input
VDD	10	I	Device power supply input (3.3 V or 5 V)
VDDQSNS	1	I	VDDQ sense input, reference input for VTTREF
VLDOIN	2	I	Power supply input for VTT/ VTTREF
VTT	3	O	Power output for VTT LDO, need to connect 10-µF or greater MLCC for stability
VTTREF	6	O	VTTREF buffered reference output. Need to connect 0.22-µF or greater MLCC for stability
VTTSNS	5	I	VTT LDO voltage sense input
Pad	–	–	Solder to the ground plane for increased thremal performance.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage range(2)	VDD, S3, S5	–0.3	7	V
	VLDOIN, VTTSNS, VDDQSNS	–0.3	3.6	V
	PGND	–0.3	0.3	
Output voltage range(2)	VTT, VTTREF	–0.3	3.6	
Junction temperature, T_J			125	°C
Operating free-air temperature, T_A		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings*(1) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Supply voltage	VDD	3.1		6.5	V
Input voltage range(1)	S3, S5	–0.1		6.5	V
	VLDOIN, VTTSNS, VDDQSNS	–0.1		3.5	
	PGND	–0.1		0.1	
Output voltage range(1)	VTT, VTTREF	–0.1		3.5	V
Operating free-air temperature, T_A		–40		85	°C

(1) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.4 Thermal Information

THERMAL METRIC(1)		TPS51206 DSQ 10 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	70.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	46.3	
θ_{JB}	Junction-to-board thermal resistance	33.8	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	33.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	16.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 5 V, VLDOIN is connected to VDDQSNS, V_{S3} = V_{S5} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{VDD(S0)}$	VDD supply current, in S0	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V, $V_{VDDQSNS}$ = 1.8 V		170		µA
$I_{VDD(S3)}$	VDD supply current, in S3	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSNS}$ = 1.8 V		80		µA
I_{VDDSDN}	VDD shutdown current, in S4/S5	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 1.8 V			1	µA
$I_{VLDOIN(S0)}$	VLDOIN supply current, in S0	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V, V_{LDION} = 1.8 V			5	µA
$I_{VLDOIN(s3)}$	VLDOIN supply current, in S3	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V, V_{LDION} = 1.8 V			5	µA
$I_{VLDOINSDN}$	VLDOIN shutdown current, in S4/S5	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V, V_{LDION} = 1.8 V			5	µA
VTTREF OUTPUT						
V_{VTTREF}	Output voltage		$V_{VDDQSNS}$/2			V
$V_{VTTREFTOL}$	Output voltage tolerance to $V_{VDDQSNS}$	$\|I_{VTTREF}\|$< 10 mA, 1.5 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	49%	50%	51%	
		$\|I_{VTTREF}\|$< 10 mA, 1.2 V ≤ $V_{VDDQSNS}$ < 1.5 V	48.75%		51.25%	
$I_{VTTREFSRC}$	Source current	$V_{VDDQSNS}$ = 1.8 V, V_{VTTREF} = 0 V	10			mA
$I_{VTTREFSNK}$	Sink current	$V_{VDDQSNS}$ = 0 V, V_{VTTREF} = 1.8 V	10			mA
$I_{VTTREFDIS}$	VTTREF Discharge current	T_A = 25°C, V_{S3} = V_{S5} = 0V, V_{VTTREF} = 0.5V		1.3		mA
VTT OUTPUT						
V_{VTT}	Output voltage		$V_{VDDQSNS}$/2			V
V_{VTTTOL}	Output voltage tolerance to $V_{VDDQSNS}$/2	$\|I_{VTT}\|$≤ 10 mA, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	–20		20	mV
		$\|I_{VTT}\|$< 1 A, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V(1)	–30		30	
		$\|I_{VTT}\|$< 2 A, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V(1)	–40		40	
		$\|I_{VTT}\|$≤ 10 mA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.4 V	–20		20	
		$\|I_{VTT}\|$< 1 A, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.4 V(1)	–30		30	
		$\|I_{VTT}\|$< 1.5 A, 1.2 V ≤ $V_{VDDQSNS}$ < 1.4 V(1)	–40		40	
$I_{VTTOCLSRC}$	Source current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTT} = V_{VTTSNS} = 0.7 V	2			A
$I_{VTTOCLSNK}$	Sink current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTT} = V_{VTTSNS} = 1.1 V	2			A
I_{VTTLK}	Leakage current	T_A = 25°C , V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = V_{VTTREF}			5	µA
$I_{VTTSNSBIAS}$	VTTSNS input bias current	V_{S3} = 5 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–0.1		0.1	µA
$I_{VTTSNSLK}$	VTTSNS leakage current	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–0.1		0.1	µA
I_{VTTDIS}	VTT Discharge current	T_A = 25°C, V_{S3} = V_{S5} = $V_{VDDQSNS}$ = 0 V, V_{VTT} = 0.5 V		7		mA
VDDQ INPUT						
$I_{VDDQSNS}$	VDDQSNS input current	$V_{VDDQSNS}$ = 1.8 V		30		µA
UVLO/LOGIC THRESHOLD						
V_{VDDUV}	VDD UVLO threshold voltage	Wake up	2.67	2.90	3.00	V
		Hysteresis		0.2		
V_{LL}	S3/S5 low-level voltage				0.5	V
V_{LH}	S3/S5 high-level voltage		1.8			V
V_{LHYST}	S3/S5 hysteresis voltage			0.3		V
I_{LHLK}	S3/S5 input leak current		–1		1	µA
OVER-TEMPERATURE PROTECTION						
T_{OTP}	Over temperature protection	Shutdown temperature(1)		150		°C
		Hysteresis(1)		10		

(1) Ensured by design. Not production tested.

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6.6 Typical Characteristics

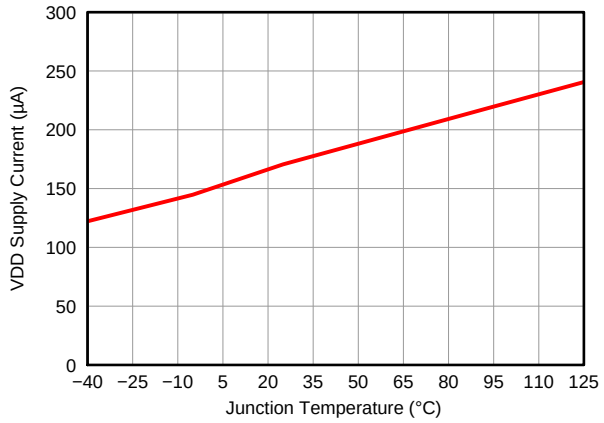


Figure 1. VDD Supply Current vs. Junction Temperature

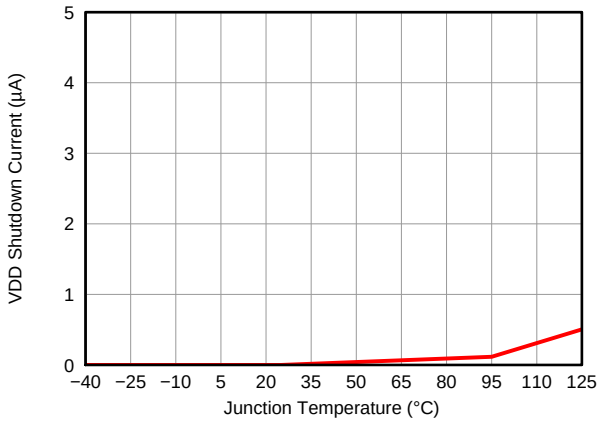


Figure 2. VDD Shutdown Current vs. Junction Temperature

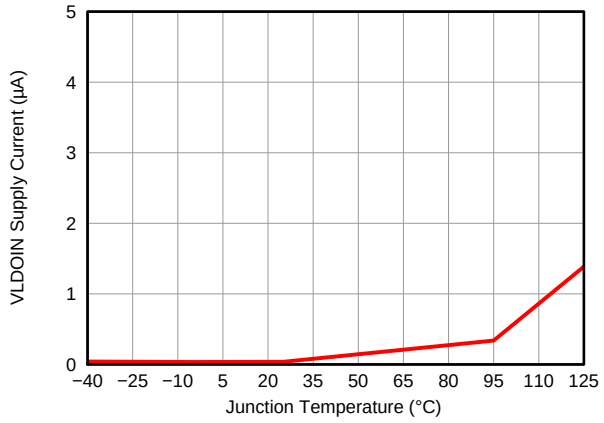


Figure 3. VLDOIN Supply Current vs. Junction Temperature

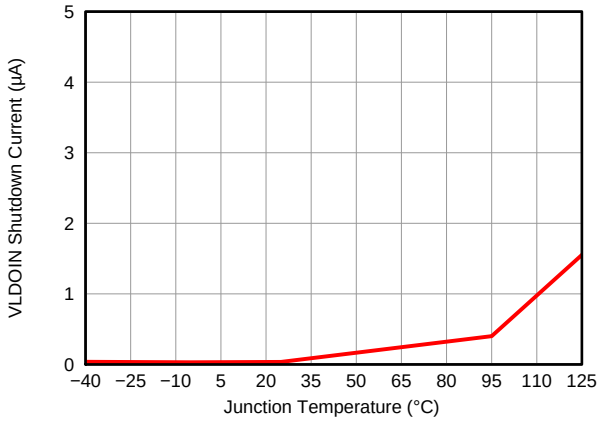


Figure 4. VLDOIN Shutdown Current vs. Junction Temperature

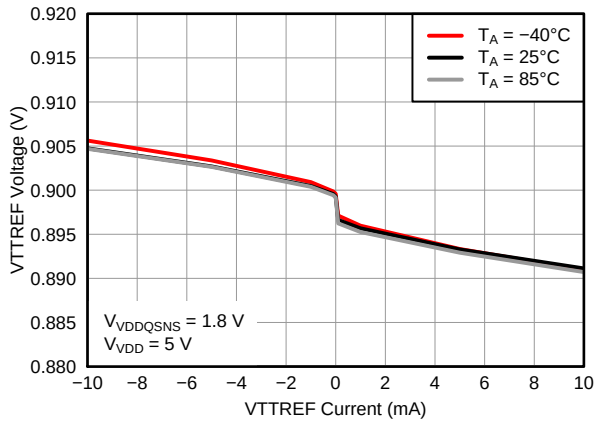


Figure 5. VTTREF Load Regulation (0.9 V)

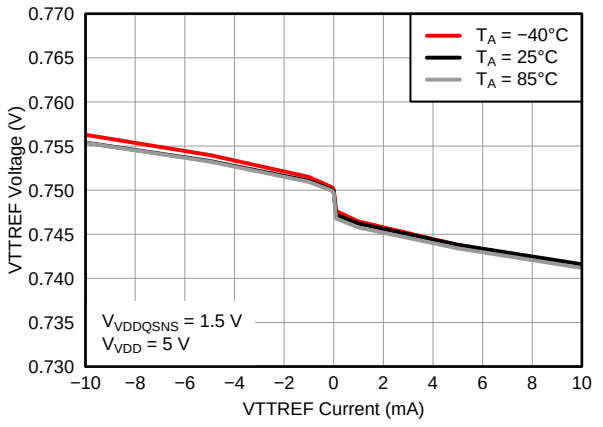


Figure 6. VTTREF Load Regulation (0.75 V)

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Typical Characteristics (continued)

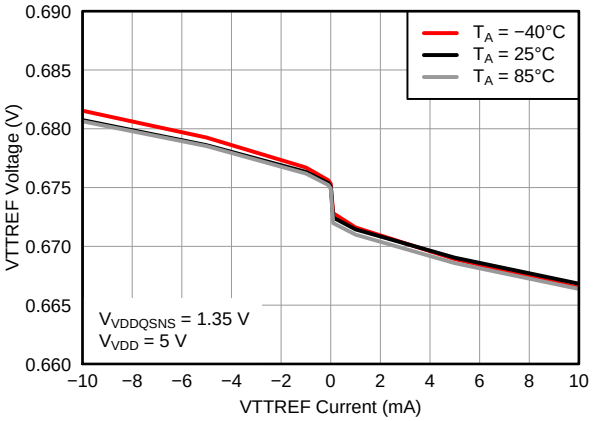


Figure 7. VTTREF Load Regulation (0.675 V)

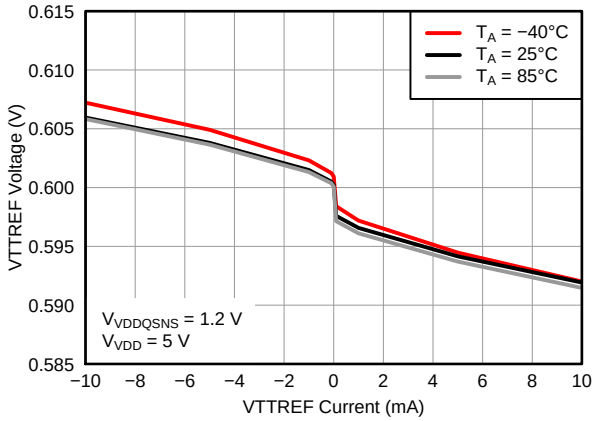


Figure 8. VTTREF Load Regulation (0.6 V)

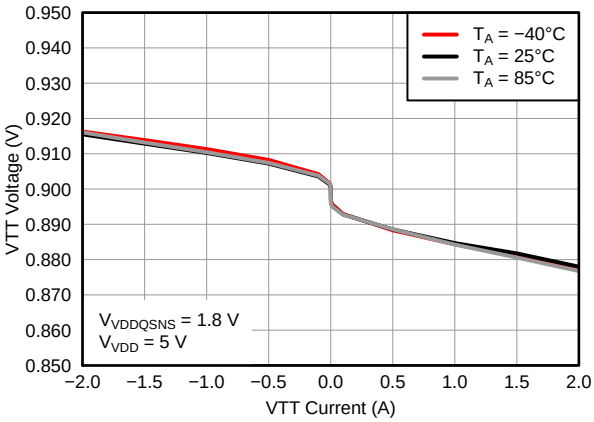


Figure 9. VTT Load Regulation (0.9 V)

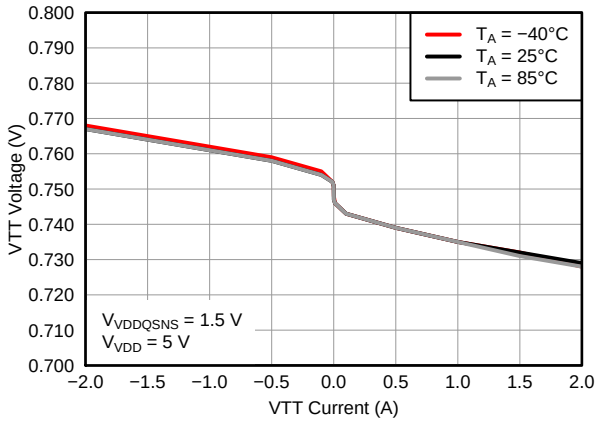


Figure 10. VTT Load Regulation (0.75 V)

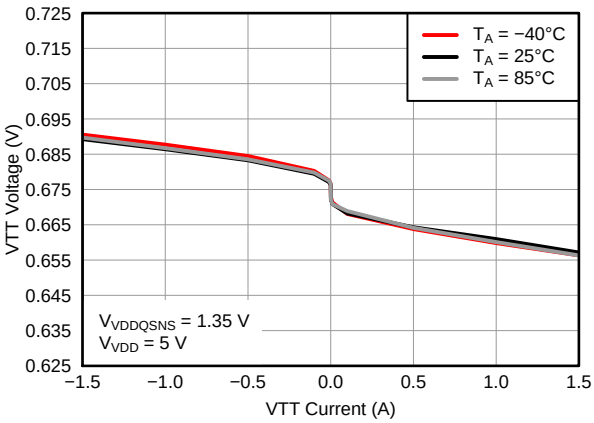


Figure 11. VTT Load Regulation (0.675 V)

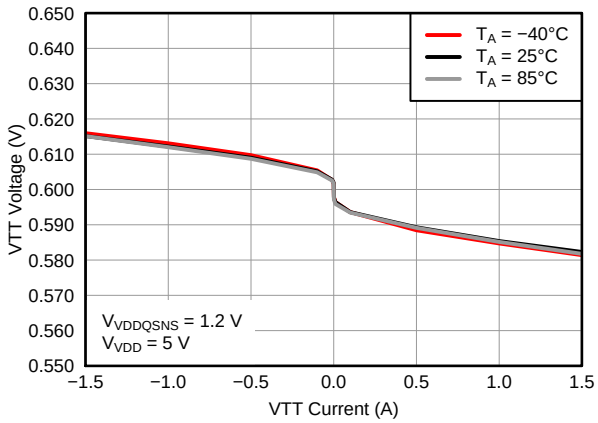


Figure 12. VTT Load Regulation (0.6 V)

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Typical Characteristics (continued)

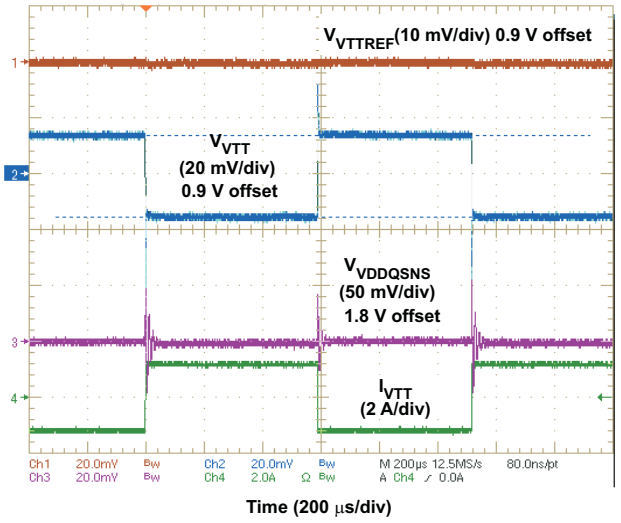


Figure 13. VTT Load Transient Response (0.9 V)

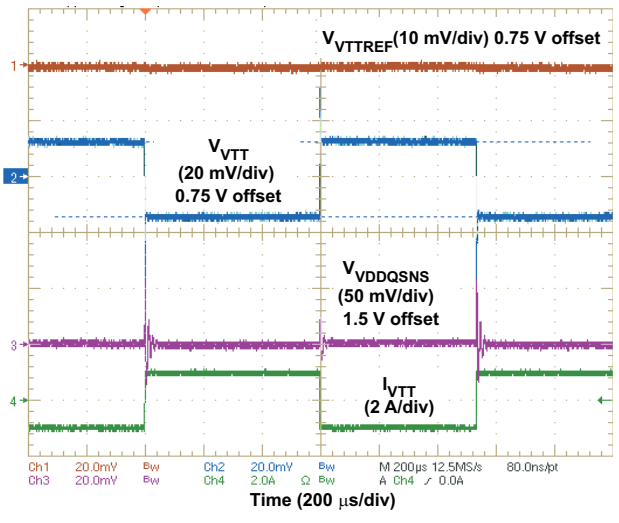


Figure 14. VTT Load Transient Response (0.75 V)

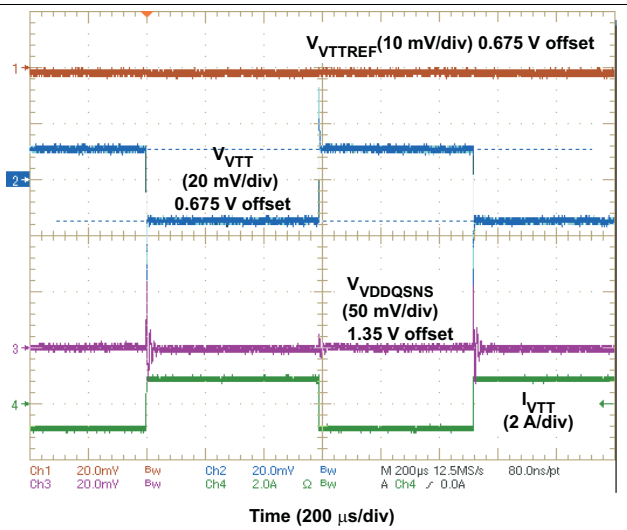


Figure 15. VTT Load Transient Response (0.675 V)

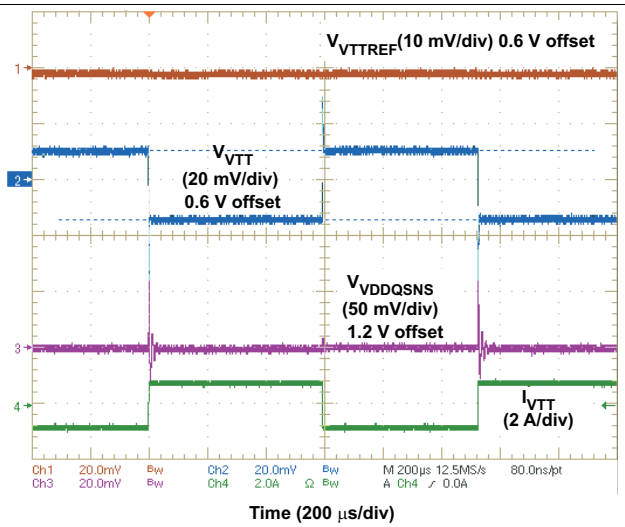


Figure 16. VTT Load Transient Response (0.6 V)

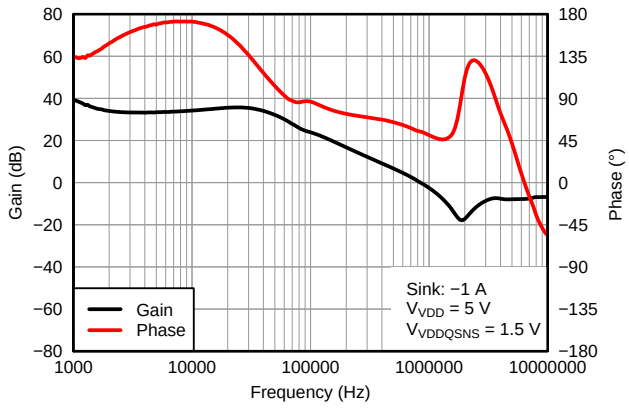


Figure 17. VTT (Sink: -1 A) Bode Plot (0.75 V)

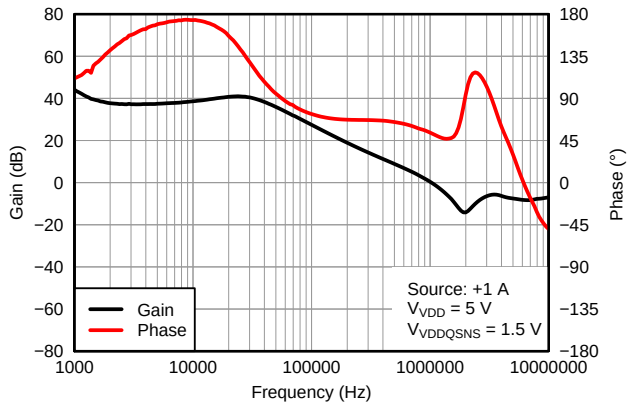


Figure 18. VTT (Source: +1 A) Bode Plot (0.75 V)

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Typical Characteristics (continued)

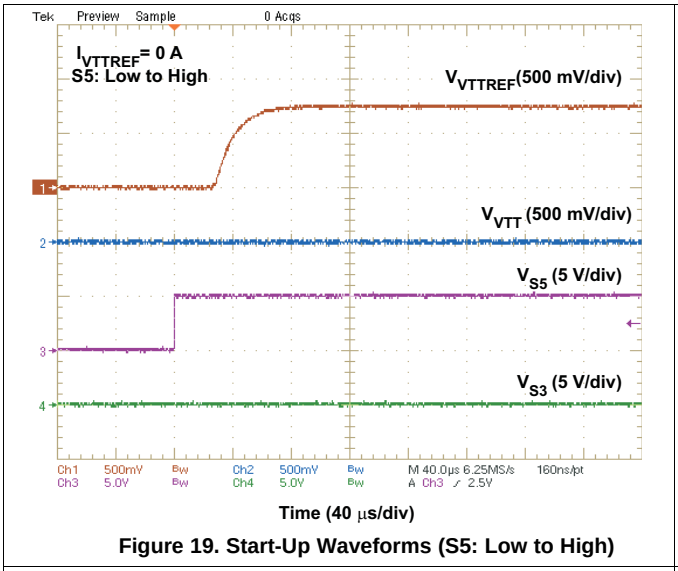


Figure 19. Start-Up Waveforms (S5: Low to High)

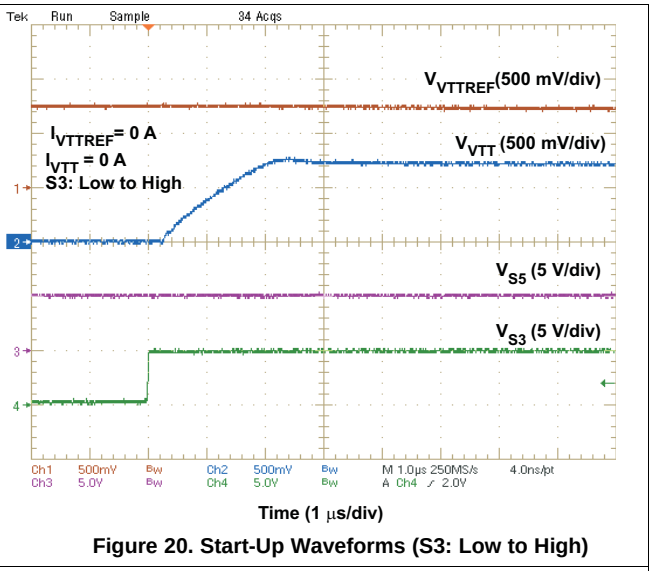


Figure 20. Start-Up Waveforms (S3: Low to High)

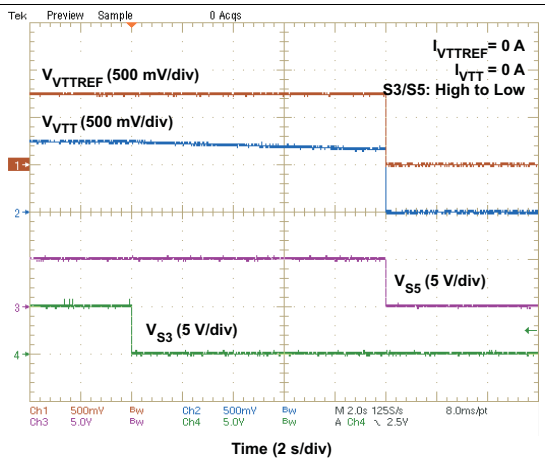


Figure 21. Shutdown Waveforms (S3/ S5: High to Low)

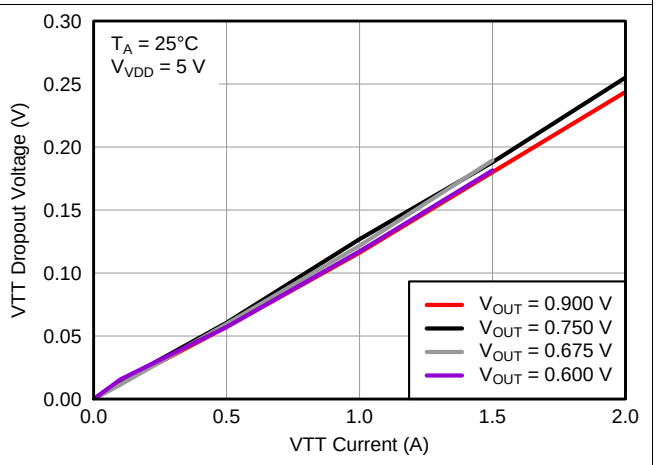


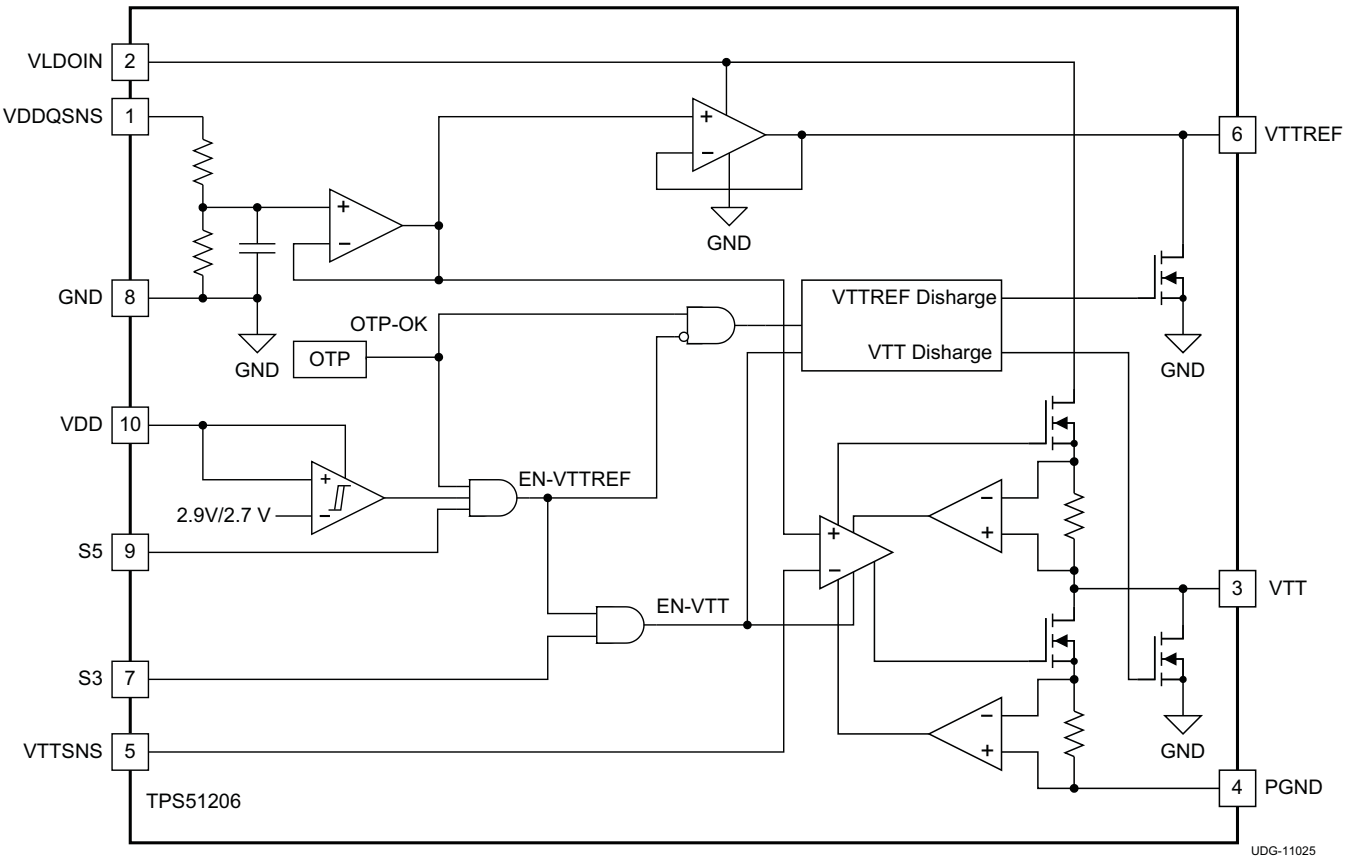
Figure 22. VTT Dropout Voltage

7 Detailed Description

7.1 Overview

The TPS51206 is a sink/source double date rate (DDR) termination regulator with VTTREF buffered reference output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VTT Sink and Source Regulator

The TPS51206 is a sink/source tracking termination regulator specifically designed for low input voltage, low cost, and low external component count systems where space is a key application parameter. The TPS51206 integrates a high-performance, low-dropout (LDO) linear regulator (VTT) that has ultimate fast response to track ½ VDDQSNS within 40 mV at all conditions, and its current capability is 2 A for both sink and source directions. A 10-µF (or greater) ceramic capacitor(s) need to be attached close to the VTT terminal for stable operation; X5R or better grade is recommended. To achieve tight regulation with minimum effect of trace resistance, the remote sensing terminal, VTTSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from the VTT pin.

The TPS51206 has a dedicated pin, VLDOIN, for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 0.4 V above the ½ VDDQSNS voltage.

7.3.2 VTTREF

The VTTREF pin includes 10 mA of sink/source current capability, and tracks ½ of VDDQSNS with ±1% accuracy. A 0.22-µF ceramic capacitor needs to be attached close to the VTTREF terminal for stable operation; X5R or better grade is recommended.

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Feature Description (continued)

7.3.3 VDD Undervoltage Lockout Protection

The TPS51206 input voltage (VDD) includes undervoltage lockout protection (UVLO). When the VDD pin voltage is lower than UVLO threshold voltage, VTT and VTTREF are shut off. This is non-latch protection.

7.3.4 Overtemperature Protection

This device features internal temperature monitoring. If the temperature exceeds the threshold value, VTT and VTTREF are shut off. This is a non-latch protection.

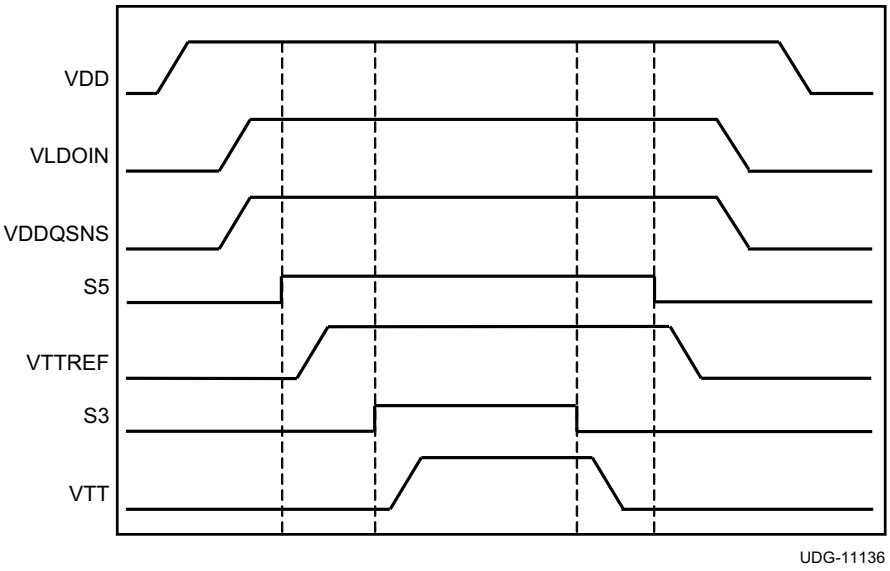


Figure 23. Typical Timing Diagram

7.4 Device Functional Modes

7.4.1 Power State Control

The TPS51206 has two input pins, S3 and S5, to provide simple control of the power state. Table 1 describes S3/S5 terminal logic state and corresponding state of VTTREF/VTT outputs. VTT is turn-off and placed to high impedance (High-Z) state in S3. The VTT output is floated and does not sink or source current in this state. When both S5 and S3 pins are LOW, the power state is set to S4/S5. In S4/S5 state, all the outputs are turn-off and discharged to GND.

Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON
S3	LO	HI	ON	OFF(High-Z)
S4/S5	LO	LO	OFF(Discharge)	OFF(Discharge)

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS51206 is typically used as a sink and source tracking termination regulator which converts a voltage from VTT+0.4 V to 3.5 V

8.2 Typical Applications

8.2.1 VLDOIN = VDDQ Configuration

Figure 24 shows an application diagram for a configuration where VLDOIN and VDDQ are connected.

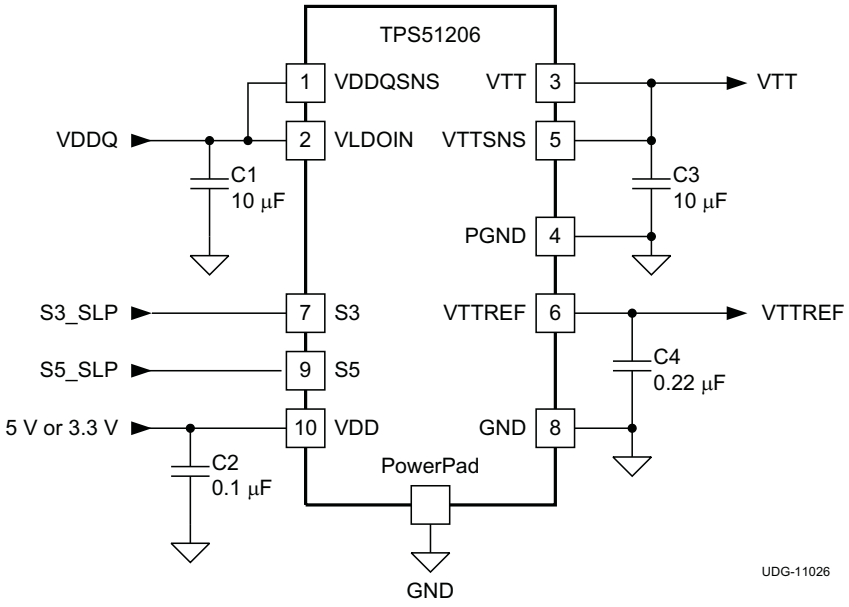


Figure 24. VLDOIN = VDDQ Configuration

8.2.1.1 Design Requirements

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply Voltage (VDD)	3.3 V or 5 V
VLDOIN = VDDQ	1.5 V
Output Current	±2 A

8.2.1.2 Detailed Design Procedure

Table 3. VLDOIN = VDDQ Configuration Components

REFERENCE DESIGNATOR	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C3	10 µF, 6.3 V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA

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Table 3. VLDOIN = VDDQ Configuration Components (continued)

REFERENCE DESIGNATOR	SPECIFICATION	MANUFACTURER	PART NUMBER
C2	0.1 µF, 6.3 V, X5R, 1005 (0402)	Taiyo Yuden	JWK105BJ104MP
C4	0.22 µF, 6.3 V, X5R, 1005 (0402)	Taiyo Yuden	JMK105BJ224KV

8.2.1.2.1 VDD Capacitor

Add a ceramic capacitor, with a value 0.1 µF (or greater) and X5R grade (or better), placed close to the VDD terminal, to stabilize the bias supply voltage from any parasitic impedance from the power supply rail.

8.2.1.2.2 VLDOIN Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-µF (or greater) and X5R grade (or better) ceramic capacitor to supply this transient charge.

8.2.1.2.3 VTTREF Capacitor

Add a ceramic capacitor, with a value 0.22 µF and X5R grade (or better), placed close to the VTTREF terminal for stable operation.

8.2.1.2.4 VTT Capacitor

For stable operation, a 10-µF (or greater) and X5R (or better) grade ceramic capacitor(s) need to be attached close to the VTT terminal. This capacitor is recommended to minimize any additional equivalent series resistance (ESR) and/or equivalent series inductance (ESL) of ground trace between the PGND terminal and the VTT capacitor(s).

8.2.1.2.5 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, the VTTSNS pin should be connected to the positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

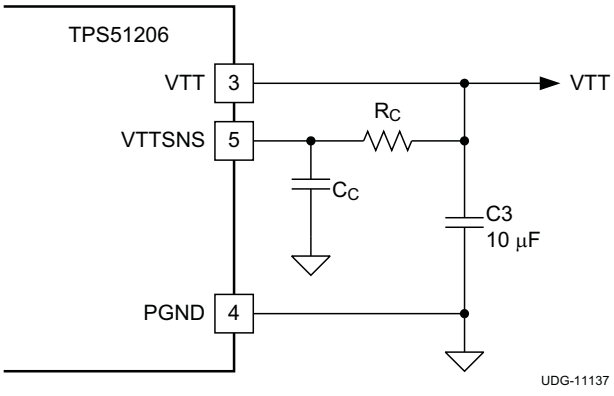


Figure 25. R-C Filter for VTTSNS

8.2.1.2.6 VDDQSNS Connection

VDDQSNS is a reference input of the VTTREF and VTT. Trace should be routed away from noise-generating lines.

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8.2.1.3 Application Curves

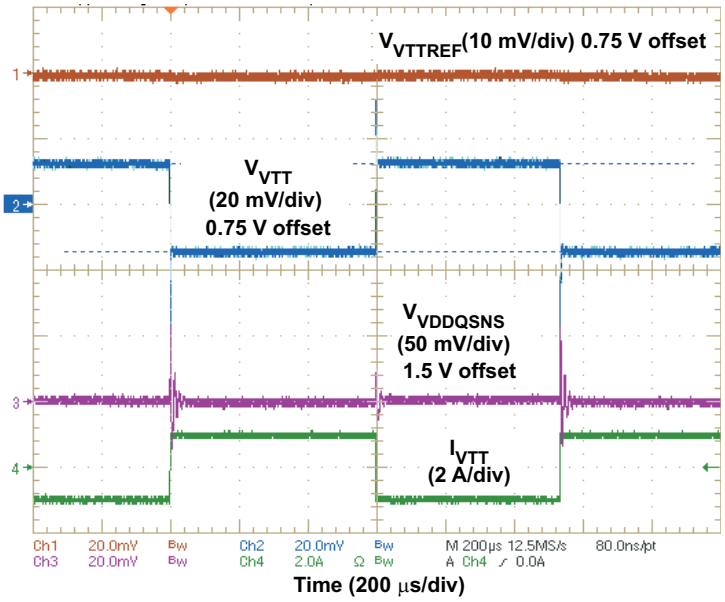


Figure 26. VTT Load Transient Response (0.75 V)

8.2.2 VLDOIN Separated from VDDQ Configuration

Figure 27 shows an application diagram for a configuration where VLDOIN and VDDQ are separated.

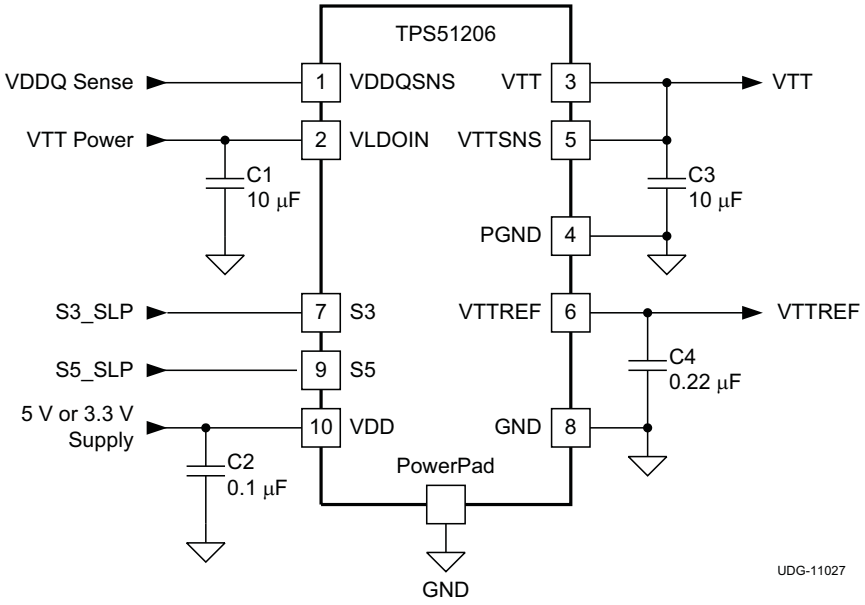


Figure 27. VLDOIN Separated from VDDQ Configuration

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8.2.2.1 Design Requirements

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply Voltage (VDD)	3.3 V or 5 V
VLDOIN = VDDQ	1.5 V
Output Current	±2 A

8.2.2.2 Detailed Design Procedure

Table 5. VLDOIN Separated from VDDQ Configuration Components

REFERENCE DESIGNATOR	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C3	10 µF, 6.3V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C2	0.1 µF, 6.3V, X5R, 1005 (0402)	Taiyo Yuden	JWK105BJ104MP
C3	10 µF, 6.3V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C4	0.22 µF, 6.3V, X5R, 1005 (0402)	Taiyo Yuden	JMK105BJ224KV

8.2.2.3 Application Curves

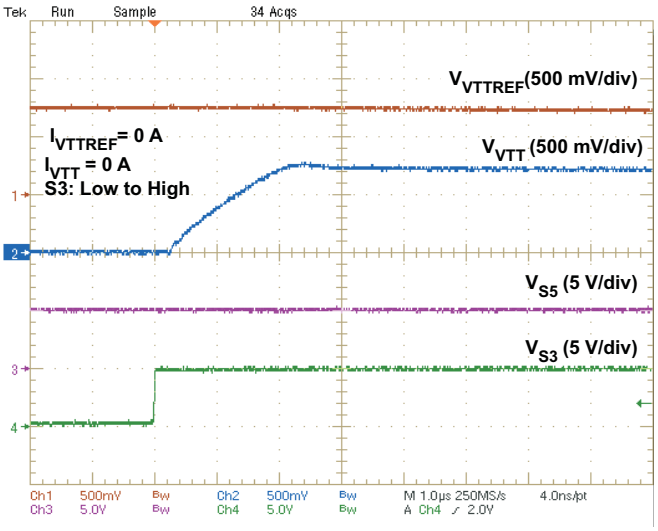


Figure 28. Start-Up Waveforms (S3: Low to High)

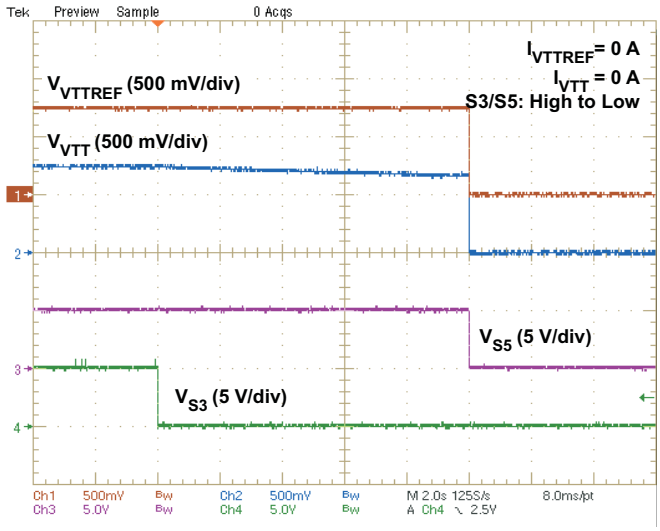


Figure 29. Shutdown Waveforms (S3 / S5: High to Low)

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9 Power Supply Recommendations

TPS51206 is designed for a sink / source double date rate (DDR) termination regulator with VTTREF buffered reference output. Supply input voltage (VDD) supports 3.3-V rail and 5-V rail; VLDOIN input voltage supports VTT+0.4 V to 3.5 V.

10 Layout

10.1 Layout Guidelines

Consider the following before beginning a TPS51206 layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the terminal with short and wide connections.
- The output capacitor for VTT should be placed close to the terminals (VTT and PGND) with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current VTT power trace. In addition, VTTSNS trace should be routed away from high current trace, on the separate layer is recommended. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor(s) at that point. In addition, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the VTT capacitor(s).
- The GND pin (and the negative node of the VTTREF output capacitor) and PGND pins (and the negative node of the VTT output capacitor) should be connected to the internal system ground planes (for better result, use at least two internal ground planes) with multiple vias. Use as many vias as possible to reduce the impedance between GND/PGND and the system ground plane.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder side ground plane(s) should also be used to help dissipation. Please consult the *TPS51206-EVM User's Guide* for more detailed layout recommendations.

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10.2 Layout Example

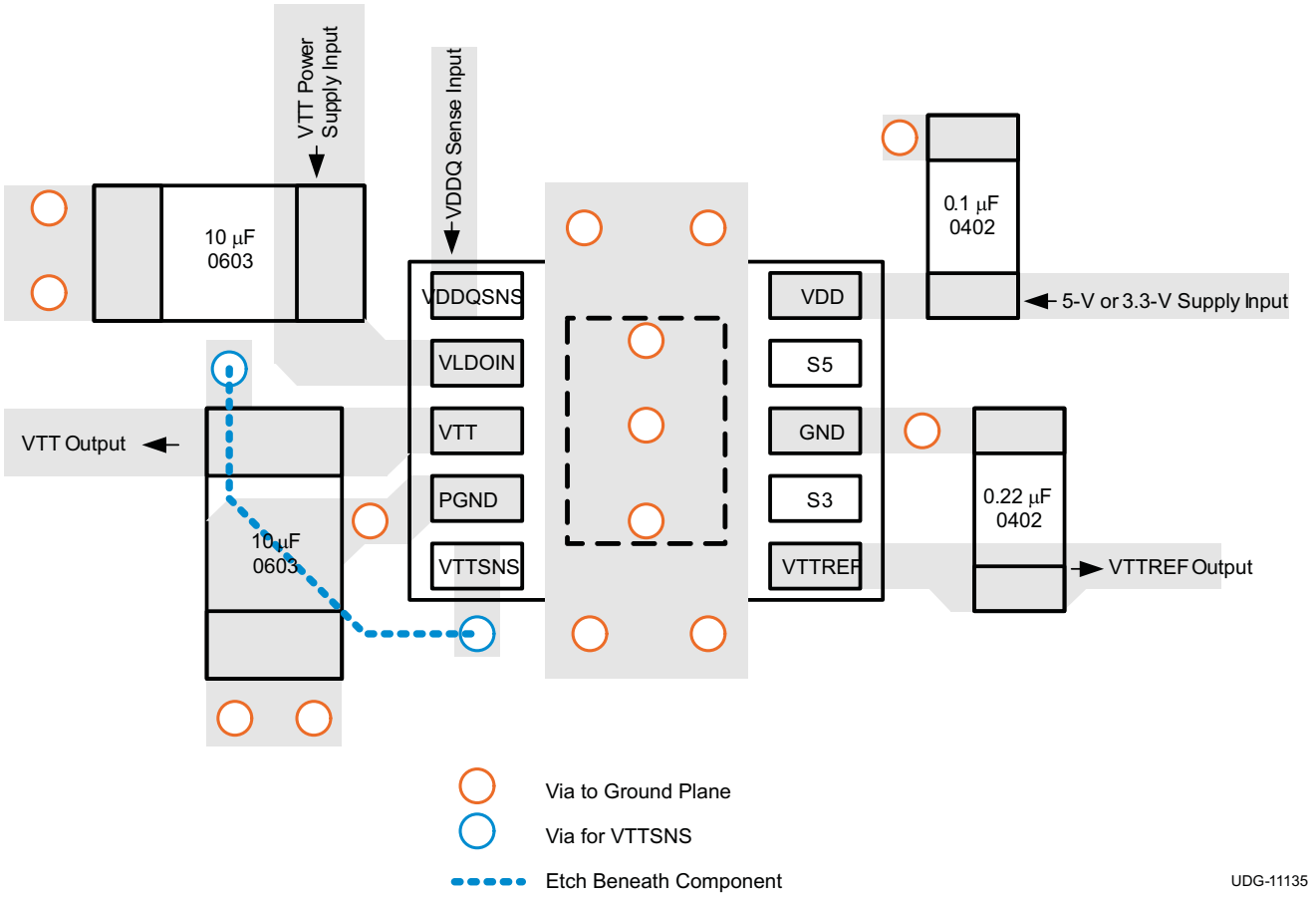


Figure 30. PCB Layout Guideline

10.3 Thermal Considerations

Because the TPS51206 is a linear regulator, the VTT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between VLDOIN and VTT times I_{VTT} (VTT current) current becomes the power dissipation as shown in Equation 1.

$$P_{DISS(src)} = (V_{VLDOIN} - V_{VTT}) \times I_{VTT(src)} \quad (1)$$

In this case, if the VLDOIN pin is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation can be calculated by Equation 2.

$$P_{DISS(snk)} = V_{VTT} \times I_{VTT(snk)} \quad (2)$$

Maximum power dissipation allowed by the package is calculated by Equation 3.

$$P_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}} \quad (3)$$

where

- $T_{J(max)}$ is 125°C
- $T_{A(max)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance from junction to ambient

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

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11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51206DSQR	ACTIVE	SON	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1206	Samples
TPS51206DSQT	ACTIVE	SON	DSQ	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1206	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

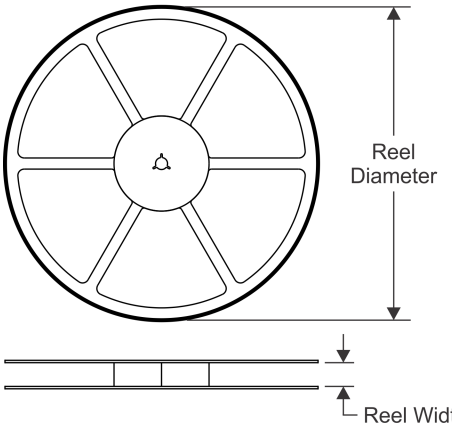
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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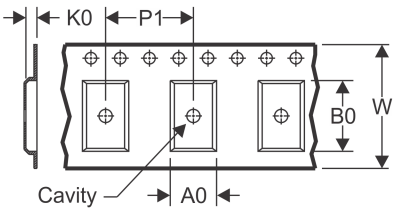
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

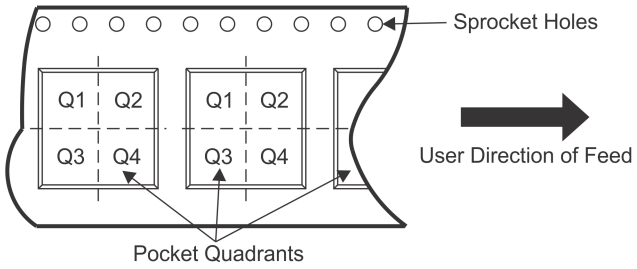


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

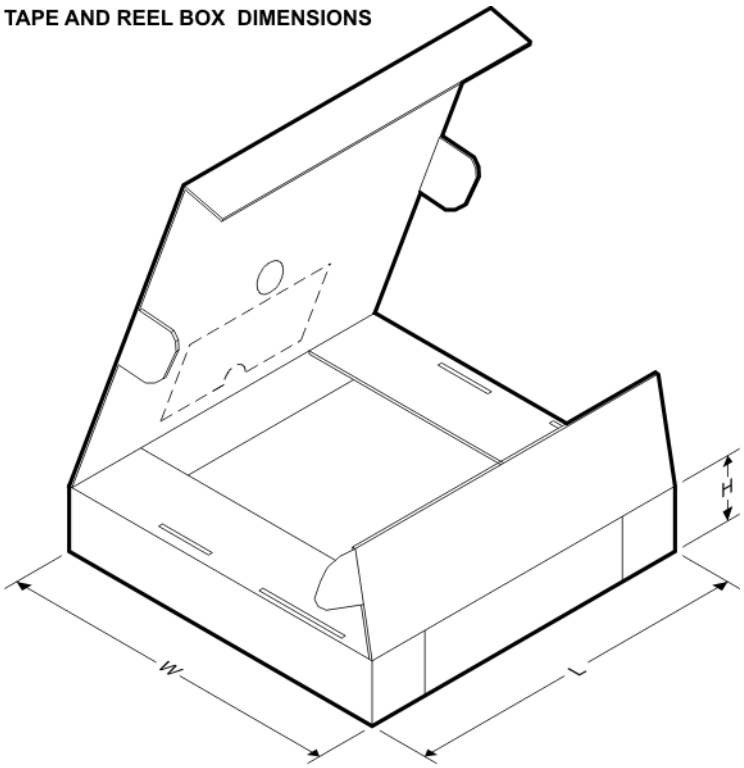
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51206DSQR	SON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQR	SON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQT	SON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

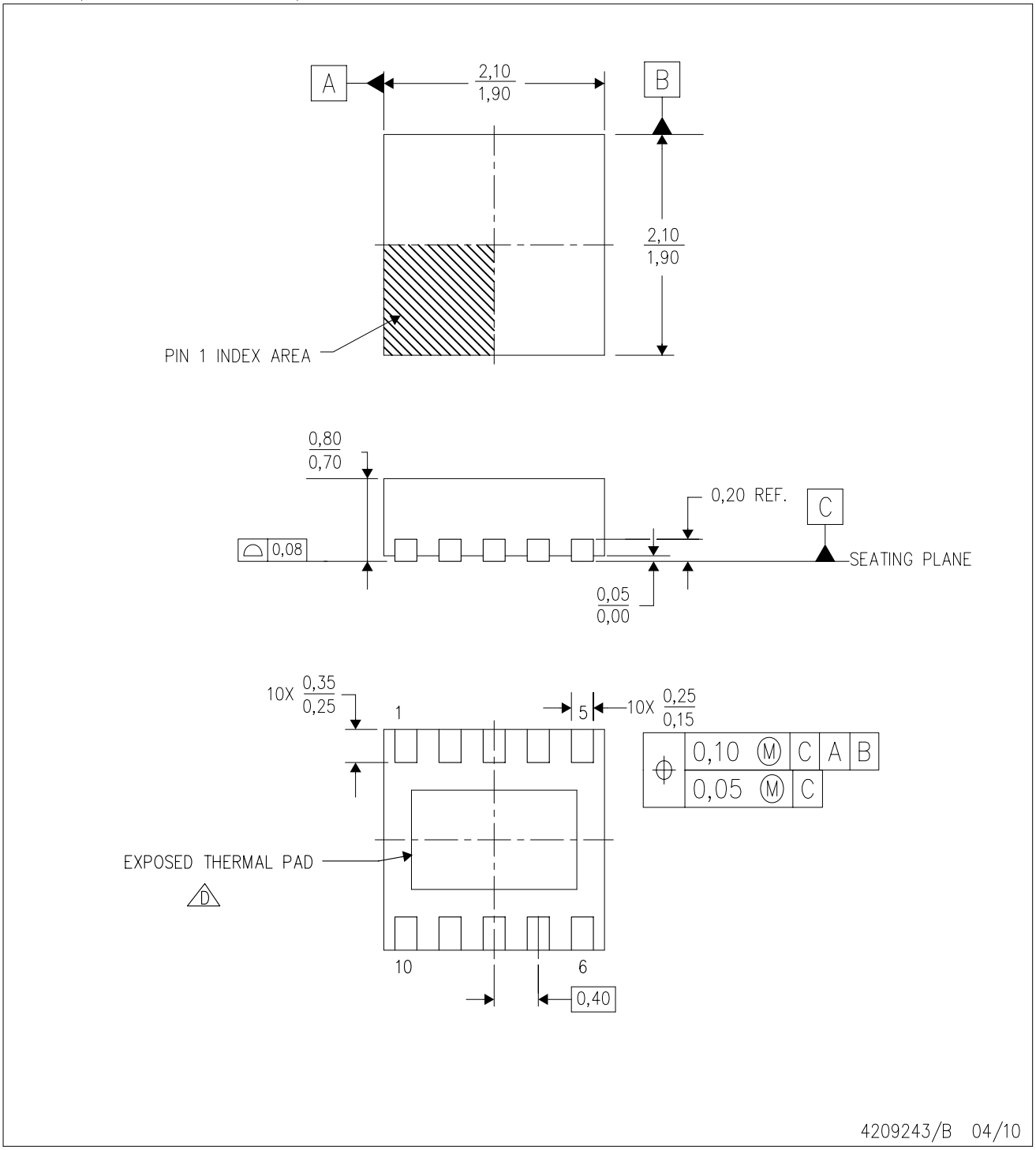
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51206DSQR	SON	DSQ	10	3000	210.0	185.0	35.0
TPS51206DSQR	SON	DSQ	10	3000	210.0	185.0	35.0
TPS51206DSQT	SON	DSQ	10	250	210.0	185.0	35.0

DSQ (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

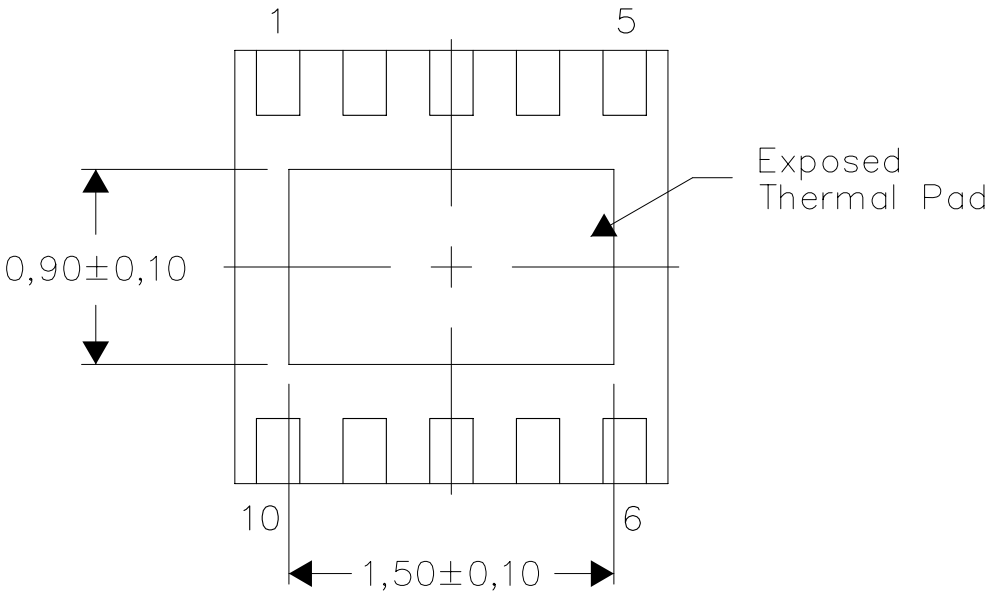
DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



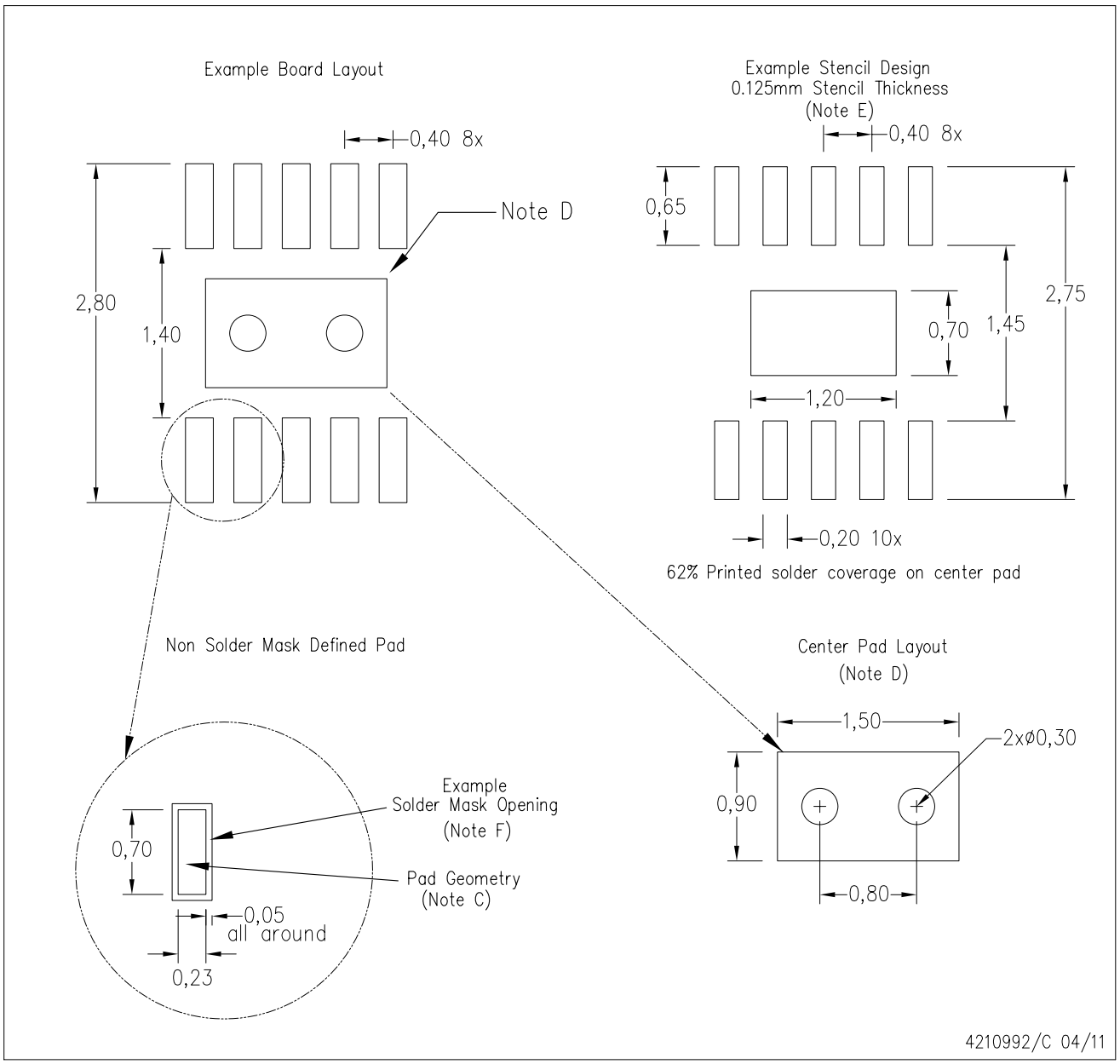
Bottom View

Exposed Thermal Pad Dimensions

4210993/C 04/11

NOTES: A. All linear dimensions are in millimeters

DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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