OptiMOS®2 Power-Transistor

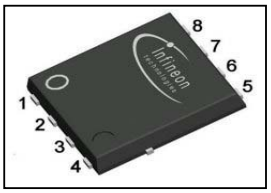
Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1)] for target application
- Ideal for high-frequency switching and synchronous rectification

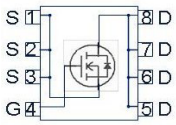
Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	19.6	mΩ
I_D	45	A

PG-TDSON-8



Type	Package	Marking
BSC196N10NS G	PG-TDSON-8	196N10NS



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	45	A
		T_C=100 °C	29	
		T_A=25 °C, R_{thJA}=45 K/W[2)]	8.5	
Pulsed drain current[3)]	$I_{D,pulse}$	T_C=25 °C	164	
Avalanche energy, single pulse	E_{AS}	I_D=45 A, R_{GS}=25 Ω	60	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	78	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

[1)] J-STD20 and JESD22

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.6	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[2)]	-	-	45	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=42 µA	2	3	4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=45 A	-	16.7	19.6	mΩ
Gate resistance	R_G		-	1	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=45 A	24	48	-	S

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

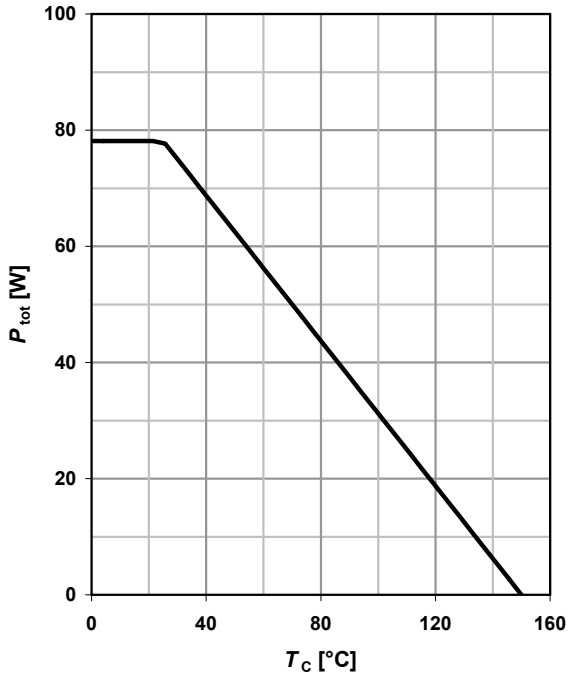
[3)] see figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz	-	1700	2300	pF
Output capacitance	C_{oss}		-	250	330	
Reverse transfer capacitance	C_{rss}		-	17	26	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50 V, V_{GS}=10 V, I_D=25 A, R_G=1.6 Ω	-	16	24	ns
Rise time	t_r		-	22	33	
Turn-off delay time	$t_{d(off)}$		-	18	28	
Fall time	t_f		-	5	8	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=50 V, I_D=25 A, V_{GS}=0 to 10 V	-	9	12	nC
Gate to drain charge	Q_{gd}		-	6	9	
Switching charge	Q_{sw}		-	10	14	
Gate charge total	Q_g		-	25	34	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V
Output charge	Q_{oss}	V_{DD}=50 V, V_{GS}=0 V	-	27	35	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	45	A
Diode pulse current	$I_{S,pulse}$		-	-	180	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=45 A, T_j=25 °C	-	1.0	1.3	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=25 A, di_F/dt=100 A/µs	-	82	-	ns
Reverse recovery charge	Q_{rr}		-	199	-	nC

[4)] See figure 16 for gate charge parameter definition

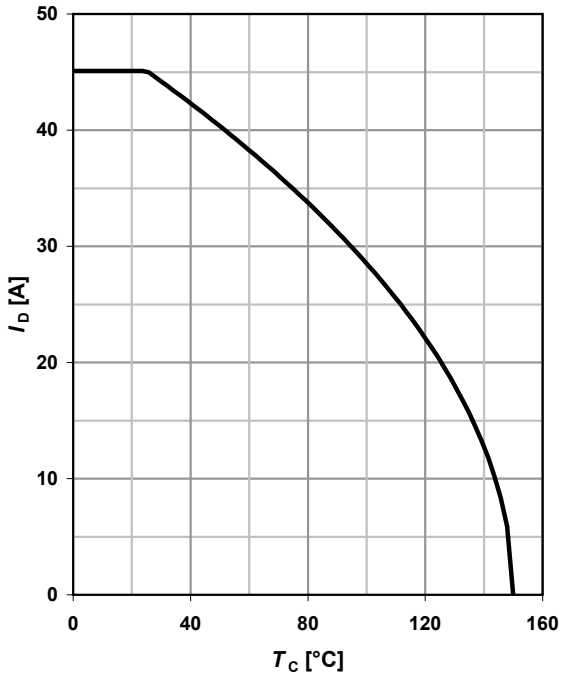
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

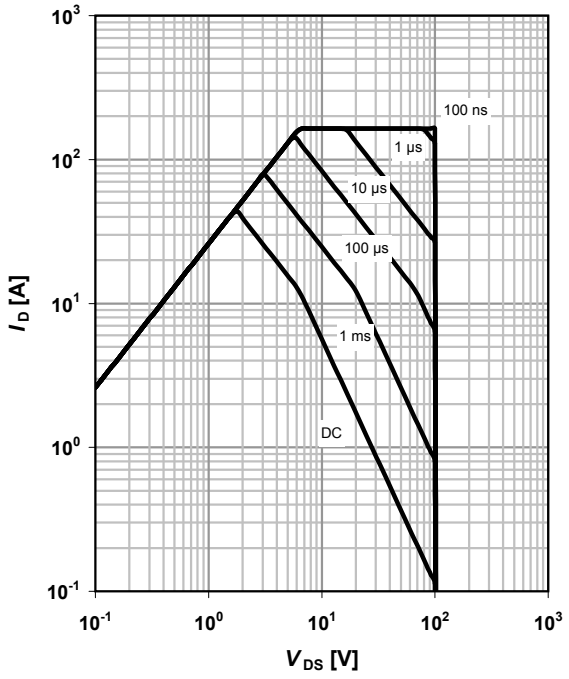
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

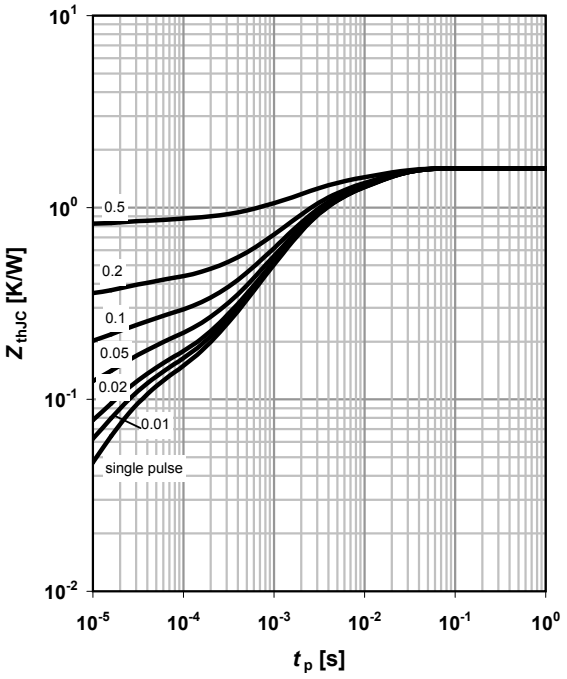
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

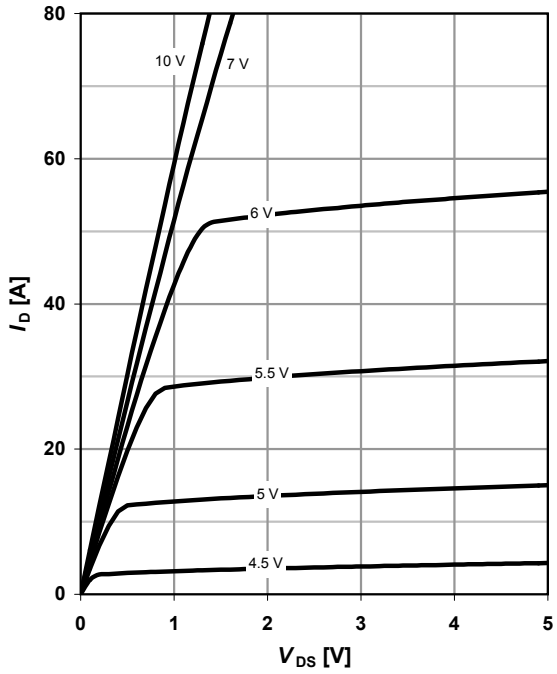
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

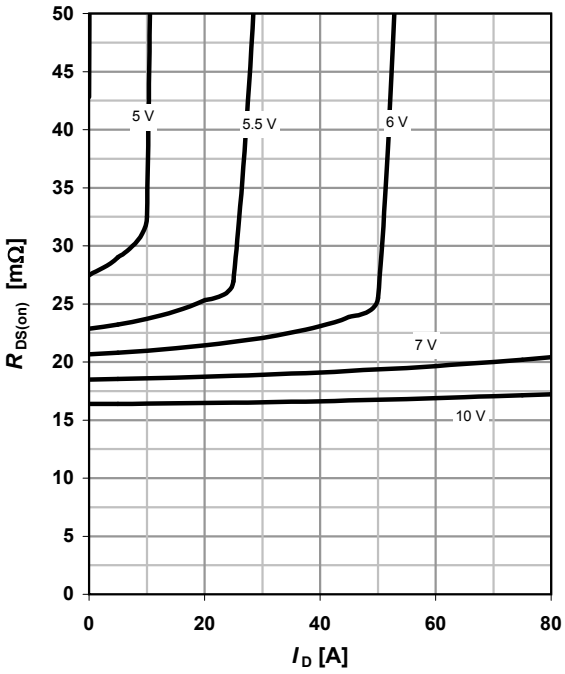
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

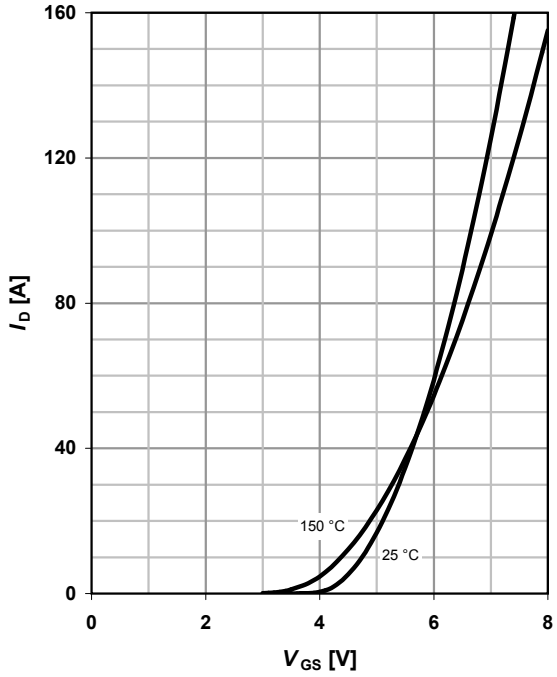
parameter: V_{GS}



7 Typ. transfer characteristics

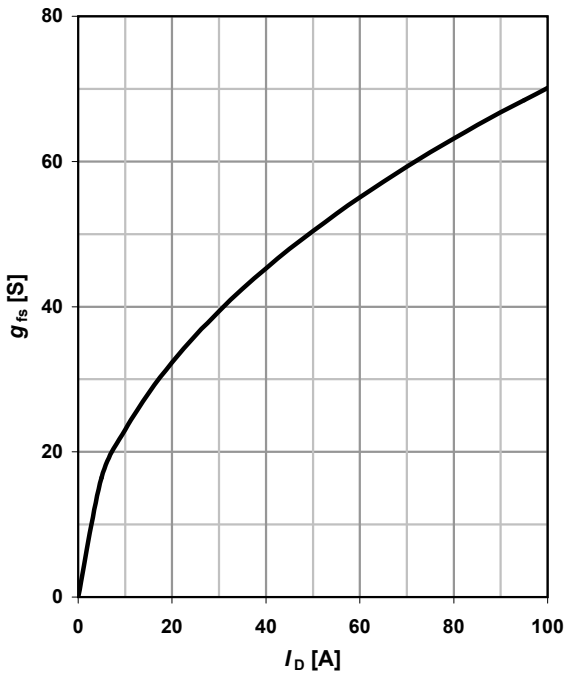
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



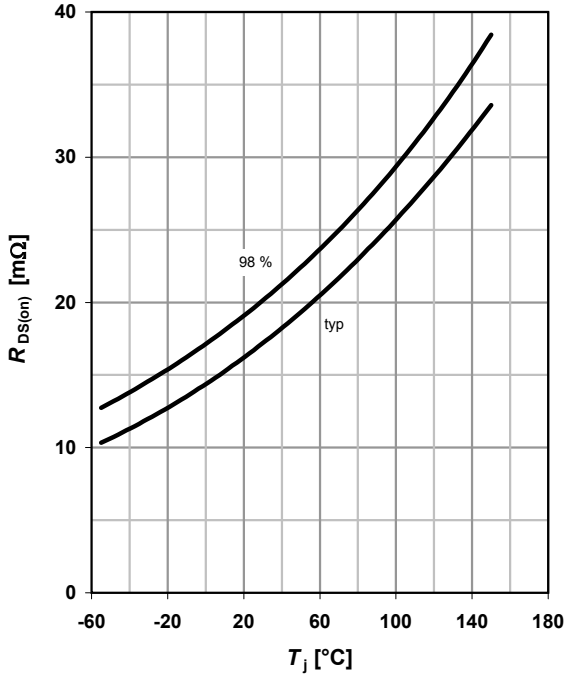
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



9 Drain-source on-state resistance

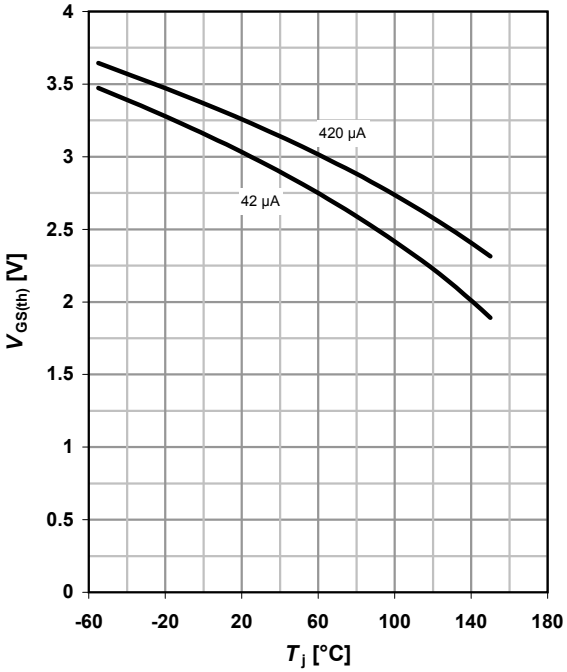
$R_{DS(on)}$=f(T_j); I_D=45 A; V_{GS}=10 V



10 Typ. gate threshold voltage

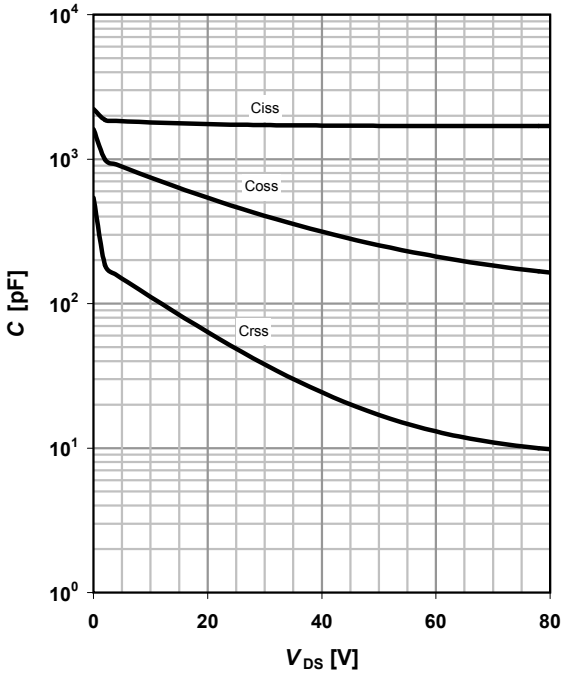
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

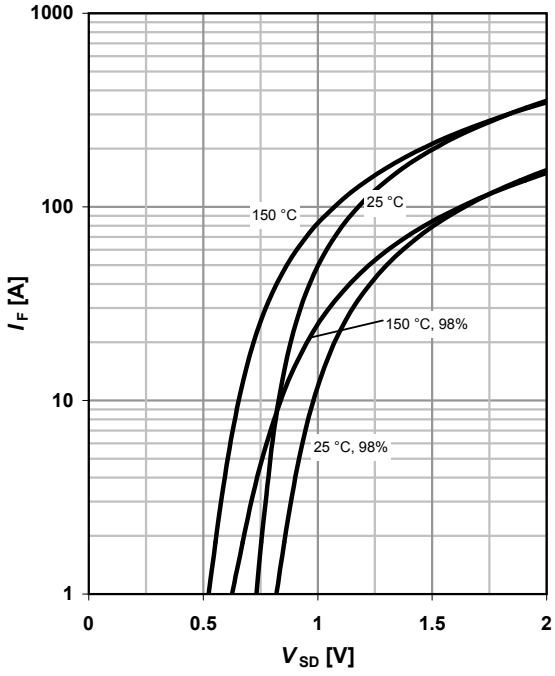
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

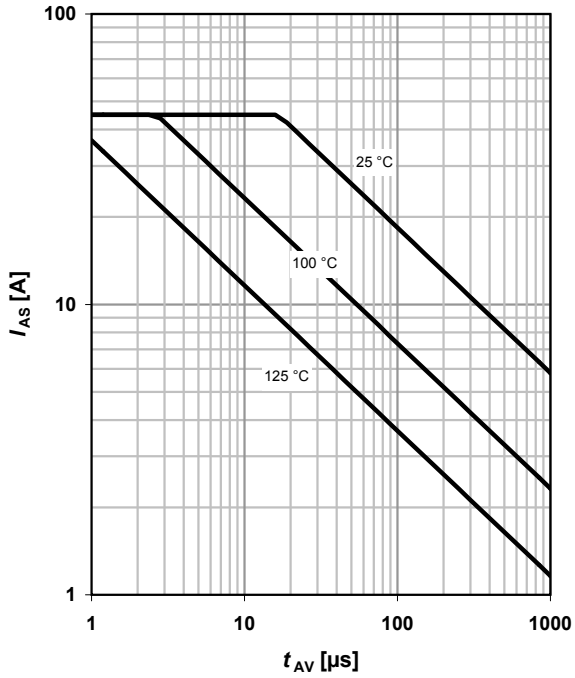
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

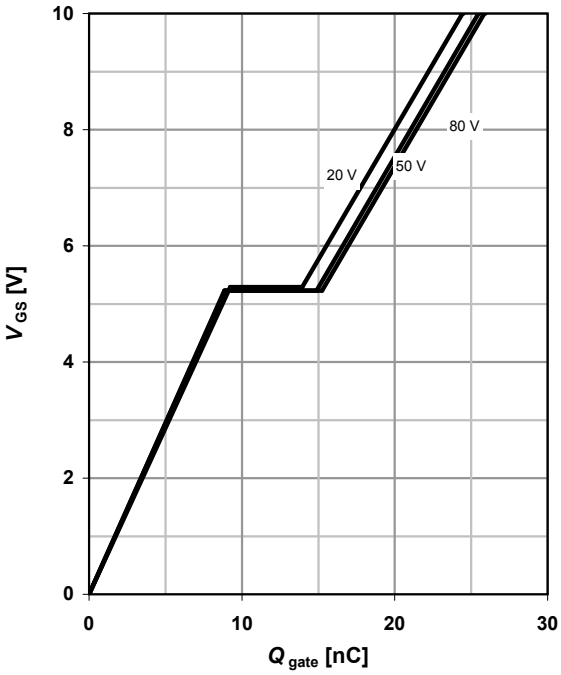
parameter: $T_{j(start)}$



14 Typ. gate charge

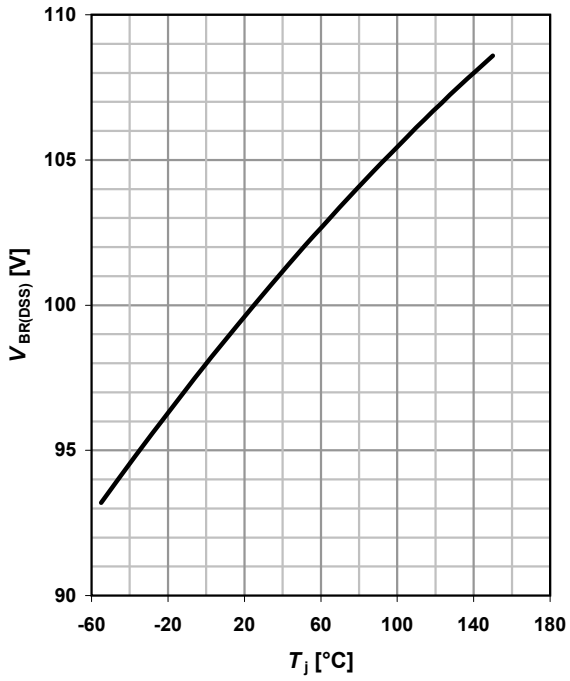
V_{GS}=f(Q_{gate}); I_D=25 A pulsed

parameter: V_{DD}

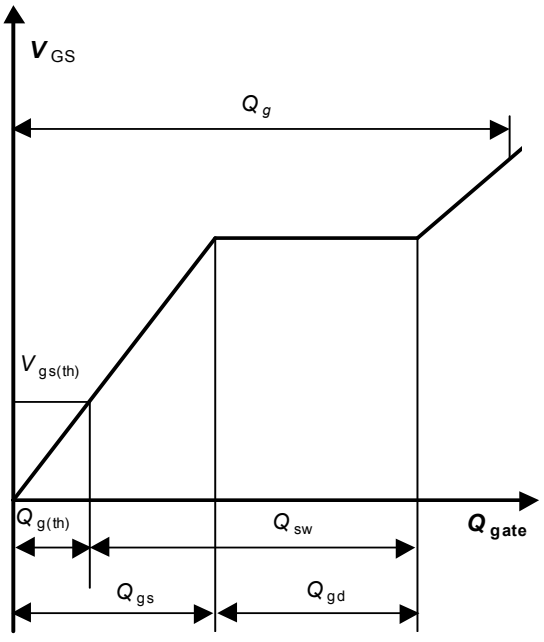


15 Drain-source breakdown voltage

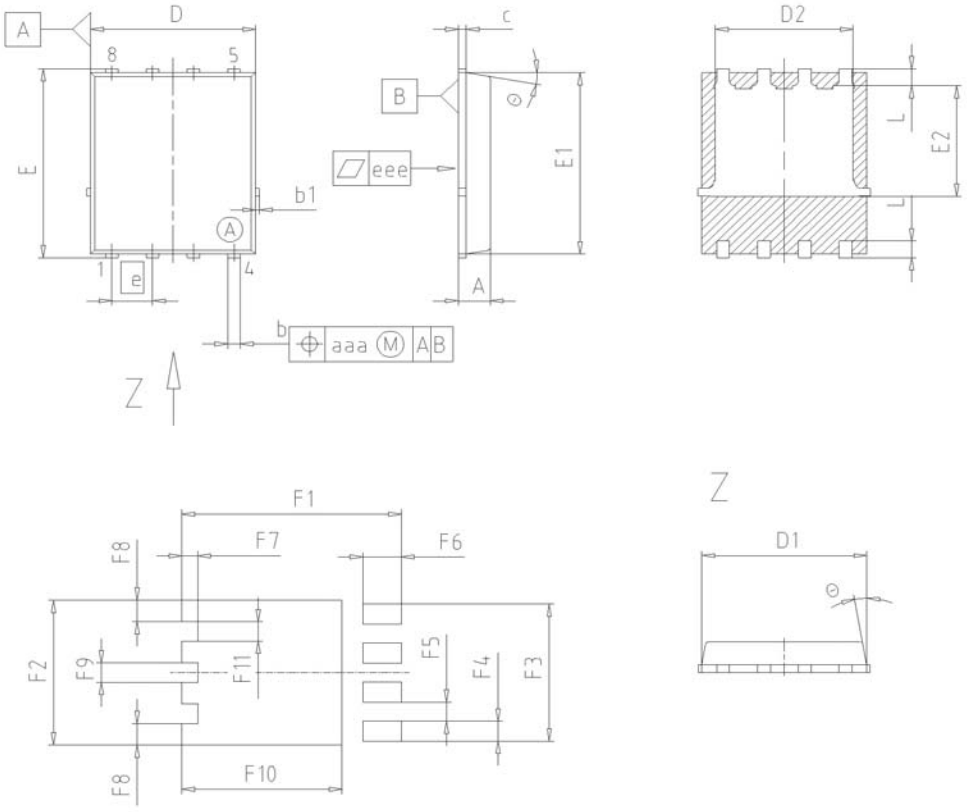
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



Package Outline: PG-TDSON-8

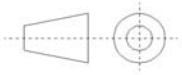


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
N	8		8	
L	0.45	0.65	0.018	0.026
□	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

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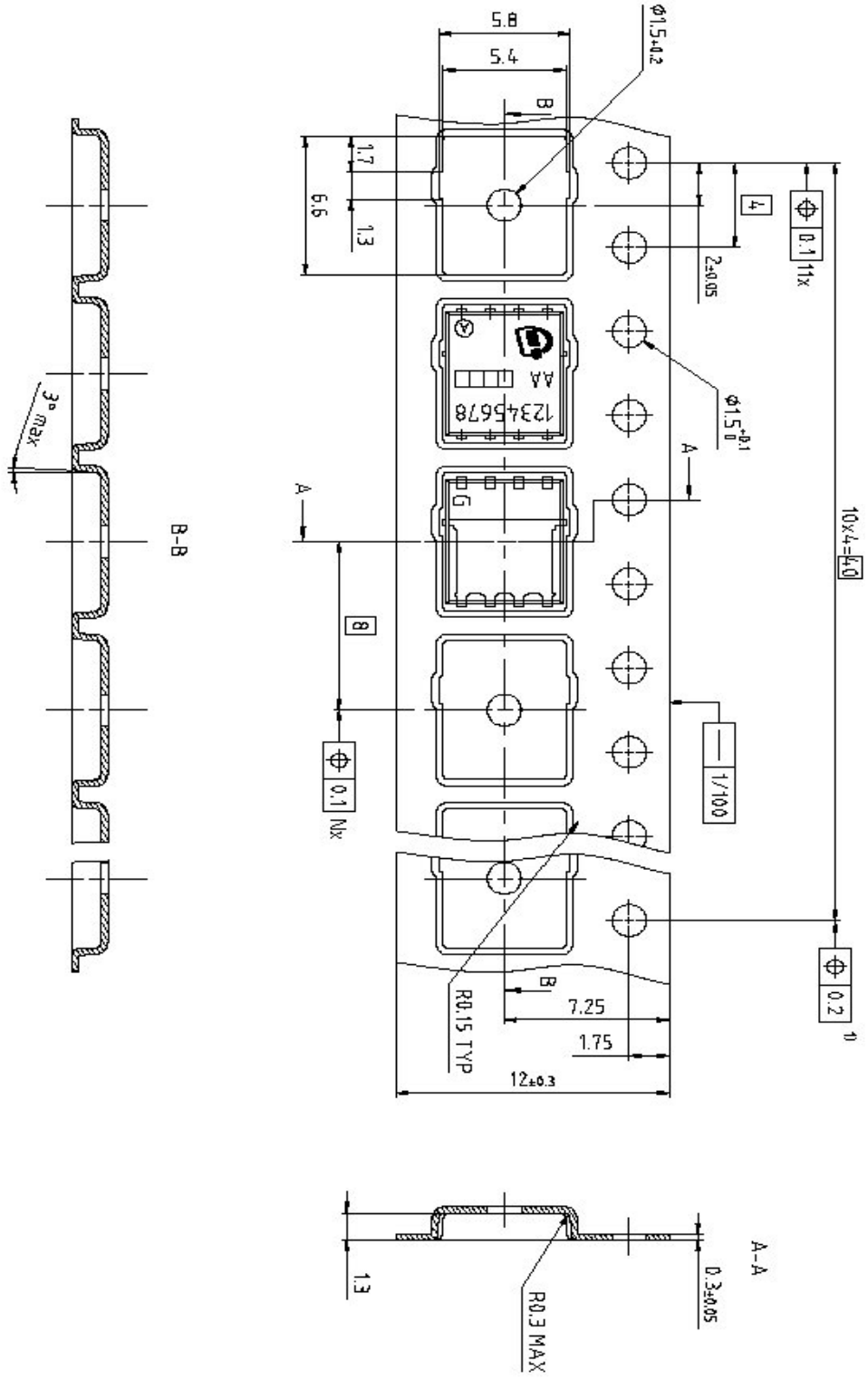
SCALE
0 2.5 0 2.5 5mm

EUROPEAN PROJECTION



ISSUE DATE
08-03-2007

REVISION
03



Dimensions in mm

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Infineon Technologies AG
81726 Munich, Germany
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