48 MHZ USB CLOCK SOURCE

ICS5OSK481

Description

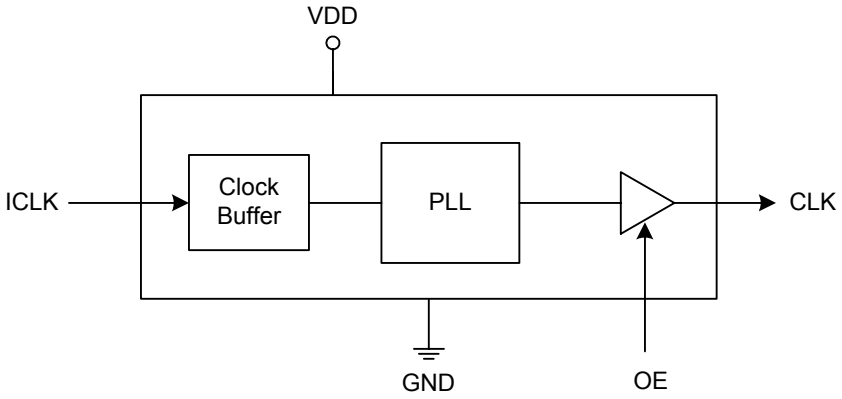
The ICS5OSK481 is a low cost integrated clock synthesizer solution designed for replacing crystals and crystal oscillators.

The ICS5OSK481 generates a very accurate 48.00 MHz clock output.

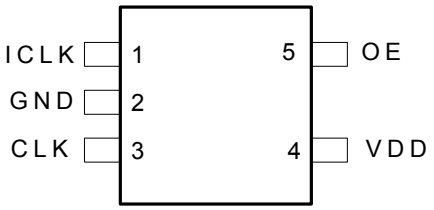
Features

- 25 MHz clock input
- The 48.00 MHz CLK output is USB2.0 reference clock compliant
- Output duty cycle 45/55% (worst case)
- Advanced, low-power CMOS process
- Industrial temperature range (-40 to +85°C)
- Packaged in 5-pin TSOT
- 3.3 V supply voltage
- Pb (lead) free package available
- Short term C-C Jitter of 100 ps

Block Diagram



Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	25 MHz clock input.
2	GND	Power	Connect to ground.
3	CLK	Output	PLL output clock. Internal pull-down resistor.
4	VDD	Power	Connect to 3.3 V.
5	OE	Input	Output Enable pin. Internal pull-up resistor. OE=0 outputs tristate with weak pull-down.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS5OSK481 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS5OSK481. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS5OSK481. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Max Supply Voltage, VDD	7 V
Logic Inputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135	+3.3	+3.465	V

DC Electrical Characteristics

VDD=3.3 V ±5%, Ambient temperature -40 to +85°C, CL = 15 pF, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, ICLK only	V_{IH}	ICLK	VDD/2+1			V
Input Low Voltage, ICLK only	V_{IL}	ICLK			VDD/2-1	V
Input High Voltage	V_{IH}	OE	2.0			V
Input Low Voltage	V_{IL}	OE			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
IDD Operating Supply Current	IDD	No Load		TBD		mA
Short Circuit Current	I_{OS}	CLK output		±50		mA
Internal Pull-up Resistor	R_{PU}	OE		270		kΩ
Input Capacitance, ICLK, OE	C_{IN}	OE, select pins		4		pF
Nominal Output Impedance				20		Ω

AC Electrical Characteristics

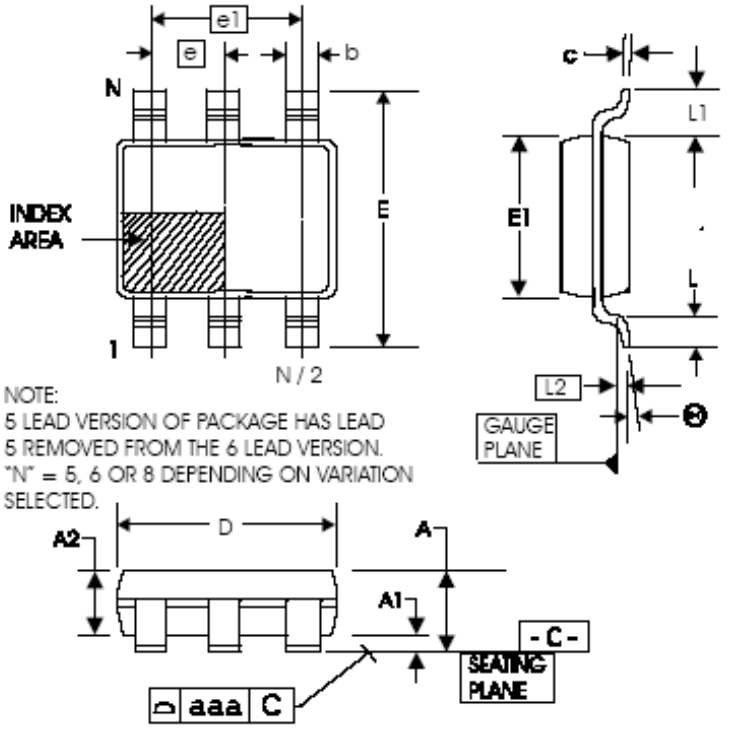
VDD = 3.3 V ±5%, Ambient Temperature -40 to +85°C, CL = 15 pF, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency, clock input	f_{IN}		0.5	25		MHz
Output Frequency	f_{OUT}			48		MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V, Note 1		1		ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V, Note 1		1		ns
Output Clock Duty Cycle	t_{DC}	1.5 V	45	50	60	%
Output Frequency Error				0		ppm
Output Enable Time, OE high to output on				50		ns
Output Disable Time, OE low to tri-state				50		ns
Absolute Clock Period Jitter	t_{JA}	Deviation from mean, Note 1		100		ps

Note 1: Measured with a 15 pF load.

Package Outline and Package Dimensions (5-pin TSOT)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	Min	Max
A	—	1.00
A1	0.01	0.10
A2	0.84	0.90
b	0.30	0.45
c	0.12	0.20
D	2.90 BASIC	
E	2.80 BASIC	
E1	1.60 BASIC	
e	0.95 BASIC	
e1	1.90 BASIC	
L	0.30	0.50
L1	0.60 REF	
L2	0.25 BASIC	
θ	0°	8°
aaa	—	0.10

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS5OSK481TILF	1TIL	Tubes	5-pin TSOT	-40 to +85° C
ICS5OSK481TILFT	1TIL	Tape and Reel	5-pin TSOT	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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