High Efficiency, Main Power Supply Controller for Notebook Computer

General Description

The RT8223P is a dual step-down, switch-mode power supply controller generating logic-supply voltages in battery-powered systems. It includes two Pulse Width Modulation (PWM) controllers adjustable from 2V to 5.5V, and also features fixed 5V/3.3V linear regulators. Each linear regulator provides up to 100mA output current with automatic linear regulator bootstrapping to the PWM outputs. The RT8223P includes on-board power up sequencing, a power good output, internal soft-start, and soft-discharge output that prevents negative voltage during shutdown.

The constant on-time PWM scheme can operate without sense resistors and provide 100ns load transient response while maintaining nearly constant switching frequency. To eliminate noise in audio applications, an ultrasonic mode is included, which maintains the switching frequency above 25kHz. Moreover, the diode-emulation mode maximizes efficiency for light load applications. The RT8223P is available in a WQFN-24L 4x4 package.

Ordering Information

RT8223P □□

Package Type
QW : WQFN-24L 4x4 (W-Type)

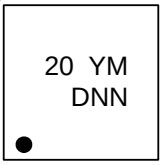
Lead Plating System
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



20 : Product Code

YMDNN : Date Code

Features

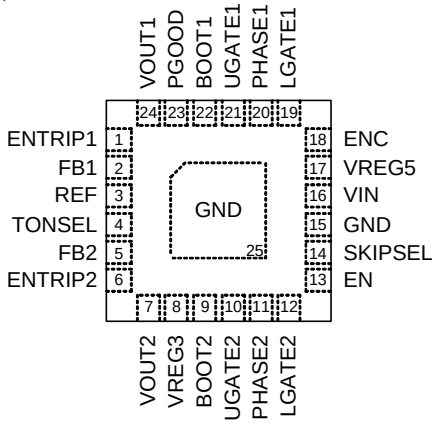
- **Constant On-time Control with 100ns Load Step Response**
- **Wide Input Voltage Range : 6V to 25V**
- **Dual Adjustable Outputs from 2V to 5.5V**
- **Fixed 3.3V and 5V LDO Output : 100mA**
- **2V Reference Voltage**
- **Frequency Selectable via TONSEL Setting**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing**
- **Programmable Current Limit Combined with Enable Control**
- **Selectable PWM, DEM, or Ultrasonic Mode**
- **Internal Soft-Start and Soft-Discharge**
- **High Efficiency up to 97%**
- **5mW Quiescent Power Dissipation**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook and Sub-Notebook Computers
- 3-Cell and 4-Cell Li+ Battery-Powered Devices

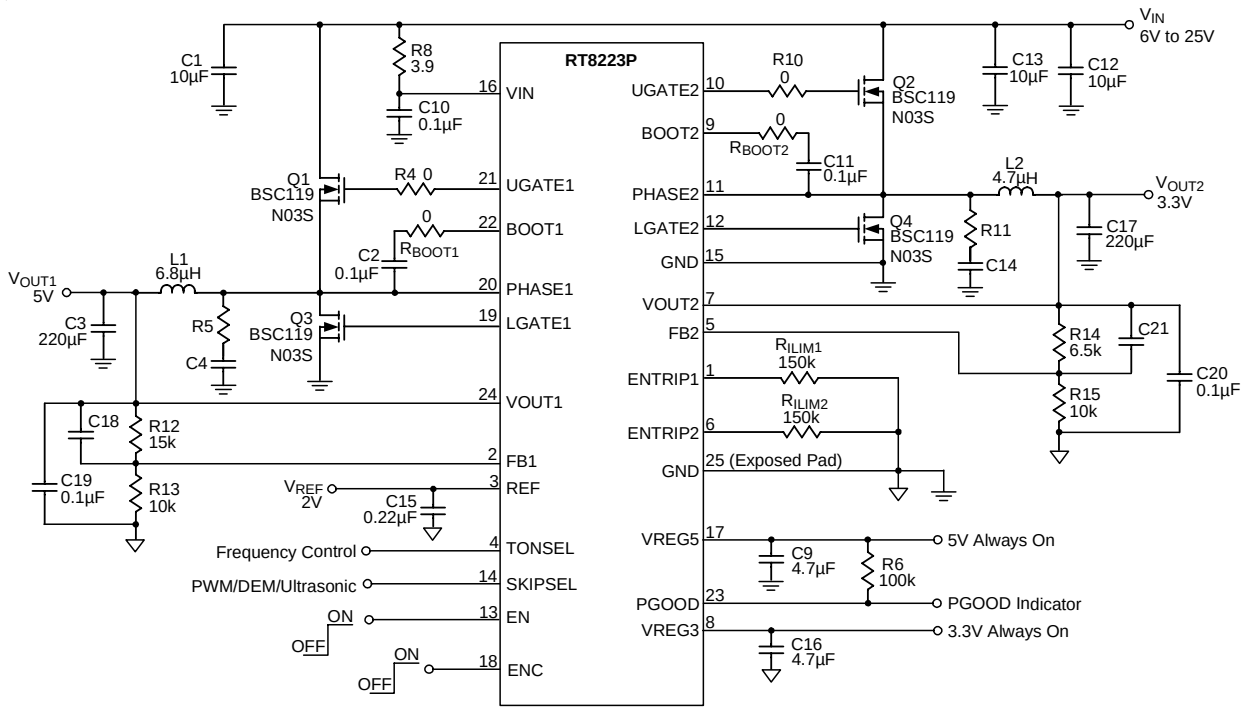
Pin Configurations

(TOP VIEW)



WQFN-24L 4x4

Typical Application Circuit



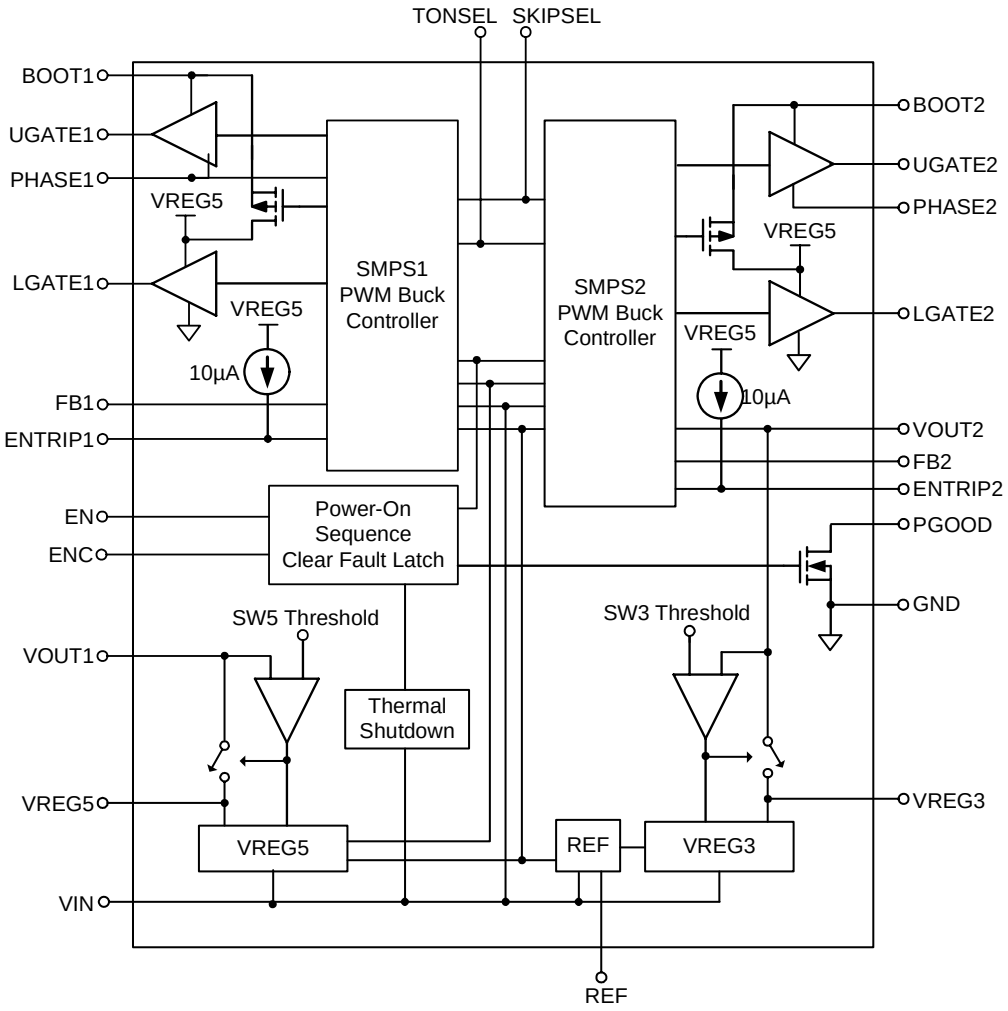
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	ENTRIP1	Channel 1 Enable and Current Limit Setting Input. Connect a resistor to GND to set the threshold for channel 1 synchronous $R_{DS(ON)}$ sense. The GND – PHASE1 current limit threshold is 1/10th the voltage seen at ENTRIP1 over a 0.515V to 3V range. There is an internal 10µA current source from VREG5 to ENTRIP1. Leave ENTRIP1 floating or short ENTRIP1 to GND to shut down channel 1.
2	FB1	SMPS1 Feedback Input. Connect FB1 to a resistive voltage divider from VOUT1 to GND to adjust output from 2V to 5.5V.
3	REF	2V Reference Output. Bypass to GND with a minimum 0.22µF capacitor. REF can source up to 100µA for external loads. Loading REF degrades FBx and output accuracy according to the REF load-regulation error.
4	TONSEL	Frequency Selectable Input for VOUT1/VOUT2 respectively. 400kHz/500kHz : Connect to VREG5 or VREG3 300kHz/375kHz : Connect to REF 200kHz/250kHz : Connect to GND
5	FB2	SMPS2 Feedback Input. Connect FB2 to a resistive voltage divider from VOUT2 to GND to adjust output voltage from 2V to 5.5V.
6	ENTRIP2	Channel 2 Enable and Current Limit Setting Input. Connect a resistor to GND to set the threshold for channel 2 synchronous $R_{DS(ON)}$ sense. The GND – PHASE2 current limit threshold is 1/10th the voltage seen at ENTRIP2 over a 0.515V to 3V range. There is an internal 10µA current source from VREG5 to ENTRIP2. Leave ENTRIP2 floating or short ENTRIP2 to GND to shut down channel 2.
7	VOUT2	Bypass Pin for SMPS2. Connect to the SMPS2 output to bypass efficient power for VREG3 pin. VOUT2 is also for the SMPS2 output soft-discharge.
8	VREG3	3.3V Linear Regulator Output.

To be continued

Pin No.	Pin Name	Pin Function
9	BOOT2	Boost Flying Capacitor Connection for SMPS2. Connect to an external capacitor according to the typical application circuits.
10	UGATE2	Upper Gate Driver Output for SMPS2. UGATE2 swings between PHASE2 and BOOT2.
11	PHASE2	Switch Node for SMPS2. PHASE2 is the internal lower supply rail for the UGATE2 high side gate driver. PHASE2 is also the current-sense input for the SMPS2.
12	LGATE2	Lower Gate Driver Output for SMPS2. LGATE2 swings between GND and VREG5.
13	EN	Master Enable Input. The REF/VREG5/VREG3 are enabled if it is within logic high level and disabled if it is less than the logic low level.
14	SKIPSEL	Operation Mode Selectable Input. Connect to VREG5 or VREG3 : Ultrasonic Mode Connect to REF : PWM Mode Connect to GND : DEM Mode
16	VIN	Supply Input for 5V/3.3V LDO and Feed Forward On-Time circuitry.
17	VREG5	5V Linear Regulator Output. VREG5 is also the supply voltage for the lower gate driver and analog supply voltage for the device.
18	ENC	SMPS Enable Input. Pull up to VREG3 or VREG5 to turn on both switch channels. Short to GND to shutdown them.
19	LGATE1	Lower Gate Driver Output for SMPS1. LGATE1 swings between GND and VREG5.
20	PHASE1	Switch Node for SMPS1. PHASE1 is the internal lower supply rail for the UGATE1 high side gate driver. PHASE1 is also the current-sense input for the SMPS1.
21	UGATE1	Upper Gate Driver Output for SMPS1. UGATE1 swings between PHASE1 and BOOT1.
22	BOOT1	Boost Flying Capacitor Connection for SMPS1. Connect to an external capacitor according to the typical application circuits.
23	PGOOD	Power Good Output for Channel 1 and Channel 2. (Logical AND).
24	VOUT1	Bypass Pin for SMPS1. Connect to the SMPS1 output to bypass efficient power for VREG5 pin. VOUT1 is also for the SMPS1 output soft-discharge.
15, 25 (Exposed Pad)	GND	Ground for SMPS Controller. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN, EN to GND ---------- –0.3V to 30V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - < 20ns ---------- –8V to 38V
- BOOTx to PHASEx ---------- –0.3V to 6V
- ENTRIPx, SKIPSEL, TONSEL, PGOOD to GND ---------- –0.3V to 6V
- VREG5, VREG3, FBx, VOUTx, ENC, REF to GND ---------- –0.3V to 6V
- UGATEx to PHASEx
  - DC ---------- –0.3V to (VREG5 + 0.3V)
  - < 20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to (VREG5 + 0.3V)
  - < 20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-24L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 2)
  - WQFN-24L 4x4, θ_{JA} ---------- 52°C/W
  - WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 6V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{EN} = V_{ENC} = 5V, $V_{ENTRIP1}$ = $V_{ENTRIP2}$ = 2V, No Load, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Supply							
VIN Standby Current	I_{VIN_SBY}	V_{IN} = 6V to 25V, ENTRIPx = GND		--	200	--	μA
VIN Shutdown Supply Current	I_{VIN_SHDN}	V_{IN} = 6V to 25V, ENTRIPx = EN = GND		--	20	40	μA
Quiescent Power Consumption	P_{VIN} +P_{PVCC}	Both SMPS On, V_{FBx} = 2.1V, SKIPSEL = GND, V_{OUT1} = 5V, V_{OUT2} = 3.3V (Note 5)		--	5	7	mW
SMPS Output and FB Voltage							
FBx Voltage	V_{FBx}	DEM Mode		1.975	2	2.025	V
		PWM Mode (Note 6)		--	2	--	
		Ultrasonic Mode		--	2.032	--	
Output Voltage Adjust Range	V_{OUTx}	SMPS1, SMPS2		2	--	5.5	V
V_{OUTx} Discharge Current		V_{OUTx} = 0.5V, $V_{ENTRIPx}$ = 0V		10	45	--	mA
On-Time							
On-Time Pulse Width	t_{ON}	TONSEL = GND	V_{OUT1} = 5.05V (200kHz)	1895	2105	2315	ns
			V_{OUT2} = 3.33V (250kHz)	999	1110	1221	
		TONSEL = REF	V_{OUT1} = 5.05V (300kHz)	1227	1403	1579	
			V_{OUT2} = 3.33V (375kHz)	647	740	833	
		TONSEL = REG5	V_{OUT1} = 5.05V (400kHz)	895	1052	1209	
			V_{OUT2} = 3.33V (500kHz)	475	555	635	
Minimum Off-Time	t_{OFF}	V_{FBx} = 1.9V		200	300	400	ns
Ultrasonic Mode Frequency		SKIPSEL = VREG5 or VREG3		22	33	--	kHz
Soft-Start							
Soft-Start Time	t_{SSx}	Internal Soft-Start		--	2	--	ms
Current Sense							
ENTRIPx Source Current	$I_{ENTRIPx}$	$V_{ENTRIPx}$ = 0.9V		9.4	10	10.6	μA
ENTRIPx Current Temperature Coefficient	$TC_{IENTRIPx}$	In Comparison with 25°C (Note 6)		--	4700	--	ppm/°C
ENTRIPx Adjustment Range		$V_{ENTRIPx}$ = $I_{ENTRIPx}$ x $R_{ENTRIPx}$		0.515	--	3	V
Current Limit Threshold		GND – PHASEx, $V_{ENTRIPx}$ = 2V		180	200	220	mV
Zero-Current Threshold		GND – PHASEx in DEM		--	3	--	mV

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Regulator and Reference						
VREG5 Output Voltage	V_{VREG5}	V_{OUT1} = GND, I_{VREG5} < 100mA	4.8	5	5.2	V
		V_{OUT1} = GND, 6.5V < V_{IN} < 25V, I_{VREG5} < 100mA	4.75	5	5.25	
		V_{OUT1} = GND, 5.5V < V_{IN} < 25V, I_{VREG5} < 50mA	4.75	5	5.25	
VREG3 Output Voltage	V_{VREG3}	V_{OUT2} = GND, I_{VREG3} < 100mA	3.2	3.33	3.46	V
		V_{OUT2} = GND, 6.5V < V_{IN} < 25V, I_{VREG3} < 100mA	3.13	3.33	3.5	
		V_{OUT2} = GND, 5.5V < V_{IN} < 25V, I_{VREG3} < 50mA	3.13	3.33	3.5	
VREG5 Output Current	I_{VREG5}	V_{VREG5} = 4.5V, V_{OUT1} = GND	100	175	250	mA
VREG3 Output Current	I_{VREG3}	V_{VREG3} = 3V, V_{OUT2} = GND	100	175	250	mA
VREG5 Switch-over Threshold to V_{OUT1}	V_{SW5}	V_{OUT1} Rising Edge	4.6	4.75	4.9	V
		V_{OUT1} Falling Edge	4.3	4.4	4.5	
VREG3 Switch-over Threshold to V_{OUT2}	V_{SW3}	V_{OUT2} Rising Edge	2.975	3.125	3.25	V
		V_{OUT2} Falling Edge	2.775	2.875	2.975	
VREGx Switch-over Equivalent Resistance	R_{SWx}	VREGx to V_{OUTx}, 10mA	--	1.5	3	Ω
REF Output Voltage	V_{REF}	No External Load	1.98	2	2.02	V
REF Load Regulation		0 < I_{LOAD} < 100μA	--	10	--	mV
REF Sink Current		REF in Regulation	5	--	--	μA
UVLO						
VREG5 Under Voltage Lockout Threshold		Rising Edge	--	4.2	4.45	V
		Falling Edge	3.7	3.9	4.1	
VREG3 Under Voltage Lockout Threshold		SMPSx off	--	2.5	--	V
Power Good						
PGOOD Threshold		PGOOD Detect, FBx falling Edge	82	85	88	%
		Hysteresis, Rising Edge with SS Delay Time	--	6	--	
PGOOD Propagation Delay		Falling Edge, 50mV Overdrive	--	10	--	μs
PGOOD Leakage Current		High State, Forced to 5.5V	--	--	1	μA
PGOOD Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
Fault Detection						
Over Voltage Protection Trip Threshold	V_{FB_OVP}	OVP Detect, FBx Rising Edge	109	112	116	%
Over Voltage Protection Propagation Delay		FBx = 2.35V	--	5	--	μs
Under Voltage Protection Trip Threshold	V_{FB_UVP}	UVP Detect, FBx Falling Edge	49	52	56	%

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Shutdown Blanking Time		t_{SHDN_UVP}	From ENTRIPx Enable	--	5	--	ms
Thermal Shutdown							
Thermal Shutdown		T_{SHDN}		--	150	--	°C
Thermal Shutdown Hysteresis				--	10	--	°C
Logic Input							
SKIPSEL Input Voltage			Low Level (DEM Mode)	--	--	0.8	V
			REF Level (PWM Mode)	1.8	--	2.3	
			High Level (Ultrasonic Mode)	2.7	--	--	
ENTRIPx Input Voltage		$V_{ENTRIPx}$	Low Level (SMPS Off)	--	--	0.25	V
			On Level (SMPS On)	0.515	--	3	
			High Level (SMPS Off)	4.5	--	--	
ENTRIPx Low Level Threshold			Rising Edge	--	0.4	0.515	V
			Falling Edge	0.25	0.36	--	
EN Threshold Voltage	Logic-High	V_{IH}		2.4	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
EN Voltage		V_{EN}	Floating, Default Enable	2.4	3.3	4.2	V
EN Current		I_{EN}	V_{EN} = 0.2V, Source	1.5	3	5	μA
			V_{EN} = 5V, Sink	--	3	8	
ENC Threshold Voltage	Logic-High	V_{IH_ENC}		2	--	--	V
	Logic-Low	V_{IL_ENC}		--	--	0.6	
TONSEL Setting Voltage			V_{OUT1} / V_{OUT2} = 200kHz/250kHz	--	--	0.8	V
			V_{OUT1} / V_{OUT2} = 300kHz/375kHz	1.8	--	2.3	
			V_{OUT1} / V_{OUT2} = 400kHz/500kHz	2.7	--	--	
Input Leakage Current			V_{TONSEL}, $V_{SKIPSEL}$ = 0V or 5V	–1	--	1	μA
			V_{ENC} = 0V or 5V	–1	--	1	
Internal BOOT Switch							
Internal Boost Switch On-Resistance			VREG5 to BOOTx, 10mA	--	40	80	Ω
Power MOSFET Drivers							
UGATEx On-Resistance			UGATEx, High State, BOOTx to PHASEx Forced to 5V	--	4	8	Ω
			UGATEx, Low State, BOOTx to PHASEx Forced to 5V	--	1.5	4	
LGATEx On-Resistance			LGATEx, High State	--	4	8	Ω
			LGATEx, Low State	--	1.5	4	
Dead Time			LGATEx Rising	--	30	--	ns
			UGATEx Rising	--	40	--	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

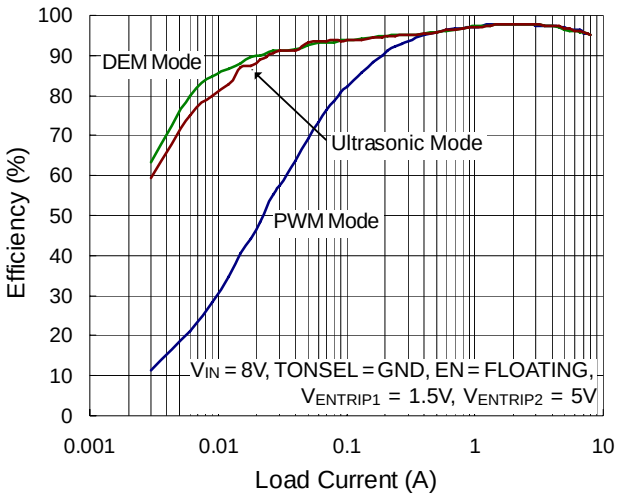
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. $P_{VIN} + P_{VREG5}$

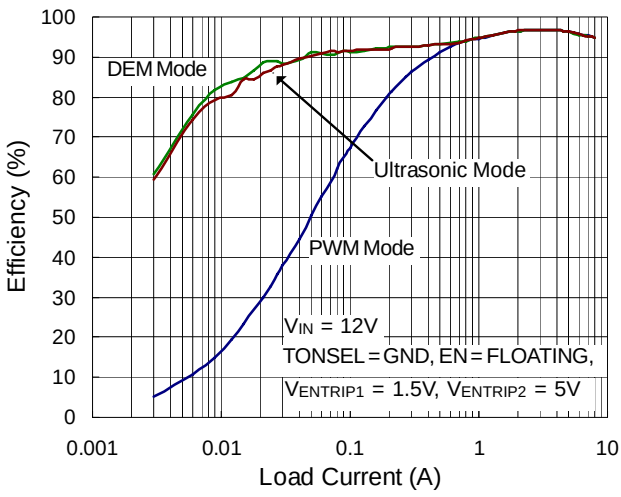
Note 6. Guaranteed by Design.

Typical Operating Characteristics

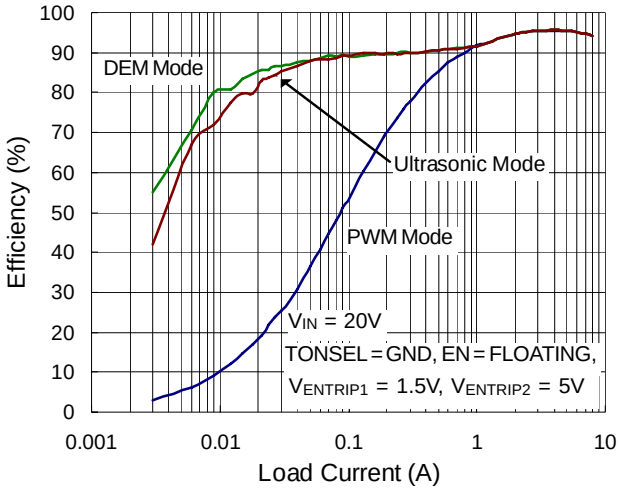
VOUT1 Efficiency vs. Load Current



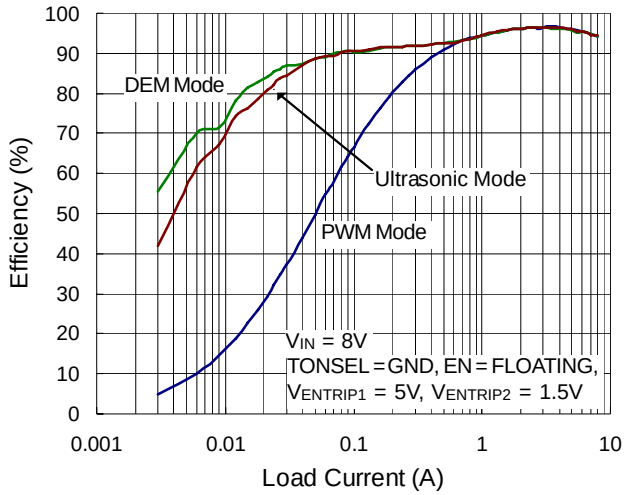
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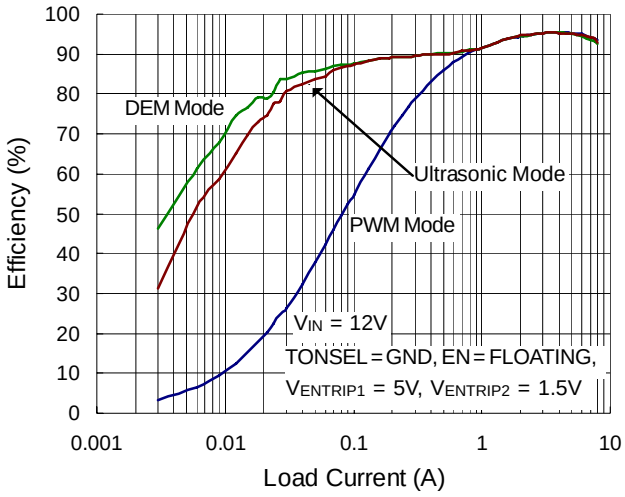
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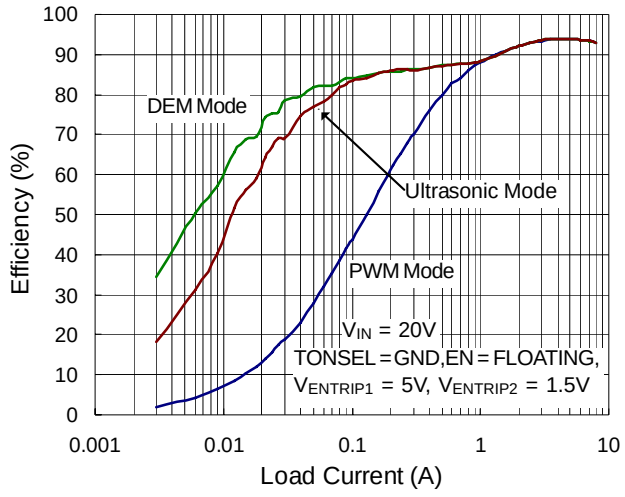
VOUT2 Efficiency vs. Load Current



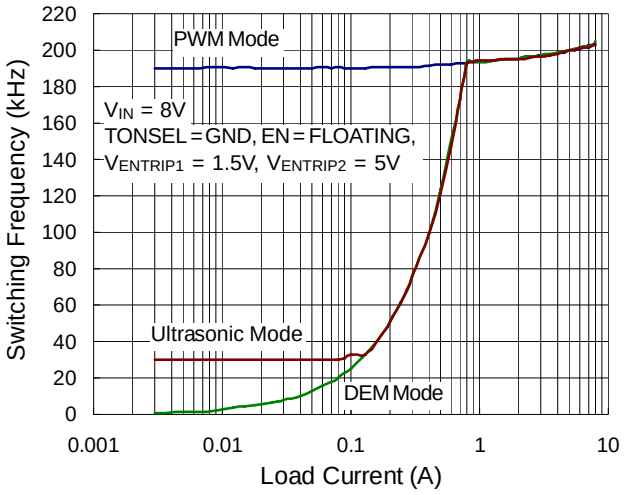
VOUT2 Efficiency vs. Load Current



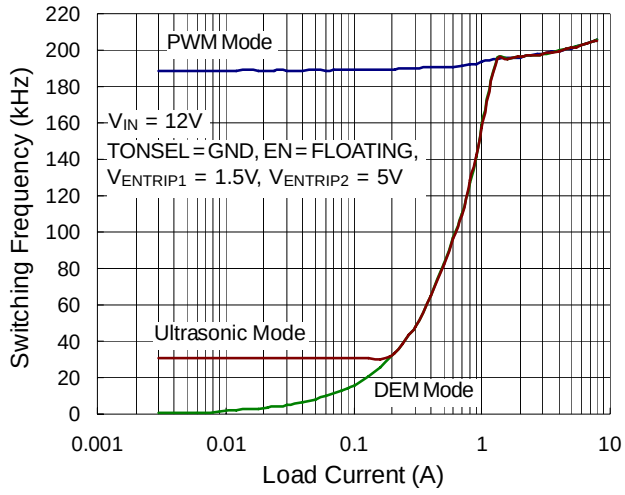
VOUT2 Efficiency vs. Load Current



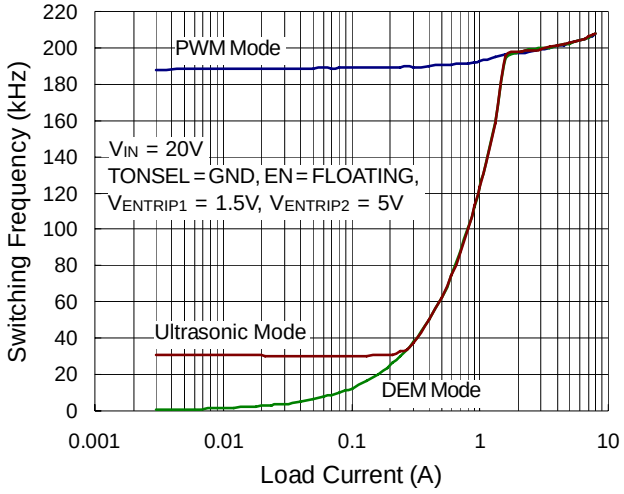
VOUT1 Switching Frequency vs. Load Current



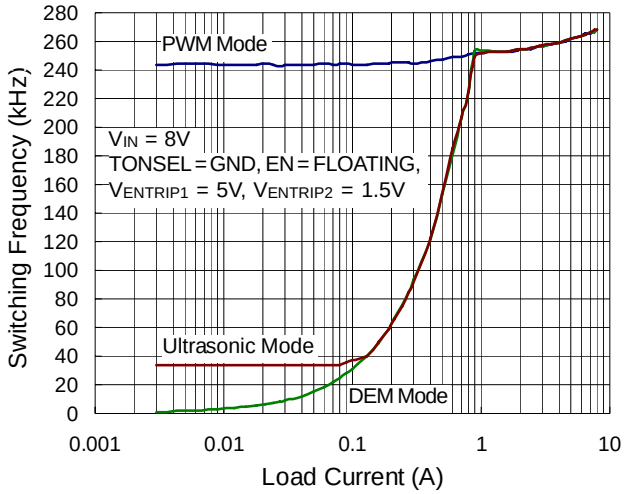
VOUT1 Switching Frequency vs. Load Current



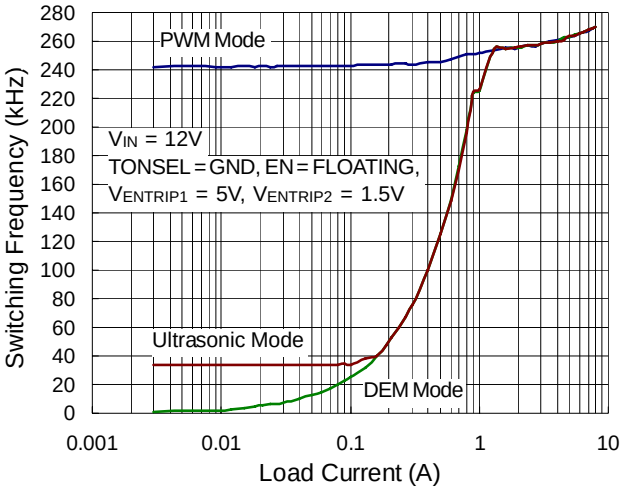
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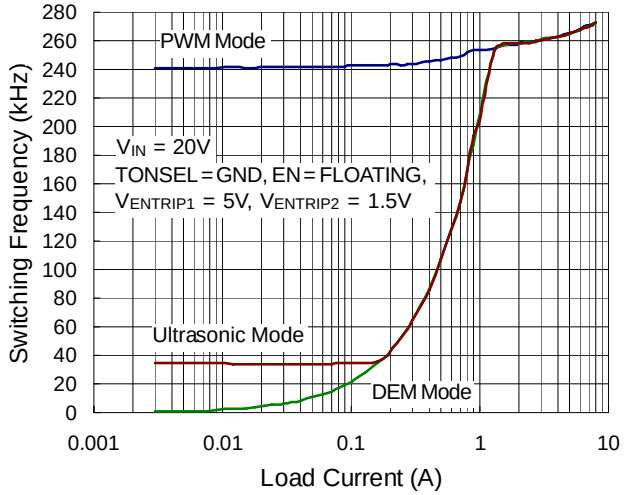
VOUT2 Switching Frequency vs. Load Current



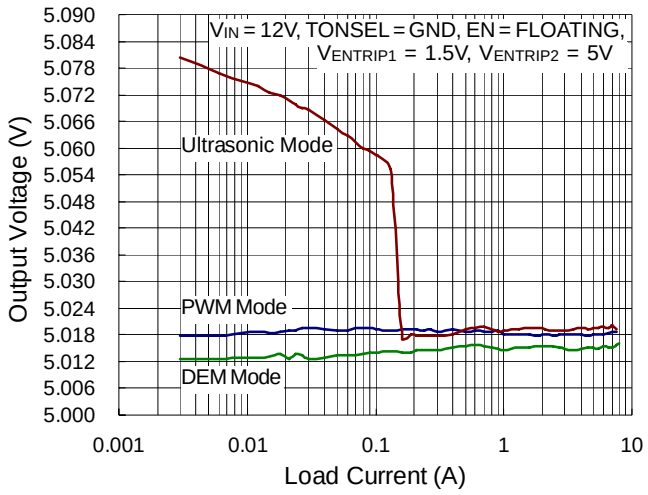
VOUT2 Switching Frequency vs. Load Current



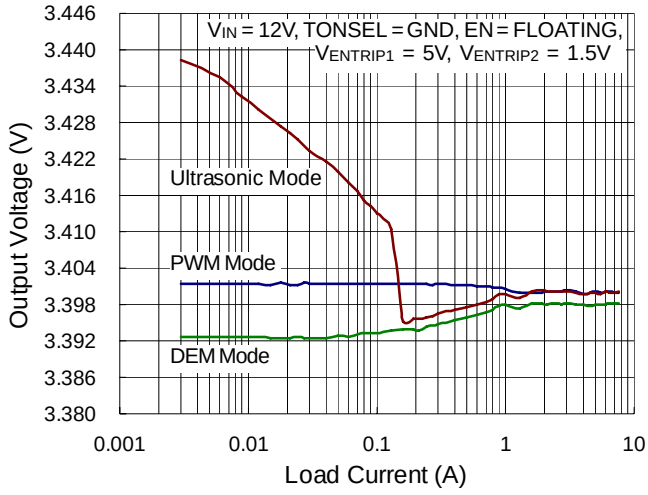
VOUT2 Switching Frequency vs. Load Current



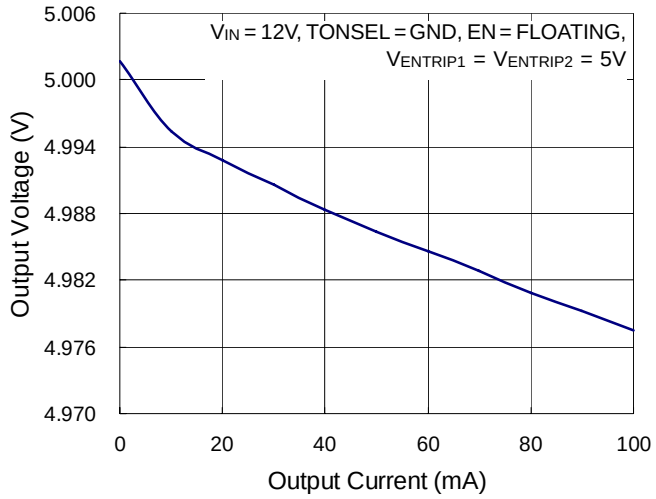
VOUT1 Output Voltage vs. Load Current



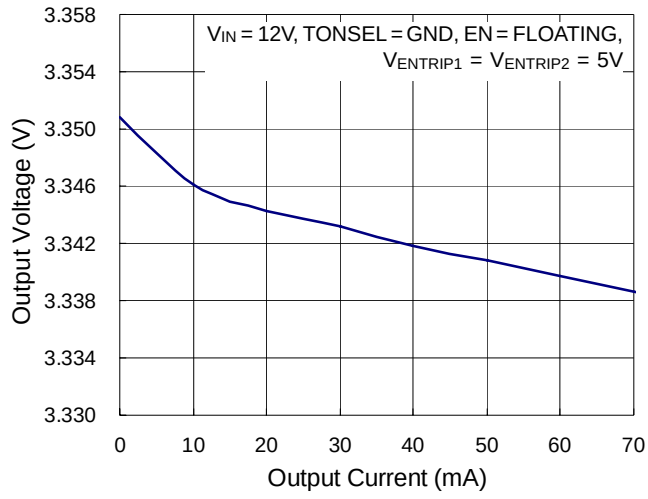
VOUT2 Output Voltage vs. Load Current



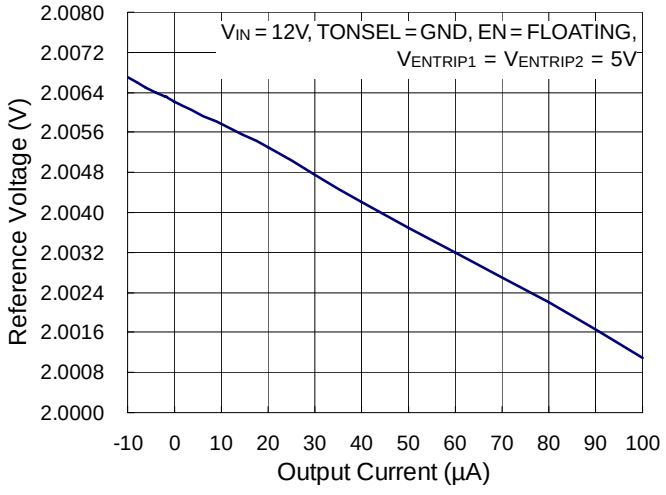
VREG5 Output Voltage vs. Output Current



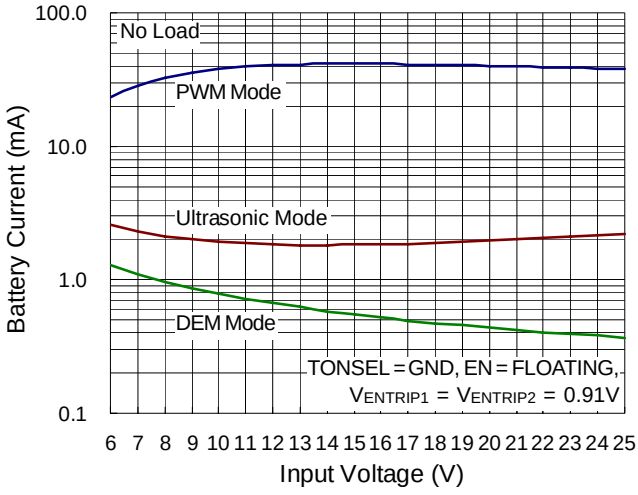
VREG3 Output Voltage vs. Output Current



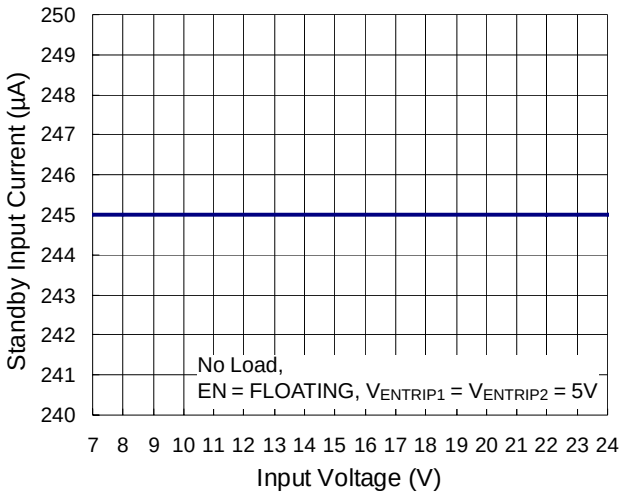
Reference Voltage vs. Output Current



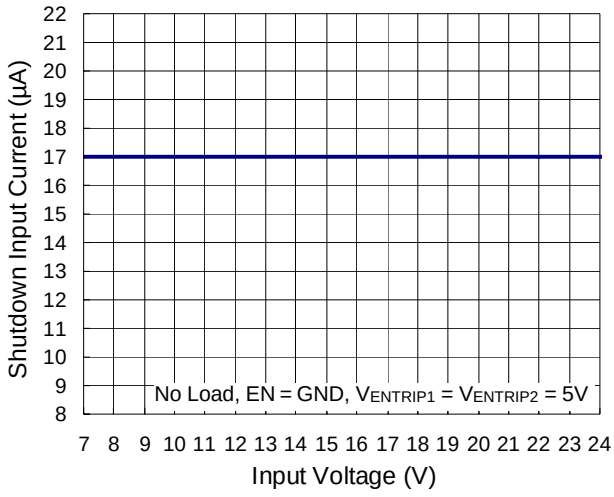
Battery Current vs. Input Voltage



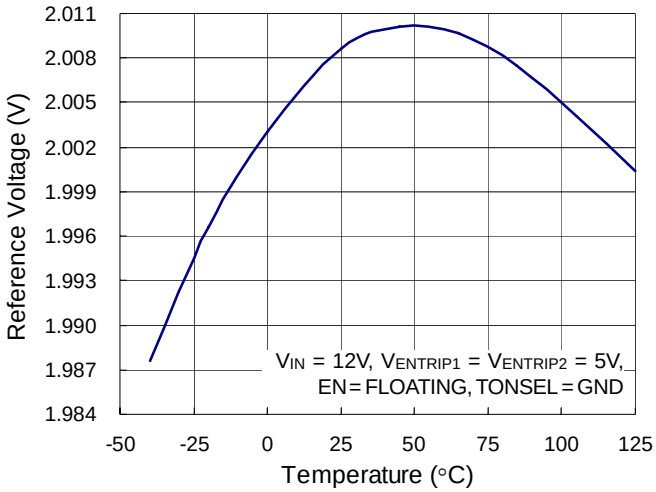
Standby Input Current vs. Input Voltage



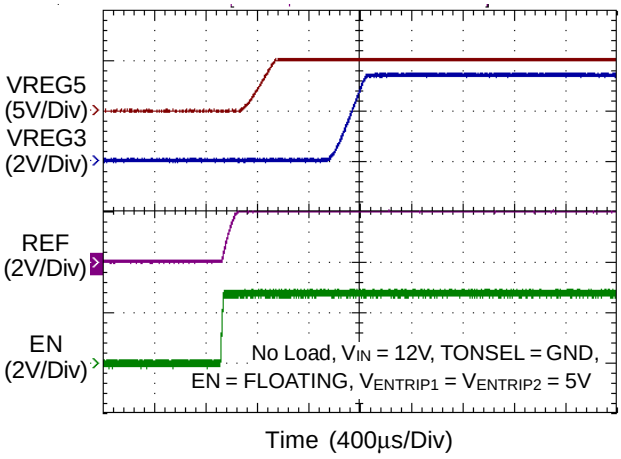
Shutdown Input Current vs. Input Voltage



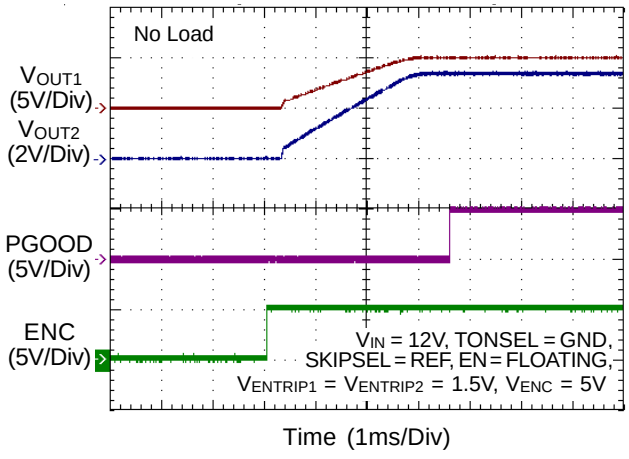
Reference Voltage vs. Temperature



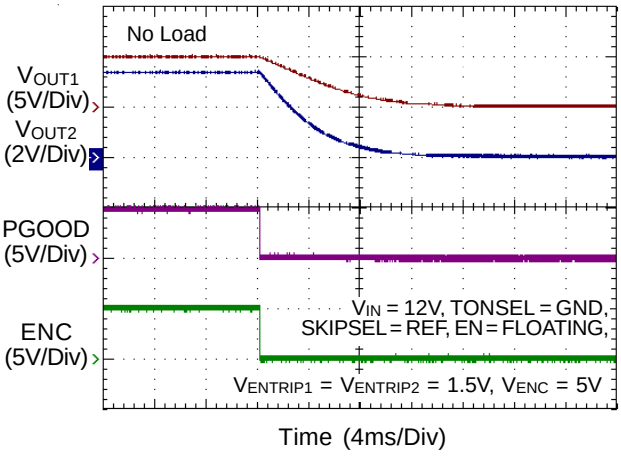
VREG5, VREG3 and REF Start Up



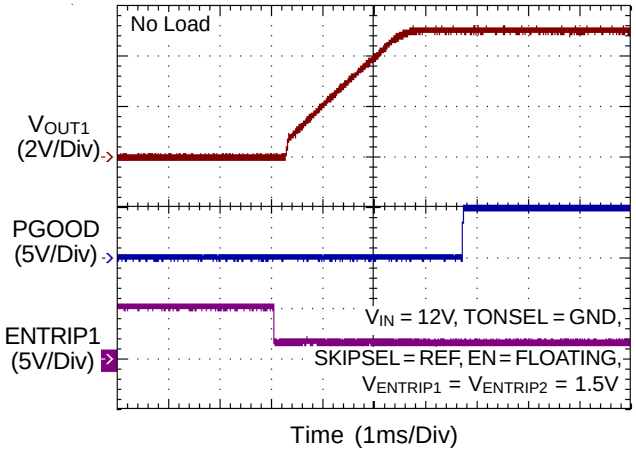
Power On From ENC



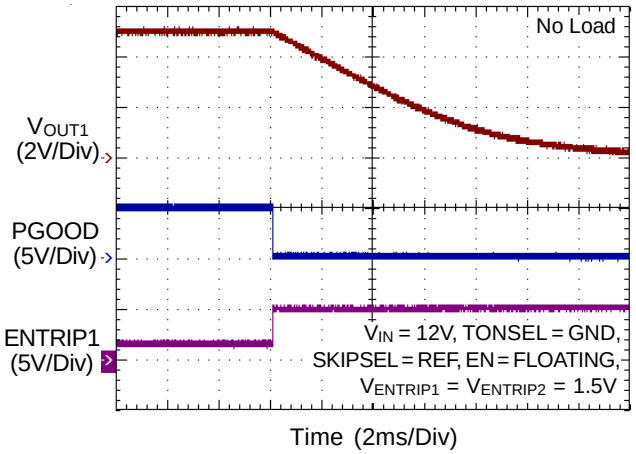
Power Off From ENC



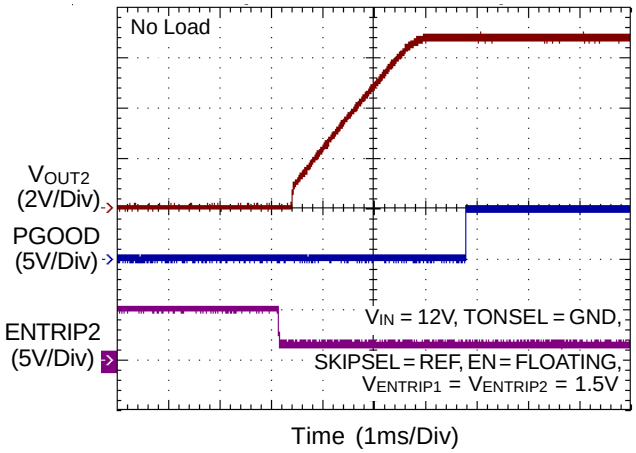
Power On from ENTRIP1



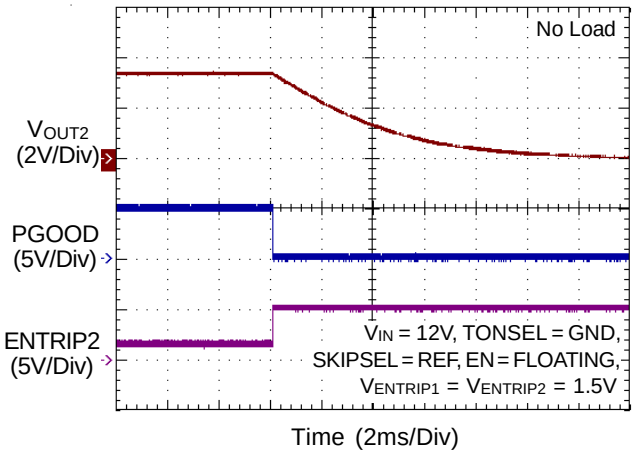
Power Off from ENTRIP1



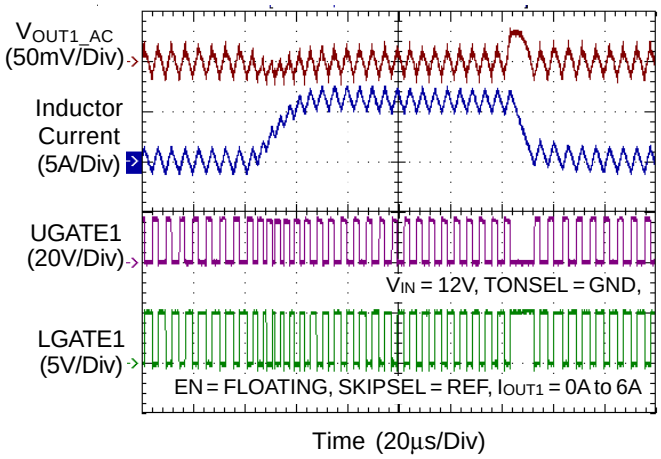
Power On from ENTRIP2



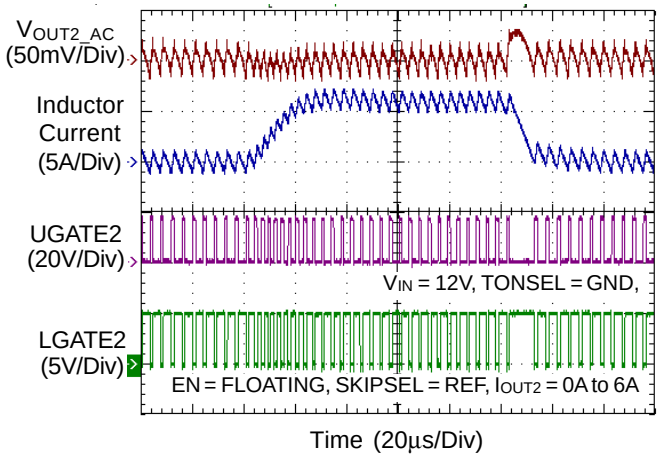
Power Off from ENTRIP2



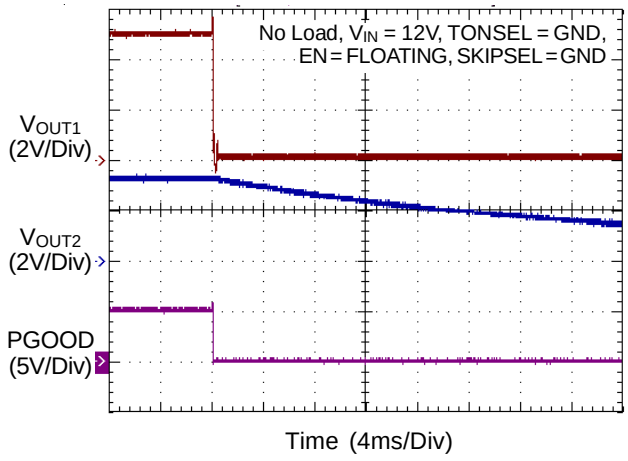
VOUT1 PWM Mode Load Transient Response



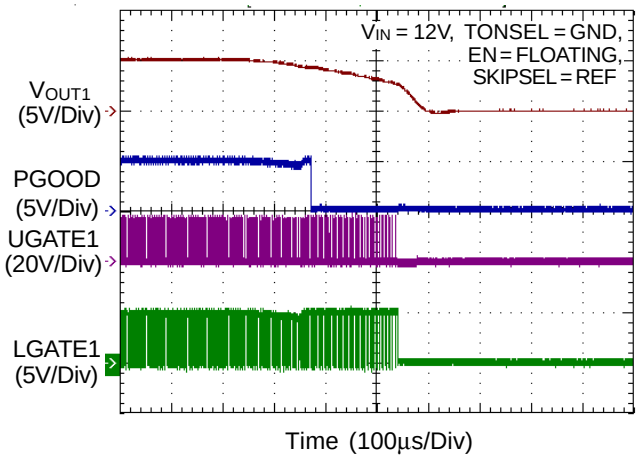
VOUT2 PWM Mode Load Transient Response



OVP


No Load, VIN = 12V, TONSEL = GND,
EN = FLOATING, SKIPSEL = GND
VOUT1
(2V/Div)
VOUT2
(2V/Div)
PGOOD
(5V/Div)
Time (4ms/Div)

UVP


VIN = 12V, TONSEL = GND,
EN = FLOATING,
SKIPSEL = REF
VOUT1
(5V/Div)
PGOOD
(5V/Div)
UGATE1
(20V/Div)
LGATE1
(5V/Div)
Time (100µs/Div)

Application Information

The RT8223P is a dual, Mach Response™ DRV™ dual ramp valley mode synchronous buck controller. The controller is designed for low voltage power supplies for notebook computers. Richtek's Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load-transient timing problems of fixed-frequency current mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a dual output application. The RT8223P includes 5V (VREG5) and 3.3V (VREG3) linear regulators. VREG5 linear regulator can step down the battery voltage to supply both internal circuitry and gate drivers. The synchronous-switch gate drivers are directly powered from VREG5. When VOUT1 voltage is above 4.75V, an automatic circuit will switch the power of the device from VREG5 linear regulator to VOUT1.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the RT8223P's function block diagram, the synchronous high side MOSFET will be turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range. Another one shot sets a minimum off-time (300ns typ.). The on-time one shot will be triggered if the error comparator is high, the low side switch current is below the current limit threshold, and the minimum off-time one shot has timed out.

PWM Frequency and On-Time Control

The Mach Response™ control architecture runs with pseudo constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The high side switch on-time is inversely proportional to the input voltage as measured by V_{IN}, and proportional to the output voltage. There are two benefits of a constant switching frequency. First, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band. Second, the inductor ripple current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. Frequency for the 3V SMPS is set at 1.25 times higher than the frequency for 5V SMPS. This is done to prevent audio-frequency "Beating" between the two sides, which switch asynchronously for each side. The frequencies are set by the TONSEL pin connection as shown in Table 1. The on-time is given by :

$$t_{ON} = K \times (V_{OUT} / V_{IN})$$

where "K" is set by the TONSEL pin connection (Table 1). The on-time guaranteed in the Electrical Characteristics table is influenced by switching delays in the external high side power MOSFET. Two external factors that influence switching frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead time effect. These effects are the largest contributors to the change in frequency with changing load current. The dead-time effect increases the effective on-time by reducing the switching frequency. It occurs only in PWM mode (SKIPSEL= REF) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes PHASEx to go high earlier than normal, thus extending the on-time by a period equal to the low-to-high dead time. For loads above the critical conduction point, the actual switching frequency is :

$$f = (V_{OUT} + V_{DROP1}) / (t_{ON} \times (V_{IN} + V_{DROP1} - V_{DROP2}))$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, which includes the synchronous rectifier, inductor, and PC board resistances. V_{DROP2} is the sum of the resistances in the charging path, and t_{ON} is the on-time.

Table 1. TONSEL Connection and Switching Frequency

TONSEL	SMPS 1 K-Factor (μs)	SMPS 1 Frequency (kHz)	SMPS 2 K-Factor (μs)	SMPS 2 Frequency (kHz)	Approximate K-Factor Error (%)
GND	5	200	4	250	±10
REF	3.33	300	2.67	375	±10
VREG5 or VREG3	2.5	400	2	500	±10

Operation Mode Selection (SKIPSEL)

The RT8223P supports three operation modes : Diode-Emulation Mode, Ultrasonic Mode, and Forced-CCM Mode. User can set operation mode via the SKIPSEL pin.

Diode-Emulation Mode (SKIPSEL=GND)

In Diode-Emulation Mode, the RT8223P automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy-load condition, the inductor current is also reduced and eventually comes to the point when its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current when the inductor free-wheeling current becomes negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy-load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light-load operation is shown as follows (Figure 1) :

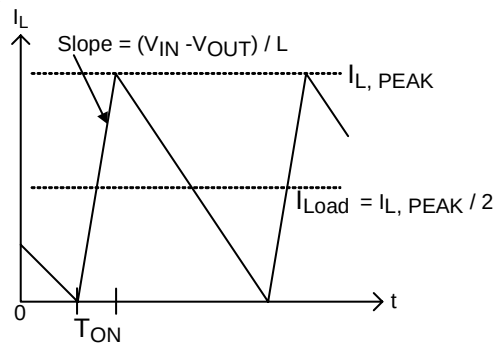


Figure 1. Boundary Condition of CCM/DEM

$$I_{LOAD\ (SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the On-time.

The switching waveforms may appear noisy and asynchronous when light loading causes Diode-Emulation Mode operation. However this is normal and results in high efficiency. Trade-offs in PFM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple.

Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input-voltage levels).

Ultrasonic Mode (SKIPSEL = VREG5 or VREG3)

The RT8223P activates an unique Diode-Emulation Mode with a minimum switching frequency of 25kHz, called the Ultrasonic Mode. The Ultrasonic Mode avoids audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In Ultrasonic Mode, the high side switch gate driver signal is OR with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the controller enters constant off-time control. When output voltage reaches the setting peak threshold, the controller turns on the low side MOSFET until the controller detects that the inductor current dropped has below the zero-crossing threshold. The internal timer provides a constant off-time control and it is effective to regulate the output voltage under light load conditions.

Forced CCM Mode (SKIPSEL = REF)

The low noise, Forced CCM mode (SKIPSEL = REF) disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate-driver waveform to become the complement of the high side gate-driver waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio of V_{OUT}/V_{IN}. The benefit of Forced CCM Mode is to keep the switching frequency fairly constant, but it comes at a cost. The no load battery current can be from 10mA to 40mA, depending on the external MOSFETs.

Reference and linear Regulators (REF, VREGx)

The 2V reference (REF) is accurate within ±1% over the entire operating temperature range, making REF useful as a precision system reference. Bypass REF to GND with a minimum 0.22µF ceramic capacitor. REF can supply up to 100µA for external loads. Loading REF reduces the VOUTx output voltage slightly because of the reference load-regulation error.

The RT8223P includes 5V (VREG5) and 3.3V (VREG3) linear regulators. The VREG5 regulator supplies a total of 100mA for internal and external loads, including the MOSFET gate driver and PWM controller. The VREG3 regulator supplies up to 100mA for external loads. Bypass VREG5 and VREG3 with a minimum 4.7µF ceramic capacitor.

When the 5V main output voltage is above the VREG5 switch over threshold (4.75V), an internal 1.5Ω P-Channel MOSFET switch connects VOUT1 to VREG5, while simultaneously shutting down the VREG5 linear regulator. Similarly, when the 3.3V main output voltage is above the VREG3 switch over threshold (3.125V), an internal 1.5Ω P-Channel MOSFET switch connects VOUT2 to VREG3, while simultaneously shutting down the VREG3 linear regulator. It can decrease the power dissipation from the same battery, because the converted efficiency of SMPS is better than the converted efficiency of the linear regulator.

Current-Limit Setting (ENTRIPx)

The RT8223P has a cycle-by-cycle current-limit control. The current-limit circuit employs an unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASEx is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are functions of the sense resistance, inductor value, and battery and output voltage.

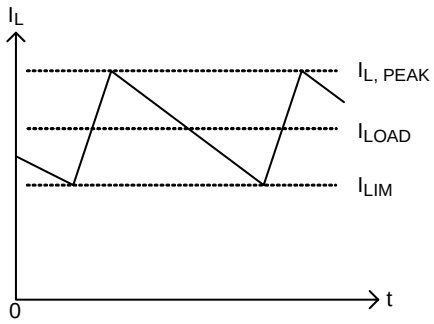


Figure 2. "Valley" Current-Limit

The RT8223P uses the on-resistance of the synchronous rectifier as the current-sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The R_{ILIMX} resistor between the $ENTRIP_X$ pin and GND sets the current-limit threshold. The resistor R_{ILIMX} is connected to a current source from ENTRIPx, which is 10µA typically at room temperature. The current source has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across the sense resistor or low side MOSFET equals 1/10 the voltage across the R_{ILIMX} resistor, positive current limit will be activated. The high side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/10 the voltage across the R_{ILIMX} resistor.

Choose a current limit resistor by following equations

$V_{ILIMx} = (R_{ILIMx} \times 10\mu A)/10 = I_{ILIMx} \times R_{DS(ON)}$

$R_{ILIMx} = (I_{ILIMx} \times R_{DS(ON)}) \times 10/10\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal at PHASEx and GND. Mount or place the IC close to the low side MOSFET.

MOSFET Gate Driver (UGATEx, LGATEx)

The high side driver is designed to drive high-current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, a 5V bias voltage is delivered from the VREG5 supply.

The average drive current is calculated by the gate charge at V_{GS} = 5V times the switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOTx and PHASEx pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to the low side MOSFET on, and the low side MOSFET off to the high side MOSFET on.

The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The internal pull-down transist or that drives $LGATE_X$ low is robust, with a 1.5Ω typical on-resistance. A 5V bias voltage is delivered from the VREG5 supply. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency killing, EMI-producing shoot-through currents. This can be remedied by adding a resistor in series with BOOTx, which increases the turn-on time of the high side MOSFET without degrading the turn-off time (Figure 3).

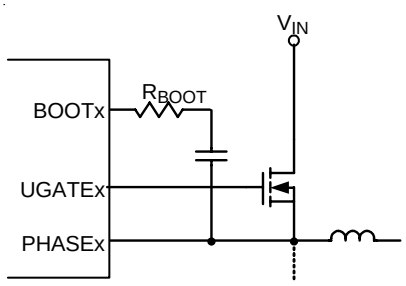


Figure 3. Increasing the UGATEx Rise Time

Soft-Start

The RT8223P provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FBx signal. The typical soft-start duration is 2 ms. A unique PWM duty limit control that prevents output over voltage during soft-start period is designed specifically for FBx floating.

UVLO Protection

The RT8223P features VREG5 under voltage lockout protection (UVLO). When the VREG5 voltage is lower than 3.9V (typ.) and the VREG3 voltage is lower than 2.5V (typ.), both switch power supplies are shut off. This is non-latch protection.

Power Good Output (PGOOD)

PGOOD is an open-drain type output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when both output voltages are above 91% of the nominal regulation point. The PGOOD goes low if either output turns off or is 15% below its nominal regulator point.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage. If the output voltage exceeds 12% of its set voltage threshold, the over voltage protection is triggered and the LGATEx low side gate drivers are forced high. This activates the low side MOSFET switch, which rapidly discharges the output capacitor and pulls the input voltage downward.

The RT8223P is latched once OVP is triggered and can only be released by toggling EN, ENTRIPx or cycling V_{IN}. There is a 5μs delay built into the over voltage protection circuit to prevent false alarm.

Note that the LGATEx latching high causes the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over-voltage condition is caused by a short in the high side switch, completely turning on the low side MOSFET can create an electrical short between the battery and GND, which will blow the fuse and disconnect the battery from the output.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. If the output is less than 52% of its set voltage threshold, under voltage protection will be triggered, and then both UGATEx and LGATEx gate drivers will be forced low. The UVP will be ignored for at least 5ms (typ.) after start-up or a rising edge on ENTRIPx. Toggle

ENTRIPx or cycle V_{IN} to reset the UVP fault latch and restart the controller.

Thermal Protection

The RT8223P features thermal shutdown protection to prevent overheat damage to the device. Thermal shutdown occurs when the die temperature exceeds 150°C. All internal circuitry is inactive during thermal shutdown. The RT8223P triggers thermal shutdown if VREGx is not supplied from VOUTx, while the input voltage on V_{IN} and the drawing current from VREGx are too high. Even if VREGx is supplied from VOUTx, large power dissipation on automatic switches caused by overloading VREGx, may also result in thermal shutdown.

Discharge Mode (Soft-Discharge)

When ENTRIPx is low and a transition to standby or shutdown mode occurs, or the output under voltage fault latch is set, the output discharge mode will be triggered. During discharge mode, the output capacitors' residual charge will be discharged to GND through an internal switch.

Shutdown Mode

The RT8223P SMPS1, SMPS2, VREG3 and VREG5 have independent enabling controls. Drive EN, ENTRIP1 and ENTRIP2 below the precise input falling-edge trip level to place the RT8223P in its low power shutdown state. The RT8223P consumes only 20μA of input current while in shutdown. When shutdown mode is activated, the reference turns off. The accurate 0.4V falling-edge threshold on the EN pin can be used to detect a specific analog voltage level as well as to shutdown the device. Once in shutdown, the 2.4V rising-edge threshold activates, providing sufficient hysteresis for most applications.

Power Up Sequencing and On/Off Controls (ENC)

ENTRIP1 and ENTRIP2 control the SMPS power up sequencing. When the RT8223P is in single channel mode, ENTRIP1 or ENTRIP2 enables the respective output when ENTRIPx voltage descends below 3V. Furthermore, the RT8223P can also be in dual channel mode. In this mode, outputs are enabled when ENC voltage rises above 2V.

Table 2. Operation Mode Truth Table

MODE	Condition	Comment
Power UP	VREGx < UVLO threshold	Transitions to discharge mode after a VIN POR and after REF becomes valid. VREG5, VREG3, and REF remain active.
RUN	EN = high, VOUT1 or VOUT2 enabled	Normal Operation.
Over Voltage Protection	Either output > 111% of the nominal level.	LGATEx is forced high. VREG3, VREG5 and REF active. Exited by VIN POR or by toggling EN, ENTRIPx, ENC
Under Voltage Protection	Either output < 52% of the nominal level after 3ms time-out expires and output is enabled	Both UGATEx and LGATEx are forced low and enter discharge mode. VREG3, VREG5 and REF are active. Exited by VIN POR or by toggling EN, ENTRIPx, ENC
Discharge	Either SMPS output is still high in either standby mode or shutdown mode	During discharge mode, there is one path to discharge the outputs capacitor residual charge. That is output capacitor discharge to GND through an internal switch.
Standby	$ENTRIP_X$ < startup threshold, EN = high.	VREG3, VREG5 and REF are active.
Shutdown	EN = low	All circuitry off.
Thermal Shutdown	T_J > 150°C	All circuitry off. Exit by VIN POR or by toggling EN, ENTRIPx, ENC

Table 3. Power Up Sequencing

EN (V)	ENC (V)	ENTRIP1	ENTRIP2	REF	VREG5	VREG3	SMPS1	SMPS2
Low	Low	X	X	Off	Off	Off	Off	Off
“>2.4V” => High	Low	X	X	On	On	On	Off	Off
“>2.4V” => High	“>2V” => High	Off	Off	On	On	On	Off	Off
“>2.4V” => High	“>2V” => High	Off	On	On	On	On	Off	On
“>2.4V” => High	“>2V” => High	On	Off	On	On	On	On	Off
“>2.4V” => High	“>2V” => High	On	On	On	On	On	On	On

Output Voltage Setting (FBx)

Connect a resistor voltage-divider at the FBx pin between VOUTx and GND to adjust the respective output voltage between 2V and 5.5V (Figure 4). Referring to Figure 4 as an example, choose R2 to be approximately 10kΩ, and solve for R1 using the equation :

$$V_{OUTX} = V_{FBX} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FBX} is 2V.

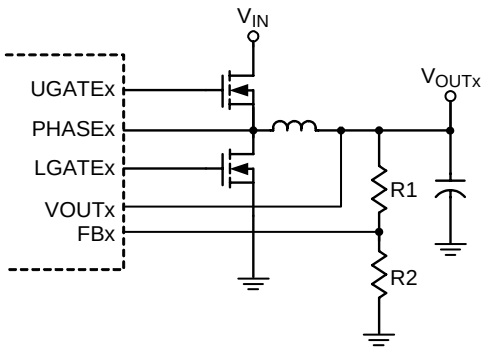


Figure 4. Setting V_{OUTX} with a Resistor Voltage Divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown in the following equation :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUTx})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak to peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left[(LIR/2) \times I_{LOAD(MAX)}\right]$$

The calculation above shall serve as a general reference. To further improve the transient response, the output inductance can be reduced even further. This needs to be considered along with the selection of the output capacitor.

Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from below equations :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (K \times \frac{V_{OUTx}}{V_{IN}} + t_{OFF(MIN)})}{2 \times C_{OUT} \times V_{OUTx} \times \left[K \times \left(\frac{V_{IN} - V_{OUTx}}{V_{IN}}\right)\right] - t_{OFF(MIN)}}$$

$$V_{SOAR} = \frac{(\Delta I_{LOAD})^2 \times L}{2 \times C_{OUT} \times V_{OUTx}}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f} \right)$$

where V_{SAG} and V_{SOAR} are the allowable amount of undershoot voltage the and overshoot voltage in load transient, V_{p-p} is the output ripple voltage, $t_{OFF(MIN)}$ is the minimum off-time, and K is a factor listed in Table 1.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8223P, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-24L 4x4 packages, the thermal resistance, θ_{JA}, is 52°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (52°C/W) = 1.923W for WQFN-24L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8223P package, the derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

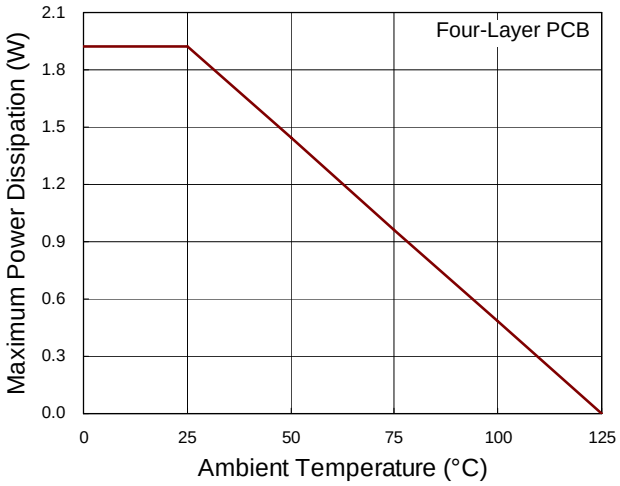


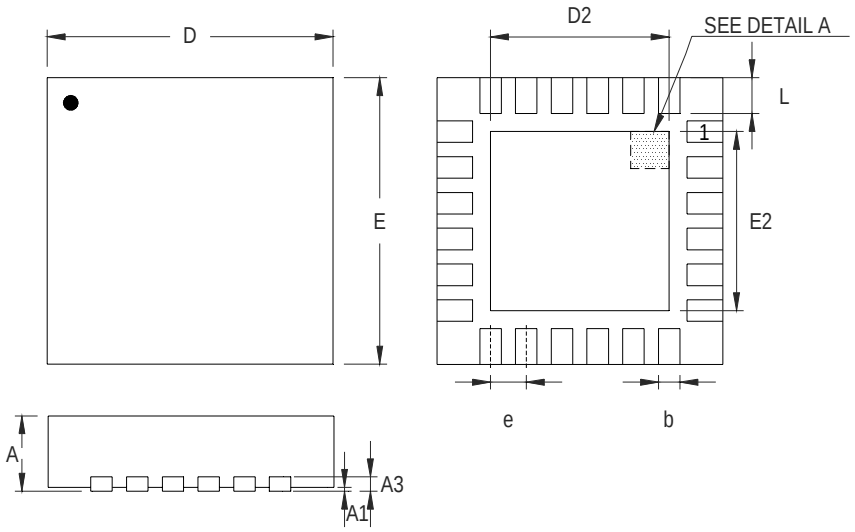
Figure 5. Derating Curve for the RT8223P Package

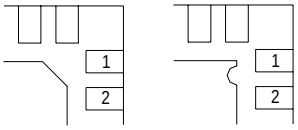
Layout Considerations

Layout is very important in high frequency switching converter designs, the PCB could radiate excessive noise and contribute to the converter instability with improper layout. Certain points must be considered before starting a layout using the RT8223P.

- Place the filter capacitor close to the IC, within 12mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching nodes.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25mils) or wider trace.
- All sensitive analog traces and components such as VOUTx, FBx, GND, ENTRIPx, PGOOD, and TONSEL should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Place the ground terminal of VIN capacitor(s), VOUTx capacitor(s), and source of low side MOSFETs as close as possible. The PCB trace defined as $PHASE_X$ node, which connects to source of high side MOSFET, drain of low side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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