CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

Check for Samples: TPS2041B-Q1, TPS2042B-Q1, TPS2051B-Q1

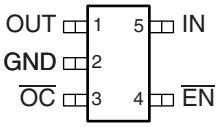
FEATURES

- **Qualified for Automotive Applications**
- **70-mΩ High-Side MOSFET**
- **500-mA Continuous Current**
- **Thermal and Short-Circuit Protection**
- **Accurate Current Limit: 0.75 A (Min), 1.25 A (Max)**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{OC}$)**
- **No $\overline{OC}$ Glitch During Power Up**
- **Maximum Standby Supply Current: 1 µA (Single, Dual) or 2 µA (Triple, Quad)**
- **Bidirectional Switch**
- **Junction Temperature Range: –40°C to 125°C**
- **ESD Protection Level Per AEC-Q100 Classification**
- **UL Recognized, File Number E169910**

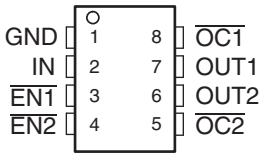
APPLICATIONS

- **Heavy Capacitive Loads**
- **Short-Circuit Protection**

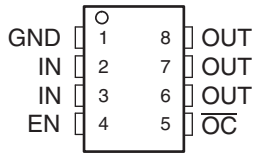
TPS2041B
DBV PACKAGE
(TOP VIEW)



TPS2042B
D PACKAGE
(TOP VIEW)



TPS2051B
D PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS204xB/TPS205xB power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporate 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1 A (typ).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

GENERAL SWITCH CATALOG

33 mΩ, single			80 mΩ, dual		80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA	0.2 A – 2 A		TPS2042B	500 mA	TPS2080	500 mA	TPS2043B 500 mA	TPS2044B 500 mA	TPS2085	500 mA
TPS202x	0.2 A – 2 A		TPS2052B	500 mA	TPS2081	500 mA	TPS2053B 500 mA	TPS2054B 500 mA	TPS2086	500 mA
TPS203x	0.2 A – 2 A		TPS2046	250 mA	TPS2082	500 mA	TPS2047 250 mA	TPS2048 250 mA	TPS2087	500 mA
			TPS2056	250 mA	TPS2090	250 mA	TPS2057 250 mA	TPS2058 250 mA	TPS2095	250 mA
			TPS2062	1 A	TPS2091	250 mA			TPS2096	250 mA
			TPS2066	1 A	TPS2092	250 mA			TPS2097	250 mA
			TPS2060	1.5 A						
			TPS2064	1.5 A						

80 mΩ, single			260 mΩ		
TPS2014	600 mA		TPS2100/1		
TPS2015	1 A		IN1	500 mA	
TPS2041B	500 mA		IN2	10 mA	
TPS2051B	500 mA		TPS2102/3/4/5		
TPS2045	250 mA		IN1	500 mA	
TPS2055	250 mA		IN2	100 mA	
TPS2061	1 A				
TPS2065	1 A				

ORDERING INFORMATION(1)

T_J	ENABLE	NO. OF SWITCHES	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Active high	Single	SOIC – D	Reel of 2500	TPS2051BQDRQ1	2051BQ
	Active low	Single	SOT-23 – DBV	Reel of 3000	TPS2041BQDBVRQ1	PLIQ
		Dual	SOIC – D	Reel of 2500	TPS2042BQDRQ1	2042B

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

$V_{I(IN)}$	Input voltage range (IN)(2)			–0.3 V to 6 V
$V_{O(OUT)}$, $V_{O(OUTx)}$	Output voltage range (OUT, OUTx)(2)			–0.3 V to 6 V
$V_{I(\overline{ENx})}$, $V_{I(EN)}$	Input voltage range ($\overline{ENx}$, EN)			–0.3 V to 6 V
$V_{I(\overline{OC})}$, $V_{I(\overline{OCx})}$	Voltage range ($\overline{OC}$, $\overline{OCx}$)			–0.3 V to 6 V
$I_{O(OUT)}$, $I_{O(OUTx)}$	Continuous output current			Internally limited
	Continuous total power dissipation			See Dissipation Ratings
T_J	Operating virtual-junction temperature range			–40°C to 125°C
T_{stg}	Storage temperature range			–65°C to 150°C
	Lead temperature, soldering		1,6 mm (1/16 in) from case for 10 s	260°C
	Electrostatic discharge (ESD) protection	TPS2041B	Human-Body Model (HBM) (H2)	2500 V
			Machine Model (MM) (M0)	50 V
			Charged-Device Model (CDM) (C5)	1500 V
		TPS2042B	Human-Body Model (HBM) (H2)	2500 V
			Machine Model (MM) (M0)	50 V
			Charged-Device Model (CDM) (C5)	1500 V
		TPS2051B	Human-Body Model (HBM) (H2)	2000 V
			Machine Model (MM) (M0)	50 V
			Charged-Device Model (CDM) (C5)	1500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATING RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D-8	585.82 mW	5.8582 mW/°C	322.20 mW	234.32 mW
DBV-5	285 mW	2.85 mW/°C	155 mW	114 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{I(IN)}$	Input voltage (IN)	2.7	5.5	V
$V_{I(\overline{ENx})}$, $V_{I(EN)}$	Input voltage ($\overline{ENx}$, EN)	0	5.5	V
$I_{O(OUT)}$, $I_{O(OUTx)}$	Continuous output current (OUT, OUTx)	0	500	mA
T_J	Operating virtual-junction temperature	–40	125	°C

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ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(\overline{ENx})}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Power Switch								
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V or 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V, I_O = 0.5 A		–40°C ≤ T_J ≤ 125°C		70	135	mΩ
	Static drain-source on-state resistance, 2.7-V operation(2)	$V_{I(IN)}$ = 2.7 V, I_O = 0.5 A		–40°C ≤ T_J ≤ 125°C		75	150	mΩ
t_r	Rise time, output(2)	$V_{I(IN)}$ = 5.5 V	C_L = 1 µF, R_L = 10 Ω	T_J = 25°C		0.6	1.5	ms
		$V_{I(IN)}$ = 2.7 V				0.4	1	ms
t_f	Fall time, output(2)	$V_{I(IN)}$ = 5.5 V			0.05		0.5	ms
		$V_{I(IN)}$ = 2.7 V			0.05		0.5	ms
Enable Input ($\overline{EN}$, $\overline{ENx}$)								
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V			2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V					0.8	V
I_I	Input current	$V_{I(\overline{ENx})}$ = 0 V or 5.5 V			–0.5		0.5	µA
t_{on}	Turn-on time(2)	C_L = 100 µF, R_L = 10 Ω					3	ms
t_{off}	Turn-off time(2)	C_L = 100 µF, R_L = 10 Ω					10	ms
Current Limit								
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit		T_J = 25°C	0.65	1	1.25	A
				–40°C ≤ T_J ≤ 125°C	0.6	1	1.3	A
Supply Current (TPS2041B/TPS2051B)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{EN})}$ = 5.5 V or $V_{I(EN)}$ = 0 V		T_J = 25°C		0.5	1	µA
				–40°C ≤ T_J ≤ 125°C		0.5	5	µA
Supply current, high-level output		No load on OUT, $V_{I(\overline{EN})}$ = 0 V or $V_{I(EN)}$ = 5.5 V		T_J = 25°C		43	60	µA
				–40°C ≤ T_J ≤ 125°C		43	70	µA
Leakage current		OUT connected to ground, $V_{I(\overline{EN})}$ = 5.5 V or $V_{I(EN)}$ = 0 V		–40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground(2)		T_J = 25°C		0		µA
Supply Current (TPS2042B)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V		T_J = 25°C		0.5	1	µA
				–40°C ≤ T_J ≤ 125°C		0.5	5	µA
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V		T_J = 25°C		50	70	µA
				–40°C ≤ T_J ≤ 125°C		50	90	µA
Leakage current		OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V		–40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground(2)		T_J = 25°C		0.2		µA
Undervoltage Lockout								
Low-level input voltage, IN, INx					2		2.5	V
Hysteresis, IN, INx				T_J = 25°C		75		mV
Overcurrent ($\overline{OC}$, $\overline{OCx}$)								
Output low voltage, $V_{OL(/OCx)}$		$I_{O(\overline{OCx})}$ = 5 mA					0.4	V
Off-state current(2)		$V_{O(\overline{OCx})}$ = 5 V or 3.3 V					1	µA
$\overline{OC}$ deglitch(2)		$\overline{OCx}$ assertion or deassertion			4	8	15	ms

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be accounted for separately.
(2) Specified by design

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ELECTRICAL CHARACTERISTICS (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(\overline{ENx})}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
Thermal Shutdown(3)					
Thermal shutdown threshold(2)		135			°C
Recovery from thermal shutdown(2)		125			°C
Hysteresis(2)			10		°C

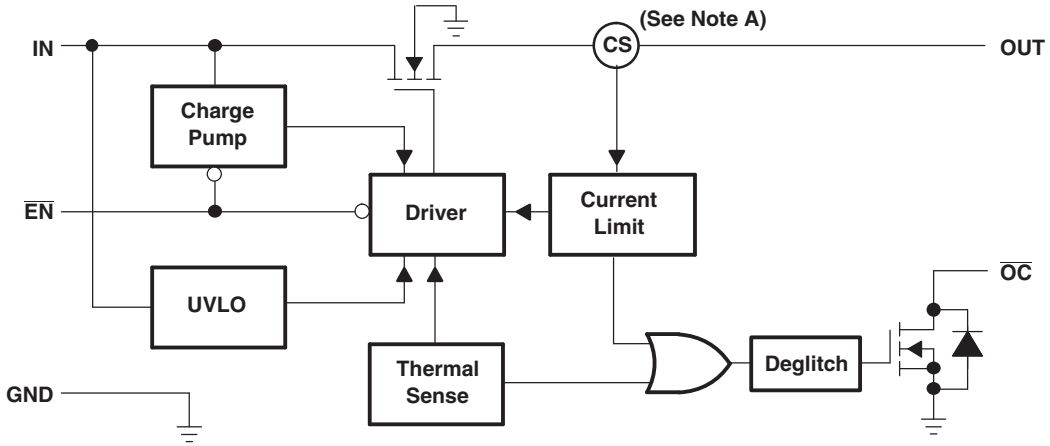
(3) The thermal shutdown only reacts under overcurrent conditions.

DEVICE INFORMATION

Terminal Functions (TPS2041B)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	4	I	Enable input, logic low turns on power switch
GND	2		Ground
IN	5	I	Input voltage
$\overline{OC}$	3	O	Overcurrent, open-drain output, active low
OUT	1	O	Power-switch output

Functional Block Diagram (TPS2041B)

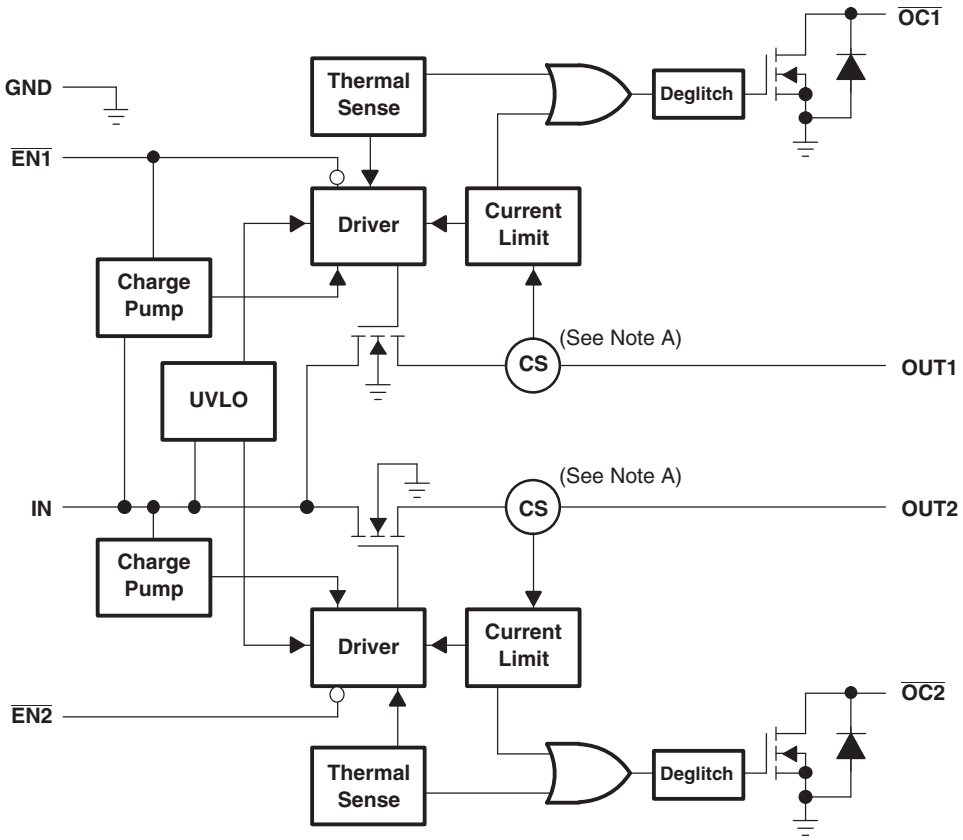


A. CS = Current sense

Terminal Functions (TPS2042B)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN1}$	3	I	Enable input, logic low turns on power switch IN-OUT1
$\overline{EN2}$	4	I	Enable input, logic low turns on power switch IN-OUT2
GND	1		Ground
IN	2	I	Input voltage
$\overline{OC1}$	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{OC2}$	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	O	Power-switch output, IN-OUT1
OUT2	6	O	Power-switch output, IN-OUT2

Functional Block Diagram (TPS2042B)



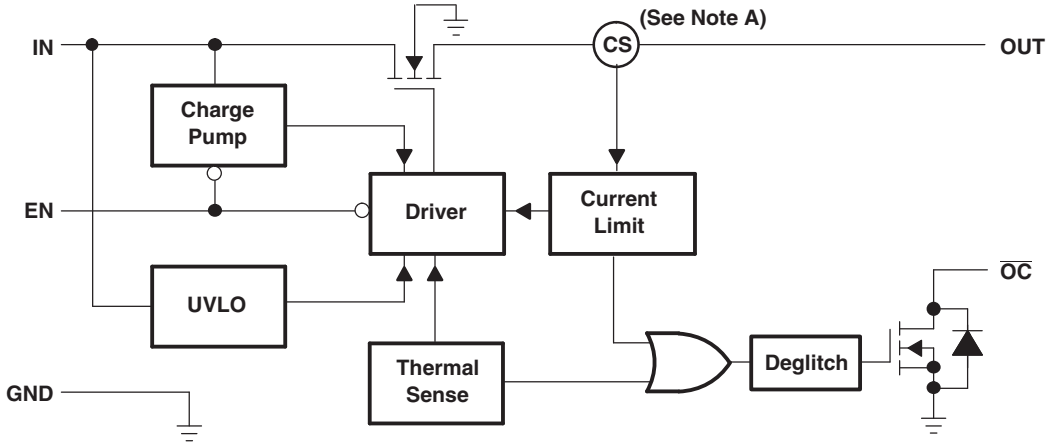
A. CS = Current sense

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Terminal Functions (TPS2051B)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Enable input, logic high turns on power switch
GND	1		Ground
IN	2, 3	I	Input voltage
$\overline{OC}$	5	O	Overcurrent open-drain output, active low
OUT	6, 7, 8	O	Power-switch output

Functional Block Diagram (TPS2051B)



A. CS = Current sense

PARAMETER MEASUREMENT INFORMATION

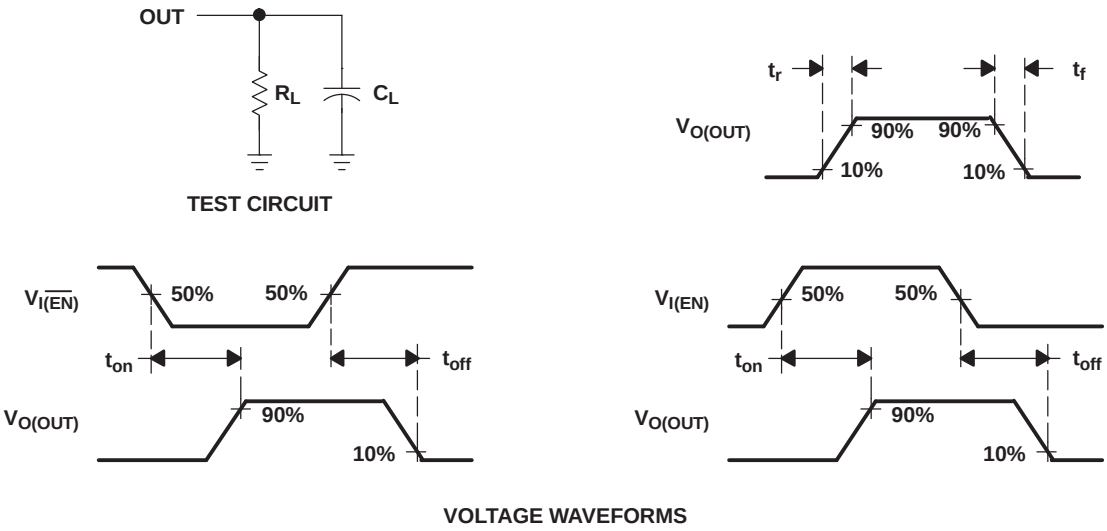


Figure 1. Test Circuit and Voltage Waveforms

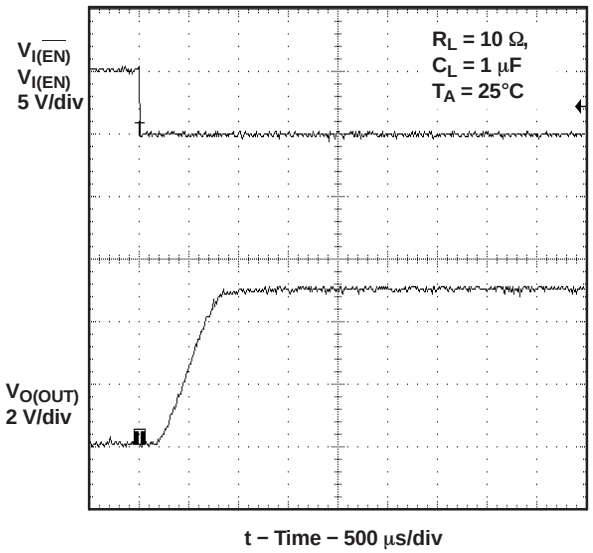


Figure 2. Turn-On Delay and Rise Time With 1-μF Load

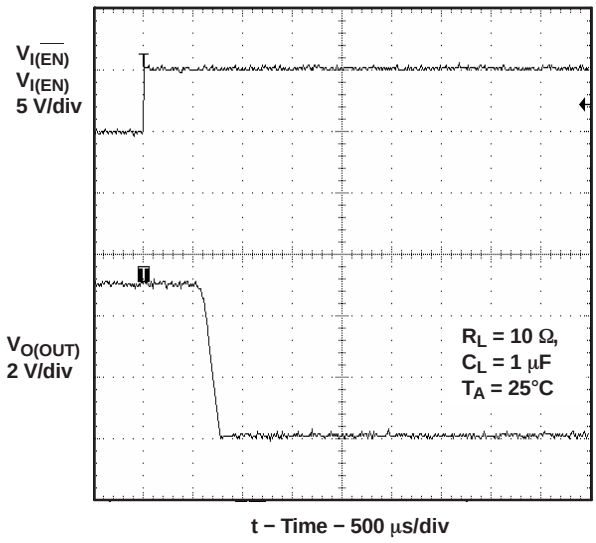


Figure 3. Turn-Off Delay and Fall Time With 1-μF Load

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PARAMETER MEASUREMENT INFORMATION (continued)

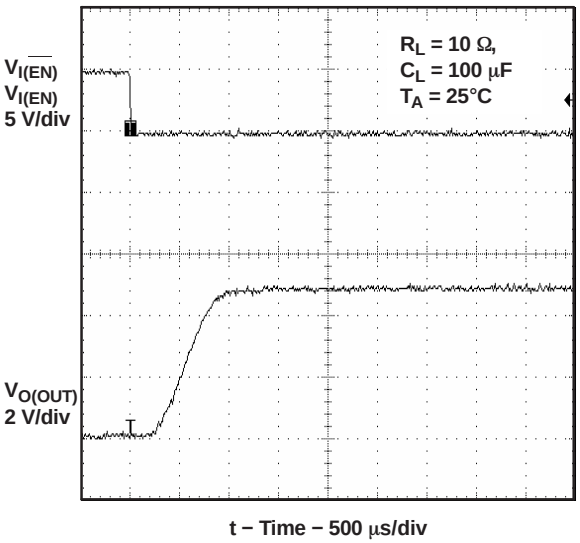


Figure 4. Turn-On Delay and Rise Time With 100-μF Load

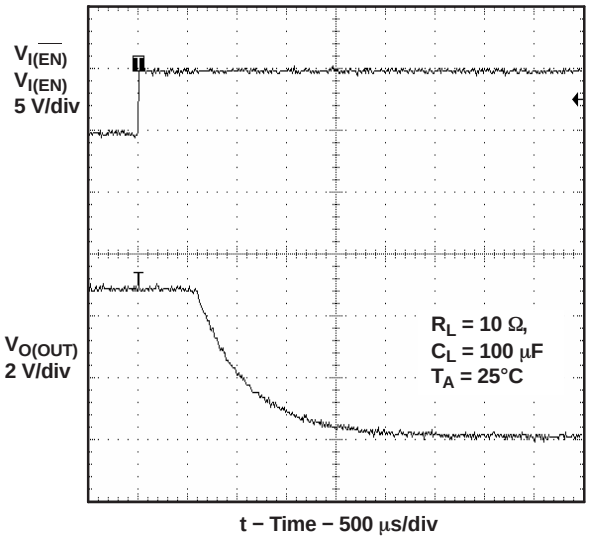


Figure 5. Turn-Off Delay and Fall Time With 100-μF Load

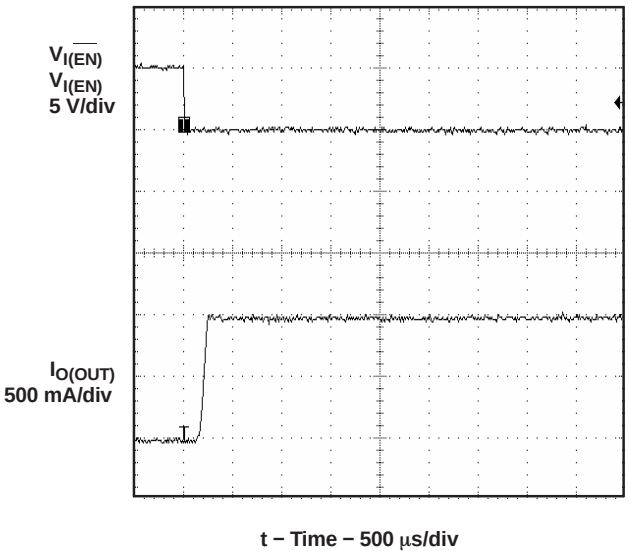


Figure 6. Short-Circuit Current, Device Enabled Into Short

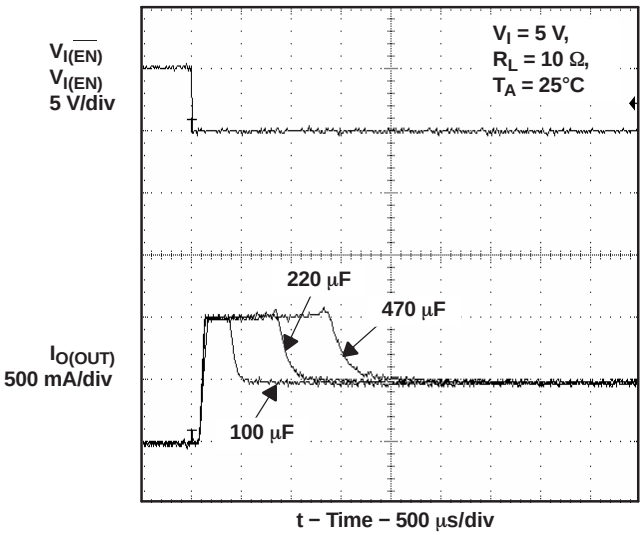


Figure 7. Inrush Current With Different Load Capacitance

PARAMETER MEASUREMENT INFORMATION (continued)

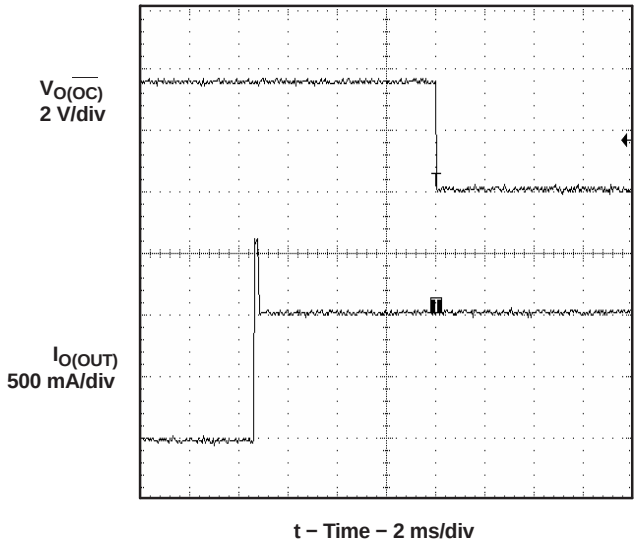


Figure 8. 3-Ω Load Connected to Enabled Device

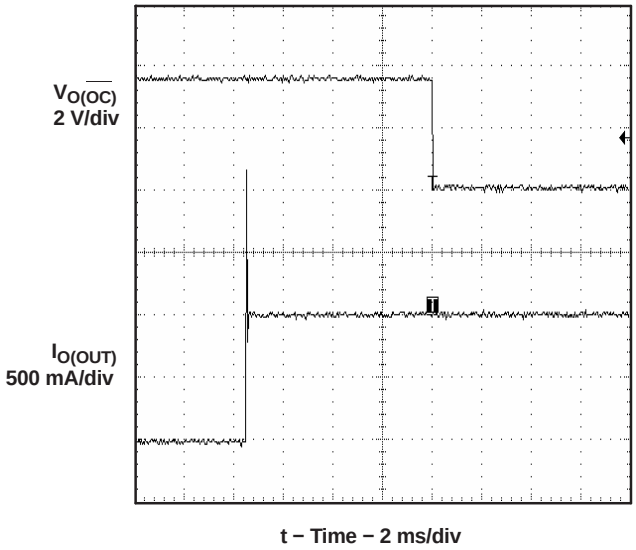


Figure 9. 2-Ω Load Connected to Enabled Device

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TYPICAL CHARACTERISTICS

TURN-ON TIME vs INPUT VOLTAGE

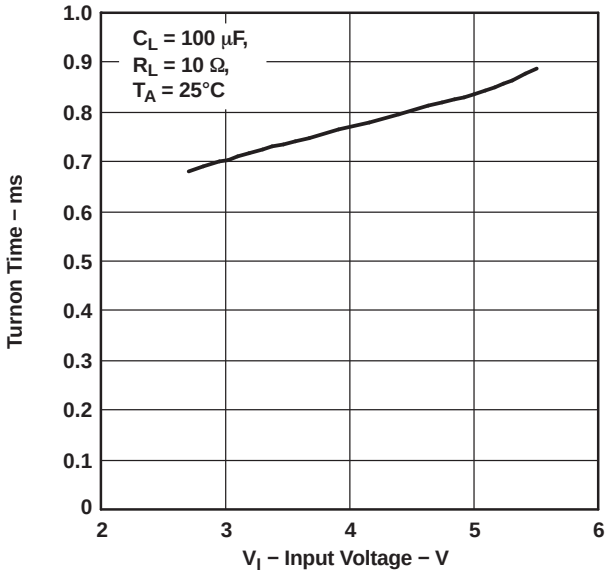


Figure 10.

TURN-OFF TIME vs INPUT VOLTAGE

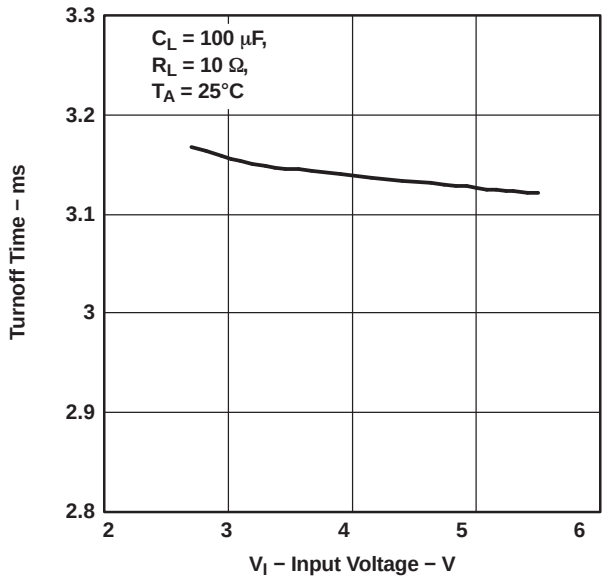


Figure 11.

RISE TIME vs INPUT VOLTAGE

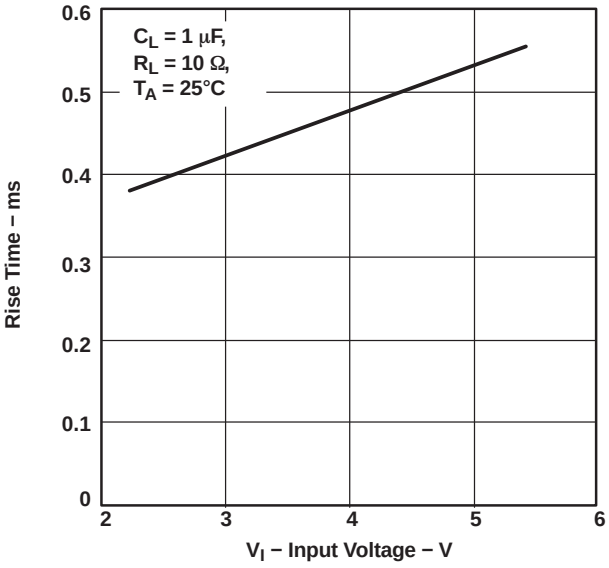


Figure 12.

FALL TIME vs INPUT VOLTAGE

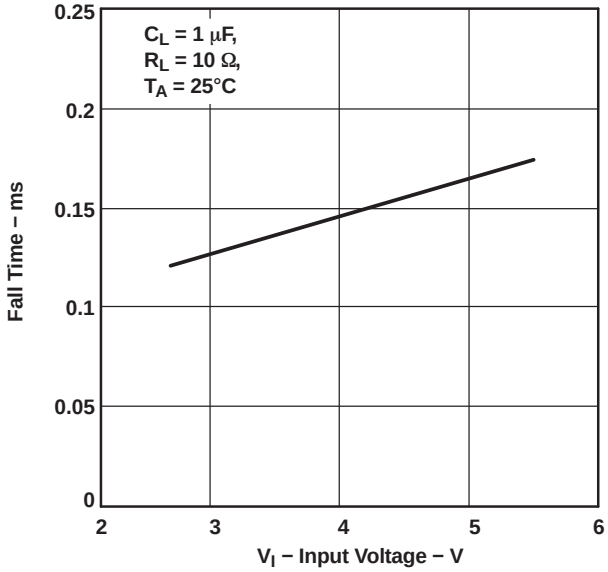


Figure 13.

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TYPICAL CHARACTERISTICS (continued)

TPS2041B/TPS2051B
SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

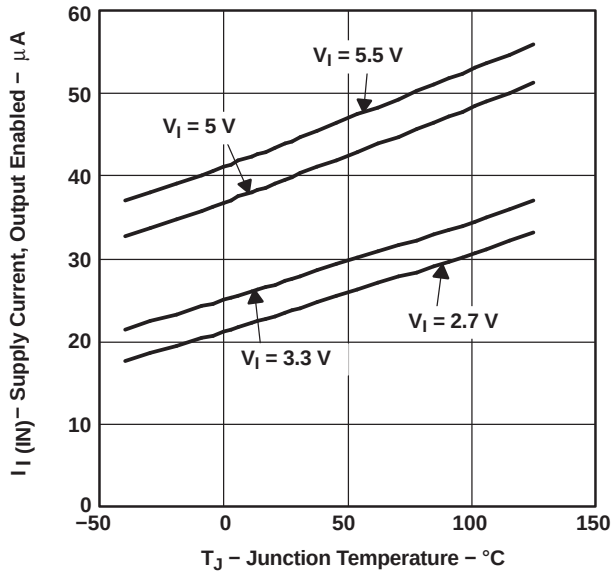


Figure 14.

TPS2042B
SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

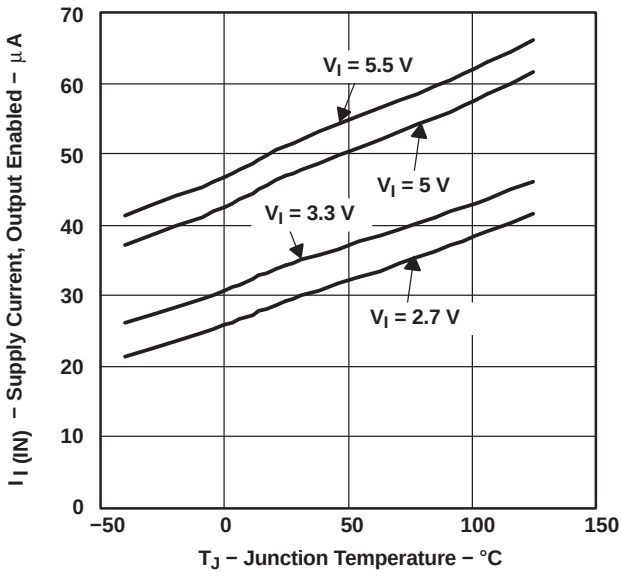


Figure 15.

TPS2041B/TPS2051B
SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

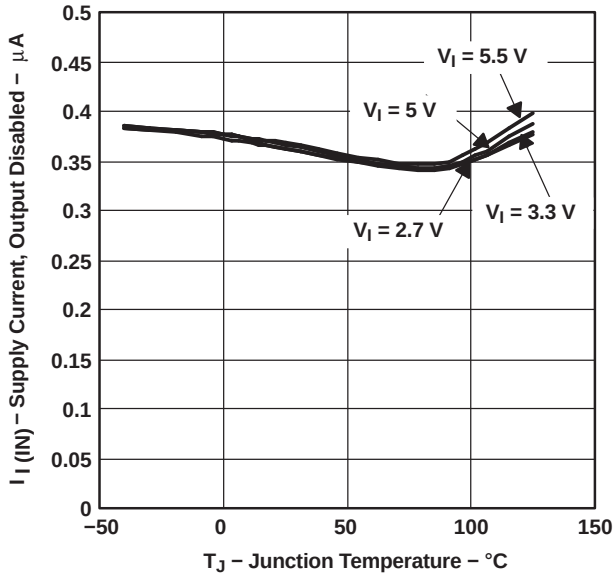


Figure 16.

TPS2042B
SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

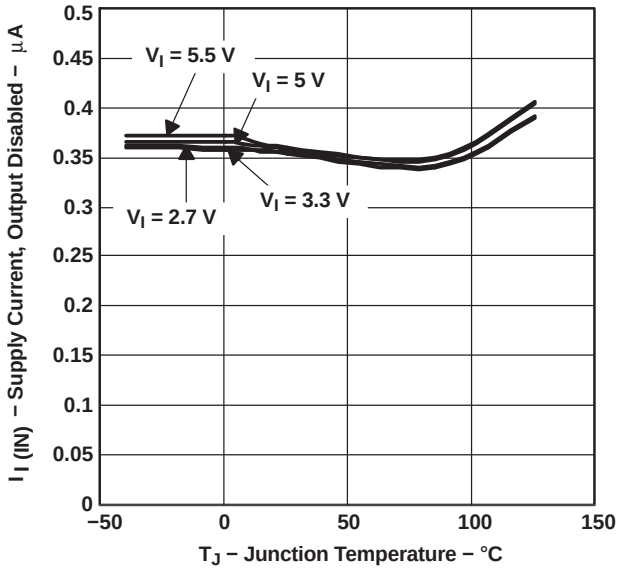


Figure 17.

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TYPICAL CHARACTERISTICS (continued)

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

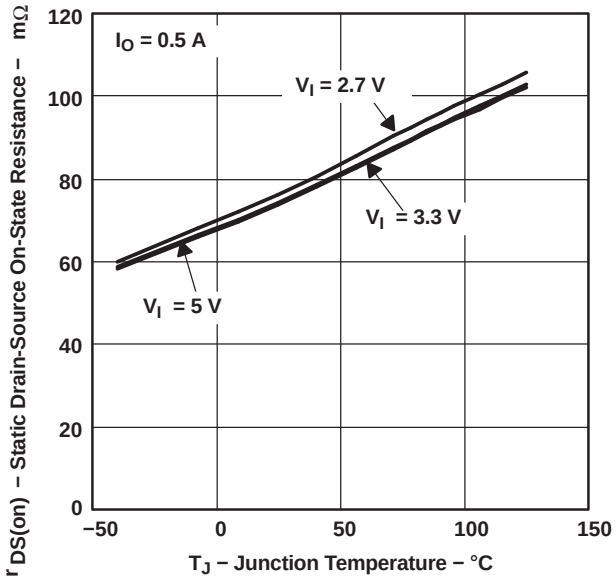


Figure 18.

SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE

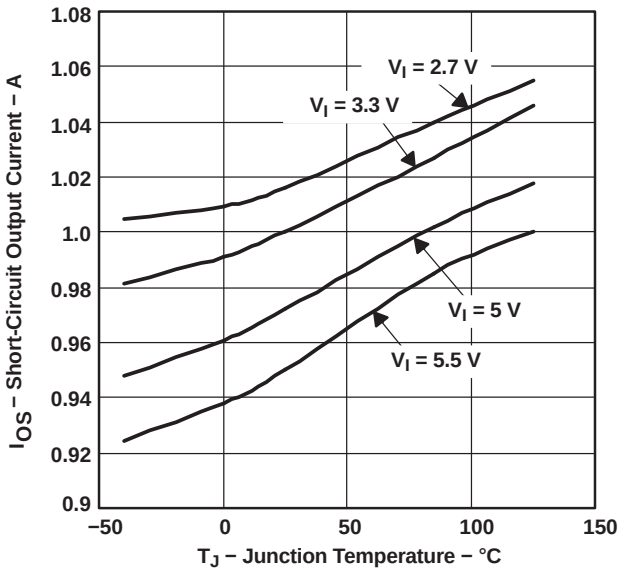


Figure 19.

THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

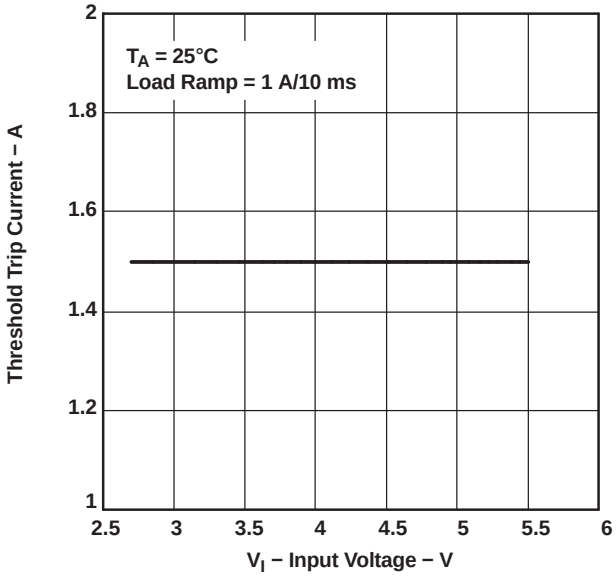


Figure 20.

UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE

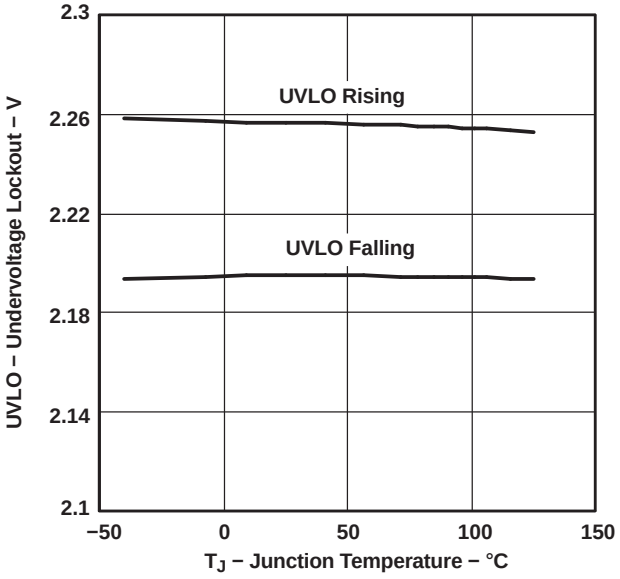


Figure 21.

TYPICAL CHARACTERISTICS (continued)

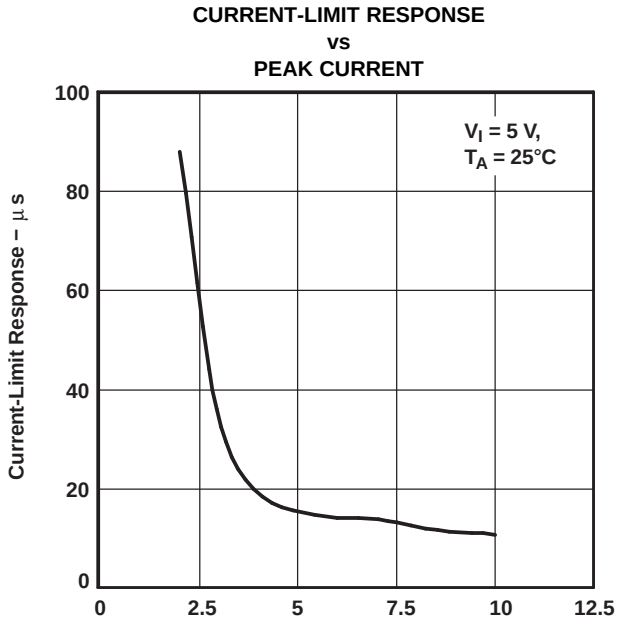


Figure 22.

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APPLICATION INFORMATION

Power-Supply Considerations

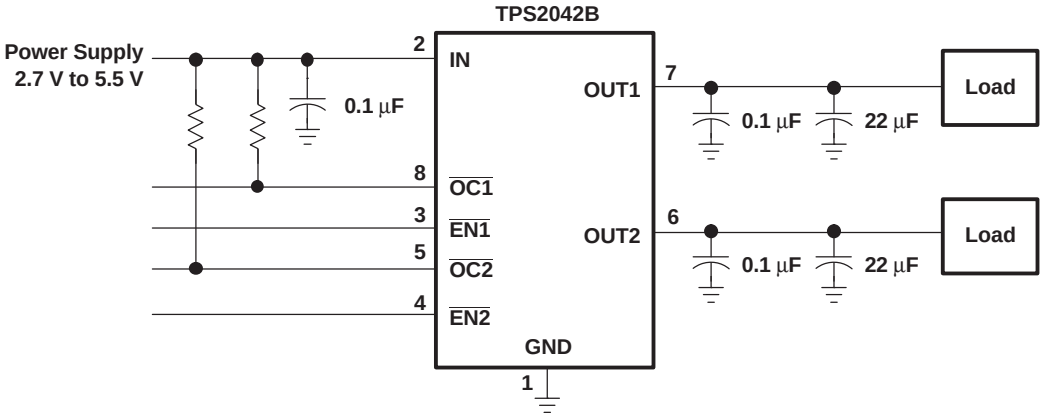


Figure 23. Typical Application (Example, TPS2042B)

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 14 and Figure 15). The TPS204xB/TPS205xB senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 16 and Figure 17). The TPS204xB/TPS205xB is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ Response

The $\overline{\text{OC}}$x open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OC}}$x occurs due to the 10-ms deglitch circuit. The TPS204xB/TPS205xB is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OC}}$x is not deglitched when the switch is turned off due to an overtemperature shutdown.

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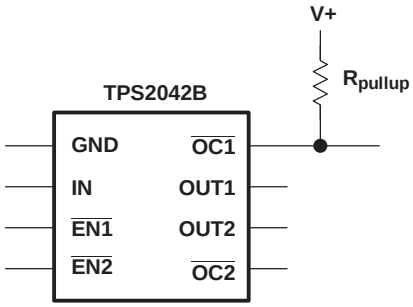


Figure 24. Typical Circuit for the $\overline{OC}$ Pin (Example, TPS2042B)

Power Dissipation and Junction Temperature

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 18. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature (°C)

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS204xB/TPS205xB implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OCx}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

Undervoltage Lockout (UVLO)

The UVLO ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

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Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPHs)
- Bus-powered hubs (BPHs)
- Low-power bus-powered functions
- High-power bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS204xB/TPS205xB can provide power-distribution solutions to many of these classes of devices.

Hosts/Self-Powered Hubs and Bus-Powered Hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 25). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

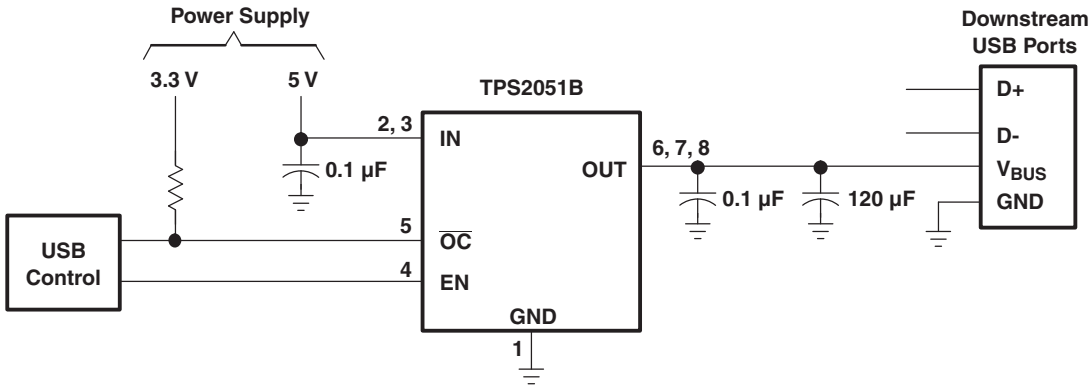


Figure 25. Typical One-Port USB Host/Self-Powered Hub

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

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Low-Power and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 26).

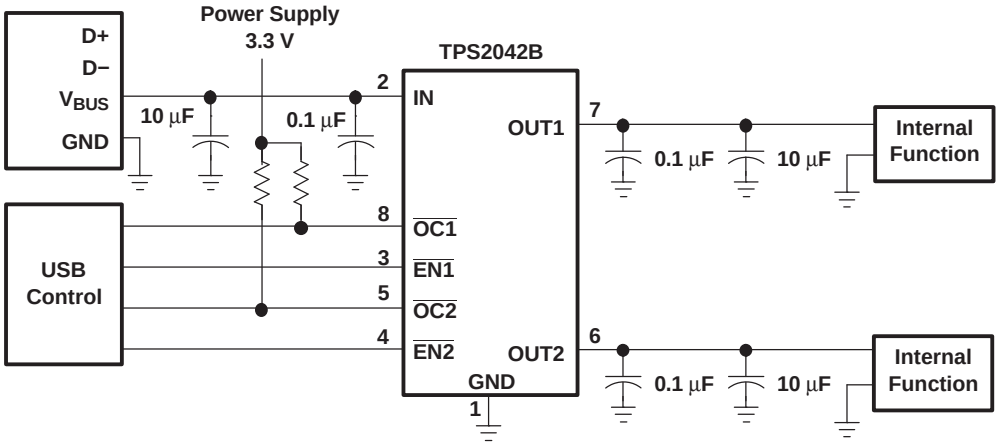


Figure 26. High-Power Bus-Powered Function (Example, TPS2042B)

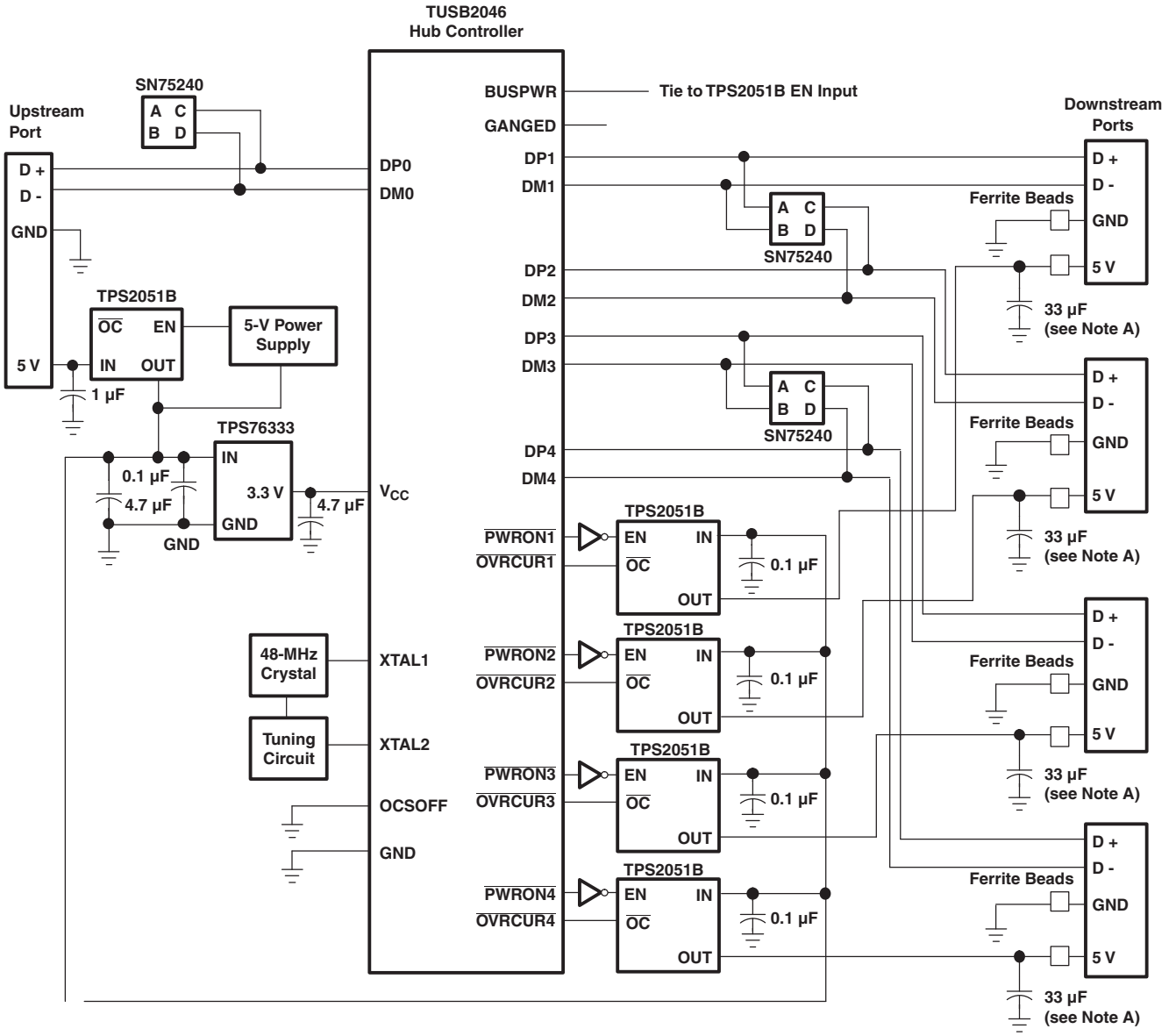
USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

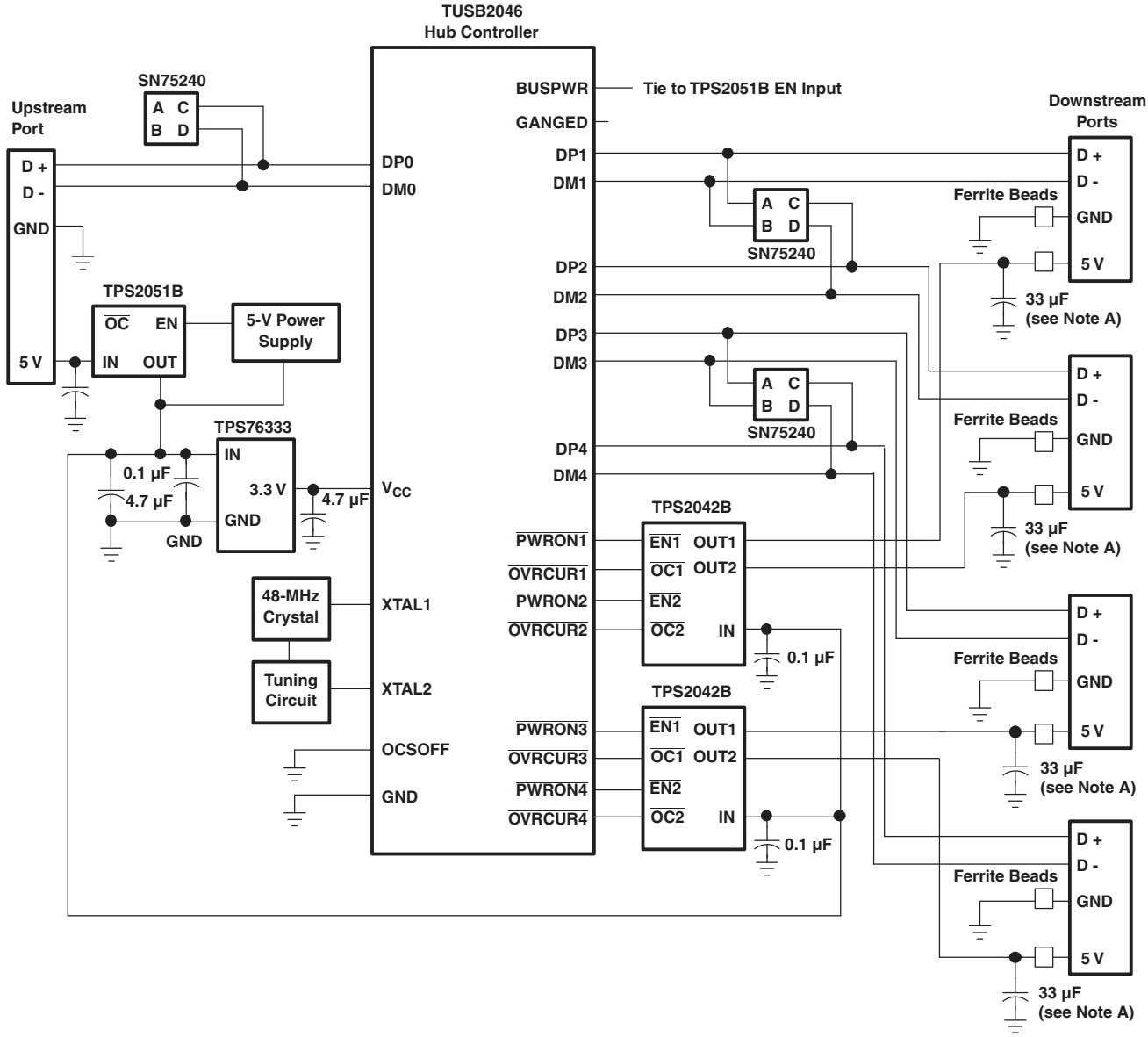
The feature set of the TPS204xB/TPS205xB allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 27 and Figure 28).

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A. USB rev 1.1 requires 120 µF per hub.

Figure 27. Hybrid Self-Powered/Bus-Powered Hub Implementation (TPS2051B)



A. USB rev 1.1 requires 120 µF per hub.

Figure 28. Hybrid Self-Powered/Bus-Powered Hub Implementation (TPS2042B)

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Generic Hot-Plug Applications

In many applications, it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS204xB/TPS205xB, these devices can be used to provide a softer startup to devices being hot-plugged into a powered system. The UVLO feature of the TPS204xB/TPS205xB also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature ensures a soft start with a controlled rise time for every insertion of the card or module.

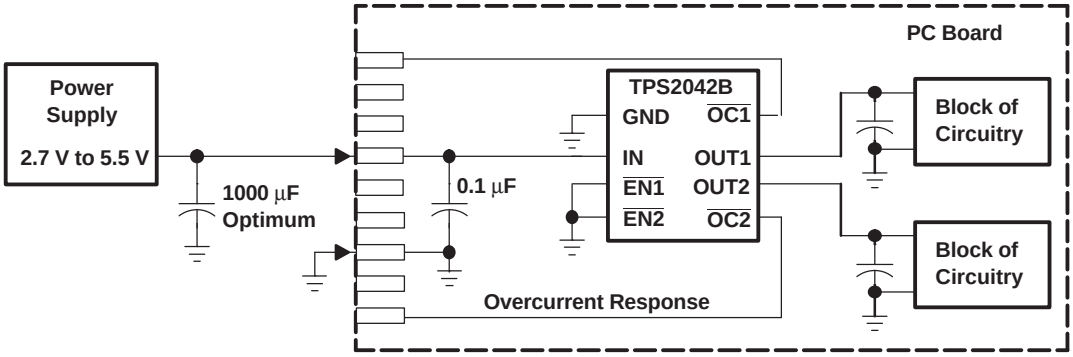


Figure 29. Typical Hot-Plug Implementation (Example, TPS2042B)

By placing the TPS204xB/TPS205xB between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

DETAILED DESCRIPTION

Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 500 mA.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Enable ($\overline{\text{ENx}}$)

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic high is present on $\overline{\text{EN}}$. A logic zero input on $\overline{\text{EN}}$ restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

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Enable (EN)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 μA or 2 μA when a logic low is present on EN. A logic high input on EN restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

Overcurrent ($\overline{OCx}$)

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OCx}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OCx}$ is asserted instantaneously.

Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

Thermal Sense

The TPS204xB/TPS205xB implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OCx}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

Undervoltage Lockout (UVLO)

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

REVISION HISTORY

Changes from Original (November 2007) to Revision A	Page
• Added the TPS2041B-Q1 device information	1

Changes from Revision A (June 2010) to Revision B	Page
• Changed orderable part number From: TPS2041QDBVRQ1 To: TPS2041BQDBVRQ1	2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2041BQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PLIQ	Samples
TPS2042BQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B	Samples
TPS2051BQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2051BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2041B-Q1, TPS2042B-Q1, TPS2051B-Q1 :

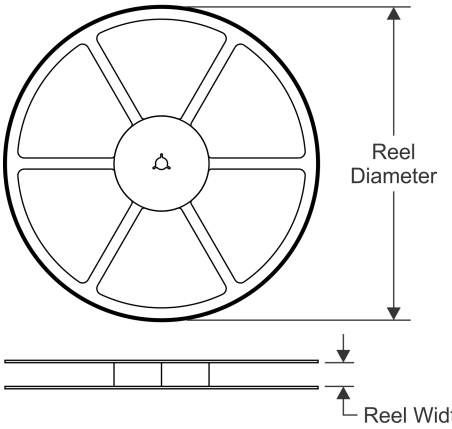
- Catalog: TPS2041B, TPS2042B, TPS2051B
- Enhanced Product: TPS2041B-EP

NOTE: Qualified Version Definitions:

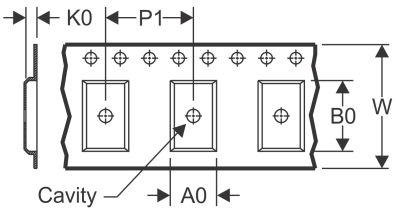
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

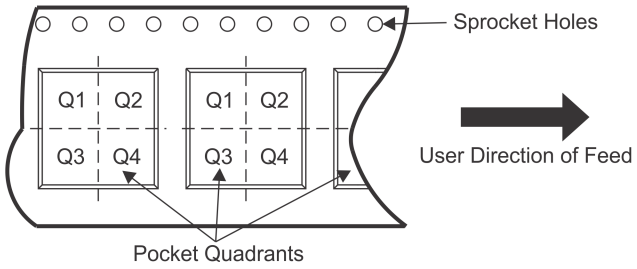


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

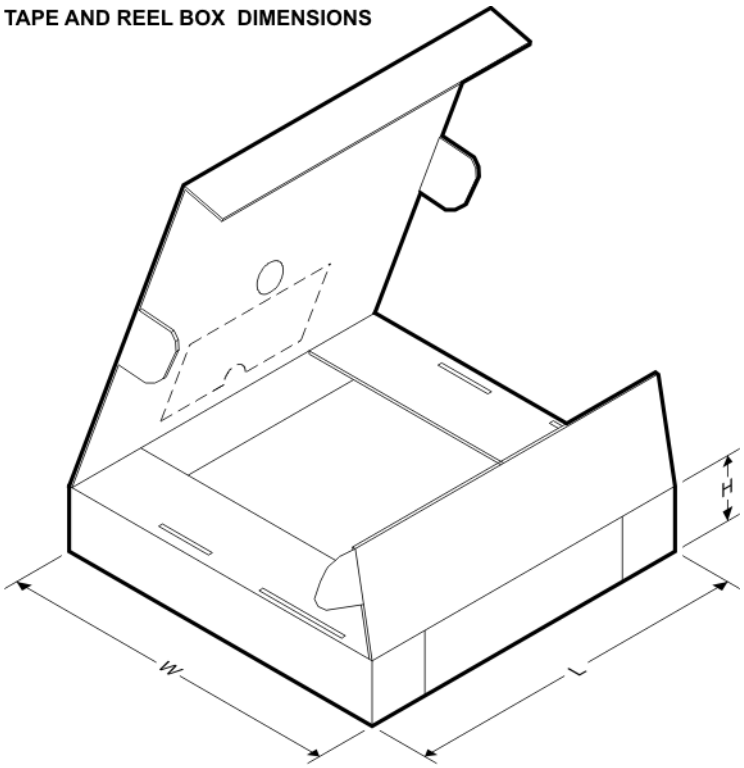
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2041BQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

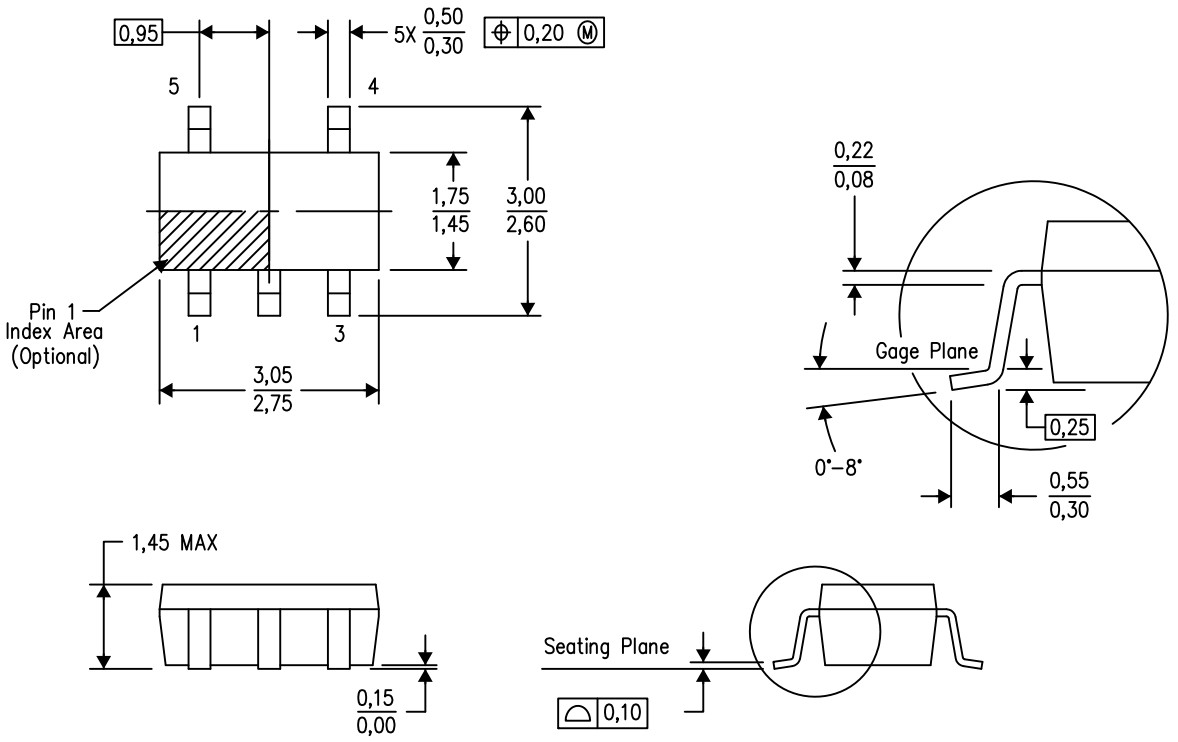
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2041BQDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS2051BQDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

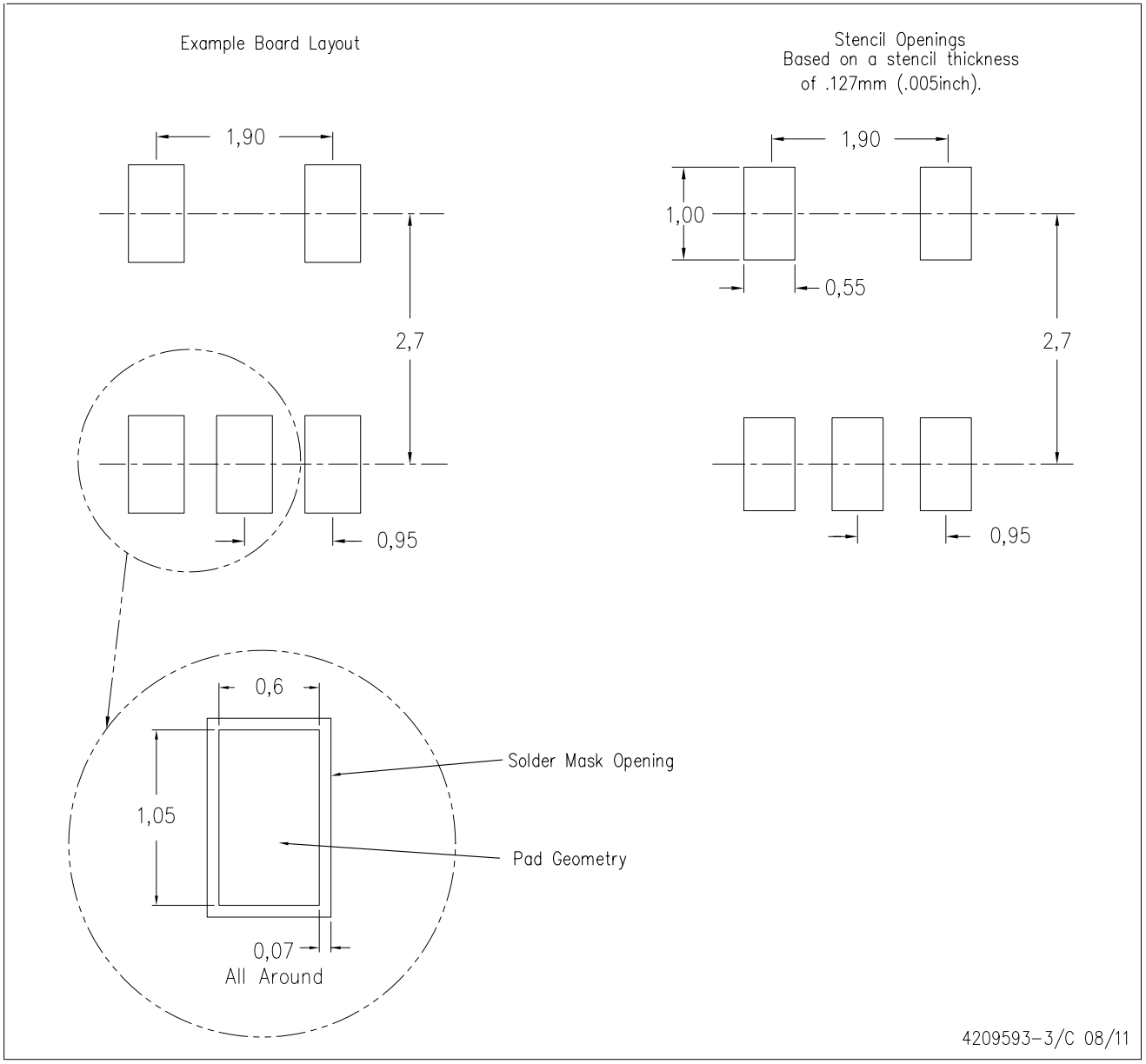
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

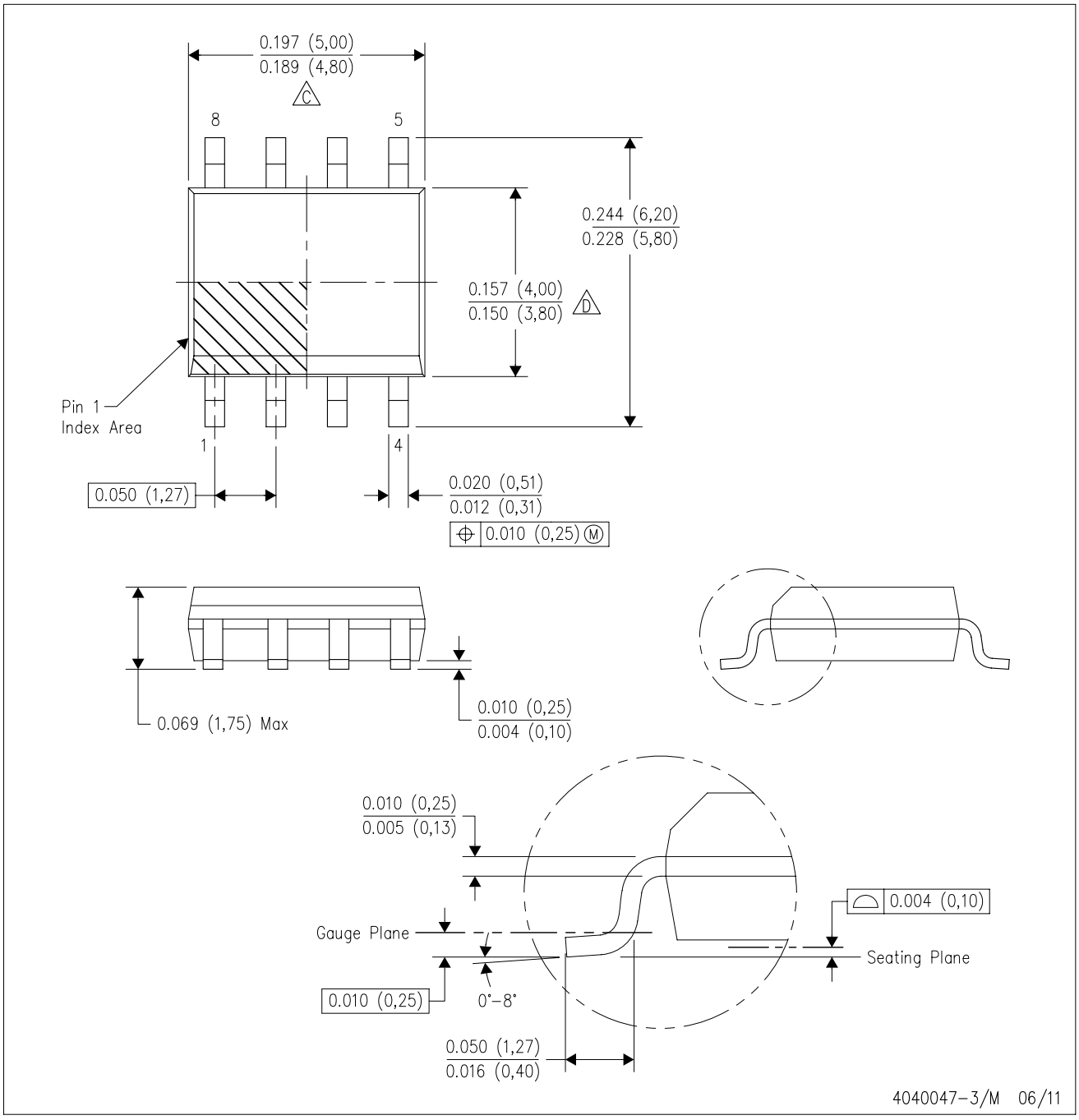
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



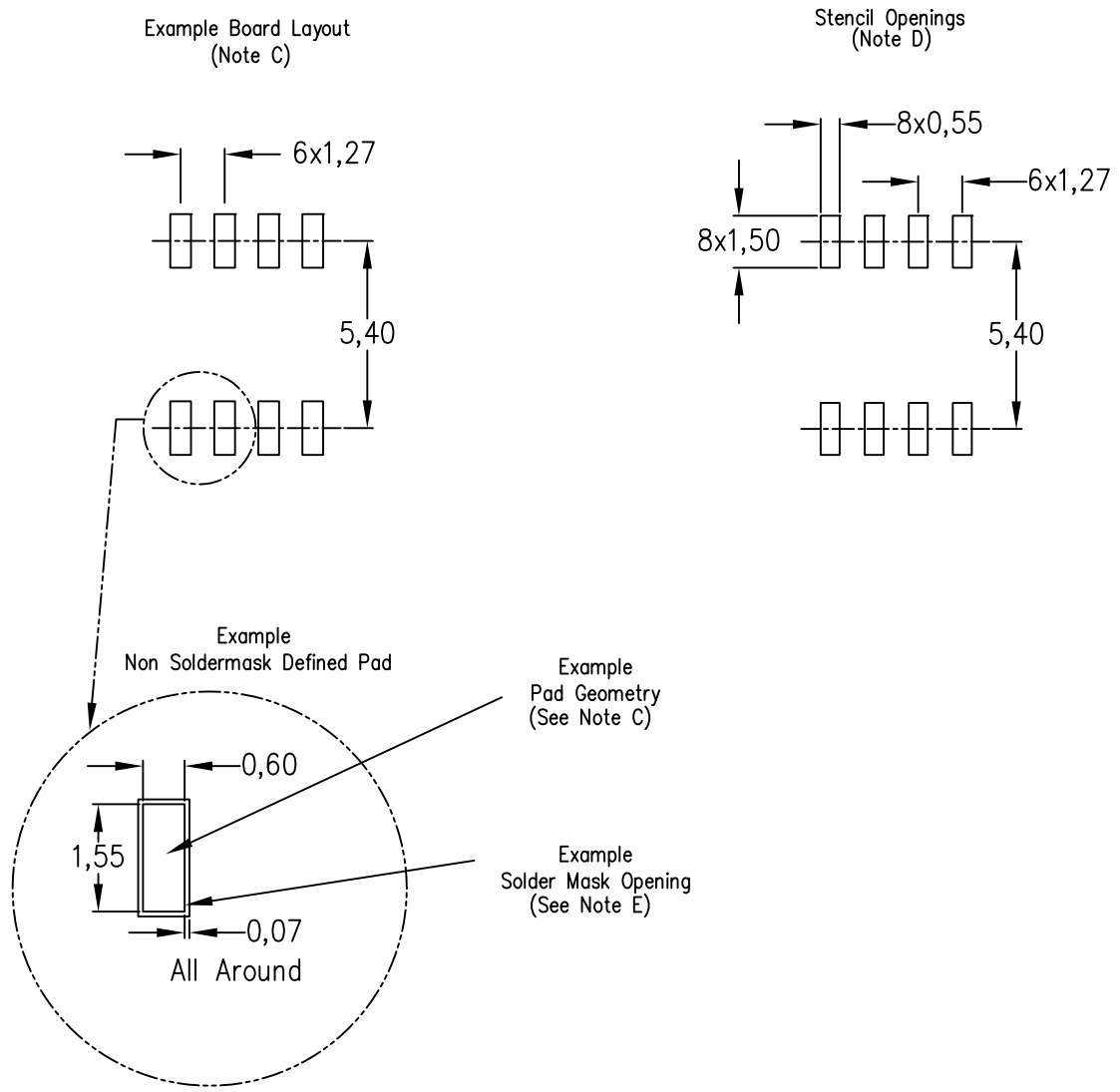
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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