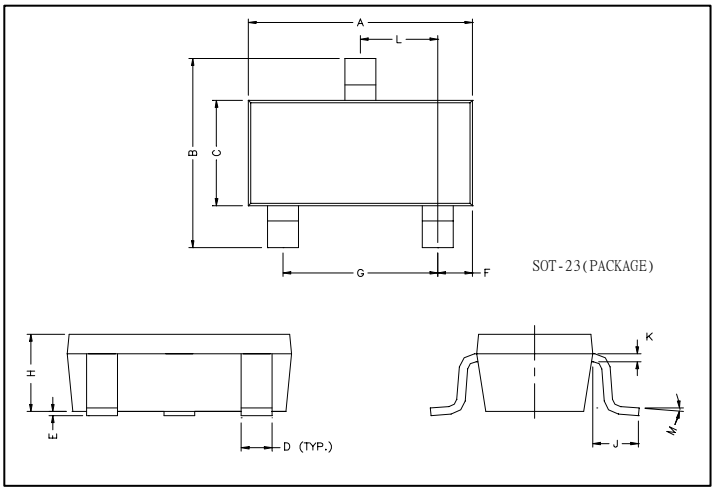
20V P-Channel Enhancement Mode MOSFET

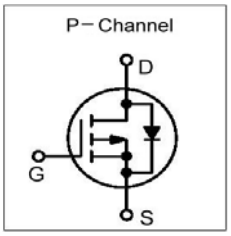
VDS= -20V
RDS(ON), Vgs@-4.5V, Ids@-2.8A ＜130mΩ
RDS(ON), Vgs@-2.5V, Ids@-2.0A ＜190mΩ

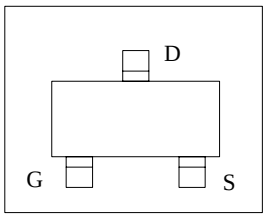
Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance

Package Dimensions







REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	1.90	REF.
B	2.40	2.80	H	1.00	1.30
C	1.40	1.60	K	0.10	0.20
D	0.35	0.50	J	0.40	-
E	0	0.10	L	0.85	1.15
F	0.45	0.55	M	0°	10°

Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current		I_D	-2.2	A
Pulsed Drain Current [1]		I_{DM}	-8	
Maximum Power Dissipation [2]	TA = 25°C	P_D	1.25	W
	TA = 75°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		R_{thJA}	100	°C/W
Junction-to-Ambient Thermal Resistance (PCB mounted) [3]			166	

Notes
1) Pulse width limited by maximum junction temperature.
2) Surface Mounted on FR4 Board, t ≤ 5 sec.
3) Surface Mounted on FR4 Board.

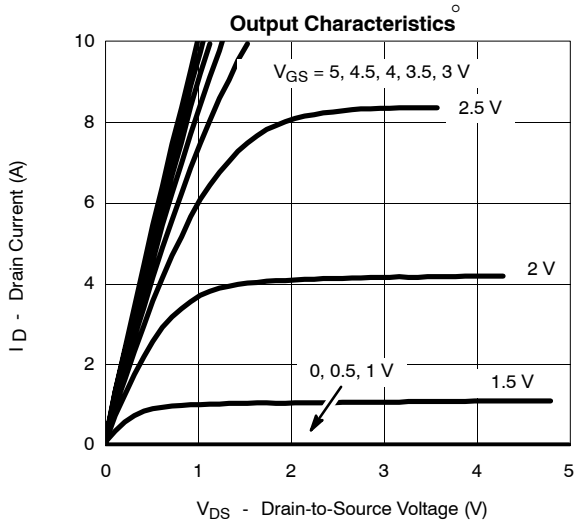
20V P-Channel Enhancement Mode MOSFET

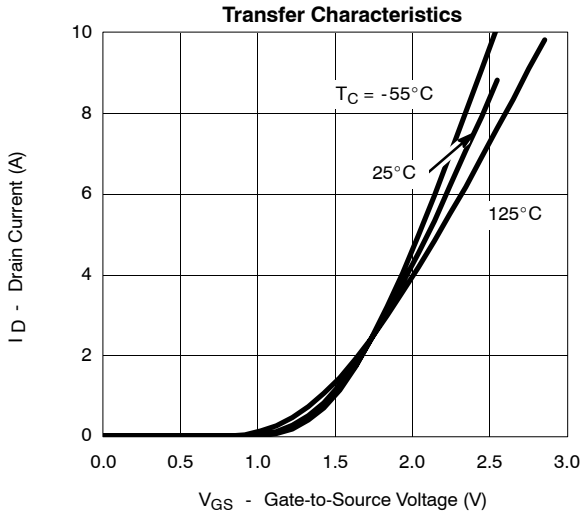
ELECTRICAL CHARACTERISTICS

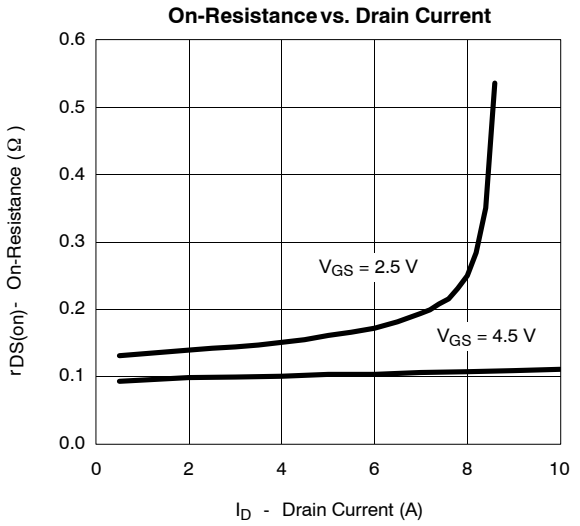
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	-20			V
Drain-Source On-State Resistance[1]	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -2.8A		105	130	mΩ
		V_{GS} = -2.5V, I_D = -2.0A		145	190	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = -250uA	-0.45			V
Zero Gate Voltage Drain Current 0	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	uA
		V_{DS} = -20V, V_{GS} = 0V TJ=55°C			-10	
Gate Body Leakage	I_{GSS}	V_{GS} = ± 8V, V_{DS} = 0V			±100	nA
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -2.8A		6.5	—	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = -6V, I_D ≅ -2.8A V_{GS} = -4.5V		5.8	10	nC
Gate-Source Charge	Q_{gs}			0.85		
Gate-Drain Charge	Q_{gd}			1.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6V, RL=6Ω I_D ≅ -1.A, V_{GEN} = -4.5V R_G = 6Ω		13	25	ns
Turn-On Rise Time	t_r			36	60	
Turn-Off Delay Time	$t_{d(off)}$			42	70	
Turn-Off Fall Time	t_f			34	60	
Input Capacitance	C_{iss}	V_{DS} = -6V, V_{GS} = 0V f = 1.0 MHz		415		pF
Output Capacitance	C_{oss}			223		
Reverse Transfer Capacitance	C_{rss}			87		
Source-Drain Diode						
Max. Diode Forward Current	I_S				-1.6	A
Diode Forward Voltage	V_{SD}	I_S = -1.6A, V_{GS} = 0V		-0.8	-1.2	V

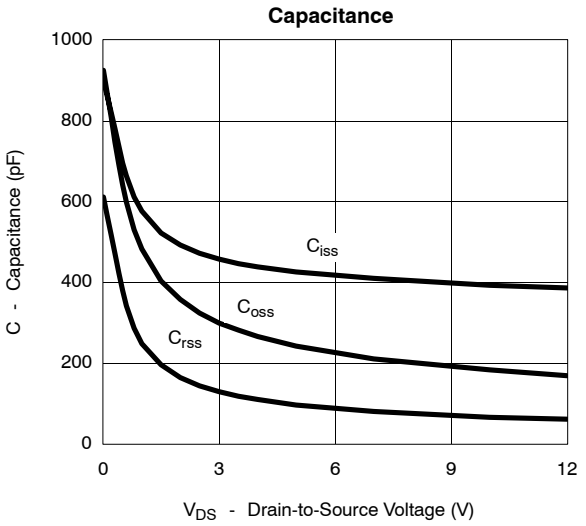
[1] Pulse test: pulse width <= 300us, duty cycle<= 2%

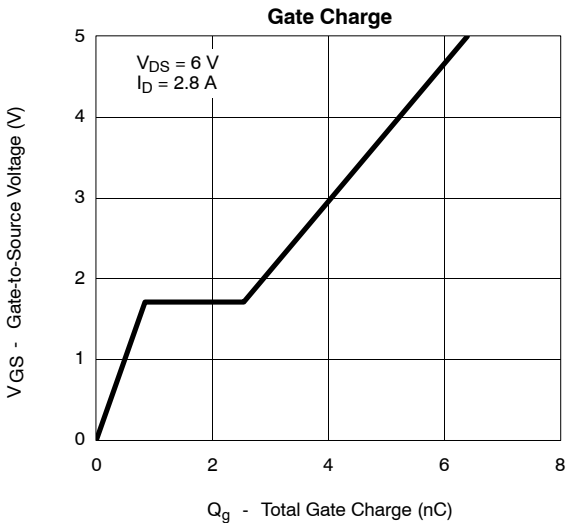
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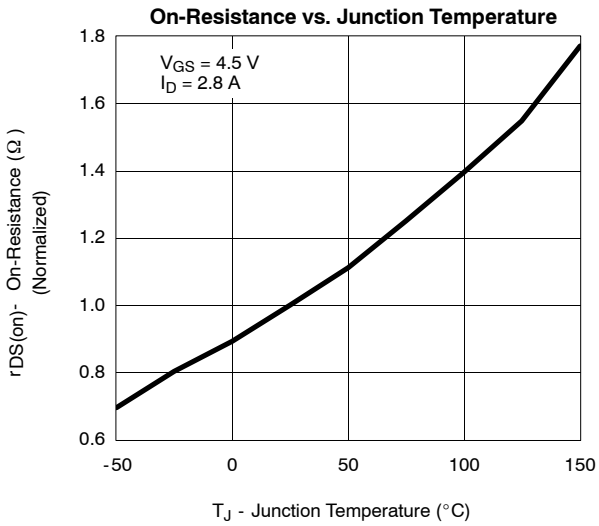






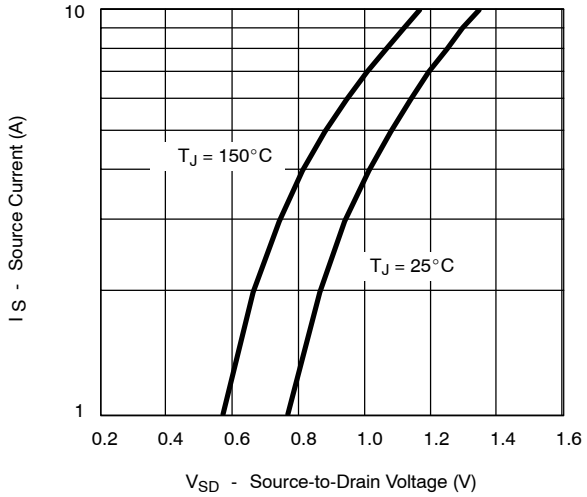




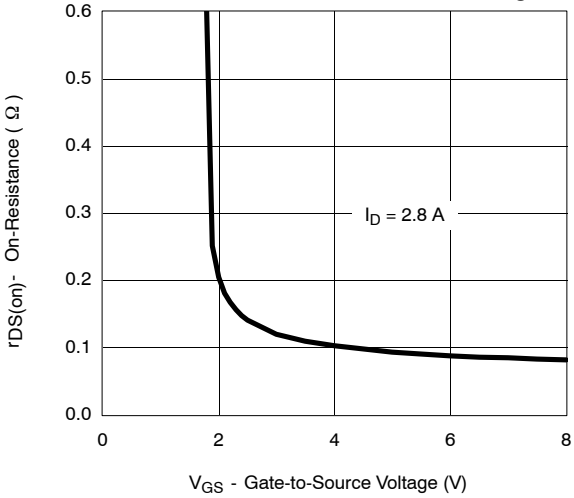


20V P-Channel Enhancement Mode MOSFET

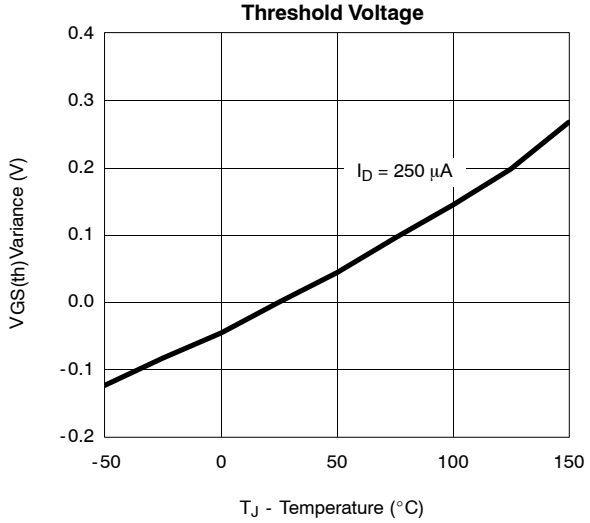
Source-Drain Diode Forward Voltage



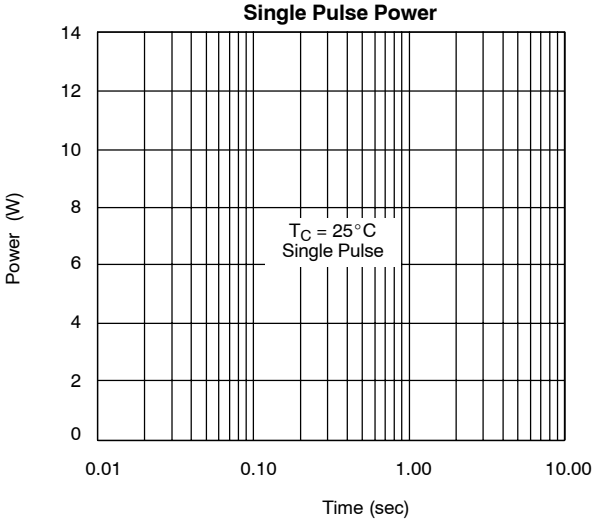
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

