ExpressCard™ POWER INTERFACE SWITCH

Check for Samples: TPS2231 TPS2236

FEATURES

- **Meets the ExpressCard™ Standard (ExpressCard|34 or ExpressCard|54)**
- **Compliant with the ExpressCard™ Compliance Checklists**
- **Fully Satisfies the ExpressCard™ Implementation Guidelines**
- **Supports Systems with WAKE Function**
- **TTL-Logic Compatible Inputs**
- **Short Circuit and Thermal Protection**
- **–40°C to 85°C Ambient Operating Temperature Range**
- **Available in a 20-pin TSSOP, a 20-pin QFN, or 24-pin PowerPAD™ HTSSOP (Single)**
- **Available in a 32-pin PowerPAD™ HTSSOP (Dual)**

APPLICATIONS

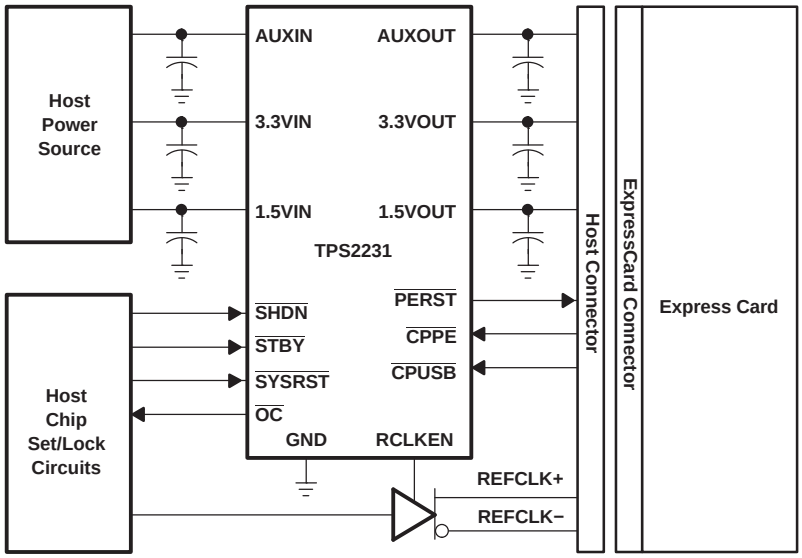
- **Notebook Computers**
- **Desktop Computers**
- **Personal Digital Assistants (PDAs)**
- **Digital Cameras**
- **TV and Set Top Boxes**

DESCRIPTION

The TPS2231 and TPS2236 ExpressCard power interface switches provide the total power management solution required by the ExpressCard specification. The TPS2231 and TPS2236 ExpressCard power interface switches distribute 3.3 V, AUX, and 1.5 V to the ExpressCard socket. Each voltage rail is protected with integrated current-limiting circuitry.

The TPS2231 supports systems with single-slot ExpressCard|34 or ExpressCard|54 sockets. The TPS2236 supports systems with dual-slot ExpressCard sockets.

End equipment for the TPS2231 and TPS2236 include notebook computers, desktop computers, personal digital assistants (PDAs), and digital cameras.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES (1) (2)		
		TSSOP	PowerPAD HTSSOP	QFN
–40°C to 85°C	Single	TPS2231PW	TPS2231PWP	TPS2231RGP
				TPS2231MRGP (3)
				TPS2231MRGP-1 (4)
				TPS2231MRGP-2 (5)
				TPS2231MRGP-3 (6)
	Dual		TPS2236DAP	

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2231PWPR).
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) The TPS2231MRGP is identical to the TPS2231 with the exception of the PowerPAD dimensions. See the Thermal Pad Mechanical data portion of this data sheet for specific information. The thermal pad for the TPS2231MRGP and TPS2231MRGP-1 is 2,2 mm × 2,2 mm; the thermal pad for the TPS2231RGP is 2,7 mm × 2,7 mm.
(4) The TPS2231MRGP-1 is identical to the TPS2231MGRP with the exception that the orientation of the part in the reel is rotated 180°. See the Package Materials Information portion of this data sheet for specific information.
(5) The TPS2231MRGP-2 is identical to the TPS2231MRGP with the exception that the orientation of the part in the reel is rotated 90° and does not have an internal pull-up resistor between AUX IN and $\overline{\text{SYSRST}}$. See the Package Materials Information portion of this data sheet for specific information.
(6) The TPS2231MRGP-3 is identical to the TPS2231MRGP with the exception that the 1.5VIN and 3.3VIN UVLO circuits are independent.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

				TPS223x	UNIT
V_I	Input voltage range for card power	$V_{I(3.3VIN)}$		–0.3 to 6	V
		$V_{I(1.5VIN)}$		–0.3 to 6	V
		$V_{I(AUXIN)}$		–0.3 to 6	V
	Logic input/output voltage			–0.3 to 6	V
V_O	Output voltage range	$V_{O(3.3VOUT)}$		–0.3 to 6	V
		$V_{O(1.5VOUT)}$		–0.3 to 6	V
		$V_{O(AUXOUT)}$		–0.3 to 6	V
	Continuous total power dissipation			See Dissipation Rating Table	
I_O	Output current	$I_{O(3.3VOUT)}$		Internally limited	
		$I_{O(AUXOUT)}$		Internally limited	
		$I_{O(1.5VOUT)}$		Internally limited	
	$\overline{\text{OC}}$ sink current			10	mA
	$\overline{\text{PERST}}$ sink/source current			10	mA
T_J	Operating virtual junction temperature range			–40 to 120	°C
T_{stg}	Storage temperature range			–55 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
ESD	Electrostatic discharge protection	Human body model (HBM) MIL-STD-883C	TPS2231	2	kV
			TPS2236, all pins except $\overline{\text{PERST}}$x and $\overline{\text{OC}}$x		
			TPS2236, $\overline{\text{PERST}}$x and $\overline{\text{OC}}$x	1.5	kV
		Charge device model (CDM)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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DISSIPATION RATINGS (Thermal Resistance = °C/W)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW (20)(1)	704.2 mW	7.41 mW/°C	370.6 mW	259.5 mW
PWP (24)(1)	3153 mW	33.19 mW/°C	1659.5 mW	1161.6 mW
RGP (20) (2)	3277.5 mW	34.5 mW/°C	1725 mW	1207.3 mW
DAP (32) (1) PowerPAD not soldered down	993.4 mW	10.46 mW/°C	522.8 mW	366 mW
DAP (32)(1)	4040.8 mW	42.55 mW/°C	2126.8 mW	1488.7 mW

(1) These devices are mounted on an JEDEC low-k board (2-oz. traces on surface), (The table is assuming that the maximum junction temperature is 120°C). The power pad on the device must be soldered down to the power pad on the board if best thermal performance is needed.
(2) This device is mounted on a JEDEC JESO51.5 high-k board (2 signal, 2 plane). The values assume a maximum junction temperature of 120°C.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{I(3.3VIN)}$	Input voltage	3.3VIN is only required for its respective functions	3	3.6	V
$V_{I(1.5VIN)}$		1.5VIN is only required for its respective functions	1.35	1.65	
$V_{I(AUXIN)}$		AUXIN is required for all circuit operations	3	3.6	
$I_{O(3.3VOUT)}$	Continuous output current	T_J = 120°C	0	1.3	A
$I_{O(1.5VOUT)}$			0	650	mA
$I_{O(AUXOUT)}$			0	275	mA
T_J	Operating virtual junction temperature		–40	120	°C

ELECTRICAL CHARACTERISTICS

T_J = 25°C, $V_{I(3.3VIN)} = V_{I(AUXIN)}$ = 3.3 V, $V_{I(1.5VIN)}$ = 1.5 V, $V_{I(/SHDNx)}$, $V_{I(/STBYx)}$ = 3.3 V, $V_{I(/CPPEx)} = V_{I(/CPUSBx)}$ = 0 V, $V_{I(/SYSRST)}$ = 3.3 V, $\overline{OCx}$ and RCLKENx and $\overline{PERSTx}$ are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH							
	Power switch resistance	3.3VIN to 3.3VOUT with two switches on for dual	T_J = 25°C, I = 1300 mA each		45		mΩ
			T_J = 100°C, I = 1300 mA each			68	
		1.5VIN to 1.5VOUT With two switches on for dual	T_J = 25°C, I = 650 mA each		46		mΩ
			T_J = 100°C, I = 650 mA each			70	
		AUXIN to AUXOUT with two switches on for dual	T_J = 25°C, I = 275 mA each		120		mΩ
			T_J = 100°C, I = 275 mA each			200	
$R_{(DIS_FET)}$	Discharge resistance on 3.3V/1.5V/AUX outputs		$V_{I(/SHDNx)}$ = 0 V, $I_{(discharge)}$ = 1 mA	100		500	Ω
I_{OS}	Short-circuit output current(1)	$I_{OS(3.3VOUT)}$ (steady-state value)	T_J (–40, 120°C]. Output powered into a short	1.35	2	2.5	A
		$I_{OS(1.5VOUT)}$ (steady-state value)		0.67	1	1.3	A
		$I_{OS(AUXOUT)}$(steady-state value)		275	450	600	mA
	Thermal shutdown	Trip point, T_J	Rising temperature, not in overcurrent condition	155	165		°C
			Overcurrent condition	120	130		
		Hysteresis			10		
	Current-limit response time	From short to the 1st threshold within 1.1 times of final current limit, T_J = 25°C	$V_{O(3.3VOUT)}$ with 100-mΩ short		43	100	µs
			$V_{O(1.5VOUT)}$ with 100-mΩ short, TPS2231		100	140	
			$V_{O(1.5VOUT)}$ with 100-mΩ short, TPS2236		110	150	
			$V_{O(AUXOUT)}$ with 100-mΩ short		38	100	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

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ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, $V_{I(3.3VIN)}$ = $V_{I(AUXIN)}$ = 3.3 V, $V_{I(1.5VIN)}$ = 1.5 V, $V_{I(/SHDNx)}$, $V_{I(/STBYx)}$ = 3.3 V, $V_{I(/CPPEx)}$ = $V_{I(/CPUSBx)}$ = 0 V, $V_{I(/SYSRST)}$ = 3.3 V, $\overline{OCx}$ and RCLKENx and $\overline{PERSTx}$ are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER				TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Operation input quiescent current	Normal operation of TPS2236	$I_{I(AUXIN)}$	Outputs are unloaded, T_J [–40, 120°C] (does not include $\overline{CPPEx}$ and $\overline{CPUSBx}$ logic pullup currents)			125	200	µA
			$I_{I(3.3VIN)}$				17.5	25	
			$I_{I(1.5VIN)}$				5.5	15	
		Normal operation of TPS2231	$I_{I(AUXIN)}$				85	150	µA
			$I_{I(3.3VIN)}$				10	15	
			$I_{I(1.5VIN)}$				2.5	10	
I_I	Total input quiescent current	Normal operation of TPS2236	$I_{I(AUXIN)}$	Outputs are unloaded, T_J[–40, 120°C] (include $\overline{CPPEx}$ and $\overline{CPUSBx}$ logic pullup currents)			200	320	µA
			$I_{I(3.3VIN)}$				17.5	25	
			$I_{I(1.5VIN)}$				5.5	15	
		Normal operation of TPS2231	$I_{I(AUXIN)}$				120	210	µA
			$I_{I(3.3VIN)}$				10	15	
			$I_{I(1.5VIN)}$				2.5	10	
		Shutdown mode of TPS2236	$I_{I(AUXIN)}$	$\overline{CPUSB}$ = $\overline{CPPE}$ = 0 V $\overline{SHDN}$ = 0 V (discharge FETs are on) (include $\overline{CPPEx}$ and $\overline{CPUSBx}$ logic pullup currents and $\overline{SHDN}$ pullup current) T_J [–40, 120°C]			250	440	µA
			$I_{I(3.3VIN)}$				3.5	20	
			$I_{I(1.5VIN)}$				0.1	20	
		Shutdown mode of TPS2231	$I_{I(AUXIN)}$				144	270	µA
			$I_{I(3.3VIN)}$				3.5	10	
			$I_{I(1.5VIN)}$				0.5	10	
$I_{lkg(FWD)}$	Forward leakage current	TPS2236	$I_{I(AUXIN)}$	$\overline{SHDN}$ = 3.3 V, $\overline{CPUSB}$ = $\overline{CPPE}$ = 3.3 V (no card present, discharge FETs are on); current measured at input pins, T_J = 120°C, includes RCLKEN pullup current			40	100	µA
			$I_{I(3.3VIN)}$				0.1	100	
			$I_{I(1.5VIN)}$				0.1	100	
		TPS2231	$I_{I(AUXIN)}$				20	50	µA
			$I_{I(3.3VIN)}$				0.1	50	
			$I_{I(1.5VIN)}$				0.1	50	
$I_{lkg(RVS)}$	Reverse leakage current (TPS2236 and TPS2231)	$I_{I(AUXOUT)}$	T_J = 25°C	$V_{O(AUXOUT)}$ = $V_{O(3.3VOUT)}$= 3.3 V; $V_{O(1.5VOUT)}$ = 1.5 V; All voltage inputs are grounded (current measured from output pins going in)			0.1	10	µA
			T_J = 120°C					50	
		$I_{I(3.3VOUT)}$	T_J = 25°C				0.1	10	µA
			T_J = 120°C					50	
		$I_{I(1.5VOUT)}$	T_J = 25°C				0.1	10	µA
			T_J = 120°C					50	
LOGIC SECTION ($\overline{SYSRST}$, $\overline{SHDNx}$, $\overline{STBYx}$, $\overline{PERSTx}$, RCLKENx, $\overline{OCx}$, $\overline{CPUSBx}$, $\overline{CPPEx}$)									
	Logic input supply current	$I_{(\overline{SYSRST})}$	Input	$\overline{SYSRST}$ = 3.6 V, sinking			0	1	µA
				$\overline{SYSRST}$ = 0 V, sourcing	TPS2231-2		0	1	
					TPS2231, TPS2231-1	10		30	
		$I_{(\overline{SHDNx})}$	Input	$\overline{SHDNx}$ = 3.6 V, sinking			0	1	µA
				$\overline{SHDNx}$ = 0 V, sourcing		10		30	
		$I_{(\overline{STBYx})}$	Input	$\overline{STBYx}$ = 3.6 V, sinking			0	1	µA
				$\overline{STBYx}$ = 0 V, sourcing		10		30	
		$I_{(RCLKENx)}$	Input	RCLKENx = 0 V, sourcing		10		30	µA
		$I_{(\overline{CPUSBx})}$ or $I_{(\overline{CPPEx})}$	Inputs	$\overline{CPUSB}$ or $\overline{CPPE}$ = 0 V, sinking			0	1	µA
				$\overline{CPUSB}$ or $\overline{CPPE}$ = 3.6 V, sourcing		10		30	
	Logic input voltage	High level				2			V
		Low level						0.8	
	RCLEN output low voltage		Output	$I_{O(RCLKEN)}$ = 60 µA				0.4	V
	$\overline{PERST}$ assertion threshold of output voltage ($\overline{PERST}$ asserted when any output voltage falls below the threshold)			3.3VOUT falling		2.7		3	V
				AUXOUT falling		2.7		3	
				1.5VOUT falling		1.2		1.35	
	$\overline{PERST}$ assertion delay from output voltage			3.3VOUT, AUXOUT, or 1.5VOUT falling				500	ns

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ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, $V_{I(3.3VIN)}$ = $V_{I(AUXIN)}$ = 3.3 V, $V_{I(1.5VIN)}$ = 1.5 V, $V_{I(/SHDNx)}$, $V_{I(/STBYx)}$ = 3.3 V, $V_{I(/CPPEx)}$ = $V_{I(/CPUSBx)}$ = 0 V, $V_{I(/SYSRST)}$ = 3.3 V, $\overline{OC}$x and RCLKENx and $\overline{PERST}$x are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	$\overline{PERST}$ de-assertion delay from output voltage	3.3VOUT, AUXOUT, and 1.5VOUT rising within tolerance	4	10	20	ms
	$\overline{PERST}$ assertion delay from $\overline{SYSRST}$	Max time from $\overline{SYSRST}$ asserted or de-asserted			500	ns
$t_{W(PERST)}$	$\overline{PERST}$ minimum pulse width	3.3VOUT, AUXOUT, or 1.5VOUT falling out of tolerance or triggered by $\overline{SYSRST}$	100	250		µs
	$\overline{PERST}$ output low voltage	$I_{O(PERST)}$ = 500 µA			0.4	V
	$\overline{PERST}$ output high voltage		2.4			V
	$\overline{OC}$ output low voltage	$I_{O(/OC)}$ = 2 mA			0.4	V
	$\overline{OC}$ leakage current	$V_{O(/OC)}$ = 3.6 V			1	µA
	$\overline{OC}$ deglitch	Falling into or out of an overcurrent condition	6		20	mS
UNDERVOLTAGE LOCKOUT (UVLO)						
	3.3VIN UVLO	3.3VIN level, below which 3.3VIN and 1.5VIN switches are off	2.6		2.9	V
		3.3VIN level, below which 3.3VIN switch is off (TPS2231-3 only)				
	1.5VIN UVLO	1.5VIN level, below which 3.3VIN and 1.5VIN switches are off	1		1.25	
		1.5VIN level, below which 1.5VIN switch is off (TPS2231-3 only)				
	AUXIN UVLO	AUXIN level, below which all switches are off	2.6		2.9	
	UVLO hysteresis			100		mV

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SWITCHING CHARACTERISTICS

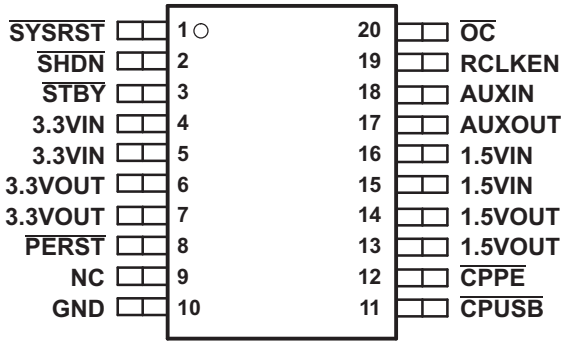
T_J = 25°C, $V_{I(3.3VIN)}$ = $V_{I(AUXIN)}$ = 3.3 V, $V_{I(1.5VIN)}$ = 1.5 V, $V_{I(/SHDNx)}$, $V_{I(/STBYx)}$ = 3.3 V, $V_{I(/CPPEx)}$ = $V_{I(/CPUSBx)}$ = 0 V, $V_{I(/SYSRST)}$ = 3.3 V, OCx and RCLKENx and PERSTx are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise times	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 0.1 µF, $I_{O(3.3VOUT)}$ = 0 A	0.1		3	ms
		AUXIN to AUXOUT	$C_{L(AUXOUT)}$ = 0.1 µF, $I_{O(AUXOUT)}$ = 0 A	0.1		3	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 0.1 µF, $I_{O(1.5VOUT)}$ = 0 A	0.1		3	
		3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 100 µF, R_L = $V_{I(3.3VIN)}$/1 A	0.1		6	
		AUXIN to AUXOUT	$C_{L(AUXOUT)}$ = 100 µF, R_L = $V_{I(AUXIN)}$/0.250 A	0.1		6	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 100 µF, R_L = $V_{I(1.5VIN)}$/0.500 A	0.1		6	
t_f	Output fall times when card removed (both CPUSB and CPPE de-asserted)	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 0.1 µF, $I_{O(3.3VOUT)}$ = 0 A	10		150	µs
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 0.1 µF, $I_{O(AUXOUT)}$ = 0 A	10		150	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 0.1 µF, $I_{O(1.5VOUT)}$ = 0 A	10		150	
		3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 20 µF, $I_{O(3.3VOUT)}$ = 0 A	2		30	ms
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 20 µF, $I_{O(AUXOUT)}$ = 0 A	2		30	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 20 µF, $I_{O(1.5VOUT)}$ = 0 A	2		30	
t_f	Output fall times when SHDN asserted (card is present)	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 0.1 µF, $I_{O(3.3VOUT)}$ = 0 A	10		150	µs
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 0.1 µF, $I_{O(AUXOUT)}$ = 0 A	10		150	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 0.1 µF, $I_{O(1.5VOUT)}$ = 0 A	10		150	
		3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 100 µF, R_L = $V_{I(3.3VIN)}$/1 A	0.1		5	ms
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 100 µF R_L = $V_{I(AUXIN)}$/0.250 A	0.1		5	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 100 µF, R_L = $V_{I(1.5VIN)}$/0.500 A	0.1		5	
$t_{pd(on)}$	Turn-on propagation delay	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 0.1 µF, $I_{O(3.3VOUT)}$ = 0 A	0.1		1	ms
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 0.1 µF, $I_{O(AUXOUT)}$ = 0A	0.05		0.5	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 0.1 µF, $I_{O(1.5VOUT)}$ = 0 A	0.1		1	
		3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 100 µF, R_L = $V_{I(3.3VIN)}$/1 A	0.1		1.5	
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 100 µF, R_L = $V_{I(AUXIN)}$/0.250 A	0.05		1	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 100 µF, R_L = $V_{I(1.5VIN)}$/0.500 A	0.1		1.5	
$t_{pd(off)}$	Turn-off propagation delay	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 0.1 µF, $I_{O(3.3VOUT)}$ = 0 A	0.1		1.5	ms
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 0.1 µF, $I_{O(AUXOUT)}$ = 0 A	0.05		0.5	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 0.1 µF, $I_{O(1.5VOUT)}$ = 0 A	0.1		1.5	
		3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$ = 100 µF, R_L = $V_{I(3.3VIN)}$/1 A	0.1		1.5	
		AUXIN to VAUXOUT	$C_{L(AUXOUT)}$ = 100 µF, R_L = $V_{I(AUXIN)}$/0.250 A	0.05		0.5	
		1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$ = 100 µF, R_L = $V_{I(1.5VIN)}$/0.500 A	0.1		1	

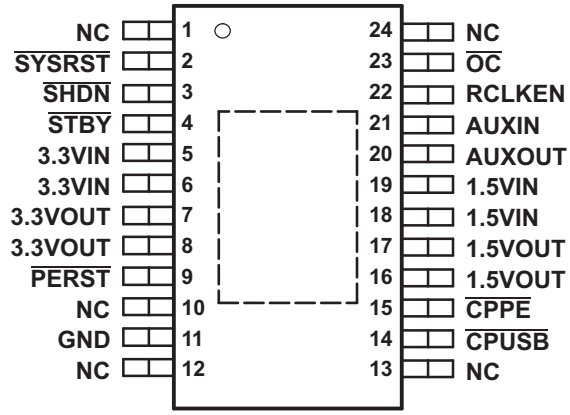
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PIN ASSIGNMENTS

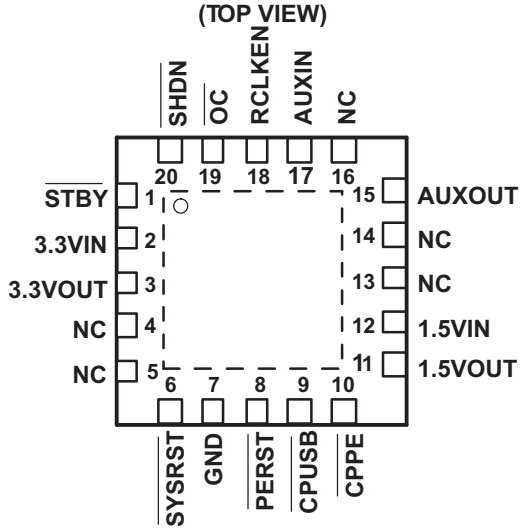
TPS2231
PW PACKAGE
(TOP VIEW)



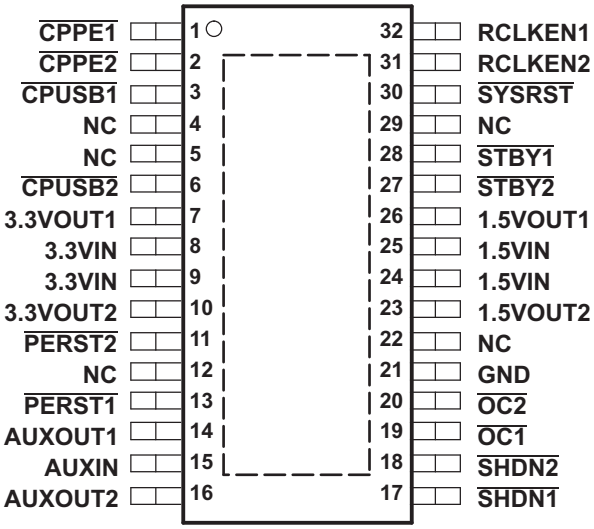
TPS2231
PWP PACKAGE
(TOP VIEW)



TPS2231
RGP PACKAGE
(TOP VIEW)



TPS2236
DAP PACKAGE
(TOP VIEW)



NC - No internal connection

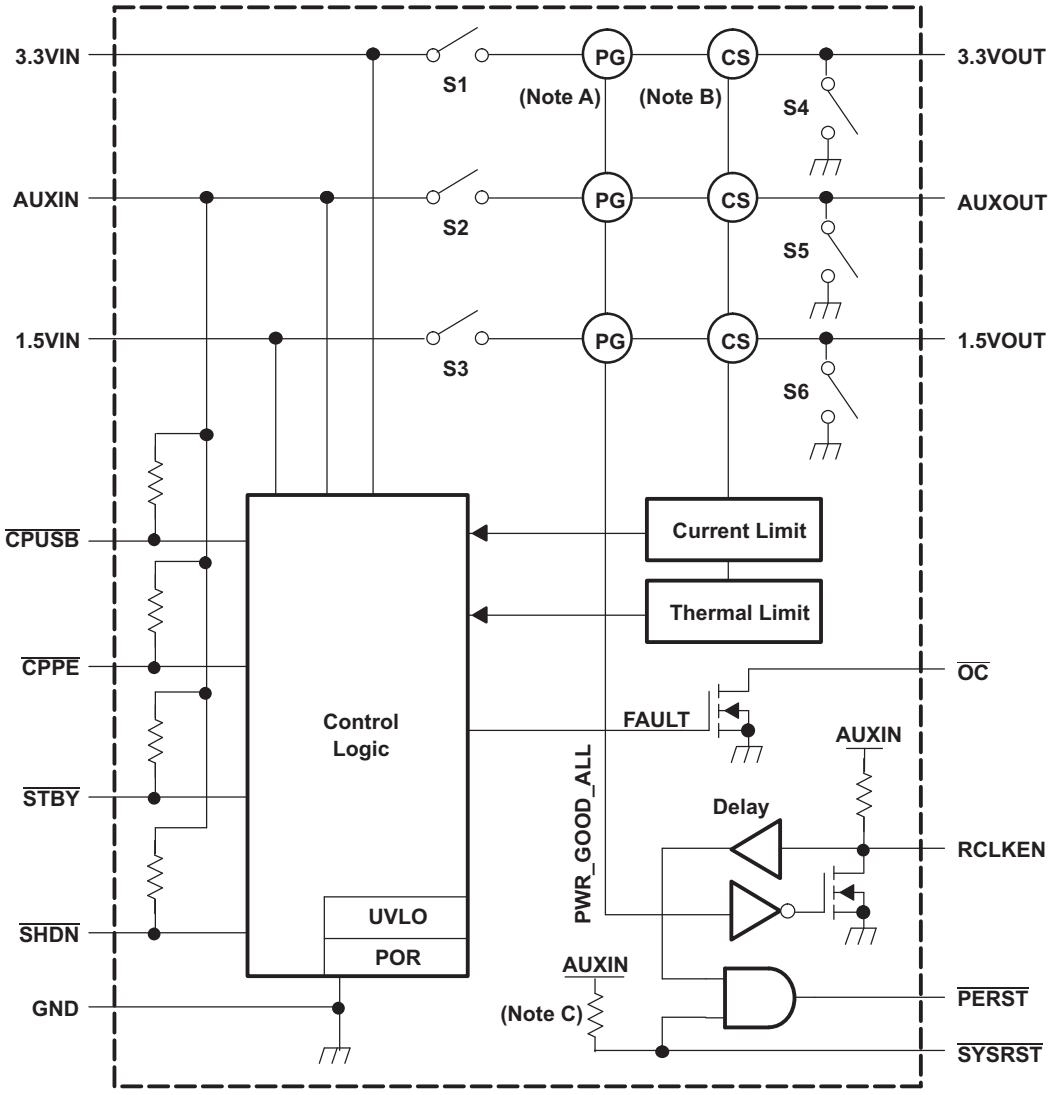
TERMINAL FUNCTIONS

TERMINAL						I/O	DESCRIPTION
TPS2231				TPS2236			
NAME	NO.			NAME	NO.		
	PW	PWP	RGP		DAP		
3.3VIN	4, 5	5, 6	2	3.3VIN	8, 9	I	3.3-V input for 3.3VOUT
1.5VIN	15, 16	18, 19	12	1.5VIN	24, 25	I	1.5-V input for 1.5VOUT
AUXIN	18	21	17	AUXIN	15	I	AUX input for AUXOUT and chip power
GND	10	11	7	GND	21		Ground
3.3VOUT	6, 7	7, 8	3	3.3VOUT1	7	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
1.5VOUT	13, 14	16, 17	11	1.5VOUT1	26	O	Switched output that delivers 0 V, 1.5 V or high impedance to card
AUXOUT	17	20	15	AUXOUT1	14	O	Switched output that delivers 0 V, AUX or high impedance to card
				3.3VOUT2	10	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
				1.5VOUT2	23	O	Switched output that delivers 0 V, 1.5 V or high impedance to card
				AUXOUT2	16	O	Switched output that delivers 0 V, AUX or high impedance to card
$\overline{\text{SYSRST}}$	1	2	6	$\overline{\text{SYSRST}}$	30	I	System Reset input – active low, logic level signal. Internally pulled up to AUXIN.
$\overline{\text{CPPE}}$	12	15	10	$\overline{\text{CPPE1}}$	1	I	Card Present input for PCI Express cards. Internally pulled up to AUXIN
$\overline{\text{CPUSB}}$	11	14	9	$\overline{\text{CPUSB1}}$	3	I	Card Present input for USB cards. Internally pulled up to AUXIN.
				$\overline{\text{CPPE2}}$	2	I	Card Present input for PCI Express cards. Internally pulled up to AUXIN.
				$\overline{\text{CPUSB2}}$	6	I	Card Present input for USB cards. Internally pulled up to AUXIN.
$\overline{\text{PERST}}$	8	9	8	$\overline{\text{PERST1}}$	13	O	A logic level power good to slot 0 (with delay)
				$\overline{\text{PERST2}}$	11	O	A logic level power good to slot 1 (with delay)
$\overline{\text{SHDN}}$	2	3	20	$\overline{\text{SHDN1}}$	17	I	Shutdown input – active low, logic level signal. Internally pulled up to AUXIN.
				$\overline{\text{SHDN2}}$	18	I	Shutdown input – active low, logic level signal. Internally pulled up to AUXIN.
$\overline{\text{STBY}}$	3	4	1	$\overline{\text{STBY1}}$	28	I	Standby input – active low, logic level signal. Internally pulled up to AUXIN.
				$\overline{\text{STBY2}}$	27	I	Standby input – active low, logic level signal. Internally pulled up to AUXIN.
RCLKEN	19	22	18	RCLKEN1	32	I/O	Reference Clock Enable signal. As an output, a logic level power good to host for slot 0 (no delay – open drain). As an input, if kept inactive (low) by the host, prevents $\overline{\text{PERST}}$ from being de-asserted. Internally pulled up to AUXIN.
				RCLKEN2	31	I/O	Reference Clock Enable signal. As an output, a logic level power good to host for slot 1 (no delay – open drain). As an input, if kept inactive (low) by the host, prevents $\overline{\text{PERST}}$ from being de-asserted. Internally pulled up to AUXIN.
$\overline{\text{OC}}$	20	23	19	$\overline{\text{OC1}}$	19	O	Overcurrent status output for slot 0 (open drain)
				$\overline{\text{OC2}}$	20	O	Overcurrent status output for slot 1 (open drain)
NC	9	1, 10, 12, 13, 24	4, 5, 13, 14, 16	NC	4, 5, 12, 22, 29		No connection

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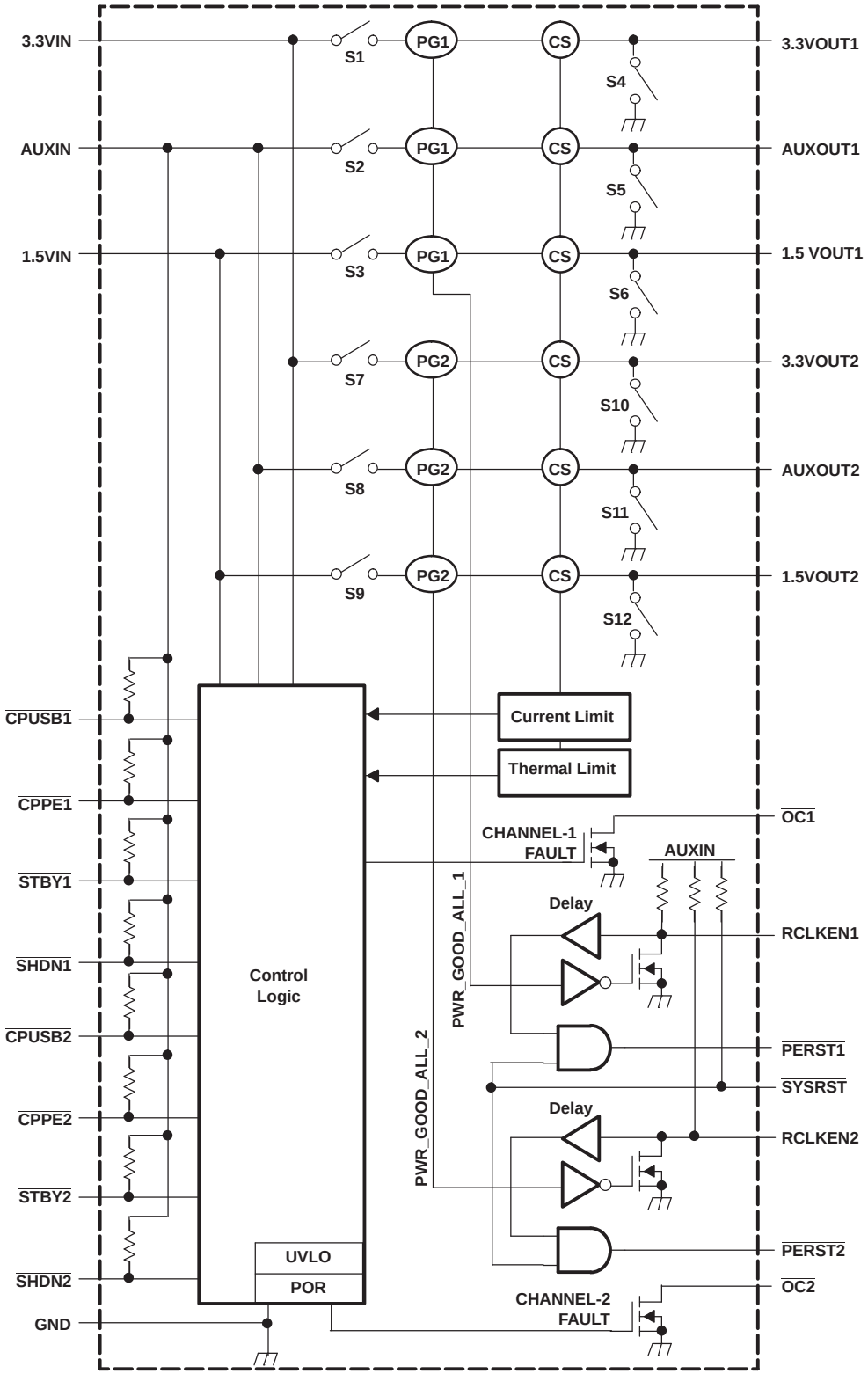
FUNCTIONAL BLOCK DIAGRAM

Single ExpressCard Power Switch



Note A: PG = power good
Note B: CS = current sense
Note C: TPS2231MRGP-2 does not have a pull-up resistor.

Dual ExpressCard Power Switch



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DETAILED PIN DESCRIPTIONS

$\overline{\text{CPPE}}$

A logic low level on this input indicates that the card present supports PCI Express functions. $\overline{\text{CPPE}}$ connects to the AUXIN input through an internal pullup. When a card is inserted, $\overline{\text{CPPE}}$ is physically connected to ground if the card supports PCI Express functions.

$\overline{\text{CPUSB}}$

A logic low level on this input indicates that the card present supports USB functions. $\overline{\text{CPUSB}}$ connects to the AUXIN input through an internal pullup. When a card is inserted, $\overline{\text{CPUSB}}$ is physically connected to ground if the card supports USB functions.

$\overline{\text{SHDN}}$

When asserted (logic low), this input instructs the power switch to turn off all voltage outputs and the discharge FETs are activated. $\overline{\text{SHDN}}$ has an internal pullup connected to AUXIN.

$\overline{\text{STBY}}$

When asserted (logic low) after the card is inserted, this input places the power switch in standby mode by turning off the 3.3-V and 1.5-V power switches and keeping the AUX switch on. If asserted prior to the card being present, $\overline{\text{STBY}}$ places the power switch in OFF Mode by turning off the AUX, 3.3-V, and 1.5-V power switches. $\overline{\text{STBY}}$ has an internal pullup connected to AUXIN.

RCLKEN

This pin serves as both an input and an output. On power up, a discharge FET keeps this signal at a low state as long as any of the output power rails are out of their tolerance range. Once all output power rails are within tolerance, the switch releases RCLKEN allowing it to transition to a high state (internally pulled up to AUXIN). The transition of RCLKEN from a low to a high state starts an internal timer for the purpose of deasserting $\overline{\text{PERST}}$. As an input, RCLKEN can be kept low to delay the start of the $\overline{\text{PERST}}$ internal timer.

Because RCLKEN is internally connected to a discharge FET, this pin can only be driven low and should never be driven high as a logic input. When an external circuit drives this pin low, RCLKEN becomes an input; otherwise, this pin is an output.

RCLKEN can be used by the host system to enable a clock driver.

$\overline{\text{PERST}}$

On power up, this output remains asserted (logic level low) until all power rails are within tolerance. Once all power rails are within tolerance and RCLKEN has been released (logic high), $\overline{\text{PERST}}$ is deasserted (logic high) after a time delay as shown in the parametric table. On power down, this output is asserted whenever any of the power rails drop below their voltage tolerance.

The $\overline{\text{PERST}}$ signal is an output from the host system and an input to the ExpressCard module. This signal is only used by PCI Express-based modules and its function is to place the ExpressCard module in a reset state.

During power up, power down, or whenever power to the ExpressCard module is not stable or not within voltage tolerance limits, the ExpressCard standard requires that $\overline{\text{PERST}}$ be asserted. As a result, this signal also serves as a power-good indicator to the ExpressCard module, and the relationship between the power rails and $\overline{\text{PERST}}$ are explicitly defined in the ExpressCard standard.

The host can also place the ExpressCard module in a reset state by asserting a system reset $\overline{\text{SYSRST}}$. This system reset generates a $\overline{\text{PERST}}$ to the ExpressCard module without disrupting the voltage rails. This is what is normally called a *warm* reset. However, in a *cold* start situation, the system reset can also be used to extend the length of time that $\overline{\text{PERST}}$ is asserted.

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$\overline{\text{SYSRST}}$

This input is driven by the host system and directly affects $\overline{\text{PERST}}$. Asserting $\overline{\text{SYSRST}}$ (logic low) forces $\overline{\text{PERST}}$ to assert. RCLKEN is not affected by the assertion of $\overline{\text{SYSRST}}$. $\overline{\text{SYSRST}}$ has an internal pullup connected to AUXIN.

$\overline{\text{OC}}$

This pin is an open-drain output. When any of the three power switches (AUX, 3.3V, and 1.5V) is in an overcurrent condition, $\overline{\text{OC}}$ is asserted (logic low) by an internal discharge FET with a deglitch delay. Otherwise, the discharge FET is open, and the pin can be pulled up to a power supply through an external resistor.

FUNCTIONAL TRUTH TABLES

Truth Table for Voltage Outputs

VOLTAGE INPUTS (1)			LOGIC INPUTS			VOLTAGE OUTPUTS (2)			MODE (3)
AUXIN	3.3VIN	1.5VIN	$\overline{\text{SHDN}}$	$\overline{\text{STBY}}$	$\overline{\text{CP}}$ (4)	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

(1) For input voltages, *On* means the respective input voltage is higher than its turnon threshold voltage; otherwise, the voltage is *Off* (for AUX input,*Off* means the voltage is close to zero volt).
(2) For output voltages, *On* means the respective power switch is turned on so the input voltage is connected to the output; *Off* means the power switch and its output discharge FET are both off; *GND* means the power switch is off but the output discharge FET is on so the voltage on the output is pulled down to 0 V.
(3) *Mode* assigns each set of input conditions and respective output voltage results to a different name. These modes are referred to as input conditions in the following *Truth Table for Logic Outputs*.
(4) $\overline{\text{CP}}$ = $\overline{\text{CPUSB}}$ and $\overline{\text{CPPE}}$ – equal to 1 when both $\overline{\text{CPUSB}}$ and $\overline{\text{CPPE}}$ signals are logic high, or equal to 0 when either $\overline{\text{CPUSB}}$ or $\overline{\text{CPPE}}$ is low.

Truth Table for Logic Outputs

INPUT CONDITIONS			LOGIC OUTPUTS	
MODE	$\overline{\text{SYSRST}}$	RCLKEN (1)	$\overline{\text{PERST}}$	RCLKEN (2)
OFF	X	X	0	0
Shutdown				
No Card				
Standby				
Card Inserted	0	Hi-Z	0	1
	0	0	0	0
	1	Hi-Z	1	1
	1	0	0	0

(1) RCLKEN as a logic input in this column. RCLKEN is an I/O pin and it can be driven low externally, left open, or connected to high-impedance terminals, such as the gate of a MOSFET. It must not be driven high externally.
(2) RCLKEN as a logic output in this column.

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POWER STATES

If AUXIN is not present, then all input-to-output power switches are kept off (*OFF* mode).

If AUXIN is present and $\overline{\text{SHDN}}$ is asserted (logic low), then all input-to-output power switches are kept off and the output discharge FETs are turned on (*Shutdown* mode). If $\overline{\text{SHDN}}$ is asserted and then de-asserted, the state on the outputs is restored to the state prior to $\overline{\text{SHDN}}$ assertion.

If 3.3VIN, AUXIN and 1.5VIN are present at the input of the power switch and no card is inserted, then all input-to-output power switches are kept off and the output discharge FETs are turned on (*No Card* mode).

If 3.3VIN, AUXIN and 1.5VIN are present at the input of the power switch prior to a card being inserted, then all input-to-output power switches are turned on once a card-present signal ($\overline{\text{CPUSB}}$ and/or $\overline{\text{CPPE}}$) is detected (*Card Inserted* mode).

If a card is present and all output voltages are being applied, then the $\overline{\text{STBY}}$ is asserted (logic low); the AUXOUT voltage is provided to the card, and the 3.3VOUT and 1.5VOUT switches are turned off (*Standby* mode).

If a card is present and all output voltages are being applied, then the 1.5VIN, or 3.3VIN is removed from the input of the power switch; the AUXOUT voltage is provided to the card and the 3.3VOUT and 1.5VOUT switches are turned off (*Standby* mode). TPS2231-3 only: If 3.3VIN is removed, the 3.3VOUT switch is turned off; and, the 1.5VOUT switch is unaffected. If 1.5VIN is removed, the 1.5VOUT switch is turned off; and, the 3.3VOUT switch is unaffected.

If prior to the insertion of a card, the AUXIN is available at the input of the power switch and 3.3VIN and/or 1.5VIN are not, or if $\overline{\text{STBY}}$ is asserted (logic low), then no power is made available to the card (*OFF* mode). If 1.5VIN and 3.3VIN are made available at the input of the power switch after the card is inserted and $\overline{\text{STBY}}$ is not asserted, all the output voltages are made available to the card (*Card Inserted* mode). TPS2231-3 only: If 1.5VIN or 3.3VIN is made available at the input of the power switch after the card is inserted and $\overline{\text{STBY}}$ is not asserted, all switches above their individual UVLO thresholds will turn on.

DISCHARGE FETs

The discharge FETs on the outputs are activated whenever the device detects that a card is not present (*No Card* mode). Activation occurs after the input-to-output power switches are turned off (break before make). The discharge FETs de-activate if either of the card-present lines go active low, unless the $\overline{\text{SHDN}}$ pin is asserted.

The discharge FETs are also activated whenever the $\overline{\text{SHDN}}$ input is asserted and stay asserted until $\overline{\text{SHDN}}$ is de-asserted.

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PARAMETER MEASUREMENT INFORMATION

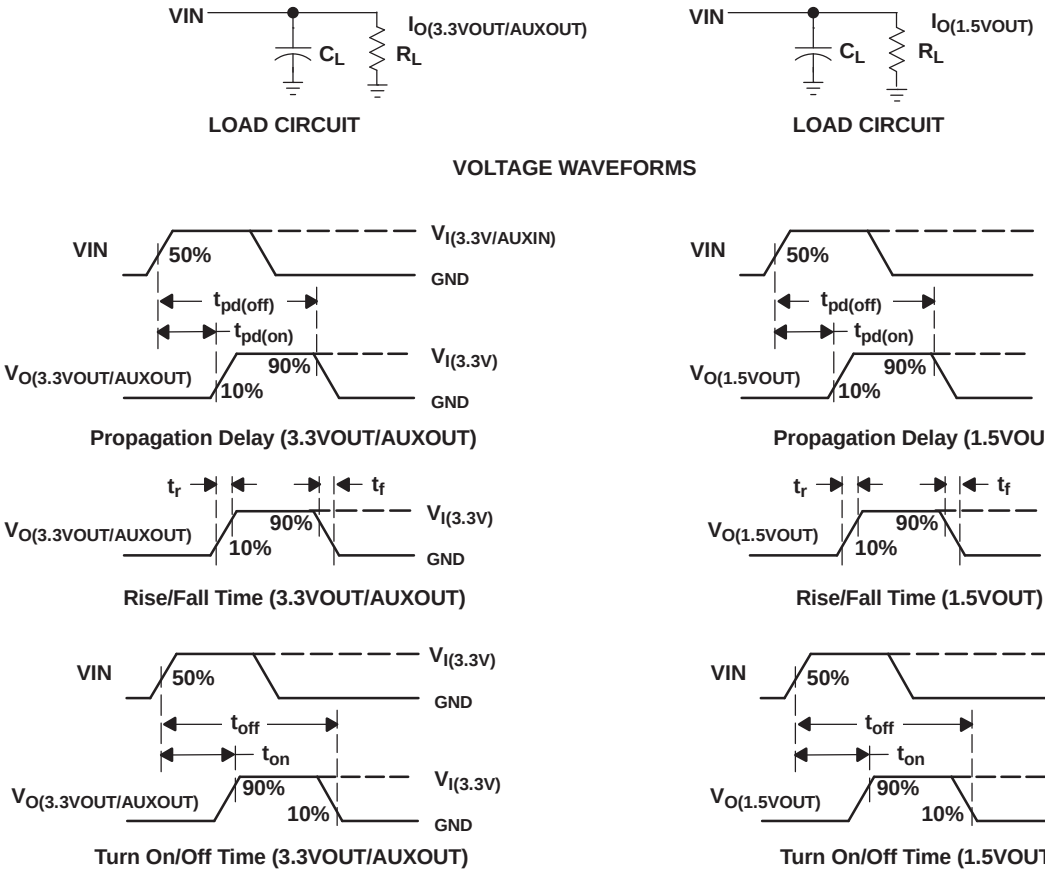


Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

		FIGURE
Output voltage when card is inserted	vs Time	2
RCLKEN and $\overline{\text{PERST}}$ voltage during power up	vs Time	3
RCLKEN and $\overline{\text{PERST}}$ voltage during power down	vs Time	4
$\overline{\text{PERST}}$ asserted by $\overline{\text{SYSRST}}$ when power is on	vs Time	5
$\overline{\text{PERST}}$ de-asserted by $\overline{\text{SYSRST}}$ when power is on	vs Time	6
Output voltage when 3.3VIN is removed	vs Time	7
Output voltage when 1.5VIN is removed	vs Time	8
$\overline{\text{OC}}$ response when powered into a short (3.3VOUT)	vs Time	9
Supply current of AUXIN	vs Junction temperature	10
Static drain-source on-state resistance	vs Junction temperature	11
3.3-V power switch current limit	vs Junction temperature	12
1.5-V power switch current limit	vs Junction temperature	13
AUX power switch current limit	vs Junction temperature	14
3.3-V power switch current limit trip	vs Junction temperature	15
1.5-V power switch current limit trip	vs Junction temperature	16
AUX power switch current limit trip	vs Junction temperature	17

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OUTPUT VOLTAGE WHEN CARD IS INSERTED vs TIME

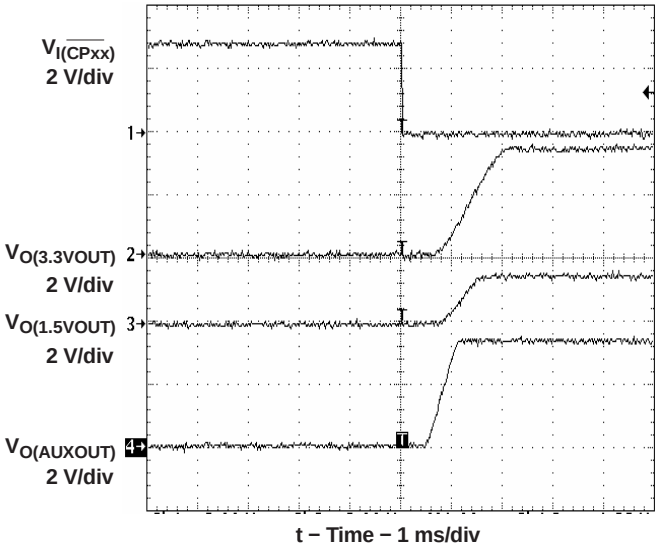


Figure 2.

RCLKEN AND $\overline{PERST}$ VOLTAGE DURING POWER UP vs TIME

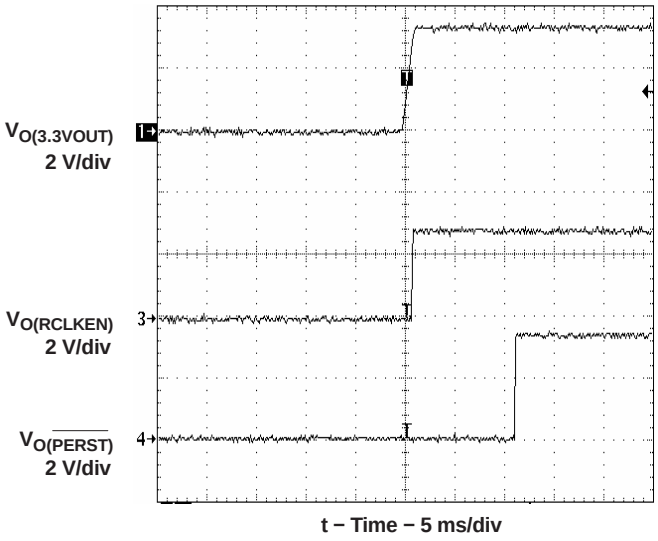


Figure 3.

RCLKEN AND $\overline{PERST}$ VOLTAGE DURING POWER DOWN vs TIME

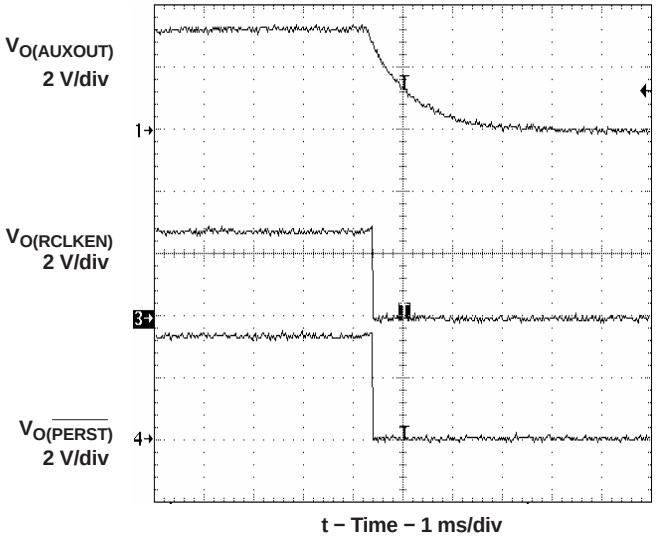


Figure 4.

$\overline{PERST}$ ASSERTED BY $\overline{SYSRST}$ WHEN POWER IS ON vs TIME

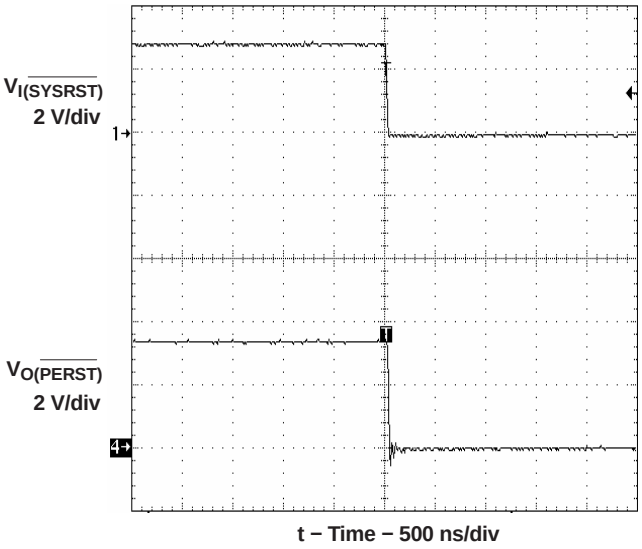


Figure 5.

$\overline{\text{PERST}}$ DE-ASSERTED BY $\overline{\text{SYSRST}}$ WHEN POWER IS ON
vs
TIME

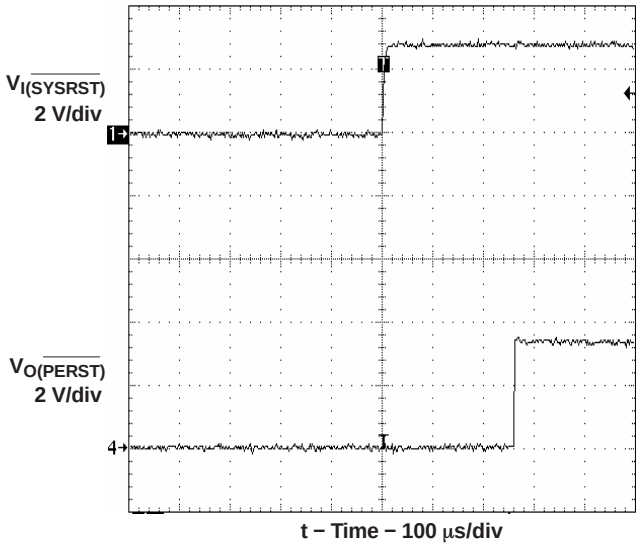


Figure 6.

OUTPUT VOLTAGE WHEN 3.3VIN IS REMOVED
vs
TIME

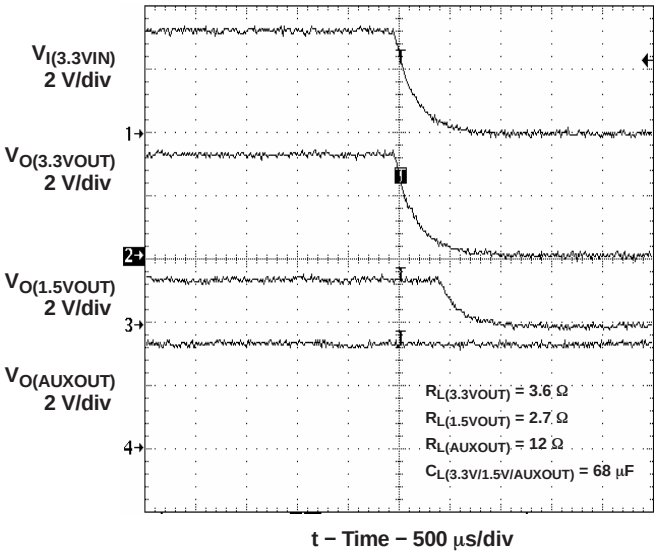


Figure 7.

OUTPUT VOLTAGE WHEN 1.5VIN IS REMOVED
vs
TIME

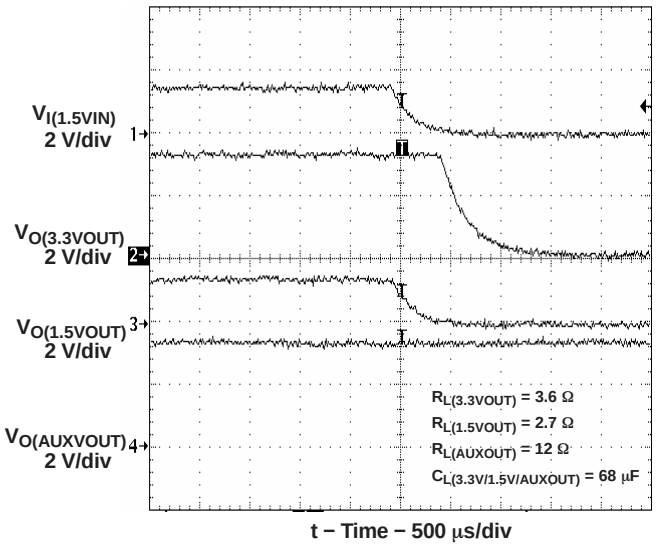


Figure 8.

$\overline{\text{OC}}$ RESPONSE WHEN POWERED INTO A SHORT (3.3VOUT)
vs
TIME

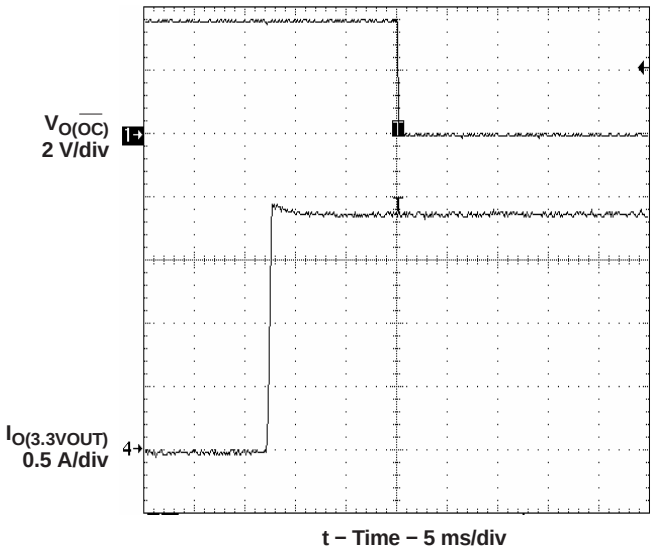


Figure 9.

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SUPPLY CURRENT OF AUXIN vs JUNCTION TEMPERATURE

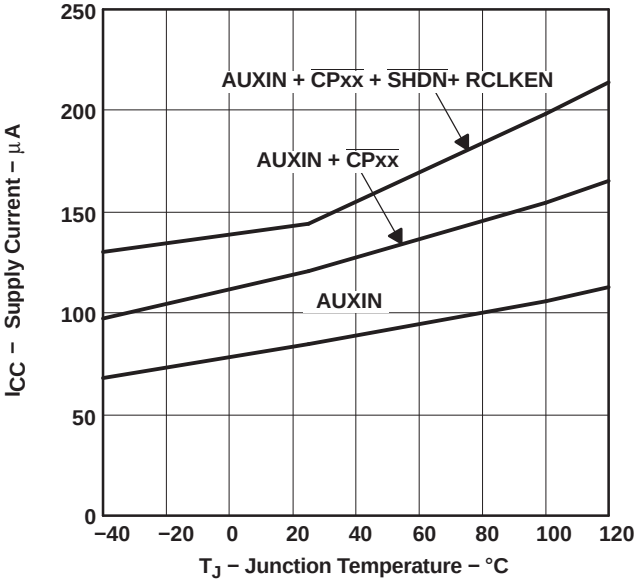


Figure 10.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

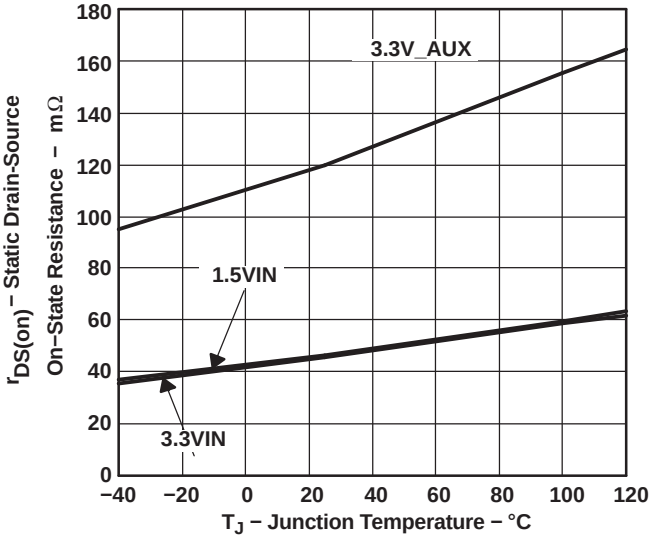


Figure 11.

3.3-V POWER SWITCH CURRENT LIMIT vs JUNCTION TEMPERATURE

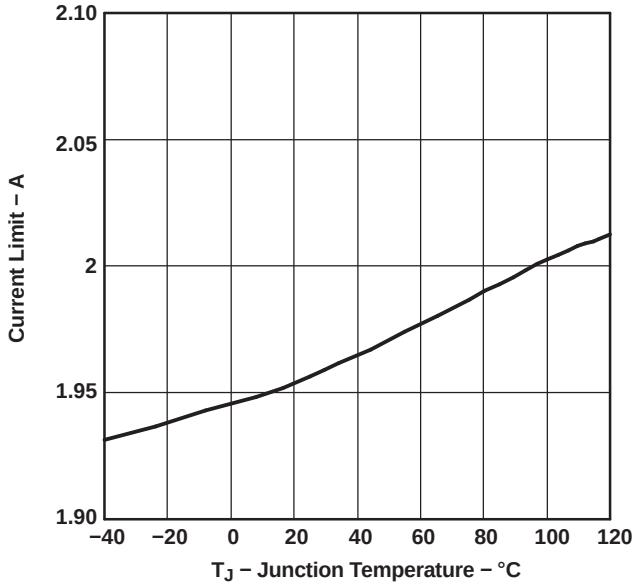


Figure 12.

1.5-V POWER SWITCH CURRENT LIMIT vs JUNCTION TEMPERATURE

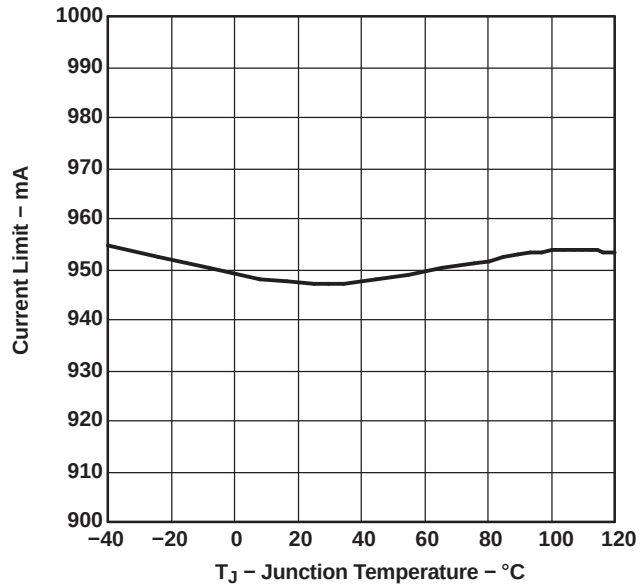


Figure 13.

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AUX POWER SWITCH CURRENT LIMIT
vs
JUNCTION TEMPERATURE

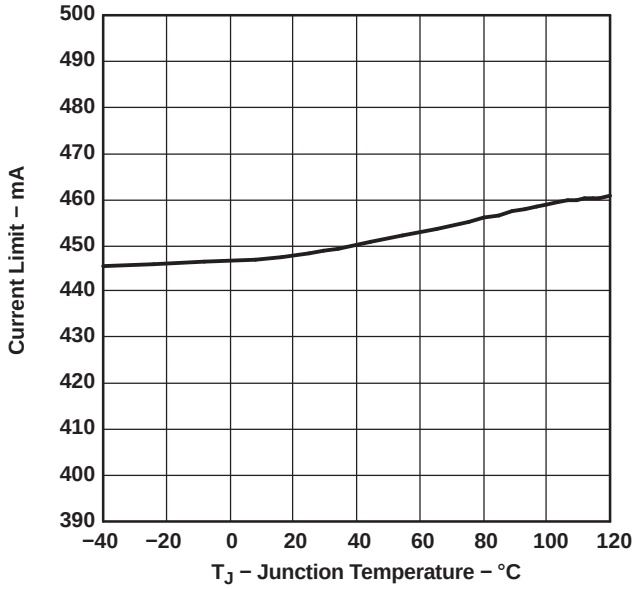


Figure 14.

3.3-V POWER SWITCH CURRENT LIMIT TRIP
vs
JUNCTION TEMPERATURE

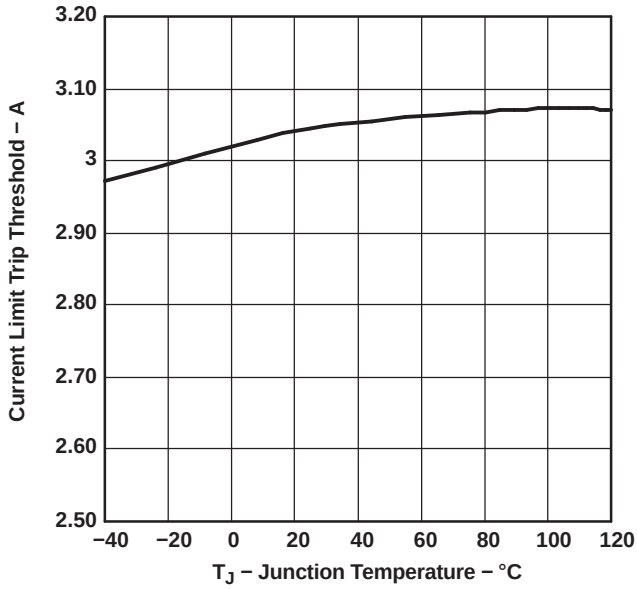


Figure 15.

1.5-V POWER SWITCH CURRENT LIMIT TRIP
vs
JUNCTION TEMPERATURE

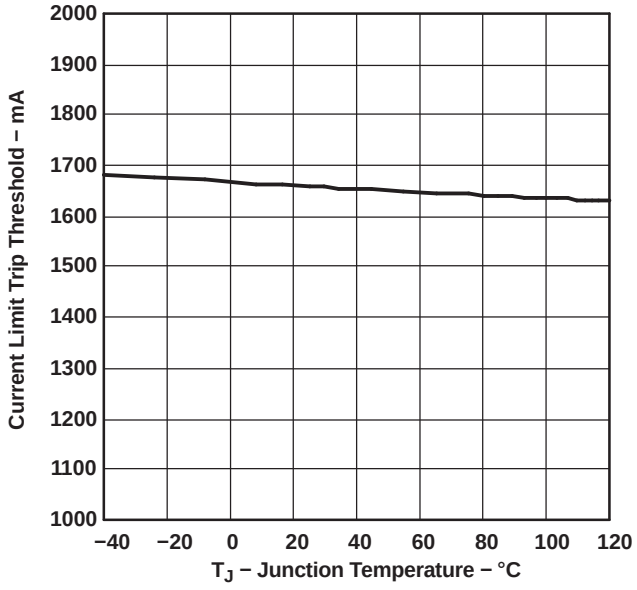


Figure 16.

AUX POWER SWITCH CURRENT LIMIT TRIP
vs
JUNCTION TEMPERATURE

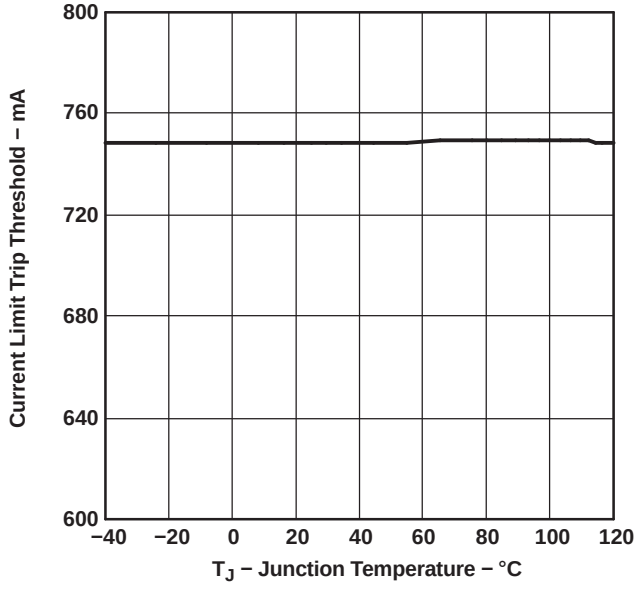


Figure 17.

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APPLICATION INFORMATION

INTRODUCTION TO ExpressCard

An ExpressCard module is an add-in card with a serial interface based on PCI Express and/or Universal Serial Bus (USB) technologies. An ExpressCard comes in two form factors defined as ExpressCard|34 or ExpressCard|54. The difference, as defined by the name, is the width of the module, 34 mm or 54 mm, respectively. Host systems supporting the ExpressCard module can support either the ExpressCard|34 or ExpressCard|54 or both.

ExpressCard POWER REQUIREMENTS

Regardless of which ExpressCard module is used, the power requirements as defined in the ExpressCard Standard apply to both on an individual slot basis. The host system is required to supply 3.3 V, 1.5 V, and AUX to each of the ExpressCard slots. However, the voltage is only applied after an ExpressCard is inserted into the slot.

The ExpressCard connector has two pins, $\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$, that are used to signal the host when a card is inserted. If the ExpressCard module itself connects the $\overline{\text{CPPE}}$ to ground, the logic low level on that signal indicates to the host that a card supporting PCI Express has been inserted. If $\overline{\text{CPUSB}}$ is connected to ground, then the ExpressCard module supports the USB interface. If both PCI Express and USB are supported by the ExpressCard module, then both signals, $\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$, must be connected to ground.

In addition to the Card Present signals ($\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$), the host system determines when to apply power to the ExpressCard module based on the state of the system. The state of the system is defined by the state of the 3.3 V, 1.5 V, and AUX input voltage rails. For the sake of simplicity, the 3.3-V and 1.5-V rails are defined as the primary voltage rails as oppose to the auxiliary voltage rail, AUX.

ExpressCard POWER SWITCH OPERATION

The ExpressCard power switch resides on the host, and its main function is to control when to send power to the ExpressCard slot. The ExpressCard power switch makes decisions based on the Card Present inputs and on the state of the host system as defined by the primary and auxiliary voltage rails.

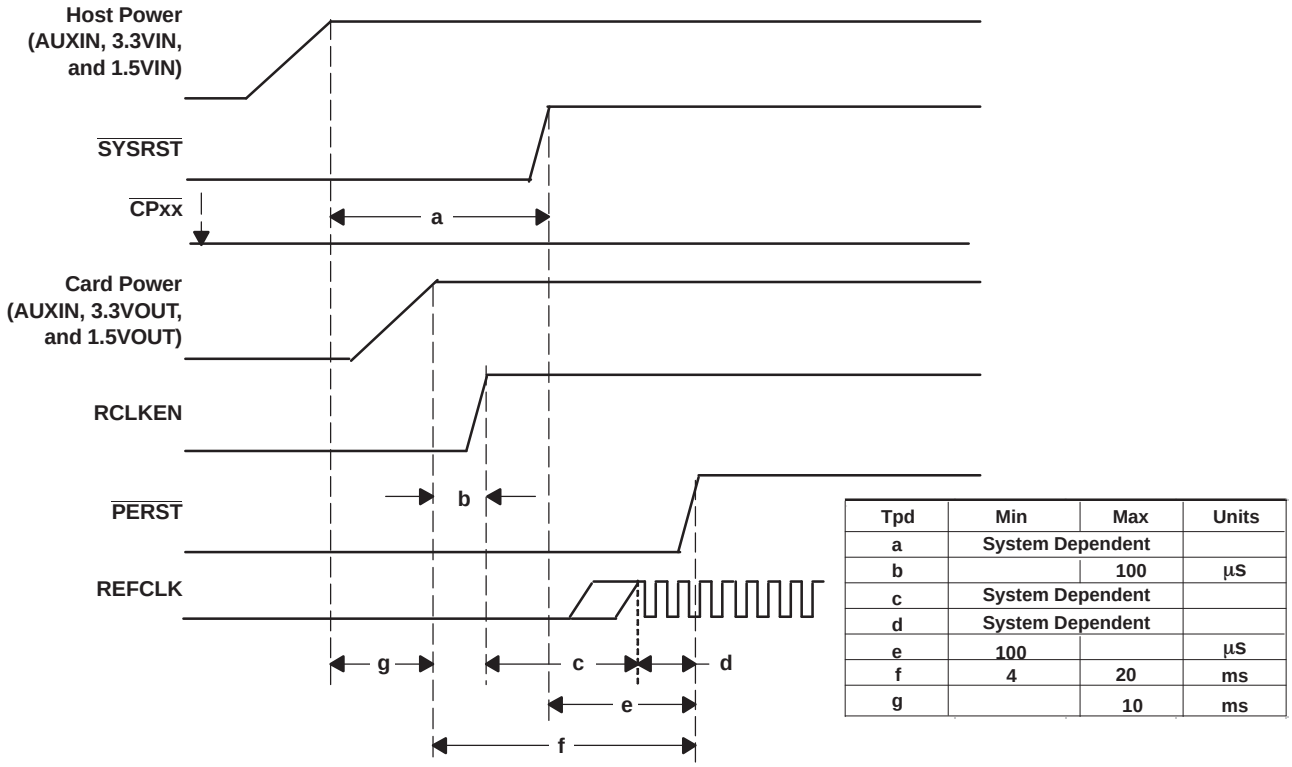
The following conditions define the operation of the host power controller:

1. When both primary power and auxiliary power at the input of the ExpressCard power switch are off, then all power to the ExpressCard connector is off regardless of whether a card is present.
2. When both primary power and auxiliary power at the input of the ExpressCard power switch are on, then power is only applied to the ExpressCard after the ExpressCard power switch detects that a card is present.
3. When primary power (either +3.3 V or +1.5 V) at the input of the ExpressCard power switch is off and auxiliary power at the input of the ExpressCard power switch is on, then the ExpressCard power switch behaves in the following manner:
   (a) If neither of the Card Present inputs is detected (no card inserted), then no power is applied to the ExpressCard slot.
   (b) If the card is inserted after the system has entered this power state, then no power is applied to the ExpressCard slot.
   (c) If the card is inserted prior to the removal of the primary power (either +3.3 V or +1.5 V or both) at the input of the ExpressCard power switch, then only the primary power (both +3.3 V and +1.5 V) is removed and the auxiliary power is sent to the ExpressCard slot.

Figure 18 through Figure 23 illustrate the timing relationships between power/logic inputs and outputs of ExpressCard.

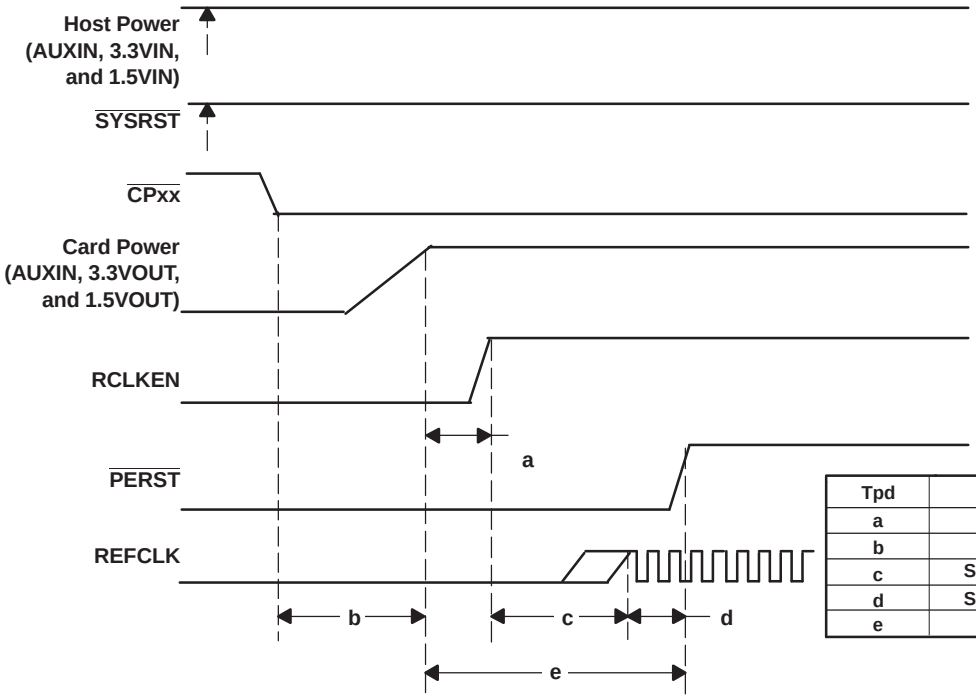
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EXPRESS CARD TIMING DIAGRAMS



Tpd	Min	Max	Units
a	System Dependent		
b		100	µS
c	System Dependent		
d	System Dependent		
e	100		µS
f	4	20	ms
g		10	ms

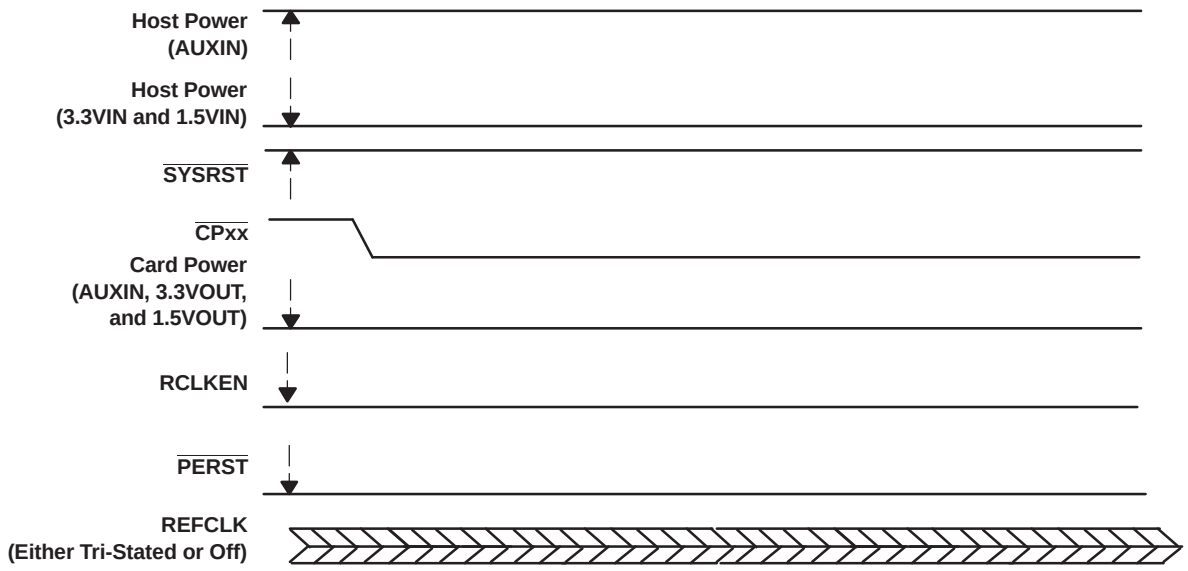
Figure 18. Timing Signals - Card Present Before Host Power Is On



Tpd	Min	Max	Units
a		100	µS
b		10	ms
c	System Dependent		
d	System Dependent		
e	4	20	ms

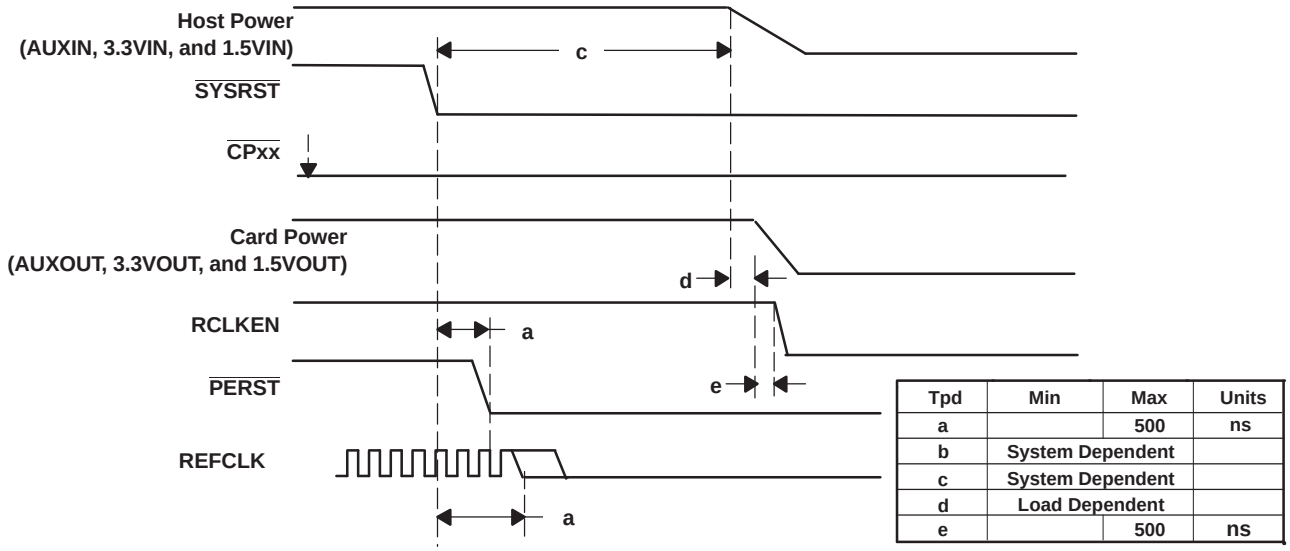
Figure 19. Timing Signals - Host Power Is On Prior to Card Insertion

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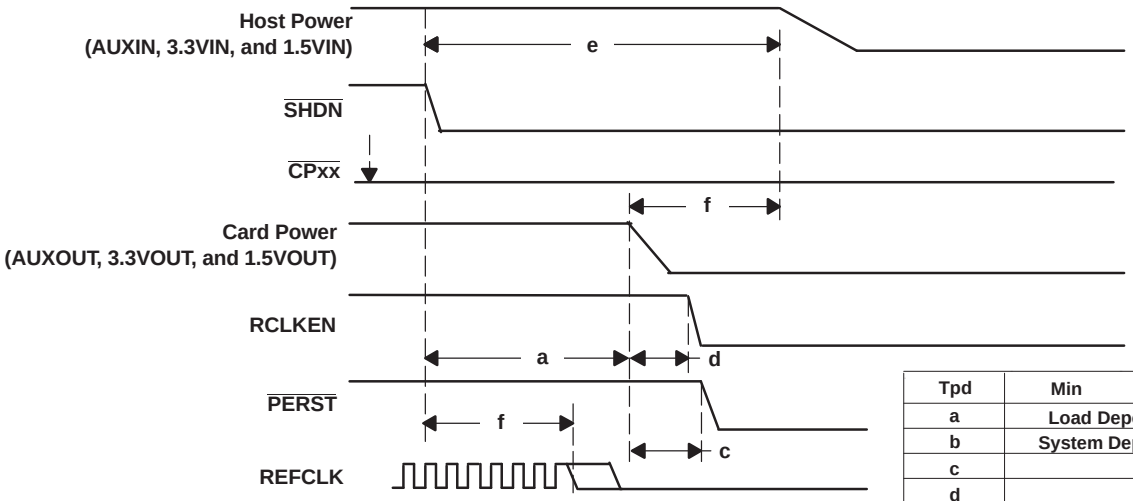
Note: Once 3.3 V and 1.5 V are applied, the power switch follows the power-up sequence of Figure 18 or Figure 19.

Figure 20. Timing Signals - Host System In Standby Prior to Card Insertion



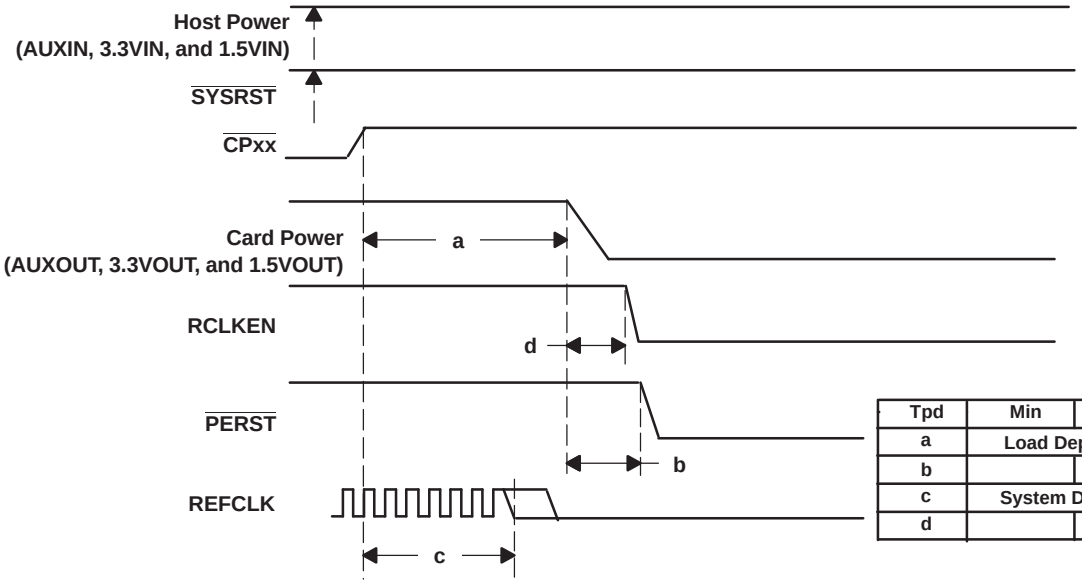
Tpd	Min	Max	Units
a		500	ns
b	System Dependent		
c	System Dependent		
d	Load Dependent		
e		500	ns

Figure 21. Timing Signals - Host-Controlled Power Down



Tpd	Min	Max	Units
a	Load Dependent		
b	System Dependent		
c		500	ns
d		500	ns
e	System Dependent		
f	System Dependent		

Figure 22. Timing Signals - Controlled Power Down When $\overline{\text{SHDN}}$ Asserted



Tpd	Min	Max	Units
a	Load Dependent		
b		500	ns
c	System Dependent		
d		500	ns

Figure 23. Timing Signals - Surprise Card Removal

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REVISION HISTORY

NOTE: Page numbers in the latest revision may differ from previous versions.

Changes from Revision F (August 2007) to Revision G — **Page**

- Changed note (1) of the Available Options table. 2

(1) The TPS2231MRGP is identical to the TPS2231 with the exception of the PowerPAD dimensions. See the Thermal Pad Mechanical data portion of this data sheet for specific information. The thermal pad for the TPS2231MRGP and TPS2231MRGP-1 is 2,2 mm × 2,2 mm; the thermal pad for the TPS2231RGP is 2,7 mm × 2,7 mm.

Changes from Revision G (August 2007) to Revision H — **Page**

- Changed From; reel is rotated 90°C To: reel is rotated 180°C 2

Changes from Revision H (September 2007) to Revision I — **Page**

- Added TPS2231MRGP-2 and (2) to the Available Options table. 2
- Added TPS2231, TPS2231-1, and TPS2231-1 values to the Logic input supply current 4
- Added Note C to the Function Block Diagram 9

(2) The TPS2231MRGP-2 is identical to the TPS2231MRGP with the exception that the orientation of the part in the reel is rotated 90° and does not have an internal pull-up resistor between AUX IN and $\overline{\text{SYSRST}}$. See the Package Materials Information portion of this data sheet for specific information.

Changes from Revision I (November 2007) to Revision J — **Page**

- Added TPS2231-3 to the Available Options table. 2
- Added explanatory footnote to Available Options table regarding TPS2231MRGP-3 2
- Added TPS2231-3 test condition statement to UVLO spec. 5
- Added power state explanation for TPS2231-3 device. 13

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2231MRGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231MRGPR-1	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231MRGPR-1G4	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231MRGPR-2	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231-2	Samples
TPS2231MRGPR-2G4	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231-2	Samples
TPS2231MRGPR-3	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231-3	Samples
TPS2231MRGPRG4	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231MRGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231MRGPT-1	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231MRGPT-1G4	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231MRGPT-3	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231-3	Samples
TPS2231MRGPTG4	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231M	Samples
TPS2231PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2231	Samples
TPS2231PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2231	Samples
TPS2231PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2231	Samples
TPS2231PWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2231	Samples
TPS2231PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2231	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2231PWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2231	Samples
TPS2231PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2231	Samples
TPS2231PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2231	Samples
TPS2231RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231	Samples
TPS2231RGPRG4	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2231	Samples
TPS2231RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		2231	Samples
TPS2231RGPTG4	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		2231	Samples
TPS2236DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2236	Samples
TPS2236DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2236	Samples
TPS2236DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2236	Samples
TPS2236DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2236	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

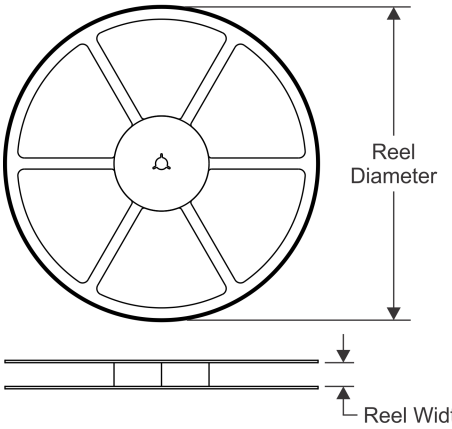
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

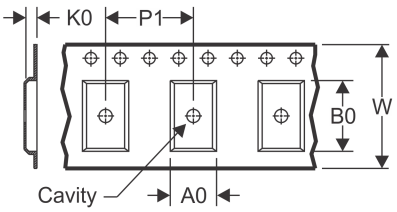
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

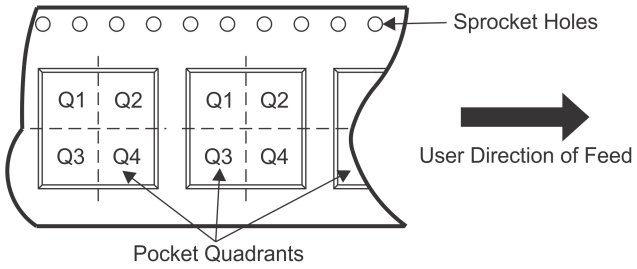


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

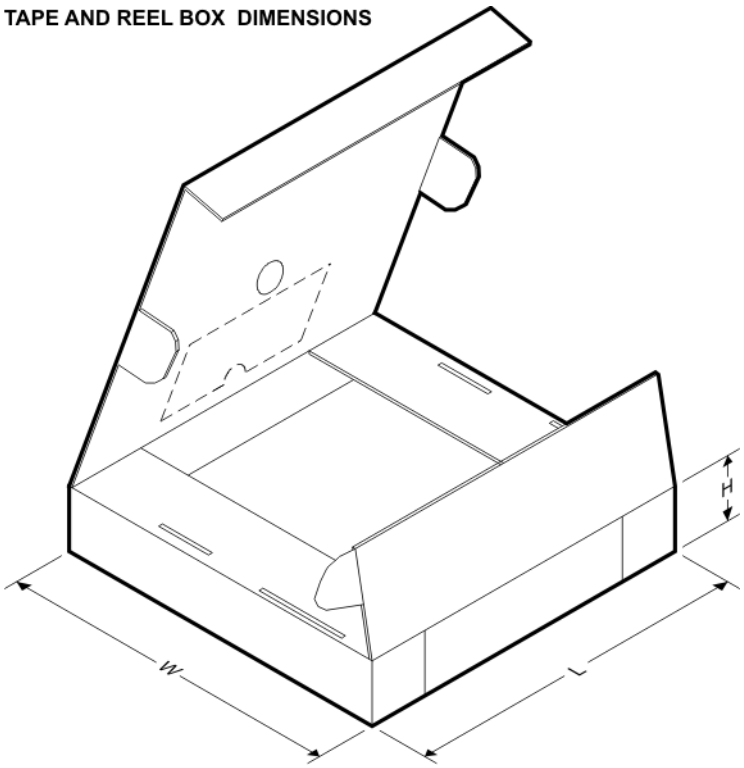
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2231MRGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2231MRGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2231MRGPR-1	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q3
TPS2231MRGPR-2	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1
TPS2231MRGPR-3	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2231MRGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2231MRGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2231MRGPT-1	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q3
TPS2231MRGPT-3	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2231PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS2231PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS2231RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2231RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2236DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

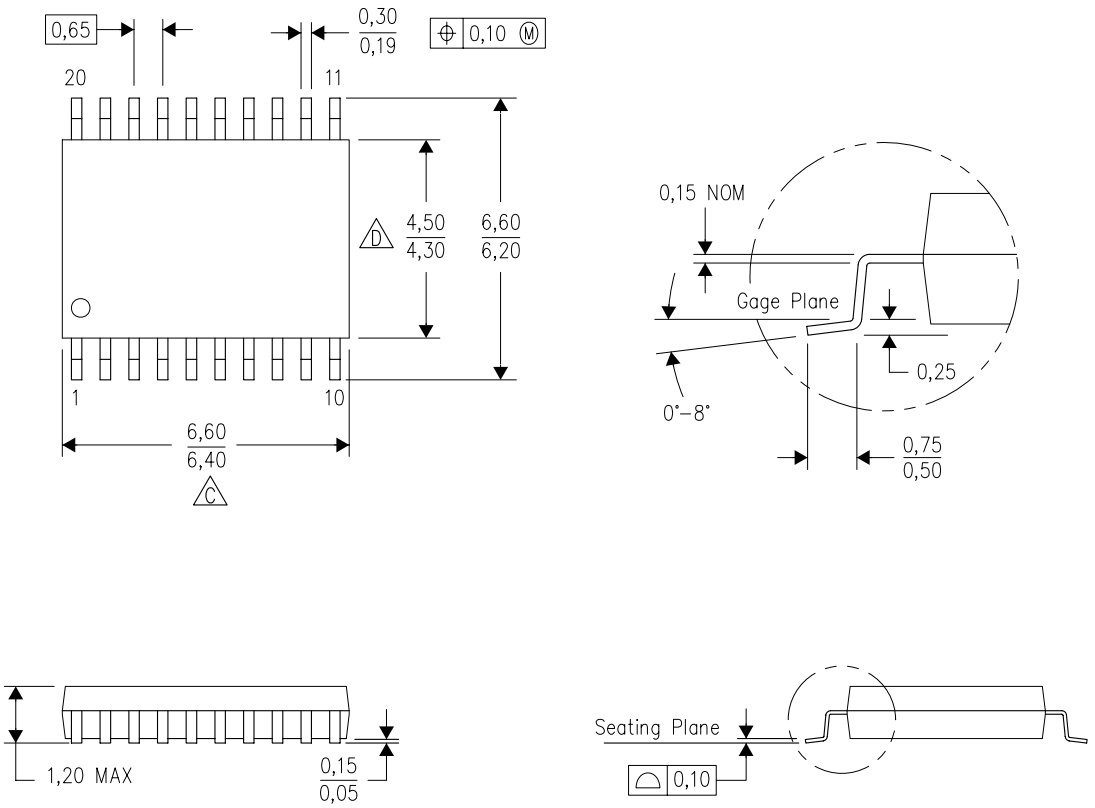
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2231MRGPR	QFN	RGP	20	3000	367.0	367.0	35.0
TPS2231MRGPR	QFN	RGP	20	3000	367.0	367.0	35.0
TPS2231MRGPR-1	QFN	RGP	20	3000	367.0	367.0	35.0
TPS2231MRGPR-2	QFN	RGP	20	3000	367.0	367.0	35.0
TPS2231MRGPR-3	QFN	RGP	20	3000	367.0	367.0	35.0
TPS2231MRGPT	QFN	RGP	20	250	210.0	185.0	35.0
TPS2231MRGPT	QFN	RGP	20	250	210.0	185.0	35.0
TPS2231MRGPT-1	QFN	RGP	20	250	210.0	185.0	35.0
TPS2231MRGPT-3	QFN	RGP	20	250	210.0	185.0	35.0
TPS2231PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
TPS2231PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TPS2231RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
TPS2231RGPT	QFN	RGP	20	250	210.0	185.0	35.0
TPS2236DAPR	HTSSOP	DAP	32	2000	367.0	367.0	45.0

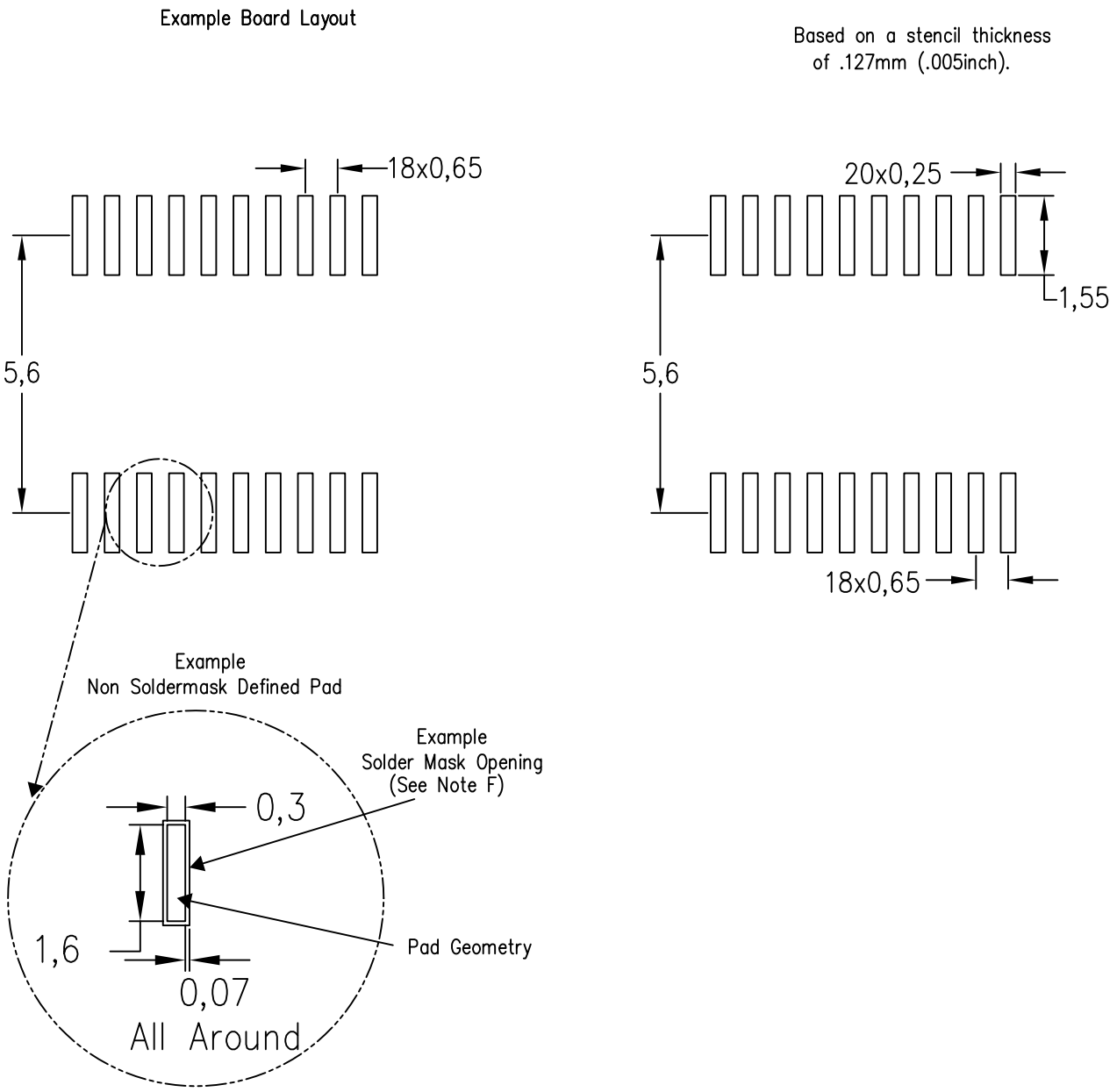
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



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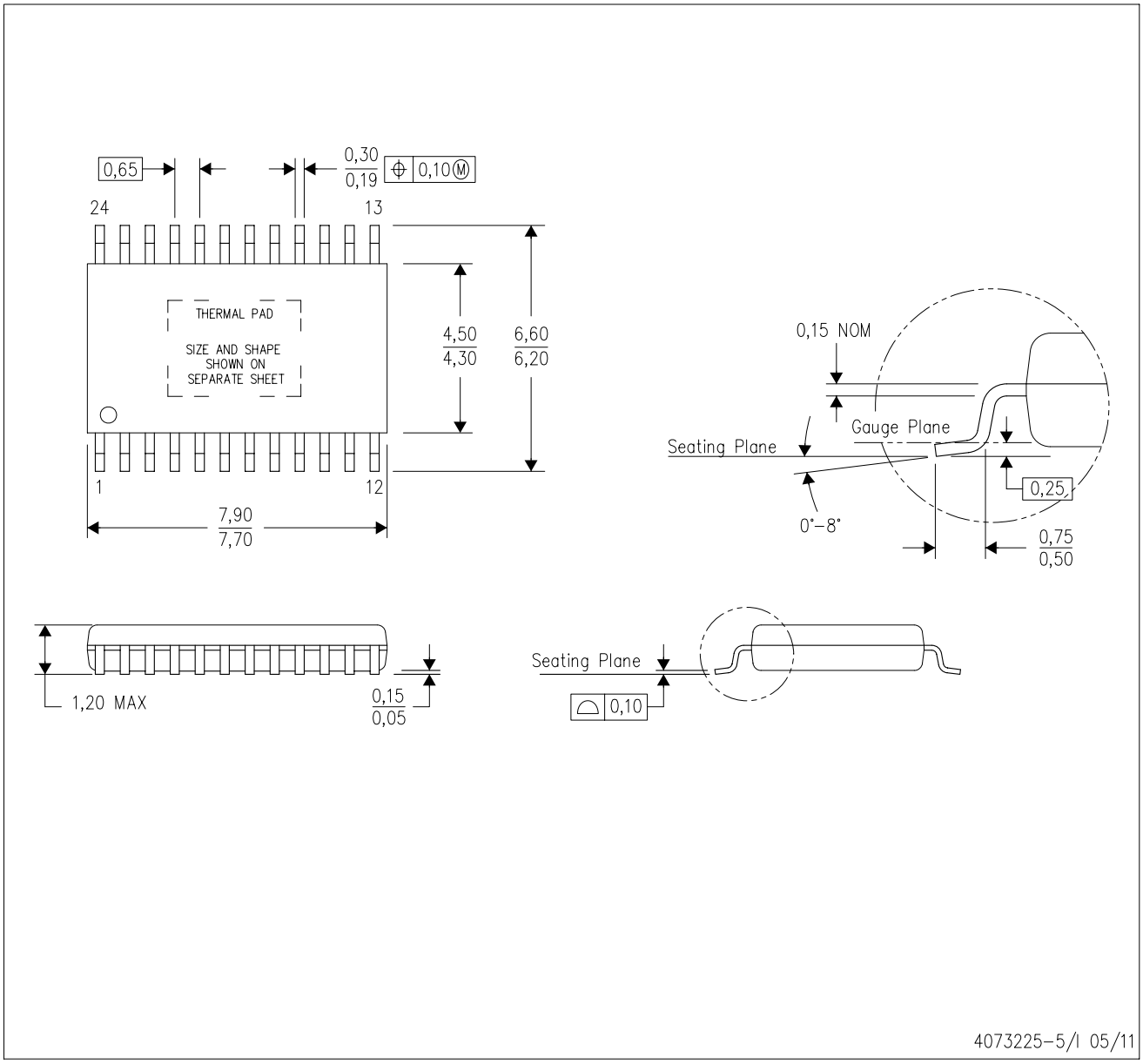
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

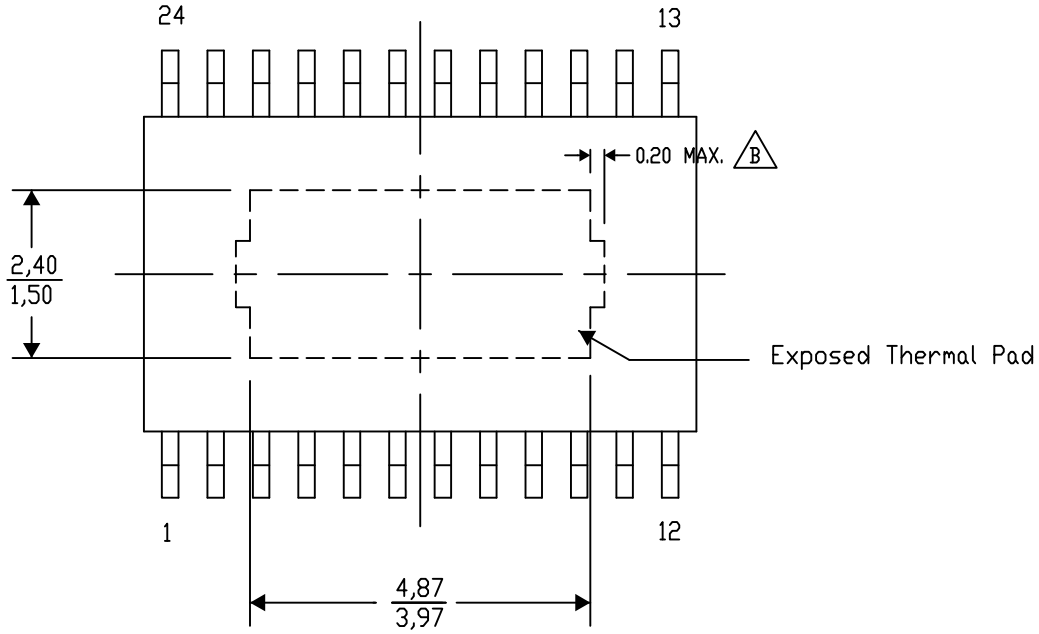
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

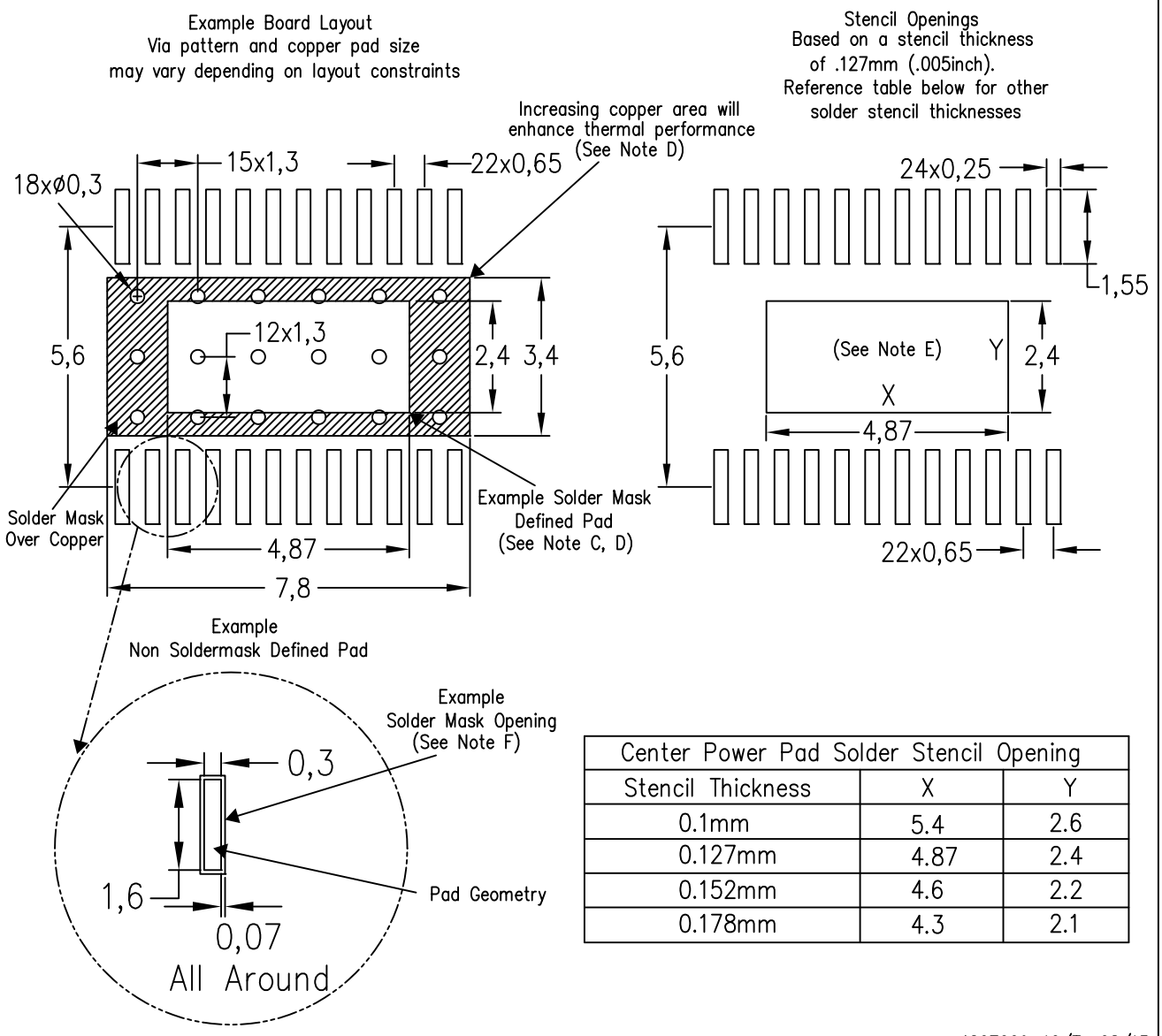
4206332–29/AH 11/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE

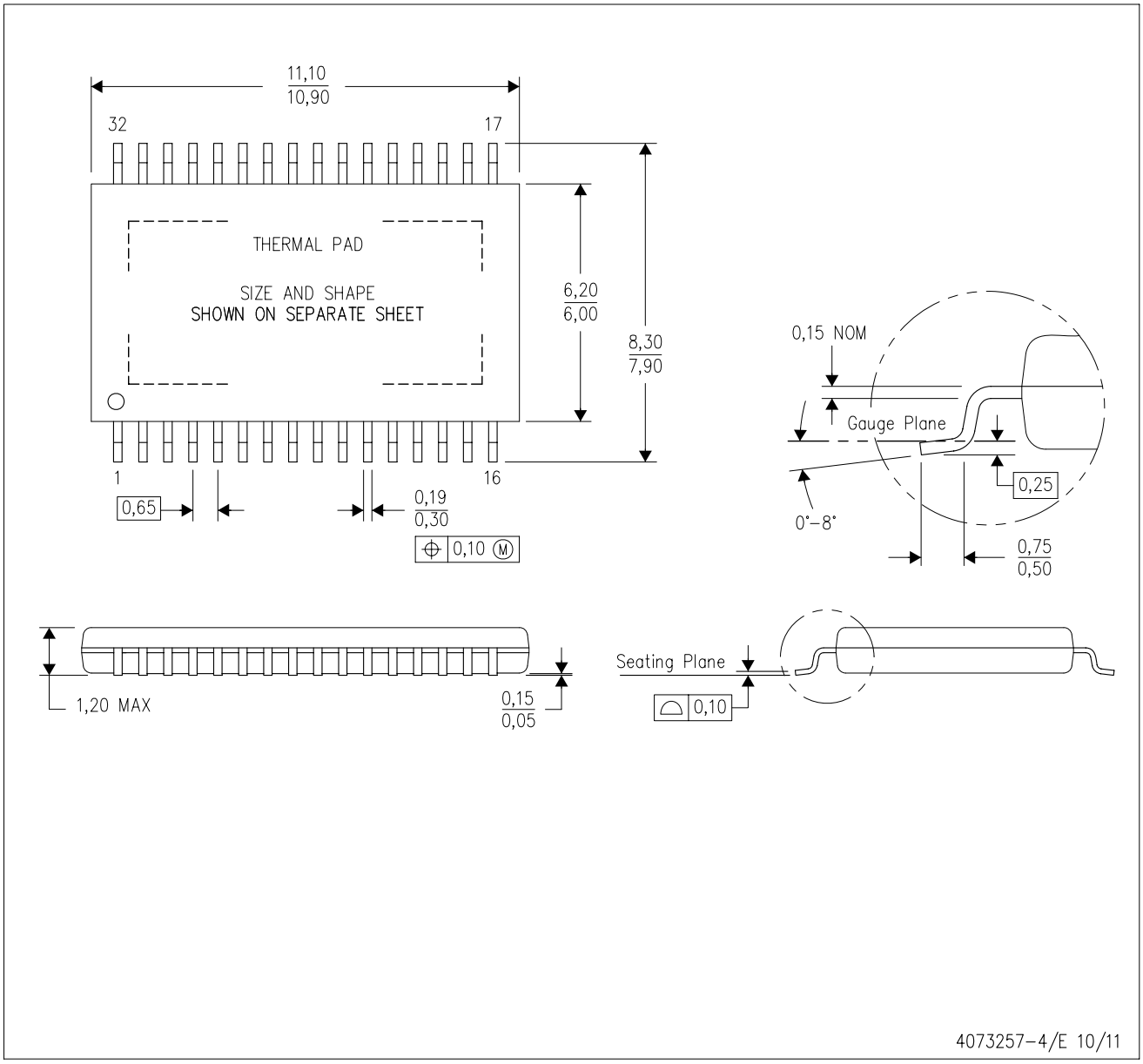


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.4	2.6
0.127mm	4.87	2.4
0.152mm	4.6	2.2
0.178mm	4.3	2.1

4207609–16/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

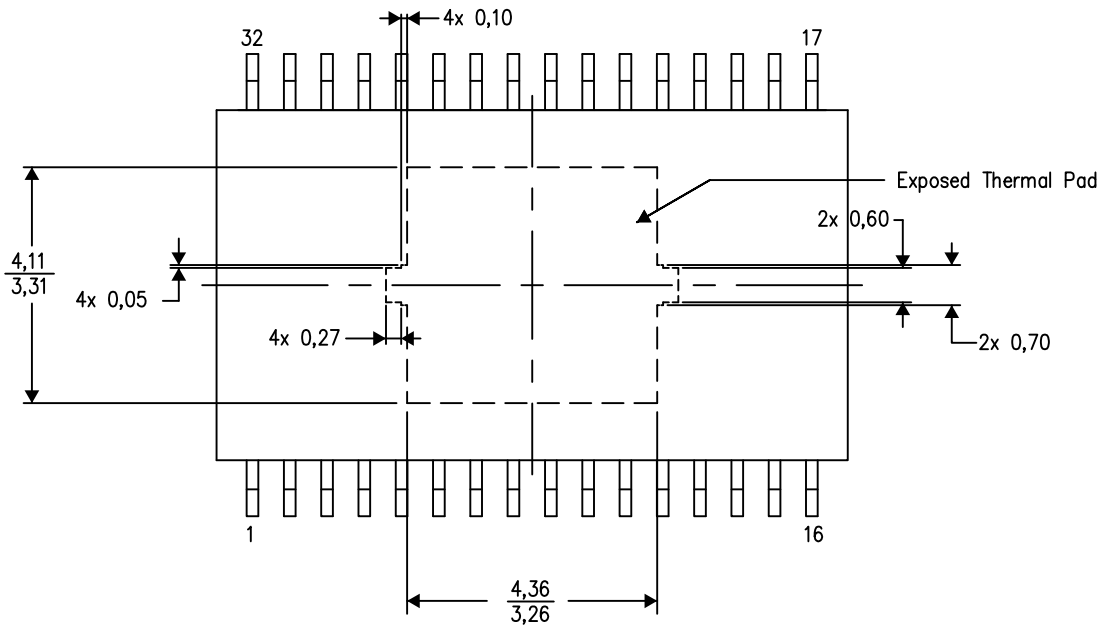
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

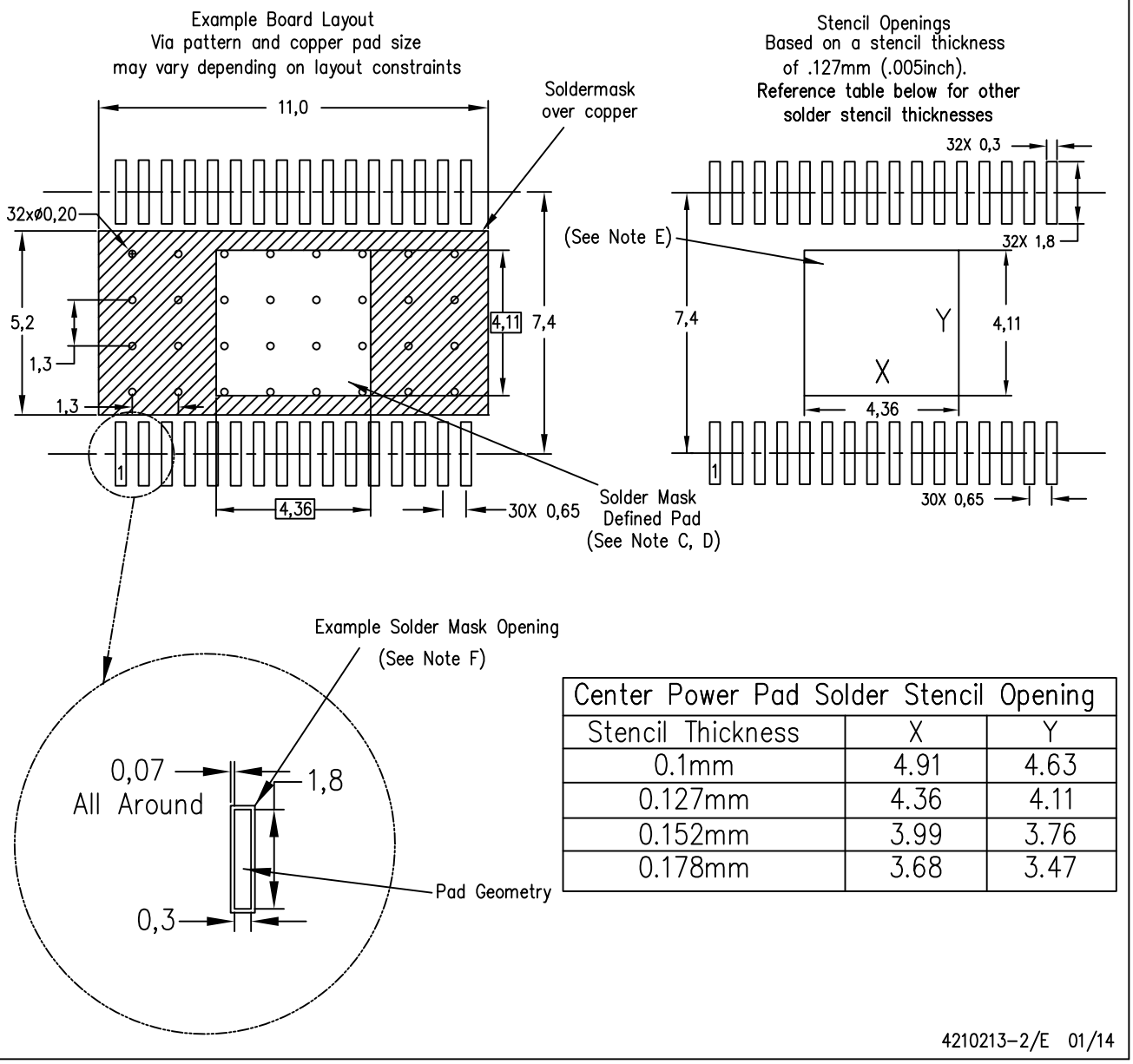
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

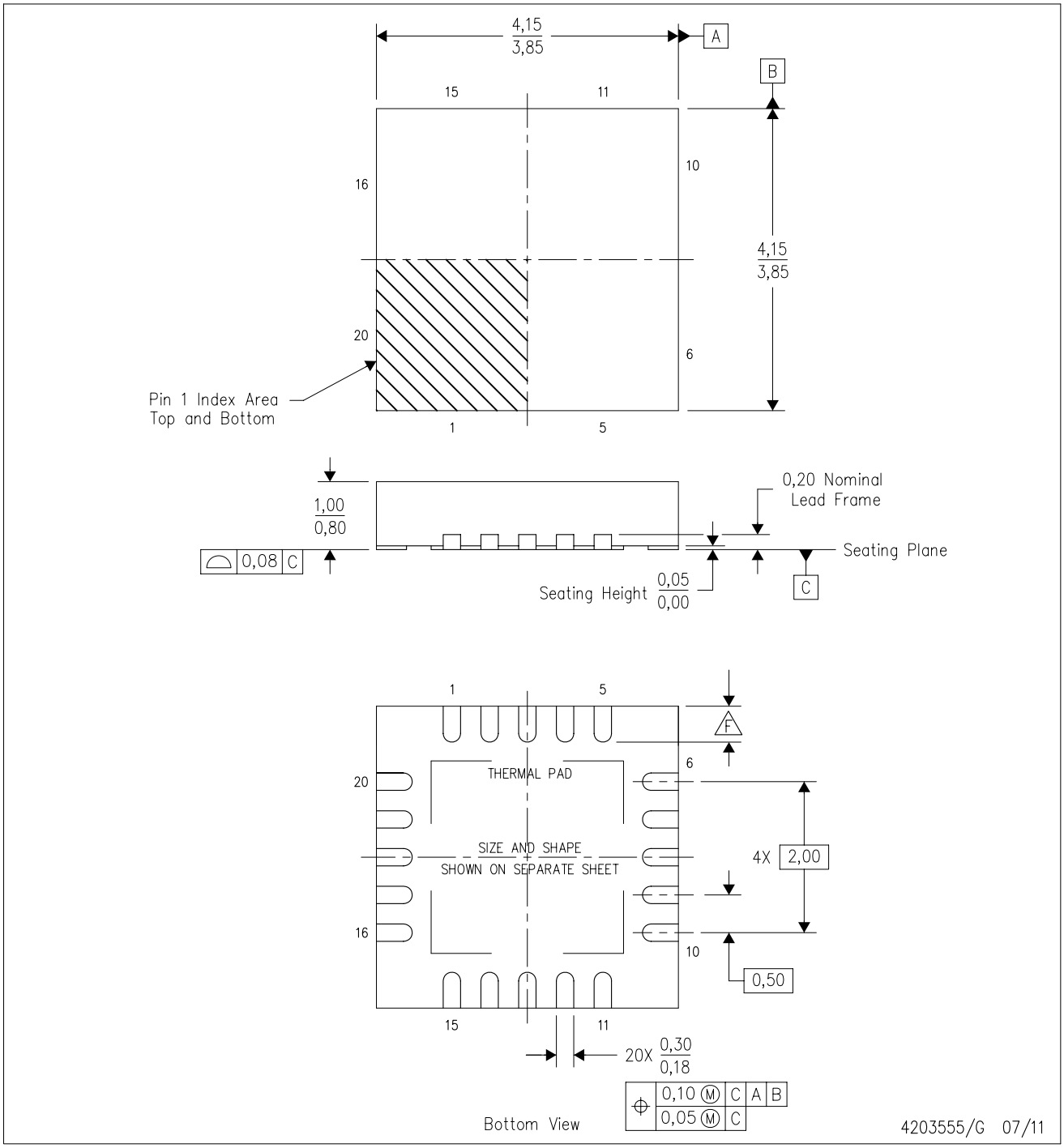


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

PowerPAD is a trademark of Texas Instruments

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

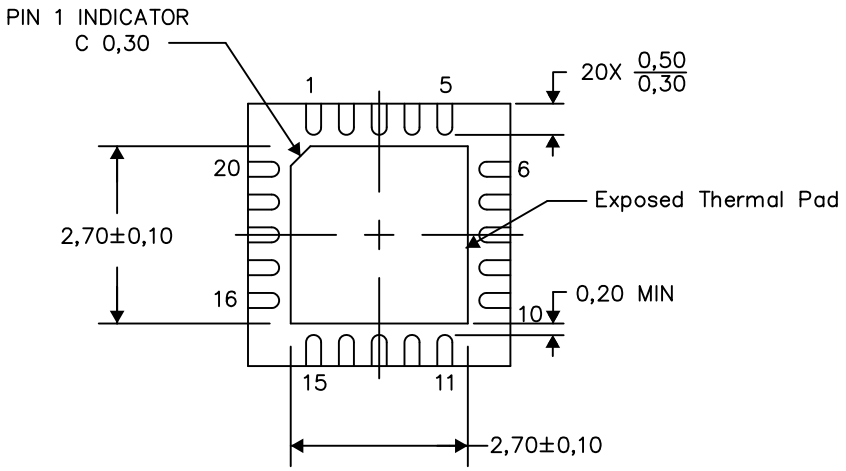
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



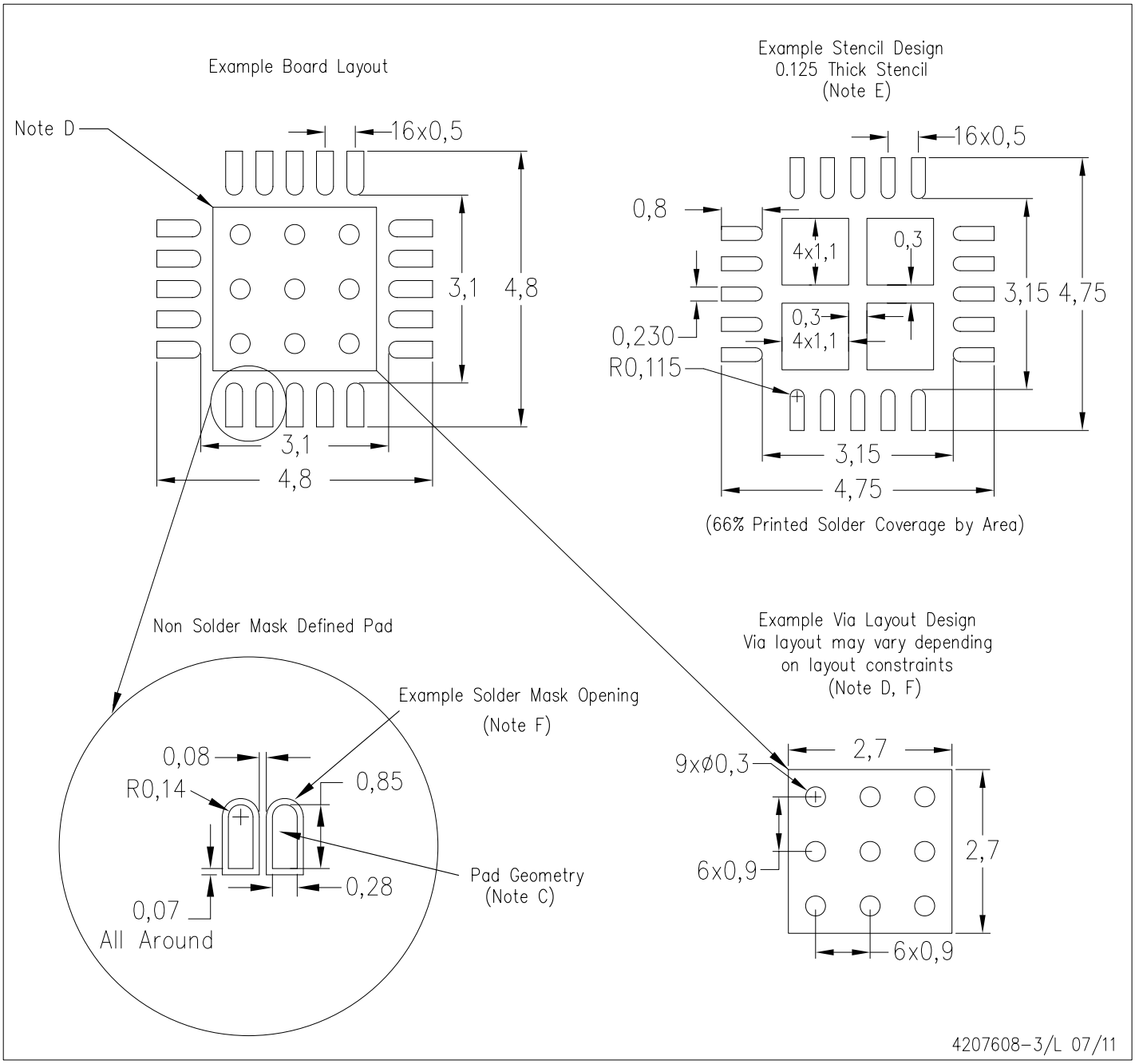
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

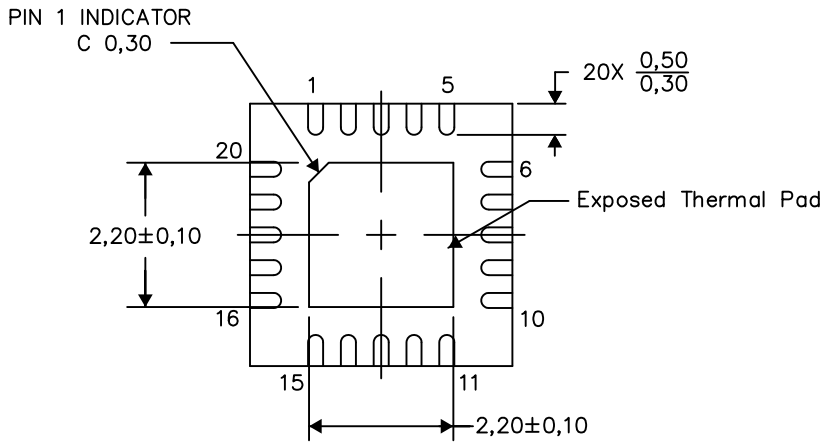
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.



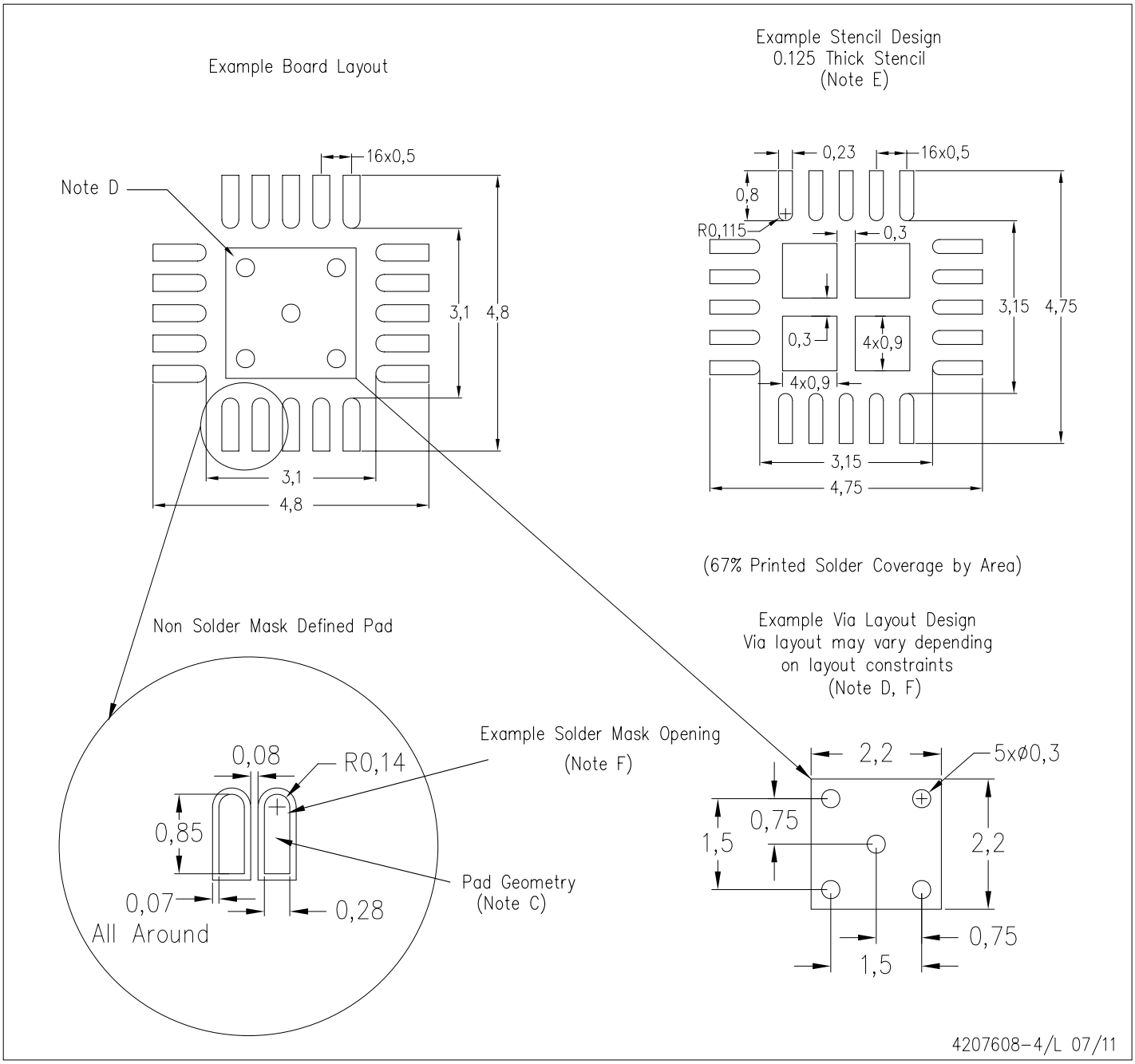
Bottom View

Exposed Thermal Pad Dimensions

4206346–4/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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