EMC2305

Multiple RPM-Based PWM Fan Controller for Five Fans

PRODUCT FEATURES

Datasheet

General Description

The EMC2305 is an SMBus compliant fan controller with up to five independently controlled PWM fan drivers. Each fan driver is controlled by a programmable frequency PWM driver and Fan Speed Control algorithm that operates in either a closed loop fashion or as a directly PWM-controlled device.

The closed loop Fan Speed Control algorithm (FSC) has the capability to detect aging fans and alert the system. It will likewise detect stalled or locked fans and trigger an interrupt.

Additionally, the EMC2305 offers a clock output so that multiple devices may be chained and slaved to the same clock source for optimal performance in large distributed systems.

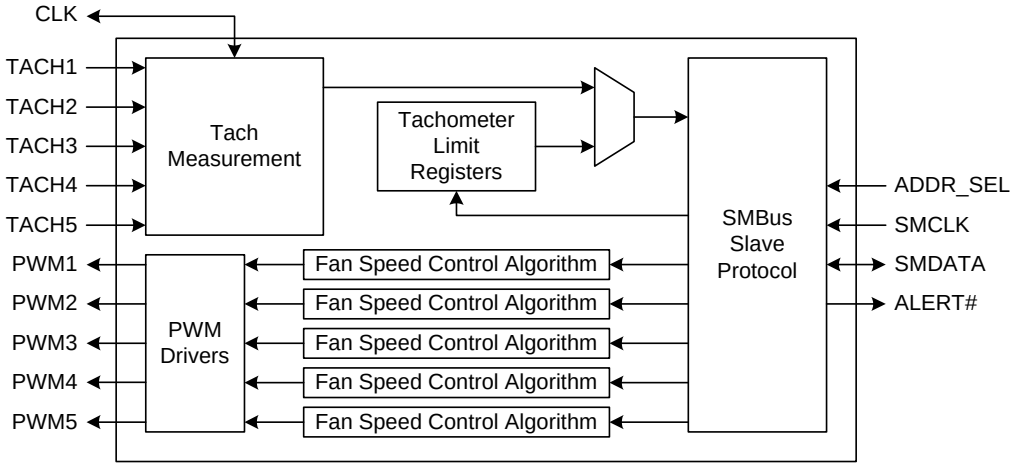
Applications

- Servers
- Projectors
- Industrial and Networking Equipment
- Notebook Computers

Features

- Five Programmable Fan Control circuits (EMC2305)
  - 4-wire fan compatible
  - High speed PWM (26 kHz)
  - Low speed PWM (9.5Hz - 2240 Hz)
  - Optional detection of aging fans
  - Fan Spin Up Control and Ramp Rate Control
  - Alert on Fan Stall
  - Up to 3 Selectable Default Fan Speeds
- Watchdog Timer
- RPM-based fan control algorithm
  - 0.5% accuracy from 500 RPM to 16k RPM (external crystal oscillator)
  - 1% accuracy from 500 RPM to 16k RPM (internal clock)
- SMBus 2.0 Compliant
  - Up to 6 selectable SMBus addresses
  - SMBus Alert compatible
- CLK Pin can provide a clock source output
- Available in a 16-pin 4mm x 4mm QFN Lead-free RoHS Compliant package

Block Diagram



Order Number:

ORDERING NUMBER	PACKAGE	FEATURES
EMC2305-1-AP-TR	16-pin QFN (Lead-free RoHS compliant)	Five RPM-based fan speed control algorithms

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Table of Contents

Chapter 1 Pin Description 7

Chapter 2 Electrical Specifications 10
2.1 Electrical Specifications 10
2.2 SMBus Electrical Specifications 11

Chapter 3 Communications 13
3.1 System Management Bus Interface Protocol 13
3.1.1 SMBus Start Bit 13
3.1.2 SMBus Address and RD / $\overline{WR}$ Bit 13
3.1.3 SMBus Data Bytes 14
3.1.4 SMBus ACK and NACK Bits 14
3.1.5 SMBus Stop Bit 14
3.1.6 SMBus Time-out 14
3.1.7 SMBus and I^2C Compliance 14
3.2 SMBus Protocols 15
3.2.1 Write Byte 15
3.2.2 Read Byte 15
3.2.3 Send Byte 15
3.2.4 Receive Byte 16
3.2.5 Block Write Protocol 16
3.2.6 Block Read Protocol 16
3.2.7 Alert Response Address 16

Chapter 4 Product Description 18
4.1 Fan Control Modes of Operation 18
4.2 PWM Fan Driver 19
4.3 RPM-based Fan Speed Control Algorithm (FSC) 19
4.3.1 Programming the RPM-based Fan Speed Control Algorithm 20
4.4 Tachometer Measurement 20
4.4.1 Stalled Fan 21
4.4.2 Aging Fan or Invalid Drive Detection 21
4.5 CLK Pin 21
4.5.1 Pull Up Decode 21
4.5.2 External Clock 22
4.5.3 Internal Clock 22
4.6 Spin Up Routine 22
4.6.1 Power Up Options 23
4.7 Ramp Rate Control 23
4.8 Watchdog Timer 24
4.8.1 Power Up Operation 24
4.8.2 Continuous Operation 25

Chapter 5 Register Set 26
5.1 Register Map 26
5.1.1 Lock Entries 31
5.2 Configuration Register 31
5.3 Fan Status Registers 32
5.3.1 Fan Status - 24h 32
5.3.2 Fan Stall Status - 25h 33

5.3.3 Fan Spin Status - 26h . . . 33
5.3.4 Fan Drive Fail Status - 27h . . . 33
5.4 Fan Interrupt Enable Register . . . 33
5.5 PWM Configuration Registers . . . 34
5.5.1 PWM Polarity Config - 2Ah . . . 34
5.5.2 PWM Output Config - 2Bh . . . 34
5.6 PWM Base Frequency Registers . . . 35
5.6.1 PWM Base Frequency 1 - 2Bh . . . 35
5.6.2 PWM Base Frequency 2 - 2Ch . . . 35
5.7 Fan Setting Registers . . . 36
5.8 PWM Divide Registers . . . 36
5.9 Fan Configuration 1 Registers . . . 37
5.10 Fan Configuration 2 Registers . . . 38
5.11 Gain Registers . . . 40
5.12 Fan Spin Up Configuration Registers . . . 41
5.13 Fan Max Step Registers . . . 43
5.14 Fan Minimum Drive Registers . . . 44
5.15 Valid TACH Count Registers . . . 44
5.16 Fan Drive Fail Band Registers . . . 45
5.17 TACH Target Registers . . . 46
5.18 TACH Reading Registers . . . 47
5.19 Software Lock Register . . . 48
5.20 Product Features Register . . . 48
5.21 Product ID Register . . . 49
5.22 Manufacturer ID Register . . . 50
5.23 Revision Register . . . 50

Chapter 6 Typical Operating Curves . . . 51

Chapter 7 Package Drawing . . . 53
7.1 EMC2305 Package Information . . . 53
7.2 Package Markings . . . 55

Chapter 8 Datasheet Revision History . . . 56

List of Figures

Figure 1.1 EMC2305 Pin Diagram (16-Pin QFN) 7
Figure 3.1 SMBus Timing Diagram 13
Figure 4.1 System Diagram of EMC2305 18
Figure 4.2 Spin Up Routine 23
Figure 4.3 Ramp Rate Control 24
Figure 7.1 Package Drawing - 16-Pin QFN 4mm x 4mm 53
Figure 7.2 Package Dimensions - 16-Pin QFN 4mm x 4mm 54
Figure 7.3 PCB Footprint - 16-Pin QFN 4mm x 4mm 54
Figure 7.4 EMC2305 Package Markings. 55

List of Tables

Table 1.1 Pin Description for EMC2305 7
Table 1.2 Pin Types 9
Table 2.1 Absolute Maximum Ratings 10
Table 2.2 Electrical Specifications 10
Table 2.3 SMBus Electrical Specifications 11
Table 3.1 ADDR_SEL Pin Decode 14
Table 3.2 Protocol Format 15
Table 3.3 Write Byte Protocol 15
Table 3.4 Read Byte Protocol 15
Table 3.5 Send Byte Protocol 15
Table 3.6 Receive Byte Protocol 16
Table 3.7 Block Write Protocol 16
Table 3.8 Block Read Protocol 16
Table 3.9 Alert Response Address Protocol 17
Table 4.1 Fan Controls Active for Operating Mode 19
Table 4.2 CLK Pin Pull-Up Decode 21
Table 5.1 EMC2305 Register Set 26
Table 5.2 Configuration Register 31
Table 5.3 Fan Status Registers 32
Table 5.4 Fan Interrupt Enable Register 33
Table 5.5 PWM Configuration Registers 34
Table 5.6 PWM Base Frequency Registers 35
Table 5.7 PWM_BASEx[1:0] Bit Decode 35
Table 5.8 Fan Driver Setting Registers 36
Table 5.9 PWM Divide Registers 36
Table 5.10 Fan Configuration 1 Registers 37
Table 5.11 Range Decode 37
Table 5.12 Minimum Edges for Fan Rotation 38
Table 5.13 Update Time 38
Table 5.14 Fan Configuration 2 Registers 38
Table 5.15 Derivative Options 39
Table 5.16 Error Range Options 40
Table 5.17 Gain Registers 40
Table 5.18 Gain Decode 41
Table 5.19 Fan Spin Up Configuration Registers 41
Table 5.20 DRIVE_FAIL_CNT[1:0] Bit Decode 41
Table 5.21 Spin Level 42
Table 5.22 Spin Time 43
Table 5.23 Fan Max Step Registers 43
Table 5.24 Minimum Fan Drive Registers 44
Table 5.25 Valid TACH Count Registers 44
Table 5.26 Fan Drive Fail Band Registers 45
Table 5.27 TACH Target Registers 46
Table 5.28 TACH Reading Registers 47
Table 5.29 Software Lock Register 48
Table 5.30 Product Features Register 48
Table 5.31 ADDR_SEL Pin Configuration 49
Table 5.32 FAN_SPD Pin Configuration 49
Table 5.33 Product ID Register 49
Table 5.34 Manufacturer ID Register 50
Table 5.35 Revision Register 50
Table 8.1 Customer Revision History 56

Chapter 1 Pin Description

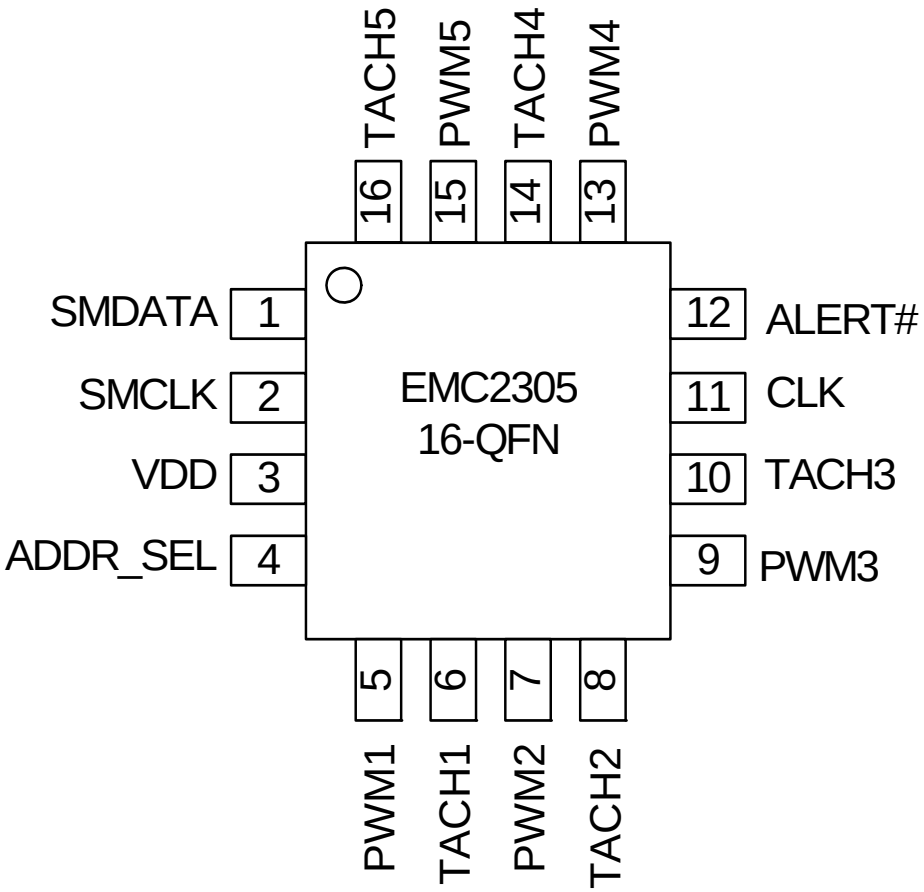


Figure 1.1 EMC2305 Pin Diagram (16-Pin QFN)

Table 1.1 Pin Description for EMC2305

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
1	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
2	SMCLK	SMBus clock input - requires external pull-up resistor	DI (5V)
3	VDD	Power Supply	Power
4	ADDR_SEL	Address selection input - requires pull-up resistor	AIO

Table 1.1 Pin Description for EMC2305 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
5	PWM1	Push-Pull PWM output driver for Fan 1	DO
		Open Drain PWM output driver for Fan 1	OD (5V)
6	TACH1	Open drain tachometer input for Fan 1- requires pull-up resistor	DI (5V)
7	PWM2	Push-Pull PWM output driver for Fan 2	DO
		Open Drain PWM output driver for Fan 2	OD (5V)
8	TACH2	Open drain tachometer input for Fan 2 - requires pull-up resistor	DI (5V)
9	PWM3	Push-Pull PWM output driver for Fan 3	DO
		Open Drain PWM output driver for Fan 3	OD (5V)
10	TACH3	Open drain tachometer input for Fan 3 - requires pull-up resistor	DI (5V)
11	CLK	Clock input for tachometer measurement	DI (5V)
		Push Pull Clock output to other fan controllers to synchronize Fan Speed Control	DO
12	ALERT#	Active low interrupt - requires external pull-up resistor.	OD (5V)
13	PWM4	Push-Pull PWM output driver for Fan 4	DO
		Open Drain PWM output driver for Fan 4	OD (5V)
14	TACH4	Open drain tachometer input for Fan 4 - requires pull-up resistor	DI (5V)
15	PWM5	Push-Pull PWM output driver for Fan 5	DO
		Open Drain PWM output driver for Fan 5	OD (5V)
16	TACH5	Open drain tachometer input for Fan 5 - requires pull-up resistor	DI (5V)
Bottom Pad	GND	Ground	Power

The pin types are described in detail below. All pins labeled with (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the 5V tolerant pad must never be more than 3.6V.

Table 1.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
AIO	Analog input / output - this pin is used for analog signals
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input / Open Drain Output this pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 2 Electrical Specifications

Table 2.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT_pin} - V_{DD}\|$) (see Note 2.1)	0 to 3.6	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Thermal Resistance - Junction to Ambient (θ_{JA})	40	°C/W
Operating Ambient Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 2.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the EMC2305 is unpowered.

2.1 Electrical Specifications

Table 2.2 Electrical Specifications

V_{DD} = 3V to 3.6V, T_A = -40°C to 125°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}		625	800	uA	
PWM Fan Driver						
PWM Resolution	PWM		256		Steps	
PWM Duty Cycle	DUTY	0		100	%	
RPM-based Fan Controller						
Tachometer Range	TACH	480		16000	RPM	
Tachometer Setting Accuracy	Δ_{TACH}		±0.5	±1	%	External oscillator 32.768kHz
	Δ_{TACH}		±1	±2	%	Internal Oscillator
Input High Voltage	V_{IH}	2.0			V	

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = -40°C to 125°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	8 mA current drive
Output Low Voltage	V_{OL}			0.4	V	8 mA current sink
Leakage current	I_{LEAK}			±5	uA	ALERT# pin Powered and unpowered 0°C < TA < 85°C pull-up voltage ≤ 3.6V

Note 2.2 All voltages are relative to ground.

2.2 SMBus Electrical Specifications

Table 2.3 SMBus Electrical Specifications

VDD= 3V to 3.6V, T_A = -40°C to 125°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	
Output Low Voltage	V_{OL}			0.4	V	4 mA current sink
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered and unpowered 0°C < TA < 85°C
Input Capacitance	C_{IN}		5		pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0			us	
Data Setup Time	$t_{SU:DAT}$	0.6			us	

Table 2.3 SMBus Electrical Specifications (continued)

VDD= 3V to 3.6V, T_A = -40°C to 125°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 3 Communications

3.1 System Management Bus Interface Protocol

The EMC2305 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the EMC2305 will not stretch the clock signal.

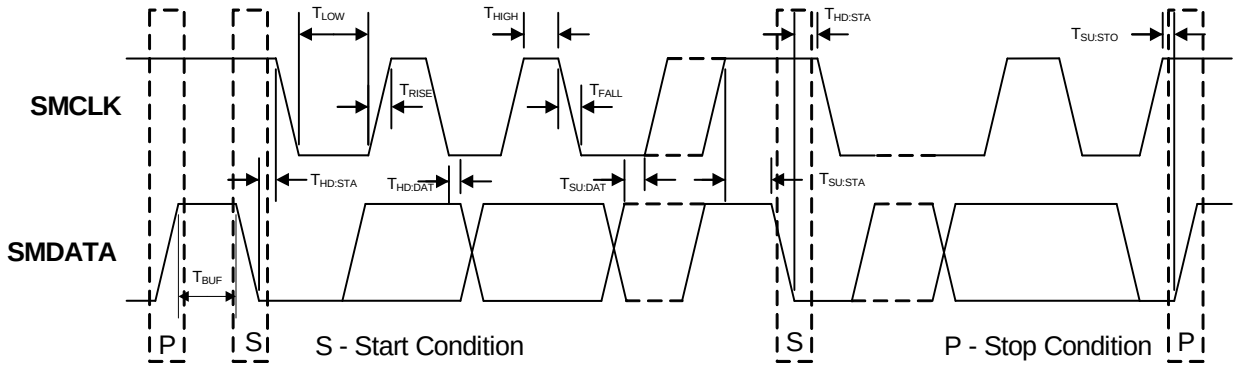


Figure 3.1 SMBus Timing Diagram

3.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

3.1.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, then the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the client device.

The SMBus client will respond to one of multiple SMBus addresses determined by the pull-up resistor on the ADDR_SEL pin. The ADDR_SEL pin decodes one of six pull-up resistors upon device power up. Depending on the resistor used, the CLK pin may also be used to select additional functionality.

Table 3.1 ADDR_SEL Pin Decode

PULL-UP RESISTOR	SMBUS ADDRESS	ADDITIONAL FUNCTIONS
4.7k Ohm ±5%	0101_110(r/w)	None - CLK pin used as clock input or output
6.8k Ohm ±5%	0101_111(r/w)	
10k Ohm ±5%	0101_100(r/w)	
15k Ohm ±5%	0101_101(r/w)	
22k Ohm ±5%	1001_100(r/w)	
33k Ohm ±5%	1001_101(r/w)	CLK pin used to determine default fan drive - see Section 4.5.1. The CLK pin cannot be used as a clock input or output

3.1.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.1.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the ALERT# pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The Host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

3.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the EMC2305 detects an SMBus Stop bit has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.1.6 SMBus Time-out

The EMC2305 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

The SMBus timeout feature is disabled by default and can be enabled via clearing the DIS_TO bit in the Configuration register (20h).

3.1.7 SMBus and I^2C Compliance

The major difference between SMBus and I^2C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz (I^2C has no minimum frequency).
2. The slave protocol will reset if the clock is held low for longer than 30ms (I^2C has no timeout).
3. The slave protocol will reset if both the clock and data lines are held high for longer than 150us.
4. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).

5. The Block Read and Block Write protocols are only compliant with I^2C data formatting. They do not support SMBus formatting for Block Read and Block Write protocols.

3.2 SMBus Protocols

The EMC2305 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and Write Byte as valid protocols as shown below. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 3.2. When reading the protocol blocks, the value of YYYY_YYYb should be replaced with the respective SMBus addresses.

Table 3.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

3.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 3.3.

Table 3.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	YYYY_YYYb	0	0	XXh	0	XXh	0	0 -> 1

3.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.4.

Table 3.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 -> 0	YYYY_YYYb	0	0	XXh	0	0 -> 1	YYYY_YYYb	1	0	XXh	1	0 -> 1

3.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3.5.

Table 3.5 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	YYYY_YYYb	0	0	XXh	0	0 -> 1

3.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3.6.

Table 3.6 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYYb	1	0	XXh	1	0 -> 1

3.2.5 Block Write Protocol

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 3.7. It is an extension of the Write Byte Protocol.

Table 3.7 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	YYYY_YYYb	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

3.2.6 Block Read Protocol

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 3.8. It is an extension of the Read Byte Protocol.

Table 3.8 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	YYYY_YYYb	0	0	XXh	0	1 ->0	YYYY_YYYb	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

3.2.7 Alert Response Address

The ALERT# output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the ALERT# pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 3.9.

Table 3.9 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100b	1	0	YYYY_YYYb	1	0 -> 1

The EMC2305 will respond to the ARA in the following way if the ALERT# pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the ALERT# pin.

Chapter 4 Product Description

The EMC2305 is an SMBus compliant fan controller with five programmable frequency PWM fan drivers. The fan drivers can be operated using two modes: the RPM-based Fan Speed Control Algorithm or the direct fan drive setting.

Figure 4.1 shows a system diagram of the EMC2305.

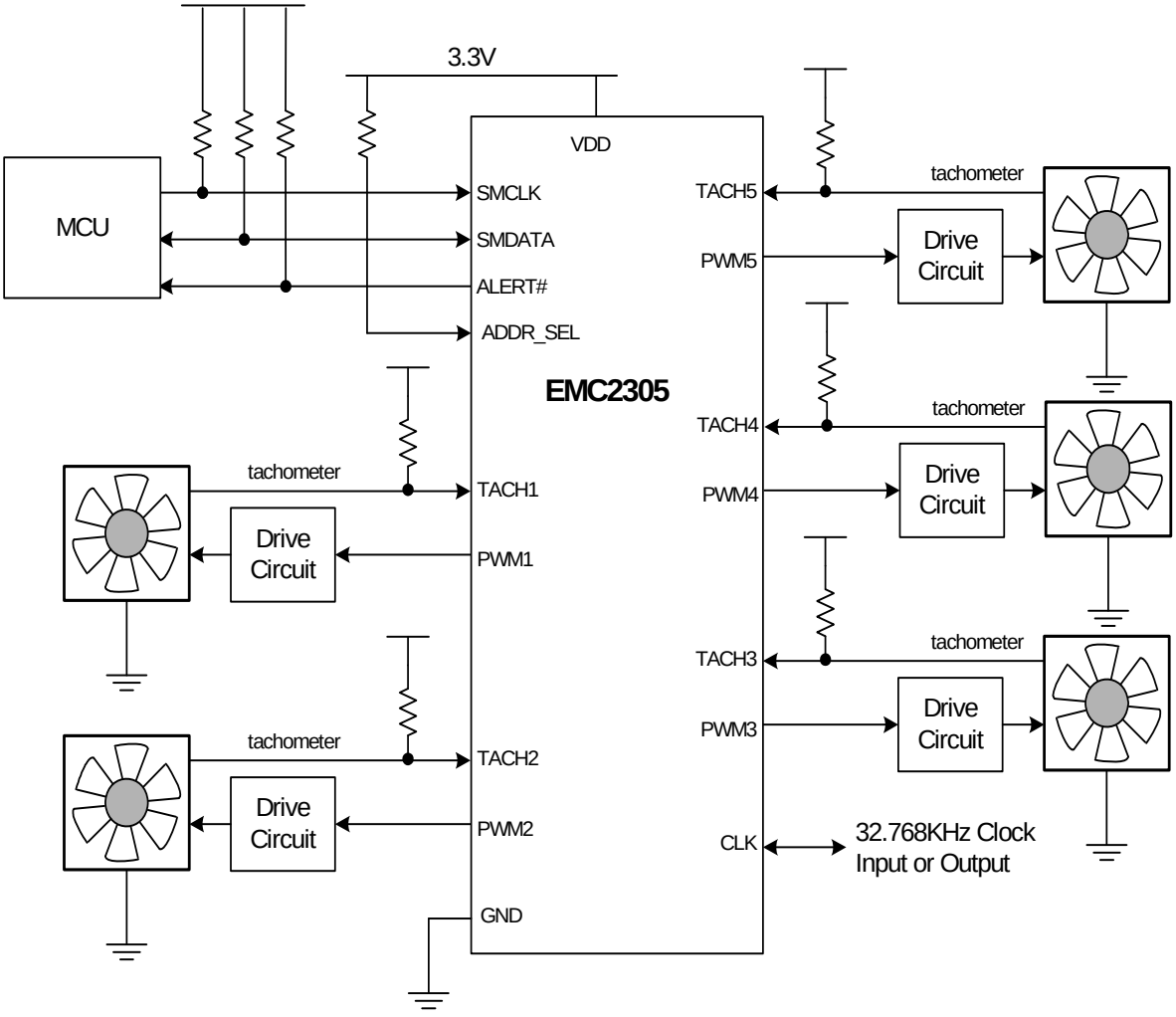


Figure 4.1 System Diagram of EMC2305

4.1 Fan Control Modes of Operation

The EMC2305 has two modes of operation for each fan driver. Each mode of operation uses the Ramp Rate control and Spin Up Routine.

1. Direct Setting Mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 5.7) will instantly update the PWM fan drive. Ramp Rate control is optional and enabled via the EN_RRC bits.

- Whenever the Direct Setting Mode is enabled, the current drive will be changed to what was last written into the Fan Driver Setting Register.

2. Fan Speed Control Mode (FSC) - in this mode of operation, the user determines a target tachometer count and the PWM drive setting is automatically updated to achieve this target speed. The algorithm uses the Spin Up Routine and has user definable ramp rate controls.
   - This mode is enabled setting the EN_ALGO bit in the Fan Configuration Register.

Table 4.1 Fan Controls Active for Operating Mode

DIRECT SETTING MODE	FSC MODE
Fan Driver Setting (read / write)	Fan Driver Setting (read only)
EDGES[1:0]	EDGES[1:0] (Fan Configuration)
-	RANGE[1:0] (Fan Configuration)
UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)
LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)
SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)
Fan Step	Fan Step
-	Fan Minimum Drive
Valid TACH Count	Valid TACH Count
-	TACH Target (read / write)
TACH Reading	TACH Reading
-	DRIVE_FAIL_CNT[1:0] and Drive Band Fail Registers

4.2 PWM Fan Driver

The EMC2305 supports 5 PWM output drivers. Each output driver can be configured to operate as an open-drain (default) or push-pull driver and each driver can be configured with normal or inverse polarity. Additionally, the PWM frequencies are independently programmable with ranges from 9.5Hz to 26kHz in four programmable frequency bands.

4.3 RPM-based Fan Speed Control Algorithm (FSC)

The EMC2305 includes 5 RPM-based Fan Speed Control Algorithms. Each algorithm operates independently and controls a separate fan driver. Each algorithm is controlled manually (by setting the target fan speed).

This fan control algorithm uses Proportional, Integral, and Derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source.

The desired tachometer count is set by the user inputting the desired number of 32.768kHz cycles that occur per fan revolution. This is done by manually setting the TACH Target Register. The user may

change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPMs, then the user would input the hexidecimal equivalent of 1296 (51h in the TACH Target Register). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs.

The EMC2305's RPM-based Fan Speed Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the ALERT# pin. The EMC2305 works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal.

The fan controller will function either with an externally supplied 32.768kHz clock source or with it's own internal 32kHz oscillator depending on the required accuracy. The EMC2305 offers a clock output that enables additional devices to be slaved to the same clock source.

4.3.1 Programming the RPM-based Fan Speed Control Algorithm

The RPM-based Fan Speed Control Algorithm is disabled upon device power up. The following registers control the algorithm. The EMC2305 fan control registers are pre-loaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

Note that steps 1 - 6 are optional and need only be performed if the default settings do not provide the desired fan response.

1. Set the Spin Up Configuration Register to the Spin Up Level and Spin Time desired.
2. Set the Fan Step Register to the desired step size.
3. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
4. Set the Update Time and Edges options in the Fan Configuration Register.
5. Set the Valid TACH Count Register to the highest tach count that indicates the fan is spinning. Refer to AN17.4 RPM to TACH Counts Conversion for examples and tables for supported RPM ranges (500, 1k, 2k, 4k).
6. Set the TACH Target Register to the desired tachometer count.
7. Enable the RPM-based Fan Speed Control Algorithm by setting the EN_ALGO bit.

4.4 Tachometer Measurement

The tachometer measurement circuitry is used in conjunction with the RPM-based Fan Speed Control Algorithm to update the fan driver output. Additionally, it can be used in Direct Setting mode as a diagnostic for host based fan control.

This method monitors the TACHx signal in real time. It constantly updates the tachometer measurement by reporting the number of clocks between a user programmed number of edges on the TACHx signal (see Table 5.12).

The tachometer measurement provides fast response times for the RPM-based Fan Speed Control Algorithm and the data is presented as a count value that represents the fan RPM period.

APPLICATION NOTE: The tachometer measurement method works independently of the drive settings. If the device is put into Direct Setting and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

4.4.1 Stalled Fan

A Stalled fan is detected if the tach counter exceeds the user-programmable Valid TACH Count setting. If a stall is detected, the device will flag the fan as stalled and trigger an interrupt.

If the RPM-based Fan Speed Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Direct Setting Mode or the Spin Up Routine is enabled, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Table 5.22) to allow the fan to reach a valid speed without generating unnecessary interrupts.
- In Direct Setting Mode, whenever the TACH Reading Register value exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When using the RPM-based Fan Speed Control Algorithm, the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

4.4.2 Aging Fan or Invalid Drive Detection

This is useful to detect aging fan conditions (where the fan's natural maximum speed degrades over time) or a speed setting that is faster than the fan is capable of. The EMC2305 contains circuitry that detects that the programmed fan speed can be reached by the fan. If the target fan speed cannot be reached within a user defined band of tach counts at maximum drive, the DRIVE_FAIL status bits are set and the ALERT# pin is asserted.

4.5 CLK Pin

The CLK pin has multiple functionality as determined by the pull-up decode of the ADDR_SEL pin and the settings of the Configuration register. The functionality associated with the CLK pin upon device power up is independent of the CLK pin functionality after the device has been configured.

4.5.1 Pull Up Decode

If additional functionality is enabled via the ADDR_SEL pin (see Section 3.1.2), then the CLK pin should be configured with a pull-up resistor to VDD and should not be used. The value of the pull-up resistor on the CLK pin is used to determine the default drive state of all fan drivers as shown in Table 4.2.

Table 4.2 CLK Pin Pull-Up Decode

PULL-UP RESISTOR	FAN DEFAULT DRIVE SETTING
4.7k Ohm ±5%	0% - OFF
6.8k Ohm ±5%	30%
10k Ohm ±5%	50%
15k Ohm ±5%	75%
22k Ohm ±5%	100%
33k Ohm ±5%	0% - OFF

4.5.2 External Clock

The EMC2305 allows the user to choose between supplying an external 32.768kHz clock or use of the internal 32kHz oscillator to measure the tachometer signal. This clock source is used by the RPM-based Fan Speed Control Algorithm to calculate the current fan speed. This fan controller accuracy is directly proportional to the accuracy of the clock source.

When this function is used, the external clock is driven into the device via the CLK pin.

4.5.3 Internal Clock

Alternately, the EMC2305 may be configured to use its internal clock as a clock output to drive other fan driver devices. When configured to operate in this mode, the device uses its internal clock for tachometer reading and drives the CLK pin using a push-pull driver.

4.6 Spin Up Routine

The EMC2305 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation.

The Spin Up Routine is initiated in Direct Setting mode when the setting value changes from 00h to anything else.

When the Fan Speed Control Algorithm is enabled, the Spin Up Routine is initiated under the following conditions:

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 5.15).
2. The RPM-based Fan Speed Control Algorithm's measured TACH Reading Register value is greater than the Valid TACH Count setting.

When the Spin Up Routine is operating, the fan driver is set to full scale (optional) for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set at a user defined level (30% through 65% drive).

After the Spin Up Routine has finished, the EMC2305 measures the TACHx signal. If the measured TACH Reading Register value is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 4.2 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

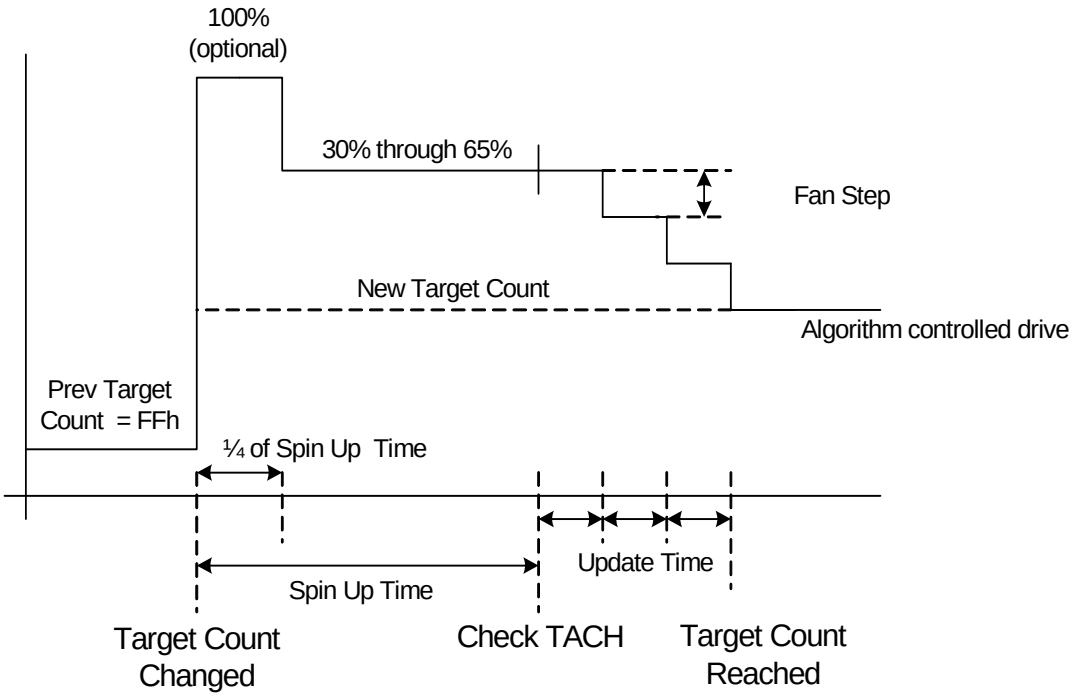


Figure 4.2 Spin Up Routine

4.6.1 Power Up Options

The EMC2305 allows for one of four fan speed options upon device power up depending on the status of the pull-up resistor on the ADDR_SEL pin and the CLK pin. If the ADDR_SEL pin decode enables the CLK pin (see Table 3.1), then the value of the pull-up resistor on the CLK pin is used to determine the default fan drive setting (see Section 4.5.1).

If the Fan drive setting is set at a non-zero value (as determined by the CLK pin), then the drive setting will be set to the desired setting. The Spin Up Routine will not be activated. This function does not disable the Watchdog timer which will continue to function normally. See Section 4.8.

4.7 Ramp Rate Control

The Fan Driver can be configured with automatic ramp rate control. Ramp rate control is accomplished by adjusting the drive output settings based on the Maximum Fan Step Register settings and the Update Time settings.

If the RPM-based Fan Speed Control Algorithm is used, then this ramp rate control is automatically used. The user programs a maximum step size for the fan drive setting and an update time. The update time varies from 100ms to 1.6s while the fan drive maximum step can vary from 1 count to 31 counts.

When a new fan drive setting is entered, the delta from the next fan drive setting and the previous fan drive setting is determined. If this delta is greater than the Max Step settings, then the fan drive setting is incrementally adjusted every 100ms to 1.6s as determined by the Update Time until the target fan drive setting is reached. See Figure 4.3.

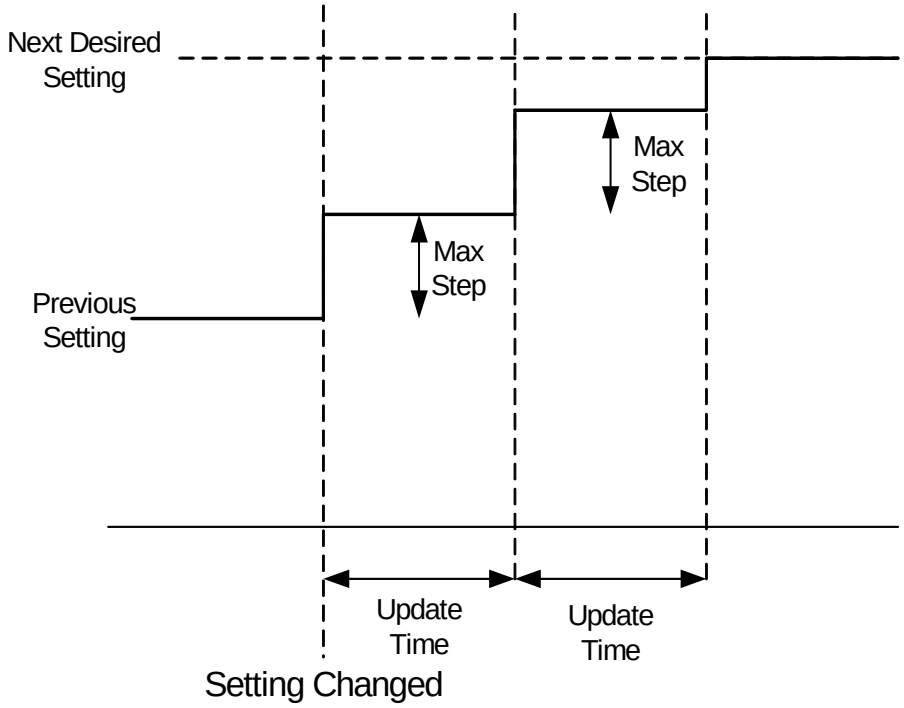


Figure 4.3 Ramp Rate Control

4.8 Watchdog Timer

The EMC2305 contains an internal Watchdog Timer for all fan drivers. The Watchdog timer monitors the SMBus traffic for signs of activity and works in two different modes based upon device operation. These modes are Power Up Operation and Continuous Operation as described below.

For either mode of operation, if four (4) seconds elapse without activity detected by the host, then the watchdog will be triggered and the following will occur:

1. The WATCH status bit will be set.
2. The fan driver will be set to full scale drive. It will remain at full scale drive until it is disabled.
3. The ALERT# pin is asserted.

APPLICATION NOTE: When the Watchdog timer is activated, the Fan Speed Control Algorithm is automatically disabled. Disabling the Watchdog will not automatically set the fan drive nor re-activate the Fan Speed Control Algorithm. This must be done manually.

4.8.1 Power Up Operation

The Watchdog Timer only starts immediately after power-up. Once it has been triggered or deactivated, it will not restart although it can be configured to operate in Continuous operation. While the Watchdog timer is active, the device will not check for a Stalled Fan condition.

In the Power Up Operation, the Watchdog Timer is disabled by any of the following actions:

1. Writing the Fan Setting Register will disable the Watchdog Timer.
2. Enabling the RPM-based Fan Speed Control Algorithm by setting the EN_ALGO bit will disable the Watchdog Timer. The fan driver will be set based on the RPM-based Fan Speed Control Algorithm.

Writing any other configuration registers will not disable the Watchdog Timer upon power up.

4.8.2 Continuous Operation

When configured to operate in Continuous Operation, the Watchdog timer will start immediately. The timer will be reset by any access (read or write) to the SMBus register set. The four second Watchdog timer will restart upon completion of SMBus activity.

Chapter 5 Register Set

5.1 Register Map

The following registers are accessible through the SMBus Interface. All register bits marked as '-' will always read '0'. A write to these bits will have no effect.

Table 5.1 EMC2305 Register Set

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Configuration and control						
20h	R/W	Configuration	Configures the clocking and watchdog functionality	40h	SWL	Page 31
24h	R-C	Fan Status	Stores the status bits for the RPM-based Fan Speed Control Algorithm	00h	No	Page 32
25h	R-C	Fan Stall Status	Stores status bits associated with a stalled fan	00h	No	Page 32
26h	R-C	Fan Spin Status	Stores status bits associated with a spin-up failure	00h	No	Page 32
27h	R-C	Drive Fail Status	Stores status bits associated with drive failure	00h	No	Page 32
29h	R/W	Fan Interrupt Enable Register	Controls the masking of interrupts on all fan related channels	00h	No	Page 33
2Ah	R/W	PWM Polarity Config	Configures Polarity of all PWM drivers	00h	No	Page 34
2Bh	R/W	PWM Output Config	Configures Output type of PWM drivers	00h	No	Page 34
2Ch	R/W	PWM Base Frequency 1	Selects the base frequency for PWM outputs 5 - 4	00h	No	Page 35
2Dh	R/W	PWM Base Frequency 2	Selects the base frequency for PWM outputs 3 - 1	00h	No	Page 35
Fan 1 Control Registers						
30h	R/W	Fan 1 Setting	Always displays the most recent fan driver input setting for Fan 1. If the RPM-based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 36
31h	R/W	PWM 1 Divide	Stores the divide ratio to set the frequency for Fan 1	01h	No	Page 36
32h	R/W	Fan 1 Configuration 1	Sets configuration values for the RPM-based Fan Speed Control Algorithm for the Fan 1 driver	2Bh	No	Page 37
33h	R/W	Fan 1 Configuration 2	Sets additional configuration values for the Fan 1 driver	28h	SWL	Page 38

Table 5.1 EMC2305 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
35h	R/W	Gain 1	Holds the gain terms used by the RPM-based Fan Speed Control Algorithm for the Fan 1 driver	2Ah	SWL	Page 40
36h	R/W	Fan 1 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 1 driver	19h	SWL	Page 41
37h	R/W	Fan 1 Max Step	Sets the maximum change per update for the Fan 1 driver	10h	SWL	Page 43
38h	R/W	Fan 1 Minimum Drive	Sets the minimum drive value for the Fan 1 driver	66h (40%)	SWL	Page 44
39h	R/W	Fan 1 Valid TACH Count	Holds the tachometer reading that indicates Fan 1 is spinning properly	F5h	SWL	Page 44
3Ah	R/W	Fan 1 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 45
3Bh	R/W	Fan 1 Drive Fail Band High Byte		00h	SWL	
3Ch	R/W	TACH 1 Target Low Byte	Holds the target tachometer reading low byte for Fan 1	F8h	No	Page 46
3Dh	R/W	TACH 1 Target High Byte	Holds the target tachometer reading high byte for Fan 1	FFh	No	Page 46
3Eh	R	TACH 1 Reading High Byte	Holds the tachometer reading high byte for Fan 1	FFh	No	Page 47
3Fh	R	TACH 1 Reading Low Byte	Holds the tachometer reading low byte for Fan 1	F8h	No	Page 47
Fan 2 Control Registers						
40h	R/W	Fan 2 Setting	Always displays the most recent fan driver input setting for Fan 2. If the RPM-based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 36
41h	R/W	PWM 2 Divide	Stores the divide ratio to set the frequency for Fan 2	01h	No	Page 36
42h	R/W	Fan 2 Configuration1	Sets configuration values for the RPM-based Fan Speed Control Algorithm for Fan 2	2Bh	No	Page 37
43h	R/W	Fan 2 Configuration 2	Sets additional configuration values for the Fan 2 driver	28h	SWL	Page 38
45h	R/W	Gain 2	Holds the gain terms used by the RPM-based Fan Speed Control Algorithm for Fan 2	2Ah	SWL	Page 40
46h	R/W	Fan 2 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 2 driver	19h	SWL	Page 41

Table 5.1 EMC2305 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
47h	R/W	Fan 2 Max Step	Sets the maximum change per update for Fan 2	10h	SWL	Page 43
48h	R/W	Fan 2 Minimum Drive	Sets the minimum drive value for the Fan 2 driver	66h (40%)	SWL	Page 44
49h	R/W	Fan 2 Valid TACH Count	Holds the tachometer reading that indicates Fan 2 is spinning properly	F5h	SWL	Page 44
4Ah	R/W	Fan 2 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 45
4Bh	R/W	Fan 2 Drive Fail Band High Byte		00h	SWL	
4Ch	R/W	TACH 2 Target Low Byte	Holds the target tachometer setting low byte for Fan 2	F8h	No	Page 46
4Dh	R/W	TACH 2 Target High Byte	Holds the target tachometer setting high byte for Fan 2	FFh	No	Page 46
4Eh	R	TACH 2 Reading High Byte	Holds the tachometer reading high byte for Fan 2	FFh	No	Page 47
4Fh	R	TACH 2 Reading Low Byte	Holds the tachometer reading low byte for Fan 2	F8h	No	Page 47
Fan 3 Control Registers						
50h	R/W	Fan 3 Setting	Always displays the most recent fan driver input setting for Fan 3. If the RPM-based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 36
51h	R/W	PWM 3 Divide	Stores the divide ratio to set the frequency for Fan 3	01h	No	Page 36
52h	R/W	Fan 3 Configuration 1	Sets configuration values for the RPM-based Fan Speed Control Algorithm for the Fan 3 driver	2Bh	No	Page 37
53h	R/W	Fan 3 Configuration 2	Sets additional configuration values for the Fan 3 driver	28h	SWL	Page 38
55h	R/W	Gain 3	Holds the gain terms used by the RPM-based Fan Speed Control Algorithm for the Fan 3 driver	2Ah	SWL	Page 40
56h	R/W	Fan 3 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 3 driver	19h	SWL	Page 41
57h	R/W	Fan 3 Max Step	Sets the maximum change per update for the Fan 3 driver	10h	SWL	Page 43
58h	R/W	Fan 3 Minimum Drive	Sets the minimum drive value for the Fan 3 driver	66h (40%)	SWL	Page 44
59h	R/W	Fan 3 Valid TACH Count	Holds the tachometer reading that indicates Fan 3 is spinning properly	F5h	SWL	Page 44

Table 5.1 EMC2305 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
5Ah	R/W	Fan 3 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 45
5Bh	R/W	Fan 3 Drive Fail Band High Byte		00h	SWL	
5Ch	R/W	TACH 3 Target Low Byte	Holds the target tachometer reading low byte for Fan 3	F8h	No	Page 46
5Dh	R/W	TACH 3 Target High Byte	Holds the target tachometer reading high byte for Fan 3	FFh	No	Page 46
5Eh	R	TACH 3 Reading High Byte	Holds the tachometer reading high byte for Fan 3	FFh	No	Page 47
5Fh	R	TACH 3 Reading Low Byte	Holds the tachometer reading low byte for Fan 3	F8h	No	Page 47
Fan 4 Control Registers						
60h	R/W	Fan 4 Setting	Always displays the most recent fan driver input setting for Fan 4. If the RPM- based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 36
61h	R/W	PWM 4 Divide	Stores the divide ratio to set the frequency for Fan 4	01h	No	Page 36
62h	R/W	Fan 4 Configuration1	Sets configuration values for the RPM-based Fan Speed Control Algorithm for Fan 4	2Bh	No	Page 37
63h	R/W	Fan 4 Configuration 2	Sets additional configuration values for the Fan 4 driver	28h	SWL	Page 38
65h	R/W	Gain 4	Holds the gain terms used by the RPM-based Fan Speed Control Algorithm for Fan 4	2Ah	SWL	Page 40
66h	R/W	Fan 4 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 4 driver	19h	SWL	Page 41
67h	R/W	Fan 4 Max Step	Sets the maximum change per update for Fan 4	10h	SWL	Page 43
68h	R/W	Fan 4 Minimum Drive	Sets the minimum drive value for the Fan 4 driver	66h (40%)	SWL	Page 44
69h	R/W	Fan 4 Valid TACH Count	Holds the tachometer reading that indicates Fan 4 is spinning properly	F5h	SWL	Page 44
6Ah	R/W	Fan 4 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 45
6Bh	R/W	Fan 4 Drive Fail Band High Byte		00h	SWL	
6Ch	R/W	TACH 4 Target Low Byte	Holds the target tachometer setting low byte for Fan 4	F8h	No	Page 46

Table 5.1 EMC2305 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
6Dh	R/W	TACH 4 Target High Byte	Holds the target tachometer setting high byte for Fan 4	FFh	No	Page 46
6Eh	R	TACH 4 Reading High Byte	Holds the tachometer reading high byte for Fan 4	FFh	No	Page 47
6Fh	R	TACH 4 Reading Low Byte	Holds the tachometer reading low byte for Fan 4	F8h	No	Page 47
Fan 5 Control Registers						
70h	R/W	Fan 5 Setting	Always displays the most recent fan driver input setting for Fan 5. If the RPM- based Fan Speed Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 36
71h	R/W	PWM 5 Divide	Stores the divide ratio to set the frequency for Fan 5	01h	No	Page 36
72h	R/W	Fan 5 Configuration1	Sets configuration values for the RPM-based Fan Speed Control Algorithm for Fan 5	2Bh	No	Page 37
73h	R/W	Fan 5 Configuration 2	Sets additional configuration values for the Fan 5 driver	28h	SWL	Page 38
75h	R/W	Gain 5	Holds the gain terms used by the RPM-based Fan Speed Control Algorithm for Fan 5	2Ah	SWL	Page 40
76h	R/W	Fan 5 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 5 driver	19h	SWL	Page 41
77h	R/W	Fan 5 Max Step	Sets the maximum change per update for Fan 5	10h	SWL	Page 43
78h	R/W	Fan 5 Minimum Drive	Sets the minimum drive value for the Fan 5 driver	66h (40%)	SWL	Page 44
79h	R/W	Fan 5 Valid TACH Count	Holds the tachometer reading that indicates Fan 5 is spinning properly	F5h	SWL	Page 44
7Ah	R/W	Fan 5 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	Page 45
7Bh	R/W	Fan 5 Drive Fail Band High Byte		00h	SWL	
7Ch	R/W	TACH 5 Target Low Byte	Holds the target tachometer setting low byte for Fan 5	F8h	No	Page 46
7Dh	R/W	TACH 5 Target High Byte	Holds the target tachometer setting high byte for Fan 5	FFh	No	Page 46
7Eh	R	TACH 5 Reading High Byte	Holds the tachometer reading high byte for Fan 5	FFh	No	Page 47
7Fh	R	TACH 5 Reading Low Byte	Holds the tachometer reading low byte for Fan 5	F8h	No	Page 47

Table 5.1 EMC2305 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Lock Register						
EF	R/W	Software Lock	Locks all SWL registers	00h	SWL	Page 48
Revision Registers						
FCh	R	Product Features	Indicates functions determined upon device power up by external pin states	00h	No	Page 48
FDh	R	Product ID	Stores the unique Product ID	34h	No	Page 49
FEh	R	Manufacturer ID	Stores the Manufacturer ID	5Dh	No	Page 50
FFh	R	Revision	Revision	80h	No	Page 50

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

5.1.1 Lock Entries

The Lock Column describes the locking mechanism, if any, used for individual registers. All SWL registers are Software Locked and therefore made read-only when the LOCK bit is set.

5.2 Configuration Register

Table 5.2 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
20h	R/W	Configuration	MASK	DIS_TO	WD_EN	-	-	-	DR_EXT_CLK	USE_EXT_CLK	40h

The Configuration Register controls the basic functionality of the EMC2305. The bits are described below. The Configuration Register is software locked.

Bit 7 - MASK - Blocks the ALERT# pin from being asserted.

- ‘0’ (default) - The ALERT# pin is unmasked. If any bit in the status registers is set, the ALERT# pin will be asserted (unless individually masked via the Fan Interrupt Enable Register).
- ‘1’ - The ALERT# pin is masked and will not be asserted.

Bit 6 - DIS_TO - Disables the SMBus timeout function for the SMBus client (if enabled).

- ‘0’ - The SMBus timeout function is enabled.
- ‘1’ (default) - The SMBus timeout function is disabled allowing the device to be fully I^2C compliant.

Bit 5 - WD_EN - Enables the Watchdog timer (see Section 4.8) to operate in Continuous Mode.

- ‘0’ (default) - The Watchdog timer does not operate continuously. It will function upon power up and at no other time (see Section 4.8.1).
- ‘1’ - The Watchdog timer operates continuously as described in Section 4.8.2.

Bit 1 - DR_EXT_CLK - Enables the internal tachometer clock to be driven out on the CLK pin so that multiple devices can be synced to the same source.

- '0' (default) - The CLK pin acts as a clock input.
- '1' - The CLK pin acts as a clock output and is a push-pull driver.

Bit 0 - USE_EXT_CLK - Enables the EMC2305 to use a clock present on the CLK pin as the tachometer clock. If the DR_EXT_CLK bit is set, then this bit is ignored and the device will use the internal oscillator.

- '0' (default) - The EMC2305 will use its internal oscillator for all Tachometer measurements.
- '1' - The EMC2305 will use the oscillator presented on the CLK pin for all Tachometer measurements.

5.3 Fan Status Registers

Table 5.3 Fan Status Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
24h	R-C	Fan Status	WATCH	-	-	-	-	DRIVE_ FAIL	FAN_ SPIN	FAN_ STALL	00h
25h	R-C	Fan Stall Status	-	-	-	FAN5_ STALL	FAN4_ STALL	FAN3_ STALL	FAN2_ STALL	FAN1_ STALL	00h
26h	R-C	Fan Spin Status	-	-	-	FAN5_ SPIN	FAN4_ SPIN	FAN3_ SPIN	FAN2_ SPIN	FAN1_ SPIN	00h
27h	R-C	Fan Drive Fail Status	-	-	-	DRIVE_ FAIL5	DRIVE_ FAIL4	DRIVE_ FAIL3	DRIVE_ FAIL2	DRIVE_ FAIL1	00h

The Fan Status registers contain the status bits associated with each fan driver.

5.3.1 Fan Status - 24h

The Fan Status register indicates that one or more of the fan drivers has stalled or failed or that the Watchdog Timer has expired (see Section 4.8).

Bit 7 - WATCH - Indicates that the Watchdog Timer has expired. When set, each fan is driven to 100% duty cycle and will remain at 100% duty cycle until they are programmed. This bit is cleared when it is read.

Bit 2 - DRIVE_FAIL - Indicates that one or more fan drivers cannot meet the programmed fan speed at maximum PWM duty cycle. This bit is set when any bit in the Fan Drive Fail Status register is set and cleared when all bits in the Fan Drive Fail Status register are cleared.

Bit 1 - FAN_SPIN - Indicates that one or more fan drivers cannot spin up. This bit is set when any bit in the Fan Spin Status register is set and cleared when all of the bits in the Fan Spin Status register are cleared.

Bit 0 - FAN_STALL - Indicates that one or more fan drivers have stalled. This bit is set when any bit in the Fan Stall Status register is set and cleared when all of the bits in the Fan Stall Status register are cleared.

5.3.2 Fan Stall Status - 25h

The Fan Stall Status register indicates which fan driver has detected a stalled condition (see Section 4.4.1). All bits are cleared upon a read if the error condition has been removed.

Bit 4 - FAN5_STALL - Indicates that Fan 5 has stalled.

Bit 3 - FAN4_STALL - Indicates that Fan 4 has stalled.

Bit 2 - FAN3_STALL - Indicates that Fan 3 has stalled.

Bit 1 - FAN2_STALL - Indicates that Fan 2 has stalled.

Bit 0 - FAN1_STALL - Indicates that Fan 1 has stalled.

5.3.3 Fan Spin Status - 26h

The Fan Spin Status register indicates which fan driver has failed to spin-up (see Section 4.6). All bits are cleared upon a read if the error condition has been removed.

Bit 4 - FAN5_SPIN - Indicates that Fan 5 has failed to spin up.

Bit 3 - FAN4_SPIN - Indicates that Fan 4 has failed to spin up.

Bit 2 - FAN3_SPIN - Indicates that Fan 3 has failed to spin up.

Bit 1 - FAN2_SPIN - Indicates that Fan 2 has failed to spin up.

Bit 0 - FAN1_SPIN - Indicates that Fan 1 has failed to spin up.

5.3.4 Fan Drive Fail Status - 27h

The Fan Drive Fail Status register indicates which fan driver cannot drive to the programmed speed even at 100% duty cycle (see Section 4.4.2 and Section 5.12). All bits are cleared upon a read if the error condition has been removed.

Bit 4 - DRIVE_FAIL5 - Indicates that Fan 5 cannot reach its programmed fan speed even at 100% duty cycle. This may be due to an aging fan or invalid programming.

Bit 3 - DRIVE_FAIL4 - Indicates that Fan 4 cannot reach its programmed fan speed even at 100% duty cycle. This may be due to an aging fan or invalid programming.

Bit 2 - DRIVE_FAIL3 - Indicates that Fan 3 cannot reach its programmed fan speed even at 100% duty cycle. This may be due to an aging fan or invalid programming.

Bit 1 - DRIVE_FAIL2 - Indicates that Fan 2 cannot reach its programmed fan speed even at 100% duty cycle. This may be due to an aging fan or invalid programming.

Bit 0 - DRIVE_FAIL1 - Indicates that Fan 1 cannot reach its programmed fan speed even at 100% duty cycle. This may be due to an aging fan or invalid programming.

5.4 Fan Interrupt Enable Register

Table 5.4 Fan Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
29h	R/W	Fan Interrupt Enable	-	-	-	FAN5_ INT_EN	FAN4_ INT_EN	FAN3_ INT_EN	FAN2_ INT_EN	FAN1_ INT_EN	00h

The Fan Interrupt Enable controls the masking for each Fan channel. When a channel is enabled, it will cause the ALERT# pin to be asserted when an error condition is detected.

Bit 4 - FAN5_INT_EN - Allows Fan 5 to assert the ALERT# pin if an error condition is detected.

Bit 3 - FAN4_INT_EN - Allows Fan 4 to assert the ALERT# pin if an error condition is detected.

Bit 2 - FAN3_INT_EN - Allows Fan 3 to assert the ALERT# pin if an error condition is detected.

Bit 1 - FAN2_INT_EN - Allows Fan 2 to assert the ALERT# pin if an error condition is detected.

Bit 0 - FAN1_INT_EN - Allows Fan 1 to assert the ALERT# pin if an error condition is detected.

- '0' (default) - An error condition on Fan X will not cause the ALERT# pin to be asserted, however the status registers will be updated normally.
- '1' - An error condition (Stall, Spin Up, Drive Fail) on Fan X will cause the ALERT# pin to be asserted.

5.5 PWM Configuration Registers

Table 5.5 PWM Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Ah	R/W	PWM Polarity Config	-	-	-	POLARITY 5	POLARITY 4	POLARITY 3	POLARITY 2	POLARITY 1	00h
2Bh	R/W	PWM Output Config	-	-	-	PWM5_OT	PWM4_OT	PWM3_OT	PWM2_OT	PWM1_OT	00h

The PWM Config registers control the output type and polarity of all PWM outputs.

5.5.1 PWM Polarity Config - 2Ah

Bit 4 - POLARITY5 - Determines the polarity of PWM 5.

Bit 3 - POLARITY4 - Determines the polarity of PWM 4.

Bit 2 - POLARITY3 - Determines the polarity of PWM 3.

Bit 1 - POLARITY2 - Determines the polarity of PWM 2.

Bit 0 - POLARITY1 - Determines the polarity of PWM 1.

- '0' (default) - the Polarity of the PWM driver is normal. A drive setting of 00h will cause the output to be set at 0% duty cycle and a drive setting of FFh will cause the output to be set at 100% duty cycle.
- '1' - The Polarity of the PWM driver is inverted. A drive setting of 00h will cause the output to be set at 100% duty cycle and a drive setting of FFh will cause the output to be set at 0% duty cycle.

5.5.2 PWM Output Config - 2Bh

Bit 4 - PWM5_OT - Determines the output type of the PWM 5 driver.

Bit 3 - PWM4_OT - Determines the output type of the of PWM 4 driver.

Bit 2 - PWM3_OT - Determines the output type of the of PWM 3 driver.

Bit 1 - PWM2_OT - Determines the output type of PWM 2 driver.

Bit 0 - PWM1_OT - Determines the output type of the PWM 1 driver.

- '0' (default) - The PWM 1 output is configured as an open drain output.
- '1' - The PWM 1 output is configured as a push-pull output.

5.6 PWM Base Frequency Registers

Table 5.6 PWM Base Frequency Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Ch	R/W	PWM Base Frequency 1	-	-	-	-	PWM_BASE5 [1:0]		PWM_BASE4 [1:0]		00h
2Dh	R/W	PWM Base Frequency 2	-	-	PWM_ BASE 3_1	PWM_ BASE 3_0	PWM_ BASE 2_1	PWM_ BASE 2_0	PWM_ BASE 1_1	PWM_ BASE 1_0	00h

The PWM Base Frequency registers determine the base frequency that is used with the PWM Divide register to determine the final PWM frequency. Each PWM frequency is set by the base frequency and its respective divide ratio (see Section 5.8).

5.6.1 PWM Base Frequency 1 - 2Bh

Controls the base frequency of PWM drivers 4 and 5.

Bits 3-2 - PWM_BASE5[1:0] - Determines the base frequency of the PWM5 driver.

Bits 1-0 - PWM_BASE4[1:0] - Determines the base frequency of the PWM4 driver.

5.6.2 PWM Base Frequency 2 - 2Ch

Controls the base frequency of PWM drivers 1-3

Bits 5-6 - PWM_BASE3[1:0] - Determines the base frequency of the PWM3 driver.

Bits 3-2 - PWM_BASE2[1:0] - Determines the base frequency of the PWM2 driver.

Bits 1-0 - PWM_BASE1[1:0] - Determines the base frequency of the PWM1 driver.

Table 5.7 PWM_BASEx[1:0] Bit Decode

PWM_BASEX[1:0]		BASE FREQUENCY
1	0	
0	0	26.00kHz (default)
0	1	19.531kHz
1	0	4,882Hz
1	1	2,441Hz

5.7 Fan Setting Registers

Table 5.8 Fan Driver Setting Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	R/W	Fan 1 Setting	128	64	32	16	8	4	2	1	00h
40h	R/W	Fan 2 Setting	128	64	32	16	8	4	2	1	00h
50h	R/W	Fan 3 Setting	128	64	32	16	8	4	2	1	00h
60h	R/W	Fan 4 Setting	128	64	32	16	8	4	2	1	00h
70h	R/W	Fan 5 Setting	128	64	32	16	8	4	2	1	00h

The Fan Setting register always displays the current setting of the respective fan driver. Reading from any of the registers will report the current fan speed setting of the appropriate fan driver regardless of the operating mode. Therefore it is possible that reading from this register will not report data that was previously written into this register.

While the RPM-based Fan Speed Control Algorithm is active, the register is read only. Writing to the register will have no effect and the data will not be stored.

The contents of the register represent the weighting of each bit in determining the final output voltage. The output drive for a PWM output is given by Equation [1].

$$Drive = \left(\frac{VALUE}{255}\right) \times 100\% \quad \textbf{[1]}$$

5.8 PWM Divide Registers

Table 5.9 PWM Divide Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
31h	R/W	Fan 1 Divide	128	64	32	16	8	4	2	1	01h
41h	R/W	Fan 2 Divide	128	64	32	16	8	4	2	1	01h
51h	R/W	Fan 3 Divide	128	64	32	16	8	4	2	1	01h
61h	R/W	Fan 4 Divide	128	64	32	16	8	4	2	1	01h
71h	R/W	Fan 5 Divide	128	64	32	16	8	4	2	1	01h

The PWM Divide registers determine the final frequency of the respective PWM Fan Driver. Each driver base frequency is divided by the value of the respective PWM Divide Register to determine the final frequency. The duty cycle settings are not affected by these settings, only the final frequency of the PWM driver. A value of 00h will be decoded as 01h.

5.9 Fan Configuration 1 Registers

Table 5.10 Fan Configuration 1 Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
32h	R/W	Fan 1 Configuration 1	EN_ ALGO1	RANGE1[1:0]		EDGES1[1:0]		UPDATE1[2:0]			2Bh
42h	R/W	Fan 2 Configuration 1	EN_ ALGO2	RANGE2[1:0]		EDGES2[1:0]		UPDATE2[2:0]			2Bh
52h	R/W	Fan 3 Configuration 1	EN_ ALGO3	RANGE3[1:0]		EDGES3[1:0]		UPDATE3[2:0]			2Bh
62h	R/W	Fan 4 Configuration 1	EN_ ALGO4	RANGE4[1:0]		EDGES4[1:0]		UPDATE4[2:0]			2Bh
72h	R/W	Fan 5 Configuration 1	EN_ ALGO5	RANGE5[1:0]		EDGES5[1:0]		UPDATE5[2:0]			2Bh

The Fan Configuration 1 registers control the general operation of the RPM-based Fan Speed Control Algorithm used for the respective Fan Driver.

Bit 7 - EN_ALGOx - enables the RPM-based Fan Speed Control Algorithm.

- '0' - (default) the control circuitry is disabled and the fan driver output is determined by the Fan Driver Setting Register.
- '1' - the control circuitry is enabled and the Fan Driver output will be automatically updated to maintain the programmed fan speed as indicated by the TACH Target Register.

Bits 6- 5 - RANGEx[1:0] - Adjusts the range of reported and programmed tachometer reading values. The RANGE bits determine the weighting of all TACH values (including the Valid TACH Count, TACH Target, and TACH reading) as shown in Table 5.11.

Table 5.11 Range Decode

RANGEX[1:0]		REPORTED MINIMUM RPM	TACH COUNT MULTIPLIER
1	**0**		
0	0	500	1
0	1	1000 (default)	2
1	0	2000	4
1	1	4000	8

Bits 4-3 - EDGESx[1:0] - determines the minimum number of edges that must be detected on the TACHx signal to determine a single rotation. A typical fan measured 5 edges (for a 2-pole fan). For more accurate tachometer measurement, the minimum number of edges measured may be increased.

Increasing the number of edges measured with respect to the number of poles of the fan will cause the TACH Reading registers to indicate a fan speed that is higher or lower than the actual speed. In order for the FSC Algorithm to operate correctly, the TACH Target must be updated by the user to accommodate this shift. The Effective Tach Multiplier shown in Table 5.12 is used as a direct multiplier term that is applied to the Actual RPM to achieve the Reported RPM. It should only be applied if the

number of edges measured does not match the number of edges expected based on the number of poles of the fan (which is fixed for any given fan).

Contact SMSC for recommended settings when using fans with more or less than 2 poles.

Table 5.12 Minimum Edges for Fan Rotation

EDGESX[1:0]		MINIMUM TACH EDGES	NUMBER OF FAN POLES	EFFECTIVE TACH MULTIPLIER (BASED ON 2 POLE FANS)
1	0			
0	0	3	1 pole	0.5
0	1	5	2 poles (default)	1
1	0	7	3 poles	1.5
1	1	9	4 poles	2

Bit 2-0 - UPDATEx[2:0] - determines the base time between fan driver updates. The Update Time, along with the Fan Step Register, is used to control the ramp rate of the drive response to provide a cleaner transition of the actual fan operation as the desired fan speed changes. The Update Time is set as shown in Table 5.13.

Table 5.13 Update Time

UPDATEX[2:0]			UPDATE TIME
2	1	0	
0	0	0	100ms
0	0	1	200ms
0	1	0	300ms
0	1	1	400ms (default)
1	0	0	500ms
1	0	1	800ms
1	1	0	1200ms
1	1	1	1600ms

5.10 Fan Configuration 2 Registers

Table 5.14 Fan Configuration 2 Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
33h	R/W	Fan 1 Configuration 2	-	EN_RRC1	GLITCH_EN1	DER_OPT1 [1:0]		ERR_RNG1[1:0]		-	28h
43h	R/W	Fan 2 Configuration 2	-	EN_RRC2	GLITCH_EN2	DER_OPT2 [1:0]		ERR_RNG2[1:0]		-	28h

Table 5.14 Fan Configuration 2 Registers (continued)

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
53h	R/W	Fan 3 Configuration 2	-	EN_ RRC3	GLITCH_ EN3	DER_OPT3 [1:0]		ERR_RNG3[1:0]		-	28h
63h	R/W	Fan 4 Configuration 2	-	EN_ RRC4	GLITCH_ EN4	DER_OPT4 [1:0]		ERR_RNG4[1:0]		-	28h
73h	R/W	Fan 5 Configuration 2	-	EN_ RRC5	GLITCH_ EN5	DER_OPT5 [1:0]		ERR_RN55[1:0]		-	28h

The Fan Configuration 2 registers control the tachometer measurement and advanced features of the RPM-based Fan Speed Control Algorithm.

Bit 6 - EN_RRCx - Enables ramp rate control when the corresponding fan driver is operated in the Direct Setting Mode.

- '0' (default) - Ramp rate control is disabled. When the fan driver is operating in Direct Setting mode, the fan setting will instantly transition to the next programmed setting.
- '1' - Ramp rate control is enabled. When the fan driver is operating in Direct Setting mode, the fan drive setting will follow the ramp rate controls as determined by the Fan Step and Update Time settings. The maximum fan drive setting step is capped at the Fan Step setting and is updated based on the Update Time as given by Table 5.13.

Bit 5 - GLITCH_ENx - Disables the low pass glitch filter that removes high frequency noise injected on the TACHx pin.

- '0' - The glitch filter is disabled.
- '1' (default) - The glitch filter is enabled.

Bits 4 - 3 - DER_OPTx[1:0] - Control some of the advanced options that affect the derivative portion of the RPM-based Fan Speed Control Algorithm as shown in Table 5.15.

Table 5.15 Derivative Options

DER_OPTX[1:0]		OPERATION
1	**0**	
0	0	No derivative options used
0	1	Basic derivative. The derivative of the error from the current drive setting and the target is added to the iterative Fan Drive Register setting (in addition to proportional and integral terms) (default)
1	0	Step derivative. The derivative of the error from the current drive setting and the target is added to the iterative Fan Drive Register setting and is not capped by the Fan Step Register.
1	1	Both the basic derivative and the step derivative are used effectively causing the derivative term to have double the effect of the derivative term.

Bit 2 - 1 - ERR_RNGx[1:0] - Control some of the advanced options that affect the error window. When the measured fan speed is within the programmed error window around the target speed, then the fan

drive setting is not updated. The algorithm will continue to monitor the fan speed and calculate necessary drive setting changes based on the error; however, these changes are ignored.

Table 5.16 Error Range Options

ERR_RNGX[1:0]		OPERATION
1	0	
0	0	0 RPM (default)
0	1	50 RPM
1	0	100 RPM
1	1	200 RPM

5.11 Gain Registers

Table 5.17 Gain Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
35h	R/W	Gain 1 Register	-	-	GAIND1[1:0]		GAINI1[1:0]		GAINP1[1:0]		2Ah
45h	R/W	Gain 2 Register	-	-	GAIND2[1:0]		GAINI2[1:0]		GAINP2[1:0]		2Ah
55h	R/W	Gain 3 Register	-	-	GAIND3[1:0]		GAINI3[1:0]		GAINP3[1:0]		2Ah
65h	R/W	Gain 4 Register	-	-	GAIND4[1:0]		GAINI4[1:0]		GAINP4[1:0]		2Ah
75h	R/W	Gain 5 Register	-	-	GAIND5[1:0]		GAINI5[1:0]		GAINP5[1:0]		2Ah

The Gain registers store the gain terms used by the proportional and integral portions of each of the RPM-based Fan Speed Control Algorithms. These gain terms are used as the KD, KI, and KP gain terms in a classic PID control solution.

Bits 5 - 4 - GAINDX[1:0] - Controls the derivative gain term used by the FSC algorithm as shown in Table 5.18.

Bits 3-2 - GAINIX[1:0] - Controls the integral gain term used by the FSC algorithm as shown in Table 5.18.

Bits 1-0 - GAINP[1:0] - Controls the proportional gain term used by the FSC algorithm as shown in Table 5.18.

Table 5.18 Gain Decode

GAIND OR GAINP OR GAINI [1:0]		RESPECTIVE GAIN FACTOR
1	**0**	
0	0	1x
0	1	2x
1	0	4x (default)
1	1	8x

5.12 Fan Spin Up Configuration Registers

Table 5.19 Fan Spin Up Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
36h	R/W	Fan 1 Spin Up Configuration	DRIVE_FAIL_ CNT1 [1:0]		NOKICK1	SPIN_LVL1[2:0]			SPINUP_TIME 1 [1:0]		19h
46h	R/W	Fan 2 Spin up Configuration	DRIVE_FAIL_ CNT2 [1:0]		NOKICK2	SPIN_LVL2[2:0]			SPINUP_TIME 2 [1:0]		19h
56h	R/W	Fan 3 Spin up Configuration	DRIVE_FAIL_ CNT3 [1:0]		NOKICK3	SPIN_LVL3[2:0]			SPINUP_TIME 3[1:0]		19h
66h	R/W	Fan 4 Spin up Configuration	DRIVE_FAIL_ CNT4 [1:0]		NOKICK4	SPIN_LVL4[2:0]			SPINUP_TIME 4 [1:0]		19h
76h	R/W	Fan 5 Spin up Configuration	DRIVE_FAIL_ CNT5 [1:0]		NOKICK5	SPIN_LVL5[2:0]			SPINUP_TIME 5 [1:0]		19h

The Fan Spin Up Configuration registers control the settings of Spin Up Routine. The Fan Spin Up Configuration registers are software locked.

Bit 7 - 6 - DRIVE_FAIL_CNTx[1:0] - Determines how many update cycles are used for the Drive Fail detection function as shown in Table 5.20. This circuitry determines whether the fan can be driven to the desired tach target.

Table 5.20 DRIVE_FAIL_CNT[1:0] Bit Decode

DRIVE_FAIL_CNTX[1:0]		NUMBER OF UPDATE PERIODS
1	**0**	
0	0	Disabled - the Drive Fail detection circuitry is disabled (default)
0	1	16 - the Drive Fail detection circuitry will count for 16 update periods

Table 5.20 DRIVE_FAIL_CNT[1:0] Bit Decode (continued)

DRIVE_FAIL_CNTX[1:0]		NUMBER OF UPDATE PERIODS
1	**0**	
1	0	32 - the Drive Fail detection circuitry will count for 32 update periods
1	1	64 - the Drive Fail detection circuitry will count for 64 update periods

Bit 5 - NOKICKx - Determines if the Spin Up Routine will drive the fan to 100% duty cycle for 1/4 of the programmed spin up time before driving it at the programmed level.

- '0' (default) - The Spin Up Routine will drive the fan driver to 100% for 1/4 of the programmed spin up time before reverting to the programmed spin level.
- '1' - The Spin Up Routine will not drive the fan driver to 100%. It will set the drive at the programmed spin level for the entire duration of the programmed spin up time.

Bits 4 - 2 - SPIN_LVLx[2:0] - Determines the final drive level that is used by the Spin Up Routine as shown in Table 5.21.

Table 5.21 Spin Level

SPIN_LVLX[2:0]			SPIN UP DRIVE LEVEL
2	**1**	**0**	
0	0	0	30%
0	0	1	35%
0	1	0	40%
0	1	1	45%
1	0	0	50%
1	0	1	55%
1	1	0	60% (default)
1	1	1	65%

Bit 1 -0 - SPINUP_TIMEx[1:0] - determines the maximum Spin Time that the Spin Up Routine will run for (see Section 4.6). If a valid tachometer measurement is not detected before the Spin Time has elapsed, an interrupt will be generated. When the RPM-based Fan Speed Control Algorithm is active, the fan driver will attempt to re-start the fan immediately after the end of the last spin up attempt.

The Spin Time is set as shown in Table 5.22.

Table 5.22 Spin Time

SPINUP_TIMEX[1:0]		TOTAL SPIN UP TIME
1	**0**	
0	0	250 ms
0	1	500 ms (default)
1	0	1 sec
1	1	2 sec

5.13 Fan Max Step Registers

Table 5.23 Fan Max Step Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
37h	R/W	Fan 1 Max Step	-	-	32	16	8	4	2	1	10h
47h	R/W	Fan 2 Max Step	-	-	32	16	8	4	2	1	10h
57h	R/W	Fan 3 Max Step	-	-	32	16	8	4	2	1	10h
67h	R/W	Fan 4 Max Step	-	-	32	16	8	4	2	1	10h
77h	R/W	Fan 5 Max Step	-	-	32	16	8	4	2	1	10h

The Fan Max Step registers, along with the Update Time, control the ramp rate of the fan driver response calculated by the RPM-based Fan Speed Control Algorithm. The value of the register represents the maximum step size each fan driver will take between update times (see Section 5.9).

When the FSC algorithm is enabled, Ramp Rate control is automatically used. When the FSC is not active, then Ramp Rate control can be enabled by asserting the EN_RRC bit (see Section 5.10).

APPLICATION NOTE: The UPDATE bits and Fan Step Register settings operate independently of the RPM-based Fan Speed Control Algorithm and will always limit the fan drive setting. That is, if the programmed fan drive setting (either as determined by the RPM-based Fan Speed Control Algorithm or by manual settings) exceeds the current fan drive setting by greater than the Fan Step Register setting, the EMC2305 will limit the fan drive change to the value of the Fan Step Register. It will use the Update Time to determine how often to update the drive settings.

APPLICATION NOTE: If the Fan Speed Control Algorithm is used, the default settings in the Fan Configuration 2 Register will cause the maximum fan step settings to be ignored.

The Fan Max Step registers are software locked.

5.14 Fan Minimum Drive Registers

Table 5.24 Minimum Fan Drive Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
38h	R/W	Fan 1 Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)
48h	R/W	Fan 2 Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)
58h	R/W	Fan 3 Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)
68h	R/W	Fan 4 Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)
78h	R/W	Fan 5 Minimum Drive	128	64	32	16	8	4	2	1	66h (40%)

The Fan Minimum Drive registers store the minimum drive setting for each RPM-based Fan Speed Control Algorithm. The RPM-based Fan Speed Control Algorithm will not drive the fan at a level lower than the minimum drive unless the target Fan Speed is set at FFh (see Section 5.17).

During normal operation, if the fan stops for any reason (including low drive), the RPM-based Fan Speed Control Algorithm will attempt to restart the fan. Setting the Fan Minimum Drive Register to a setting that will maintain fan operation is a useful way to avoid potential fan oscillations as the control circuitry attempts to drive it at a level that cannot support fan operation.

The Fan Minimum Drive Registers are software locked.

5.15 Valid TACH Count Registers

Table 5.25 Valid TACH Count Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
39h	R/W	Valid TACH Count 1	4096	2048	1024	512	256	128	64	32	F5h
49h	R/W	Valid TACH Count 2	4096	2048	1024	512	256	128	64	32	F5h
59h	R/W	Valid TACH Count 3	4096	2048	1024	512	256	128	64	32	F5h
69h	R/W	Valid TACH Count 4	4096	2048	1024	512	256	128	64	32	F5h
79h	R/W	Valid TACH Count 5	4096	2048	1024	512	256	128	64	32	F5h

The Valid TACH Count registers store the maximum TACH Reading Register value to indicate that each fan is spinning properly. The value is referenced at the end of the Spin Up Routine to determine if the fan has started operating and decide if the device needs to retry. See Equation [2] in Section 5.18 for translating the count to an RPM.

If the TACH Reading Register value exceeds the Valid TACH Count Register (indicating that the Fan RPM is below the threshold set by this count), then a stalled fan is detected. In this condition, the algorithm will automatically begin its Spin Up Routine.

If a TACH Target setting is set above the Valid TACH Count setting, then that setting will be ignored and the algorithm will use the current fan drive setting.

The Valid TACH Count registers are software locked.

5.16 Fan Drive Fail Band Registers

Table 5.26 Fan Drive Fail Band Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Ah	R/W	Fan 1 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
3Bh	R/W	Fan 1 Drive Fail Band High Byte	4096	2048	1024	512	256	128	64	32	00h
4Ah	R/W	Fan 2 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
4Bh	R/W	Fan 2 Drive Fall Band High Byte	4096	2048	1024	512	256	128	64	32	00h
5Ah	R/W	Fan 3 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
5Bh	R/W	Fan 3 Drive Fail Band High Byte	4096	2048	1024	512	256	128	64	32	00h
6Ah	R/W	Fan 4 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
6Bh	R/W	Fan 4 Drive Fall Band High Byte	4096	2048	1024	512	256	128	64	32	00h
7Ah	R/W	Fan 5 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	00h
7Bh	R/W	Fan 5 Drive Fall Band High Byte	4096	2048	1024	512	256	128	64	32	00h

The Fan Drive Fail Band Registers store the number of tach counts used by the Fan Drive Fail detection circuitry. This circuitry is activated when the fan drive setting high byte is at FFh. When it is enabled, the actual measured fan speed is compared against the target fan speed. These registers are only used when the FSC is active.

This circuitry is used to indicate that the target fan speed at full drive is higher than the fan is actually capable of reaching. If the measured fan speed does not exceed the target fan speed minus the Fan Drive Fail Band Register settings for a period of time longer than set by the DRIVE_FAIL_CNTx[1:0] bits, then the DRIVE_FAIL status bit will be set and an interrupt generated.

5.17 TACH Target Registers

Table 5.27 TACH Target Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Ch	R/W	TACH Target 1 Low Byte	16	8	4	2	1	-	-	-	F8h
3Dh	R/W	TACH Target 1 High Byte	4096	2048	1024	512	256	128	64	32	FFh
4Ch	R	TACH Target 2 Low Byte	16	8	4	2	1	-	-	-	F8h
4Dh	R/W	TACH Target 2 High Byte	4096	2048	1024	512	256	128	64	32	FFh
5Ch	R	TACH Target 3 Low Byte	16	8	4	2	1	-	-	-	F8h
5Dh	R/W	TACH Target 3 High Byte	4096	2048	1024	512	256	128	64	32	FFh
6Ch	R	TACH Target 4 Low Byte	16	8	4	2	1	-	-	-	F8h
6Dh	R/W	TACH Target 4 High Byte	4096	2048	1024	512	256	128	64	32	FFh
7Ch	R	TACH Target 5 Low Byte	16	8	4	2	1	-	-	-	F8h
7Dh	R/W	TACH Target 5 High Byte	4096	2048	1024	512	256	128	64	32	FFh

The TACH Target Registers hold the target tachometer value that is maintained by the RPM-based Fan Speed Control Algorithm.

The value in the TACH Target Registers will always reflect the current TACH Target value.

If one of the algorithms is enabled, setting the TACH Target Register to FFh will disable the fan driver (set the fan drive setting to 0%). Setting the TACH Target to any other value (from a setting of FFh) will cause the algorithm to invoke the Spin Up Routine after which it will function normally.

The Tach Target is not applied until the high byte is written. Once the high byte is written, the current value of both high and low bytes will be used as the next Tach target.

5.18 TACH Reading Registers

Table 5.28 TACH Reading Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Eh	R	Fan 1 TACH	4096	2048	1024	512	256	128	64	32	FFh
3Fh	R	Fan 1 TACH Low Byte	16	8	4	2	1	-	-	-	F8h
4Eh	R	Fan 2 TACH	4096	2048	1024	512	256	128	64	32	FFh
4Fh	R	Fan 2 TACH Low Byte	16	8	4	2	1	-	-	-	F8h
5Eh	R	Fan 3 TACH	4096	2048	1024	512	256	128	64	32	FFh
5Fh	R	Fan 3 TACH Low Byte	16	8	4	2	1	-	-	-	F8h
6Eh	R	Fan 4 TACH	4096	2048	1024	512	256	128	64	32	FFh
6Fh	R	Fan 4 TACH Low Byte	16	8	4	2	1	-	-	-	F8h
7Eh	R	Fan 5 TACH	4096	2048	1024	512	256	128	64	32	FFh
7Fh	R	Fan 5 TACH Low Byte	16	8	4	2	1	-	-	-	F8h

The TACH Reading Registers' contents describe the current tachometer reading for each of the fans. By default, the data represents the fan speed as the number of 32kHz clock periods that occur for a single revolution of the fan.

Equation [2] shows the detailed conversion from TACH measurement (COUNT) to RPM while Equation [3] shows the simplified translation of TACH Reading Register count to RPM assuming a 2-pole fan, measuring 5 edges, with a frequency of 32.768kHz. These equations are solved and tabulated for ease of use in AN17.4 RPM to TACH Counts Conversion.

Whenever the high byte register is read, the corresponding low byte data will be loaded to internal shadow registers so that when the low byte is read, the data will always coincide with the previously read high byte.

where:

poles = number of poles of the fan (typically 2)

$$RPM = \frac{1}{(poles)} \times \frac{(n-1)}{COUNT \times \frac{1}{m}} \times f_{TACH} \times 60$$ **[2]**

f_{TACH} = the tachometer measurement frequency (typically 32.768kHz)

n = number of edges measured (typically 5 for a 2 pole fan)

m = the multiplier defined by the RANGE bits

$$RPM = \frac{3{,}932{,}160 \times m}{COUNT}$$ **[3]**

COUNT = TACH Reading Register value (in decimal)

5.19 Software Lock Register

Table 5.29 Software Lock Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
EFh	R/W	Software Lock	-	-	-	-	-	-	-	LOCK	00h

The Software Lock Register controls the software locking of critical registers. This register is software locked.

Bit 0 - LOCK - this bit acts on all registers that are designated SWL. When this bit is set, the locked registers become read only and cannot be updated.

- '0' (default) - all SWL registers can be updated normally.
- '1' - all SWL registers cannot be updated and a hard-reset is required to unlock them.

5.20 Product Features Register

Table 5.30 Product Features Register

ADDRESS	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FCh	R	Product Features	-	-	ADR[2:0]			FAN_SPD [2:0]			00h

The Product Features register shows those functions that are enabled by external pin states.

Bits 5-3 - ADR[2:0] - Indicates the selected SMBus address as determined by the ADDR_SEL pin.

Table 5.31 ADDR_SEL Pin Configuration

ADR[2:0]			SLAVE ADDRESS
2	**1**	**0**	
0	0	0	0101_110(r/w)
0	0	1	0101_111(r/w)
0	1	0	0101_100(r/w)
0	1	1	0101_101(r/w)
1	0	0	1001_100(r/w)
1	0	1	1001_101(r/w)

Bits 2-0 - FAN_SPD[2:0] - Indicates the selected fan speed if the CLK pin pull-up decode is enabled via the ADDR_SEL pin.

Table 5.32 FAN_SPD Pin Configuration

FAN_SPD [2:0]			FAN SPEED
2	**1**	**0**	
0	0	0	0% Drive
0	0	1	30% Drive
0	1	0	50% Drive
0	1	1	75% Drive
1	0	0	100% Drive

5.21 Product ID Register

Table 5.33 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID	0	0	1	1	0	1	0	0	34h

The Product ID Register contains a unique 8-bit word that identifies the product.

5.22 Manufacturer ID Register

Table 5.34 Manufacturer ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	Manufacturer ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID Register contains an 8-bit word that identifies SMSC.

5.23 Revision Register

Table 5.35 Revision Register

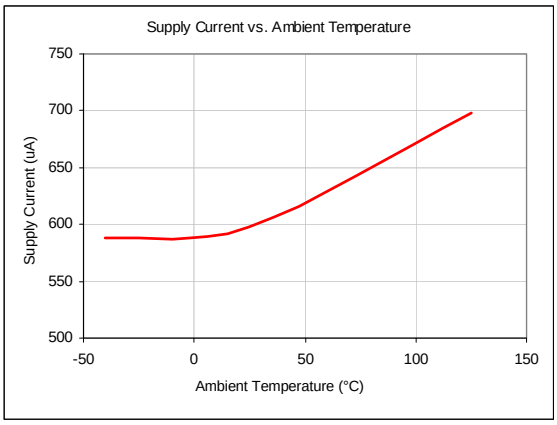
ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	1	0	0	0	0	0	0	0	80h

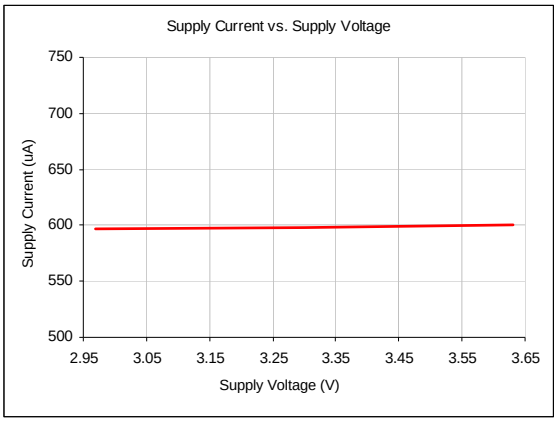
The Revision Register contains an 8-bit word that identifies the die revision.

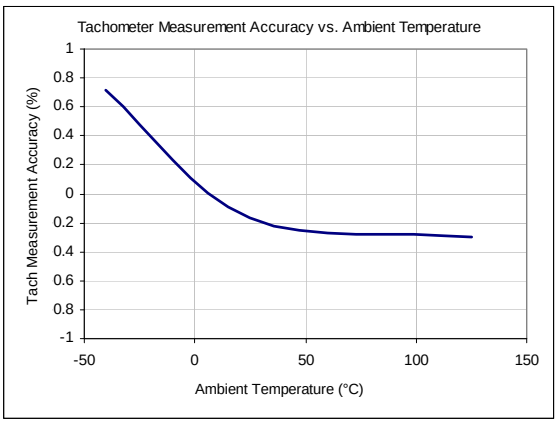
Chapter 6 Typical Operating Curves

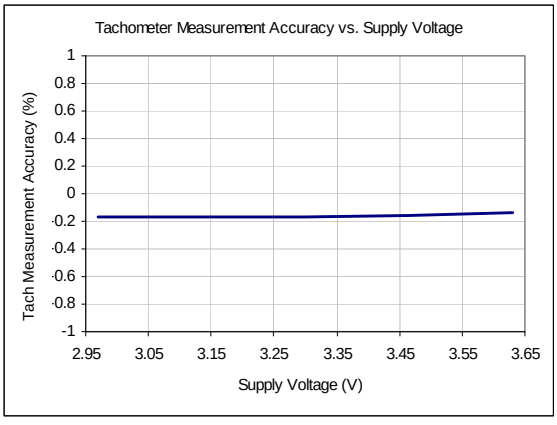
The following Typical Operating Curves are included.

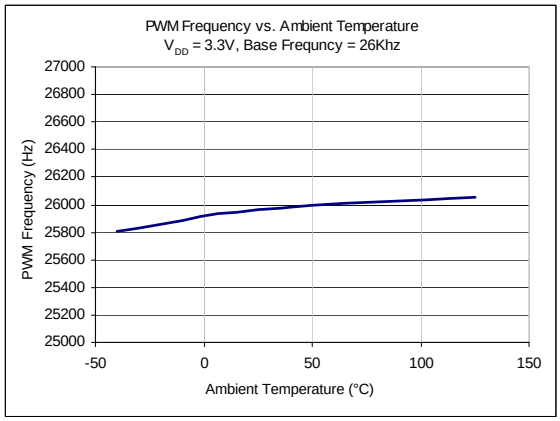
- Supply Current vs. Temperature
- Supply Current vs. Supply Voltage
- Fan TACH Accuracy vs. Temperature
- Fan TACH Accuracy vs. Supply Voltage
- PWM output frequency vs. Supply Voltage
- PWM output frequency vs. Temperature
- FSC Operation

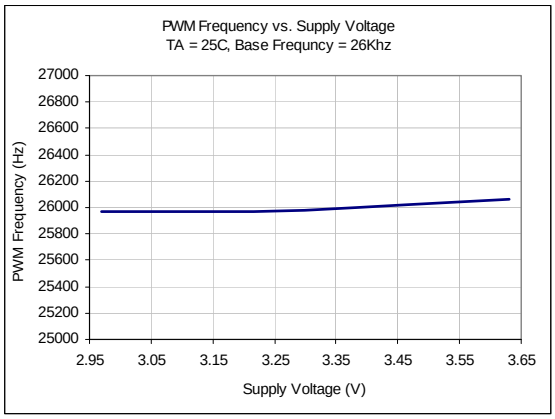


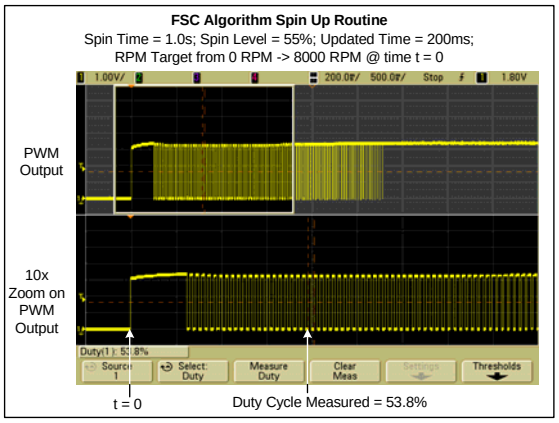


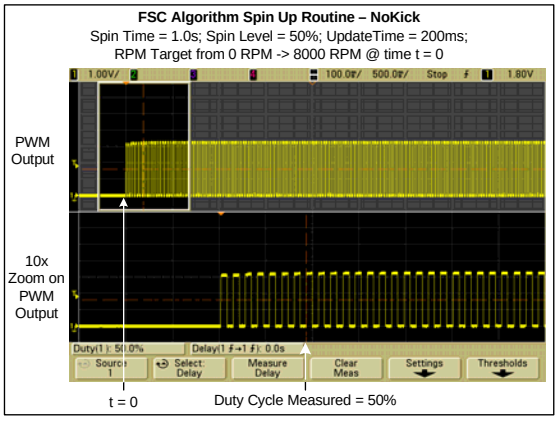


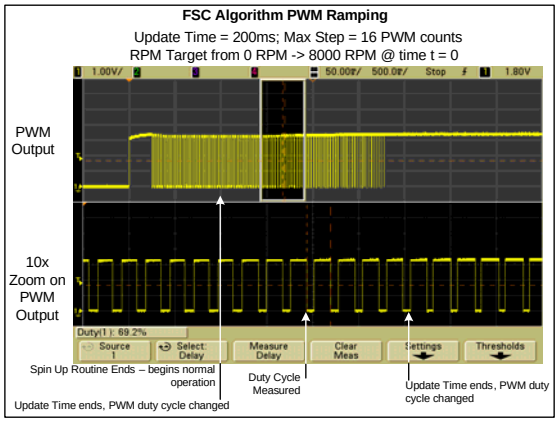



PWM Frequency vs. Ambient Temperature
V_{DD} = 3.3V, Base Frequncy = 26Khz
PWM Frequency (Hz)
27000
26800
26600
26400
26200
26000
25800
25600
25400
25200
25000
-50
0
50
100
150
Ambient Temperature (°C)


PWM Frequency vs. Supply Voltage
TA = 25C, Base Frequncy = 26Khz
PWM Frequency (Hz)
27000
26800
26600
26400
26200
26000
25800
25600
25400
25200
25000
2.95
3.05
3.15
3.25
3.35
3.45
3.55
3.65
Supply Voltage (V)


FSC Algorithm Spin Up Routine
Spin Time = 1.0s; Spin Level = 55%; Updated Time = 200ms;
RPM Target from 0 RPM -> 8000 RPM @ time t = 0
PWM Output
10x Zoom on PWM Output
t = 0
Duty Cycle Measured = 53.8%


FSC Algorithm Spin Up Routine – NoKick
Spin Time = 1.0s; Spin Level = 50%; UpdateTime = 200ms;
RPM Target from 0 RPM -> 8000 RPM @ time t = 0
PWM Output
10x Zoom on PWM Output
t = 0
Duty Cycle Measured = 50%


FSC Algorithm PWM Ramping
Update Time = 200ms; Max Step = 16 PWM counts
RPM Target from 0 RPM -> 8000 RPM @ time t = 0
PWM Output
10x Zoom on PWM Output
Spin Up Routine Ends – begins normal operation
Update Time ends, PWM duty cycle changed
Duty Cycle Measured
Update Time ends, PWM duty cycle changed

Chapter 7 Package Drawing

7.1 EMC2305 Package Information

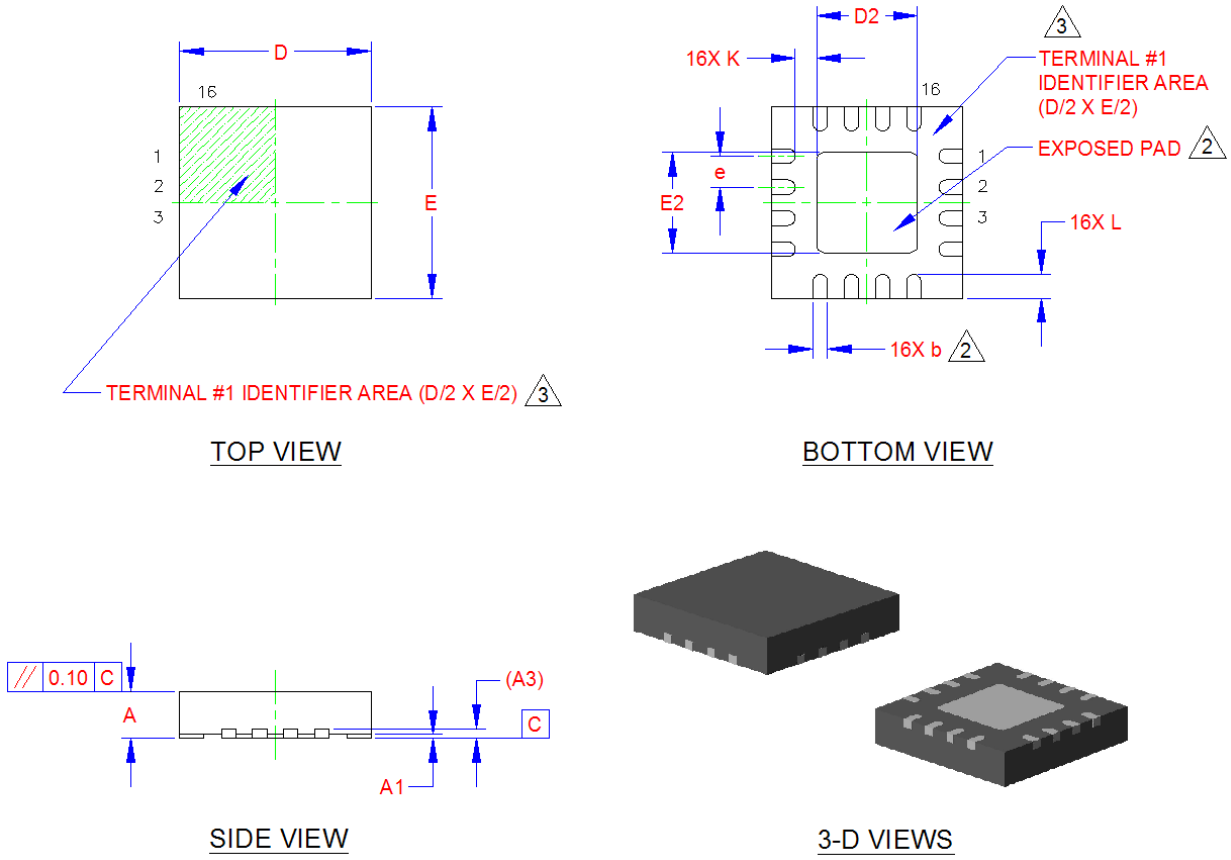
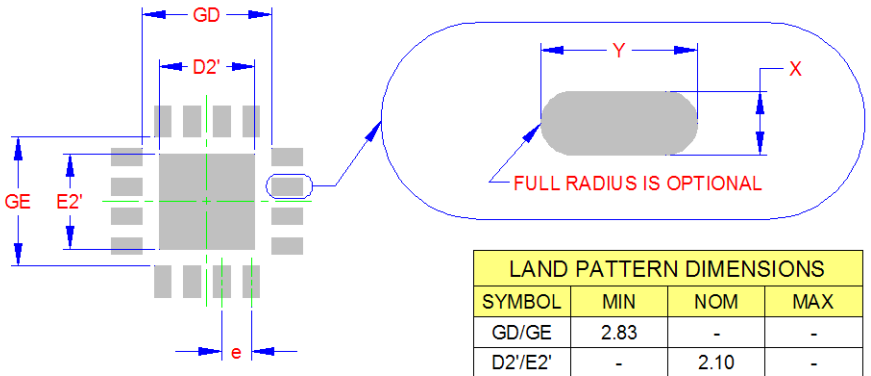


Figure 7.1 Package Drawing - 16-Pin QFN 4mm x 4mm

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.00	2.10	2.20	2	X/Y EXPOSED PAD SIZE
L	0.45	0.50	0.55	-	TERMINAL LENGTH
b	0.25	0.30	0.35	2	TERMINAL WIDTH
K	0.20	-	-	-	TERMINAL TO PAD DISTANCE
e		0.65 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 7.2 Package Dimensions - 16-Pin QFN 4mm x 4mm



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.83	-	-
D2'/E2'	-	2.10	-
X	-	-	0.37
Y	-	-	0.69
e		0.65	

RECOMMENDED PCB LAND PATTERN

Figure 7.3 PCB Footprint - 16-Pin QFN 4mm x 4mm

7.2 Package Markings

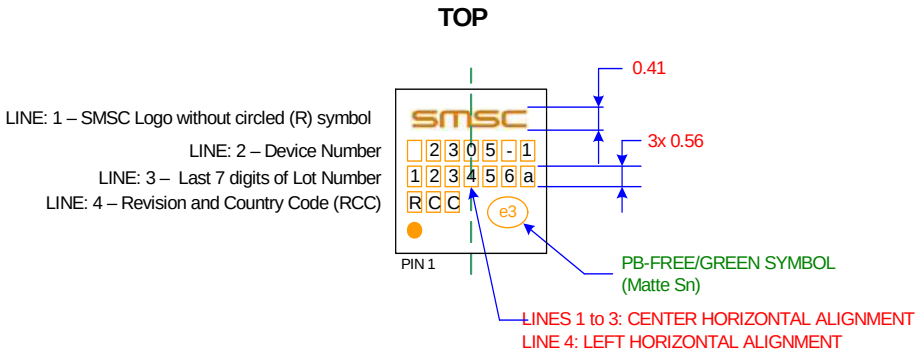


Figure 7.4 EMC2305 Package Markings

Chapter 8 Datasheet Revision History

Table 8.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.3 (05-18-11)	Section 4.8, "Watchdog Timer"	The ALERT# pin is asserted when the watchdog is triggered.
	Section 5.2, "Configuration Register"	Corrected description for MASK bit. Changed “If any bit in either status register is set, the ALERT# pins will be asserted (unless individually masked via the Mask Register)” to “If any bit in the status registers is set, the ALERT# pin will be asserted (unless individually masked via the Fan Interrupt Enable Register)”.
Rev. 1.2 (03-22-10)	Table 2.3, "SMBus Electrical Specifications"	Updated SMBus Data Hold Time spec to 0 us
Rev. 1.1 (10-12-09)	Table 2.2, "Electrical Specifications"	Tachometer Setting Accuracy max was changed from +/-3% to +/-2%.
	Chapter 6, Typical Operating Curves	Added typical operating curves
Rev. 1.0 (05-15-09)	Initial release of datasheet	