-60V P-CHANNEL Enhancement Mode MOSFET

MTP2311N3

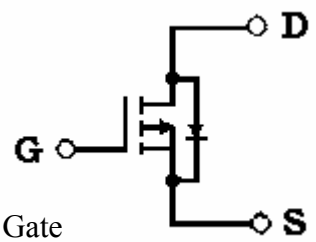
BV_{DSS}	-60V
I_D	-3.5A
R_{DSON}@V_{GS}=-10V, I_D=-2A	72mΩ(typ)
R_{DSON}@V_{GS}=-4.5V,I_D=-1.7A	98mΩ(typ)

Features

- Low gate charge
- Compact and low profile SOT-23 package
- Advanced trench process technology
- High density cell design for ultra low on resistance
- Pb-free lead plating package

Symbol

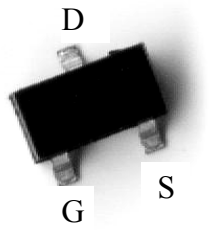
MTP2311N3



G：Gate
S：Source
D：Drain

Outline

SOT-23



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current @ T_A=25°C (Note 3)	I_D	-3.5	A
Continuous Drain Current @ T_A=100°C (Note 3)		-2.2	A
Pulsed Drain Current (Notes 1, 2)	I_{DM}	-14	A
Maximum Power Dissipation (Note 3)	P_D	1.38	W
Linear Derating Factor		0.01	W/°C
Operating Junction and Storage Temperature Range	Tj ; Tstg	-55~+150	°C

Note : 1. Pulse width limited by maximum junction temperature.
2. Pulse width≤ 300μs, duty cycle≤2%.
3. Surface mounted on 1 in² copper pad of FR-4 board; 270°C/W when mounted on minimum copper pad

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient(PCB mounted)	Rth,ja	90	°C/W

Note : Surface mounted on 1 in² copper pad of FR-4 board; 270°C/W when mounted on minimum copper pad

Electrical Characteristics (Tj=25°C, unless otherwise noted)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	-60	-	-	V	V_{GS}=0, I_D=-250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.04	-	V/°C	Reference to 25°C, I_D=-1mA
$V_{GS(th)}$	-1.0	-1.8	-3.0	V	V_{DS}=V_{GS}, I_D=-250μA
I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0
I_{DSS}	-	-	-1	μA	V_{DS}=-48V, V_{GS}=0
	-	-	-25		V_{DS}=-48V, V_{GS}=0 (Tj=70°C)
*$R_{DS(ON)}$	-	72	90	mΩ	I_D=-2A, V_{GS}=-10V
	-	98	120		I_D=-1.7A, V_{GS}=-4.5V
*G_{FS}	-	5.8	-	S	V_{DS}=-5V, I_D=-3A
Dynamic					
Ciss	-	962	-	pF	V_{DS}=-20V, V_{GS}=0, f=1MHz
Coss	-	56	-		
Crss	-	40	-		
$t_{d(ON)}$	-	5.9	-	ns	V_{DS}=-20V, I_D=-1A, V_{GS}=-10V R_G=6Ω
t_r	-	5.7	-		
$t_{d(OFF)}$	-	19.2	-		
t_f	-	6	-		
Qg	-	11	-	nC	V_{DS}=-30V, I_D=-3.5A, V_{GS}=-10V
Qgs	-	3.4	-		
Qgd	-	3.4	-		
Source-Drain Diode					
*I_S	-	-	-3.5	A	
*I_{SM}	-	-	-14		
*V_{SD}	-	-	-1.3	V	V_{GS}=0V, I_F=I_S
Trr	-	12	-	ns	V_{GS}=0V, I_F=-3.5A, dI/dt=100A/μs
Qrr	-	7	-	nC	

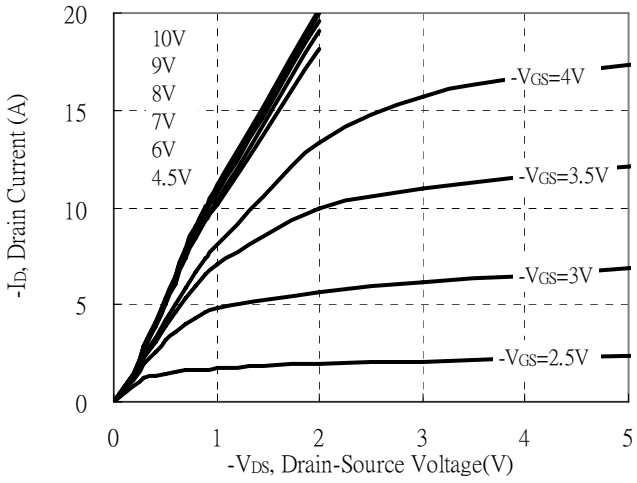
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

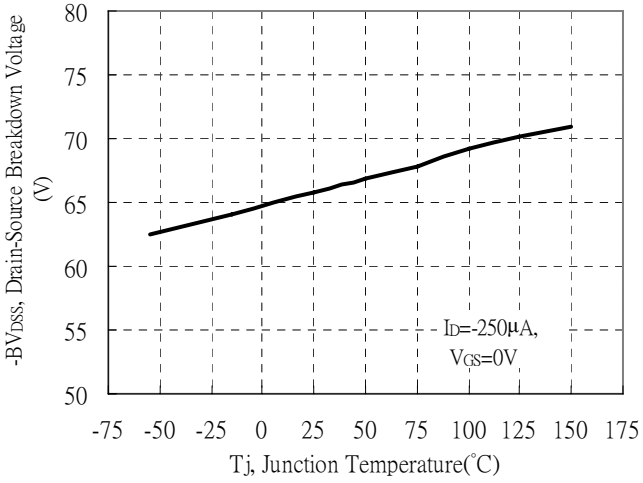
Device	Package	Shipping	Marking
MTP2311N3	SOT-23 (Pb-free lead plating package)	3000 pcs / Tape & Reel	2311

Typical Characteristics

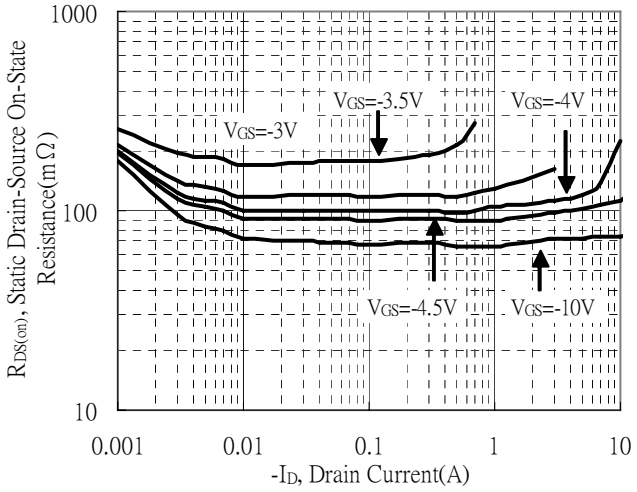
Typical Output Characteristics



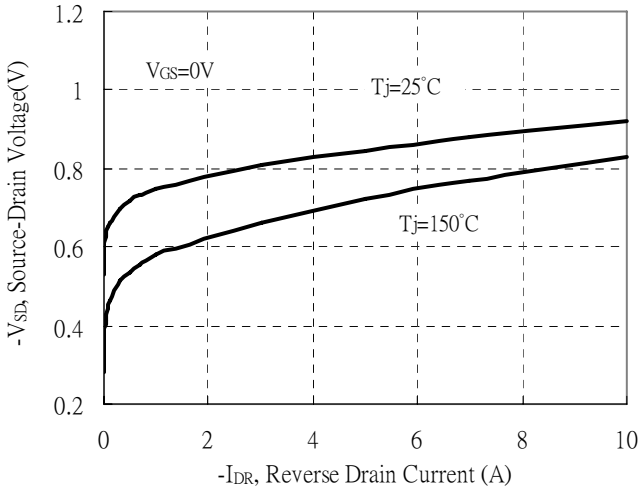
Brekdown Voltage vs Ambient Temperature



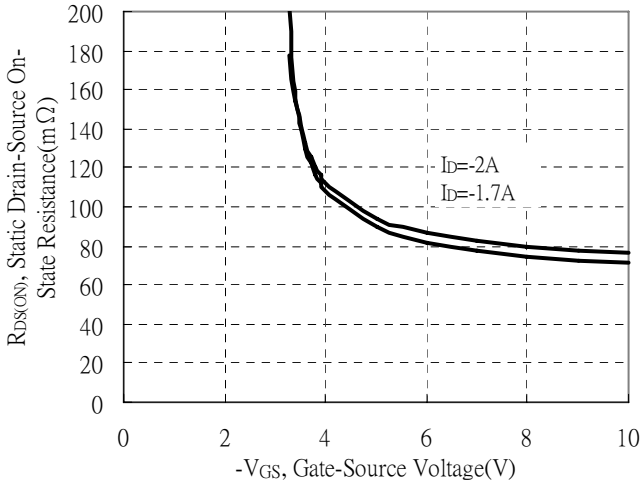
Static Drain-Source On-State resistance vs Drain Current



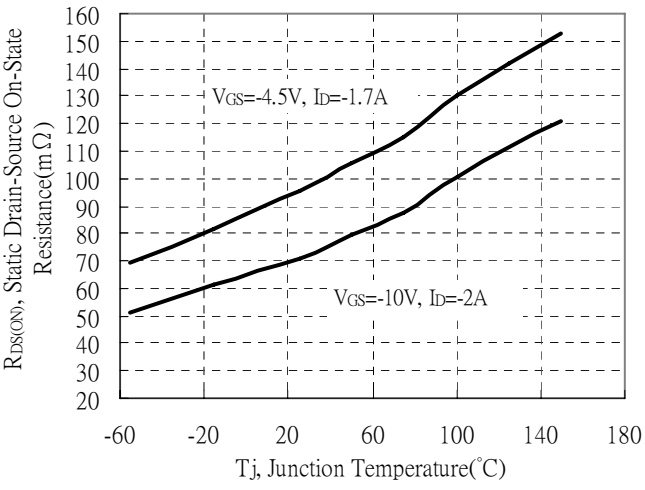
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

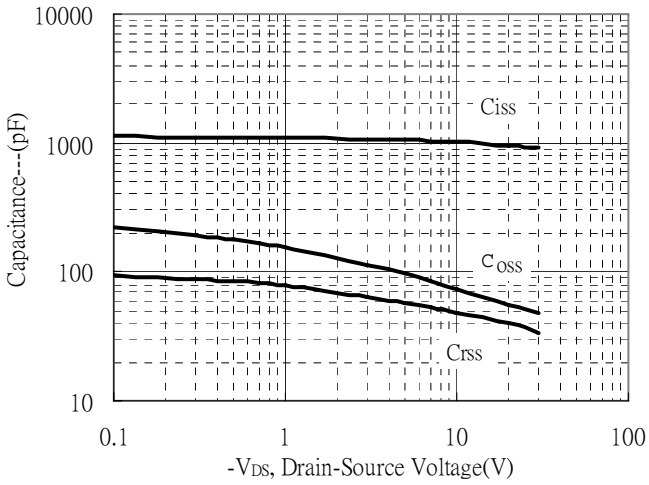


Drain-Source On-State Resistance vs Junction Tempearture

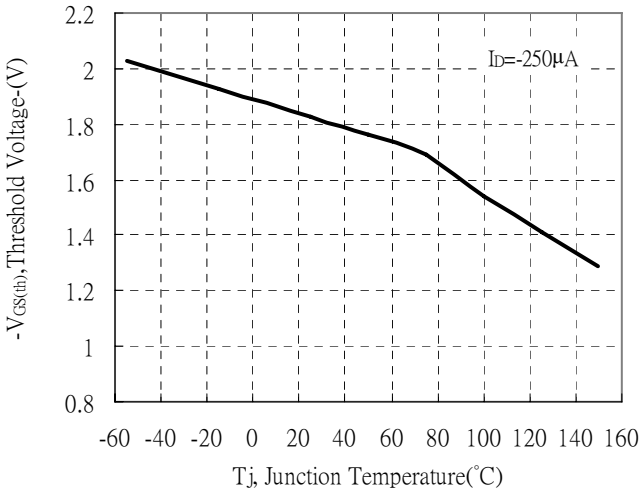


Typical Characteristics(Cont.)

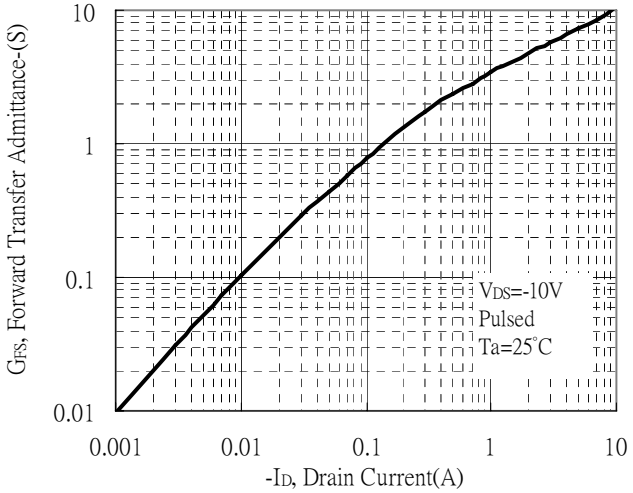
Capacitance vs Drain-to-Source Voltage



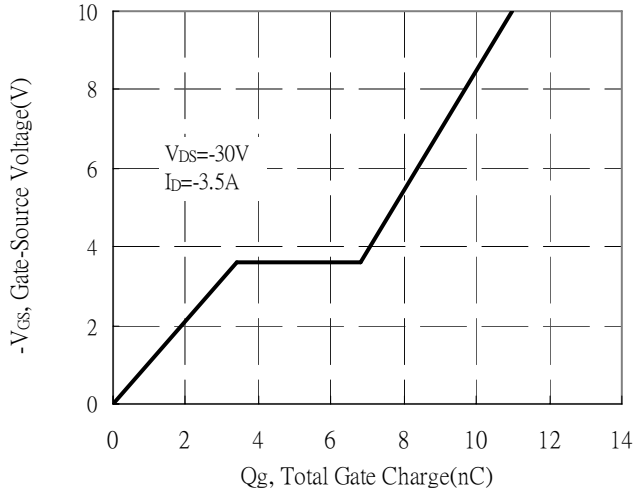
Threshold Voltage vs Junction Tempearture



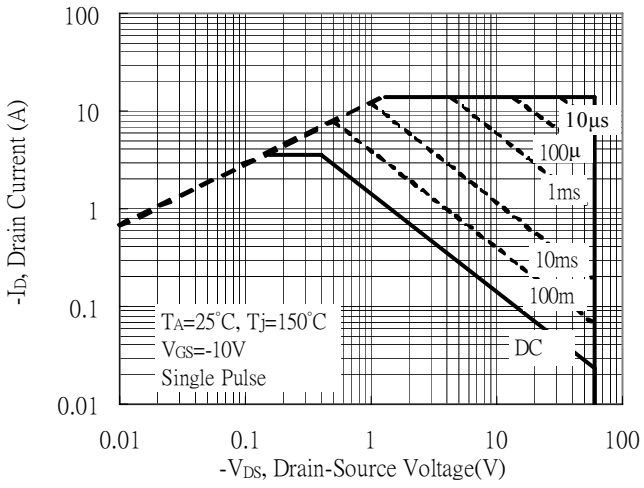
Forward Transfer Admittance vs Drain Current



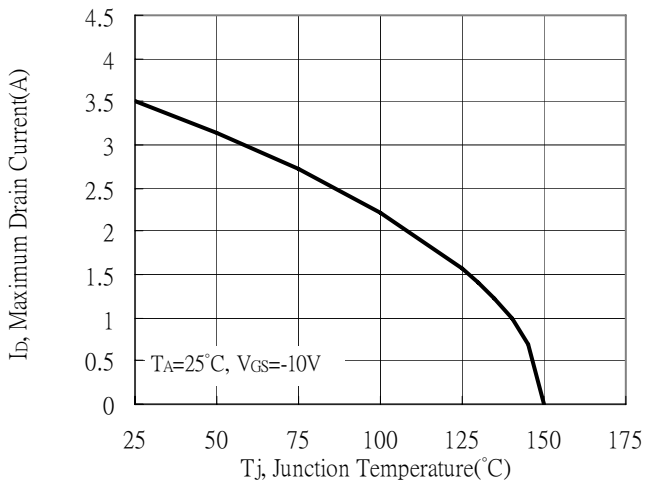
Gate Charge Characteristics



Maximum Safe Operating Area

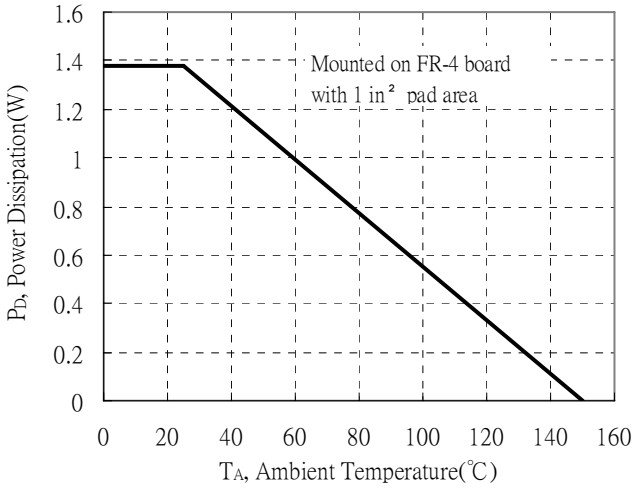


Maximum Drain Current vs JunctionTemperature

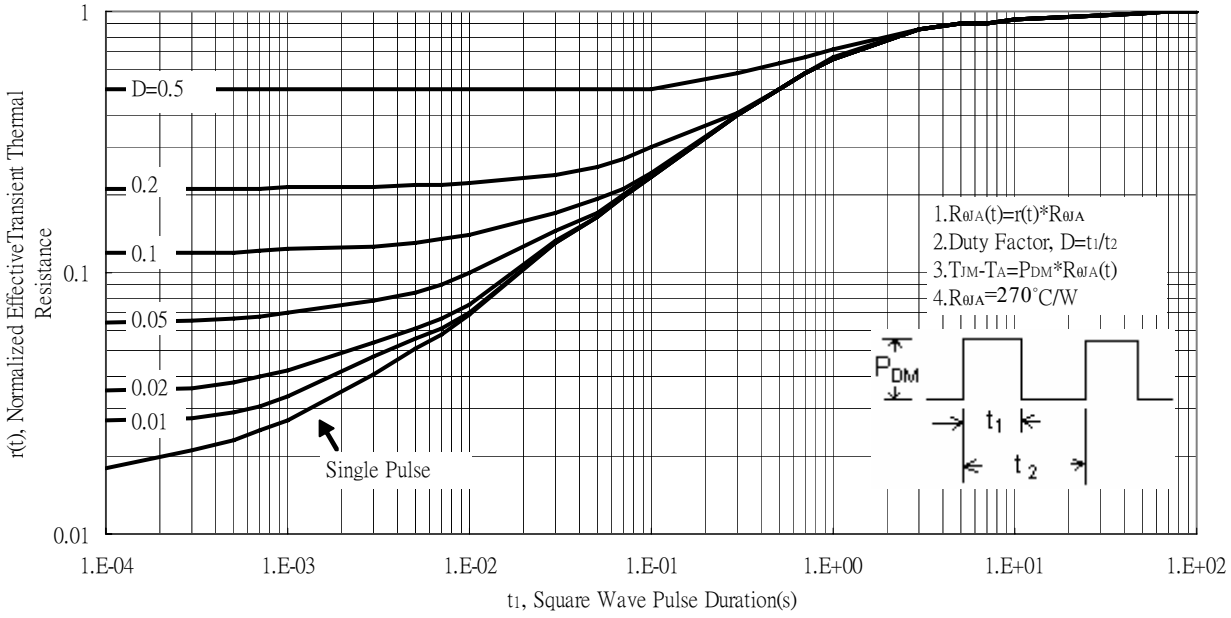


Typical Characteristics(Cont.)

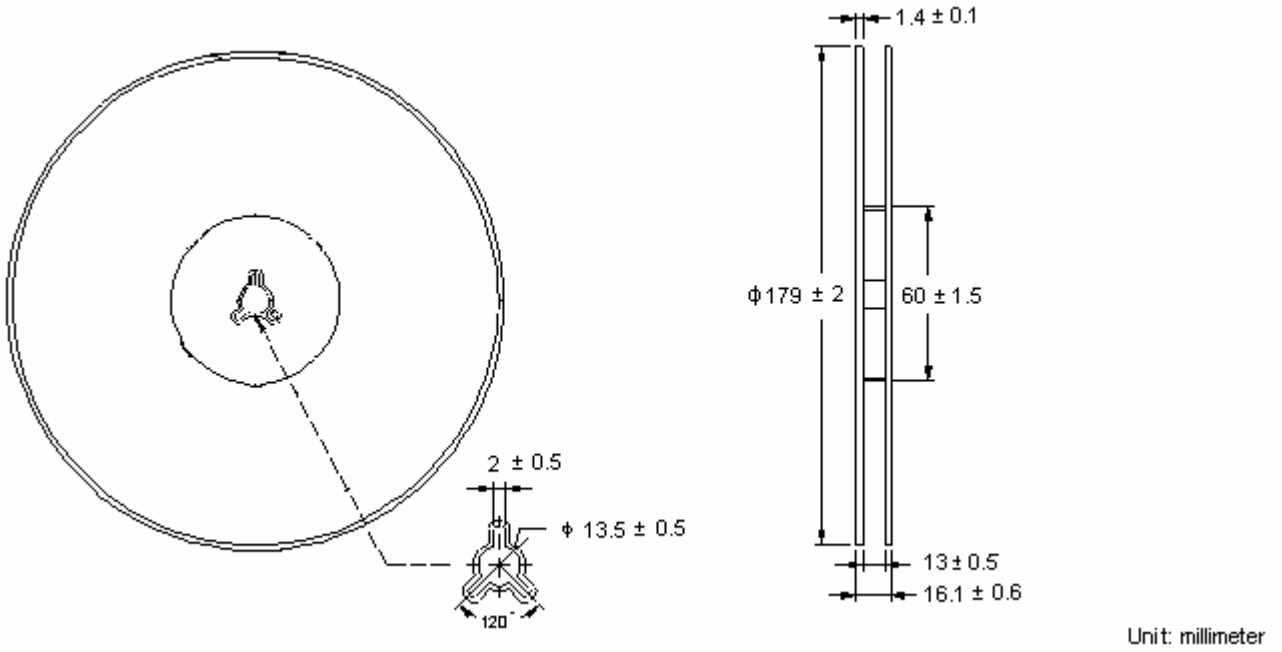
Power Derating Curve



Transient Thermal Response Curves

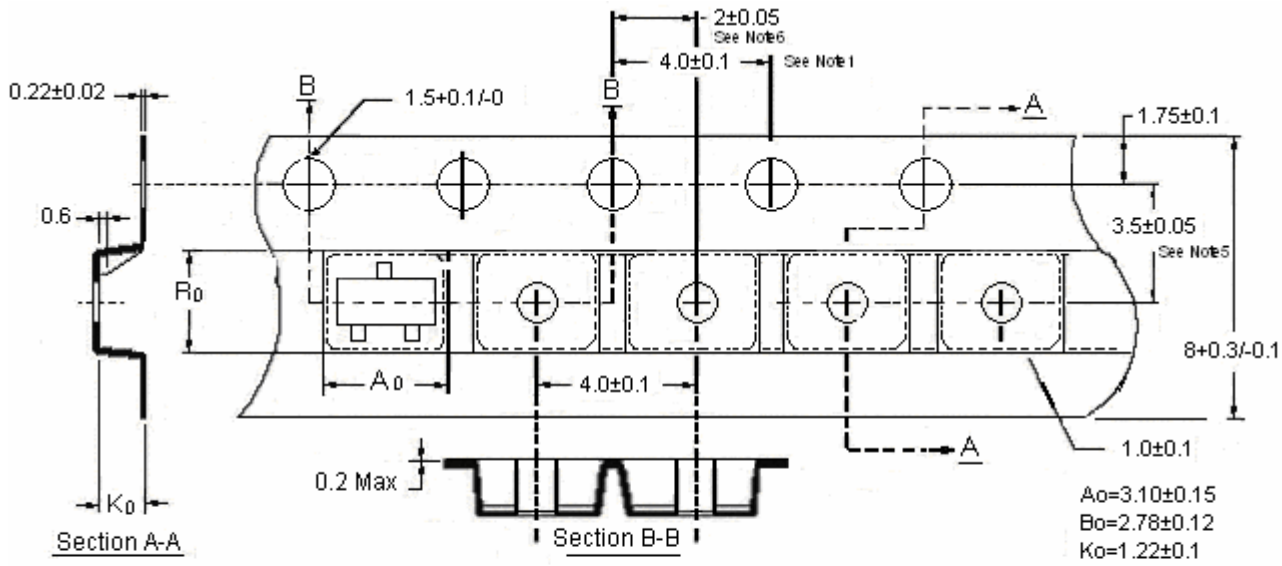


Reel Dimension



Unit: millimeter

Carrier Tape Dimension



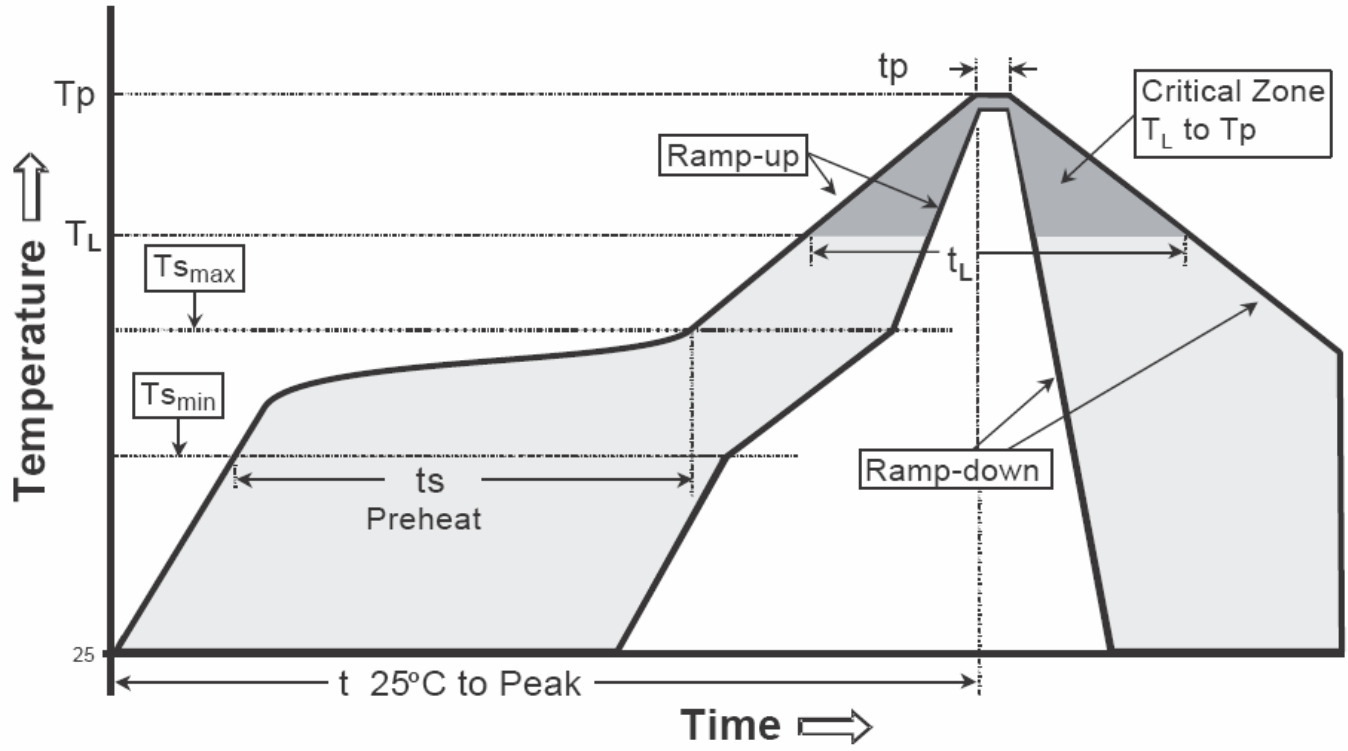
Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material : conductive Black Polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

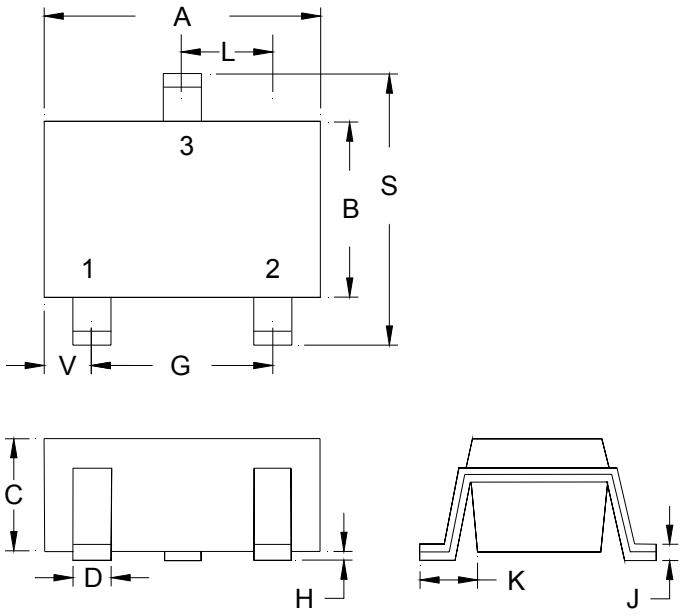
Recommended temperature profile for IR reflow



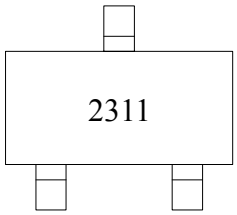
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-23 Dimension



Marking:



3-Lead SOT-23 Plastic
Surface Mounted Package
CYStek Package Code: N3

Style: Pin 1.Gate 2.Source 3.Drain

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0034	0.0070	0.085	0.177
B	0.0472	0.0630	1.20	1.60	K	0.0128	0.0266	0.32	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0005	0.0040	0.013	0.10					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.