FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27709-4E

ASSP For Power Supply Applications (Secondary battery)

DC/DC Converter IC for Charging Li-ion battery

MB3887

■ DESCRIPTION

The MB3887 is a DC/DC converter IC suitable for down-conversion, using pulse-width (PWM) charging and enabling output voltage to be set to any desired level from one cell to four cells.
These ICs can dynamically control the secondary battery's charge current by detecting a voltage drop in an AC adapter in order to keep its power constant (dynamically-controlled charging) .
The charging method enables quick charging, for example, with the AC adapter during operation of a notebook PC.

The MB3887 provides a broad power supply voltage range and low standby current as well as high efficiency, making it ideal for use as a built-in charging device in products such as notebook PC.
This product is covered by US Patent Number 6,147,477.

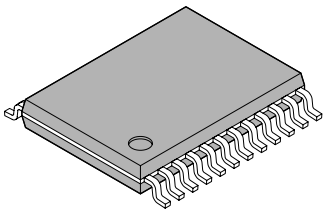
■ FEATURES

- Detecting a voltage drop in the AC adapter and dynamically controlling the charge current (Dynamically-controlled charging)

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■ PACKAGE

24-pin plastic SSOP



(FPT-24P-M03)

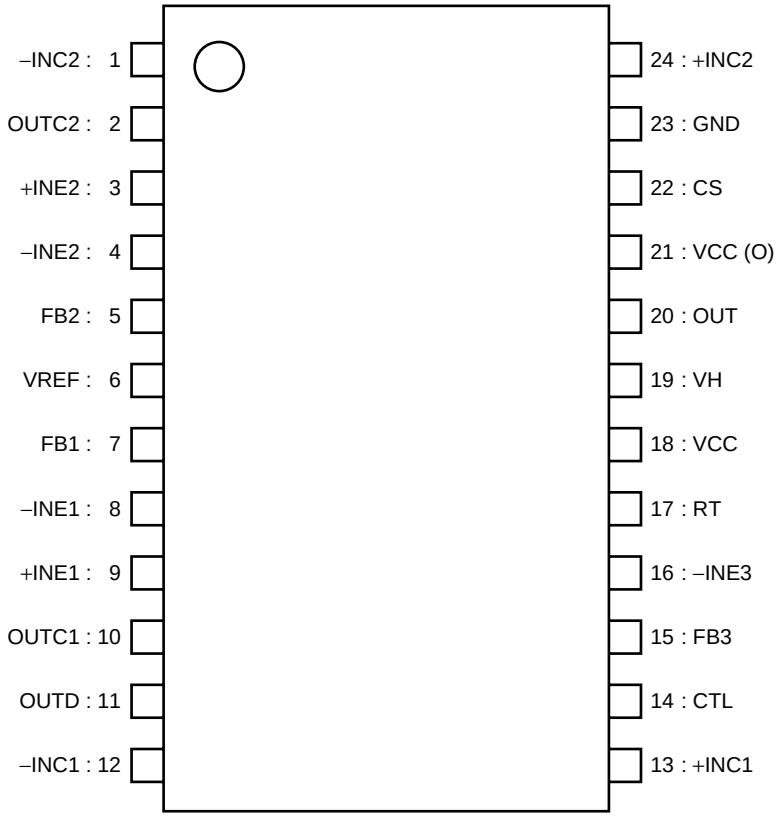
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- Output voltage setting using external resistor : 1 cell to 4 cells
- High efficiency : 96% (VIN = 19 V, Vo = 16.8 V)
- Wide range of operating supply voltages : 8 V to 25 V
- Output voltage setting accuracy : 4.2 V ± 0.74% (Ta = –10 °C to +85 °C, per cell)
- Charging current accuracy : ±5%
- Built-in frequency setting capacitor enables frequency setting using external resistor only
- Oscillation frequency range : 100 kHz to 500 kHz
- Built-in current detection amplifier with wide in-phase input voltage range : 0 V to VCC
- In standby mode, leave output voltage setting resistor open to prevent inefficient current loss
- Built-in standby current function : 0 μA (standard)
- Built-in soft-start function independent of loads
- Built-in totem-pole output stage supporting P-channel MOS FET devices

■ PIN ASSIGNMENT

(TOP VIEW)

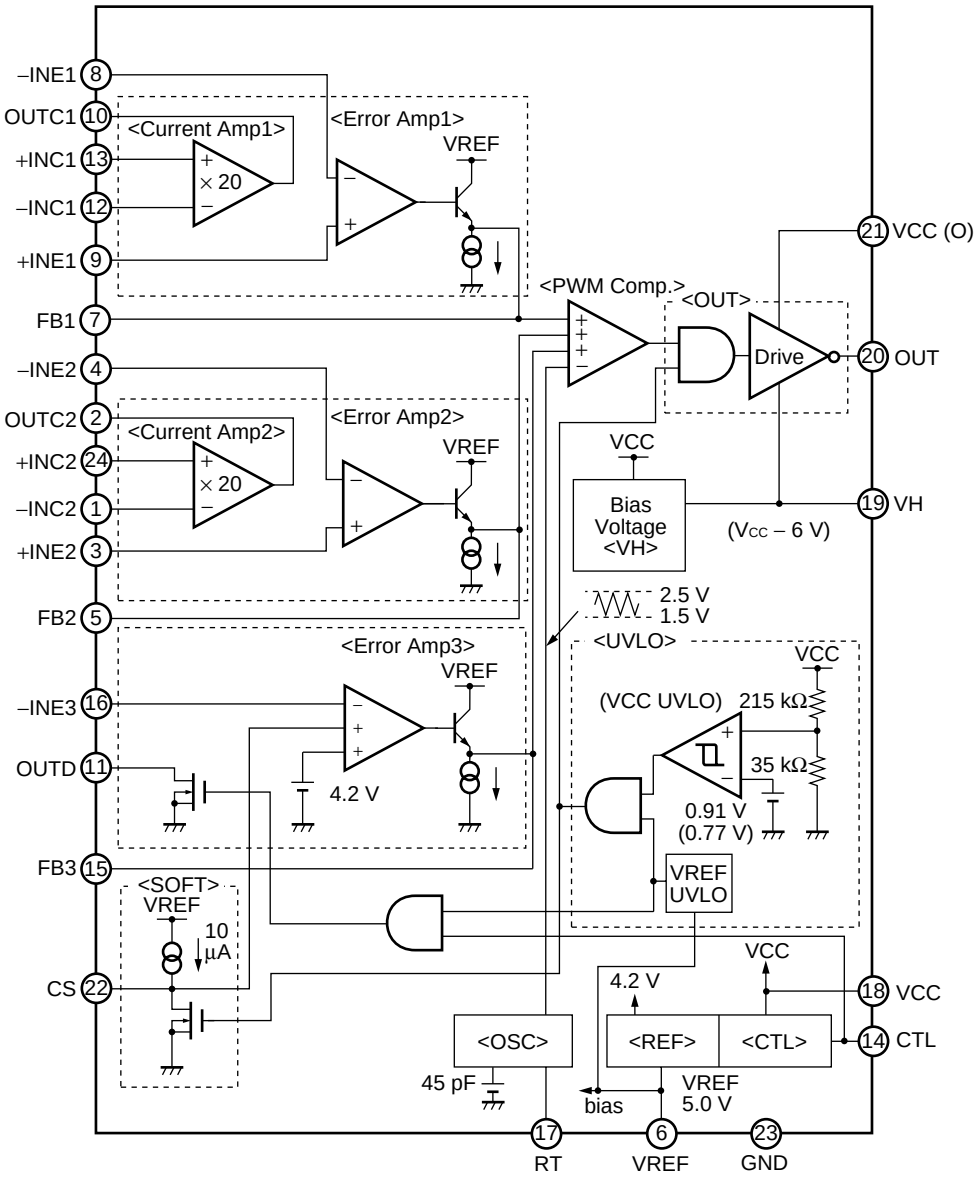


(FPT-24P-M03)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Descriptions
1	–INC2	I	Current detection amplifier (Current Amp2) input terminal.
2	OUTC2	O	Current detection amplifier (Current Amp2) output terminal.
3	+INE2	I	Error amplifier (Error Amp2) non-inverted input terminal.
4	–INE2	I	Error amplifier (Error Amp2) inverted input terminal.
5	FB2	O	Error amplifier (Error Amp2) output terminal.
6	VREF	O	Reference voltage output terminal.
7	FB1	O	Error amplifier (Error Amp1) output terminal.
8	–INE1	I	Error amplifier (Error Amp1) inverted input terminal
9	+INE1	I	Error amplifier (Error Amp1) non-inverted input terminal.
10	OUTC1	O	Current detection amplifier (Current Amp1) output terminal.
11	OUTD	O	With IC in standby mode, this terminal is set to “Hi-Z” to prevent loss of current through output voltage setting resistance. Set CTL terminal to “H” level to output “L” level.
12	–INC1	I	Current detection amplifier (Current Amp1) input terminal.
13	+INC1	I	Current detection amplifier (Current Amp1) input terminal.
14	CTL	I	Power supply control terminal. Setting the CTL terminal at “L” level places the IC in the standby mode.
15	FB3	O	Error amplifier (Error Amp3) output terminal.
16	–INE3	I	Error amplifier (Error Amp3) inverted input terminal.
17	RT	—	Triangular-wave oscillation frequency setting resistor connection terminal.
18	VCC	—	Power supply terminal for reference power supply and control circuit.
19	VH	O	Power supply terminal for FET drive circuit (VH = VCC – 6 V) .
20	OUT	O	External FET gate drive terminal.
21	VCC (O)	—	Output circuit power supply terminal.
22	CS	—	Soft-start capacitor connection terminal.
23	GND	—	Ground terminal.
24	+INC2	I	Current detection amplifier (Current Amp2) input terminal.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC, VCC (O) terminal*2	—	28	V
Output current	I_{OUT}	—	—	60	mA
Peak output current	I_{OUT}	Duty ≤ 5 % (t = 1 / f_{OSC} × Duty)	—	700	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	740*1	mW
Storage temperature	T_{STG}	—	–55	+125	°C

*1 : The package is mounted on the dual-sided epoxy board (10 cm × 10 cm) .

*2 : Refer to “ THE SEQUENCE OF THE START-UP AND OFF OF THE POWER SUPPLY” for details.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	VCC, VCC (O) terminal*	8	—	25	V
Reference voltage output current	I_{REF}	—	–1	—	0	mA
VH terminal output current	I_{VH}	—	0	—	30	mA
Input voltage	V_{INE}	–INE1 to –INE3, +INE1, +INE2 terminal	0	—	V_{CC} – 1.8	V
	V_{INC}	+INC1, +INC2, –INC1, –INC2 terminal	0	—	V_{CC}	V
OUTD terminal output voltage	V_{OUTD}	—	0	—	17	V
OUTD terminal output current	I_{OUTD}	—	0	—	2	mA
CTL terminal input voltage	V_{CTL}	—	0	—	25	V
Output current	I_{OUT}	—	–45	—	+45	mA
Peak output current	I_{OUT}	Duty ≤ 5 % (t = 1 / fosc × Duty)	–600	—	+600	mA
Oscillation frequency	f_{OSC}	—	100	290	500	kHz
Timing resistor	R_T	—	27	47	130	kΩ
Soft-start capacitor	C_S	—	—	0.022	1.0	µF
VH terminal capacitor	C_{VH}	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

* : Refer to “ THE SEQUENCE OF THE START-UP AND OFF OF THE POWER SUPPLY” for details.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, VCC = 19 V, VCC (O) = 19 V, VREF = 0 mA)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
1. Reference voltage block [REF]	Output voltage	V_{REF1}	6	Ta = +25 °C	4.967	5.000	5.041	V
		V_{REF2}	6	Ta = −10 °C to +85 °C	4.95	5.00	5.05	V
	Input stability	Line	6	VCC = 8 V to 25 V	—	3	10	mV
	Load stability	Load	6	VREF = 0 mA to −1 mA	—	1	10	mV
	Short-circuit output current	Ios	6	VREF = 1 V	−50	−25	−12	mA
2. Under voltage lockout protection circuit block [UVLO]	Threshold voltage	V_{TLH}	18	VCC = VCC (O), VCC = ↗	6.2	6.4	6.6	V
		V_{THL}	18	VCC = VCC (O), VCC = ↘	5.2	5.4	5.6	V
	Hysteresis width	V_H	18	VCC = VCC (O)	—	1.0*	—	V
	Threshold voltage	V_{TLH}	6	VREF = ↗	2.6	2.8	3.0	V
		V_{THL}	6	VREF = ↘	2.4	2.6	2.8	V
	Hysteresis width	V_H	6	—	—	0.2	—	V
3. Soft-start block [SOFT]	Charge current	I_{CS}	22	—	−14	−10	−6	µA
4. Triangular waveform oscillator circuit block [OSC]	Oscillation frequency	f_{OSC}	20	RT = 47 kΩ	260	290	320	kHz
	Frequency temperature stability	Δf/fdt	20	Ta = −30 °C to +85 °C	—	1*	—	%
5-1. Error amplifier block [Error Amp1, Error Amp2]	Input offset voltage	V_{IO}	3, 4, 8, 9	FB1 = FB2 = 2 V	—	1	5	mV
	Input bias current	I_B	3, 4, 8, 9	—	−100	−30	—	nA
	In-phase input voltage range	V_{CM}	3, 4, 8, 9	—	0	—	V_{CC} − 1.8	V
	Voltage gain	A_V	5, 7	DC	—	100*	—	dB
	Frequency bandwidth	BW	5, 7	AV = 0 dB	—	2*	—	MHz
	Output voltage	V_{FBH}	5, 7	—	4.7	4.9	—	V
		V_{FBL}	5, 7	—	—	20	200	mV
	Output source current	I_{SOURCE}	5, 7	FB1 = FB2 = 2 V	—	−2	−1	mA
	Output sink current	I_{SINK}	5, 7	FB1 = FB2 = 2 V	150	300	—	µA

* : Standard design value.

(Continued)

(Ta = +25 °C, VCC = 19 V, VCC (O) = 19 V, VREF = 0 mA)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
5-2. Error amplifier block [Error Amp3]	Threshold voltage	V_{TH1}	16	FB3 = 2 V, Ta = +25 °C	4.183	4.200	4.225	V
		V_{TH2}	16	FB3 = 2 V, Ta = –10 °C to +85 °C	4.169	4.200	4.231	V
	Input current	I_{INE3}	16	–INE3 = 0 V	–100	–30	—	nA
	Voltage gain	A_V	15	DC	—	100*	—	dB
	Frequency bandwidth	BW	15	AV = 0 dB	—	2*	—	MHz
	Output voltage	V_{FBH}	15	—	4.7	4.9	—	V
		V_{FBL}	15	—	—	20	200	mV
	Output source current	I_{SOURCE}	15	FB3 = 2 V	—	–2	–1	mA
	Output sink current	I_{SINK}	15	FB3 = 2 V	150	300	—	µA
	OUTD terminal output leak current	I_{LEAK}	11	OUTD = 17 V	—	0	1	µA
	OUTD terminal output ON resistor	R_{ON}	11	OUTD = 1 mA	—	35	50	Ω
6. Current detection amplifier block [Current Amp1, Current Amp2]	Input offset voltage	V_{IO}	1, 12, 13, 24	+INC1 = +INC2 = –INC1 = –INC2 = 3 V to VCC	–3	—	+3	mV
	Input current	I_{+INCH}	13, 24	+INC1 = +INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	—	20	30	µA
		$I_{–INCH}$	1, 12	+INC1 = +INC2 = 3 V to VCC, ΔVin = –100 mV	—	0.1	0.2	µA
		I_{+INCL}	13, 24	+INC1 = +INC2 = 0 V, ΔVin = –100 mV	–180	–120	—	µA
		$I_{–INCL}$	1, 12	+INC1 = +INC2 = 0 V, ΔVin = –100 mV	–195	–130	—	µA

* : Standard design value

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(Ta = +25 °C, VCC = 19 V, VCC (O) = 19 V, VREF = 0 mA)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
6. Current detection amplifier block [Current Amp1, Current Amp2]	Current detection voltage	V_{OUTC1}	2, 10	+INC1 = +INC2 = 3 V to VCC, ΔVin = –100 mV	1.9	2.0	2.1	V
		V_{OUTC2}	2, 10	+INC1 = +INC2 = 3 V to VCC, ΔVin = –20 mV	0.34	0.40	0.46	V
		V_{OUTC3}	2, 10	+INC1 = +INC2 = 0 V to 3 V, ΔVin = –100 mV	1.8	2.0	2.2	V
		V_{OUTC4}	2, 10	+INC1 = +INC2 = 0 V to 3 V, ΔVin = –20 mV	0.2	0.4	0.6	V
	In-phase input voltage range	V_{CM}	1, 12, 13, 24	—	0	—	V_{CC}	V
	Voltage gain	A_V	2, 10	+INC1 = +INC2 = 3 V to VCC, ΔVin = –100 mV	19	20	21	V/V
	Frequency bandwidth	BW	2, 10	AV = 0 dB	—	2*	—	MHz
	Output voltage	V_{OUTCH}	2, 10	—	4.7	4.9	—	V
		V_{OUTCL}	2, 10	—	—	20	200	mV
	Output source current	I_{SOURCE}	2, 10	OUTC1 = OUTC2 = 2 V	—	–2	–1	mA
	Output sink current	I_{SINK}	2, 10	OUTC1 = OUTC2 = 2 V	150	300	—	µA
7. PWM comparator block [PWM Comp.]	Threshold voltage	V_{TL}	5, 7, 15	Duty cycle = 0 %	1.4	1.5	—	V
		V_{TH}	5, 7, 15	Duty cycle = 100 %	—	2.5	2.6	V

* : Standard design value

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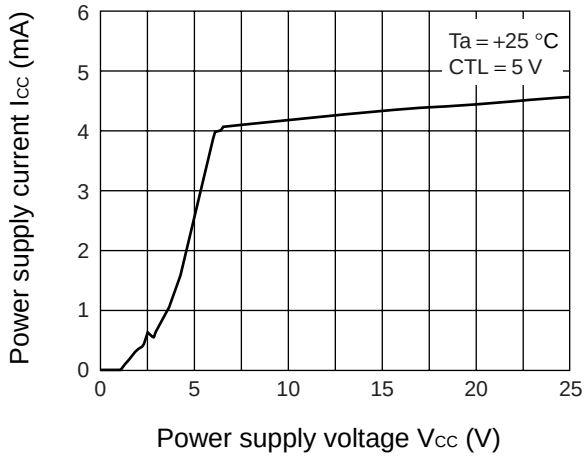
(Ta = +25 °C, VCC = 19 V, VCC (O) = 19 V, VREF = 0 mA)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
8. Output block [OUT]	Output source current	I_{SOURCE}	20	OUT = 13 V, Duty ≤ 5 % (t = 1 / fosc × Duty)	—	–400*	—	mA
	Output sink current	I_{SINK}	20	OUT = 19 V, Duty ≤ 5 % (t = 1 / fosc × Duty)	—	400*	—	mA
	Output ON resistor	R_{OH}	20	OUT = –45 mA	—	6.5	9.8	Ω
		R_{OL}	20	OUT = 45 mA	—	5.0	7.5	Ω
	Rise time	tr1	20	OUT = 3300 pF (Si4435 × 1)	—	50*	—	ns
	Fall time	tf1	20	OUT = 3300 pF (Si4435 × 1)	—	50*	—	ns
9. Control block [CTL]	CTL input voltage	V_{ON}	14	IC Active mode	2	—	25	V
		V_{OFF}	14	IC Standby mode	0	—	0.8	V
	Input current	I_{CTLH}	14	CTL = 5 V	—	100	150	µA
		I_{CTLL}	14	CTL = 0 V	—	0	1	µA
10. Bias voltage block [VH]	Output voltage	V_H	19	VCC = VCC (O) = 8 V to 25 V, VH = 0 to 30 mA	V_{CC} – 6.5	V_{CC} – 6.0	V_{CC} – 5.5	V
11. General	Standby current	I_{CCS}	18	VCC = VCC (O), CTL = 0 V	—	0	10	µA
	Power supply current	I_{CC}	18	VCC = VCC (O), CTL = 5 V	—	8	12	mA

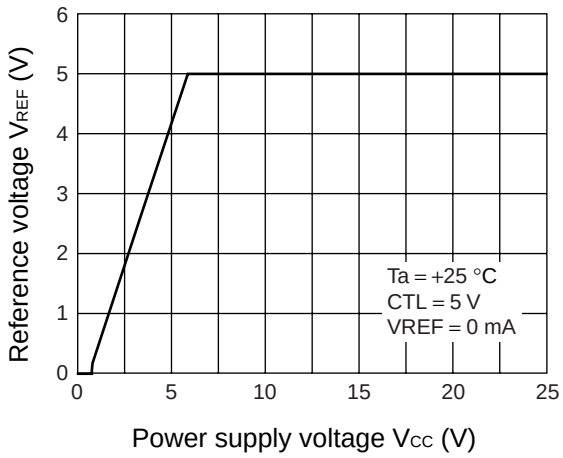
* : Standard design value

■ TYPICAL CHARACTERISTICS

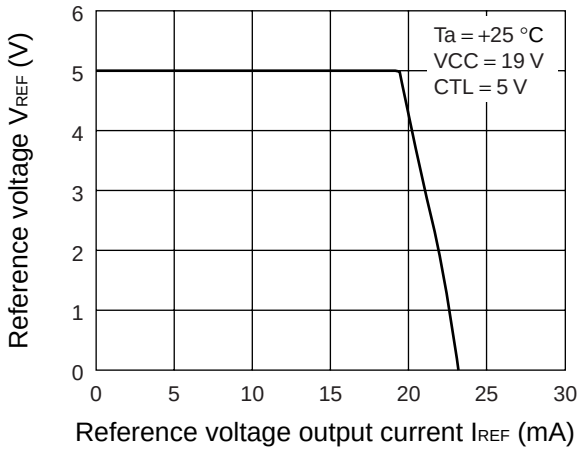
Power supply current vs. Power supply voltage



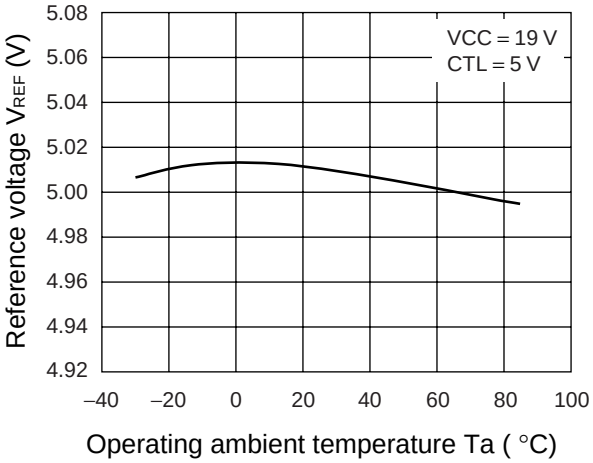
Reference voltage vs. Power supply voltage



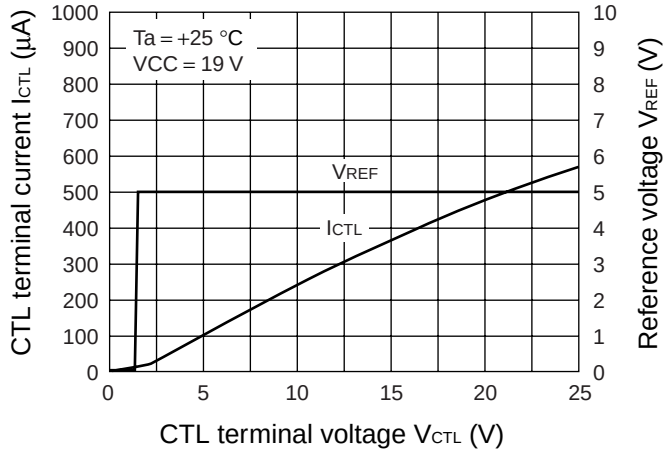
Reference voltage
vs. Reference voltage output current



Reference voltage
vs. Operating ambient temperature

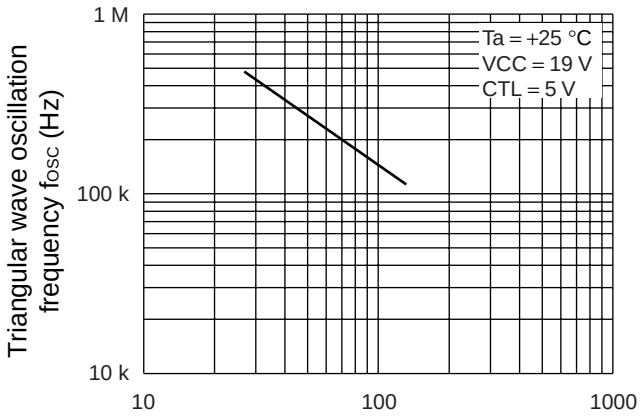


CTL terminal current, Reference voltage
vs. CTL terminal voltage

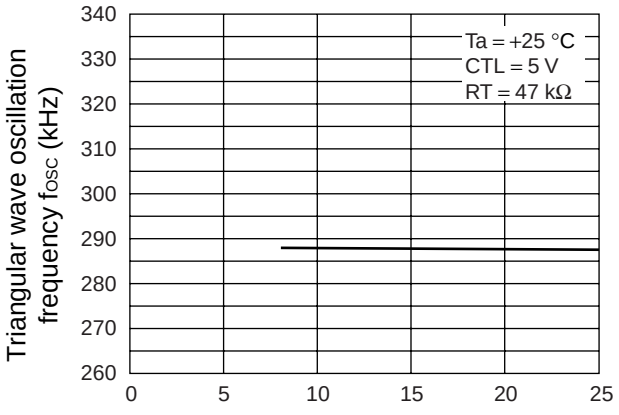


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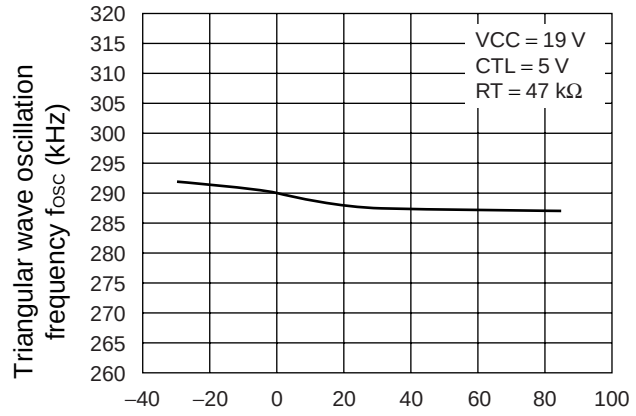
Triangular wave oscillation frequency vs. Timing resistor



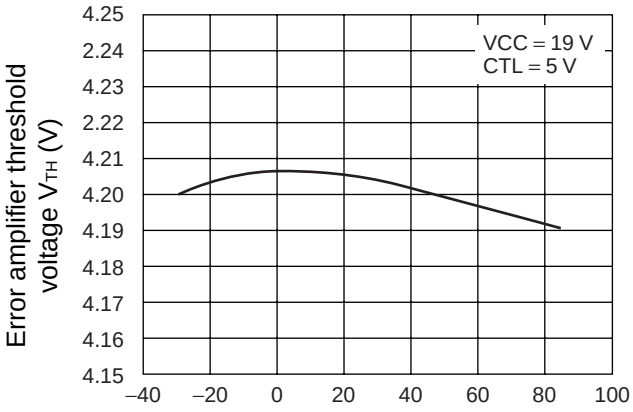
Triangular wave oscillation frequency vs. Power supply voltage



Triangular wave oscillation frequency vs. Operating ambient temperature

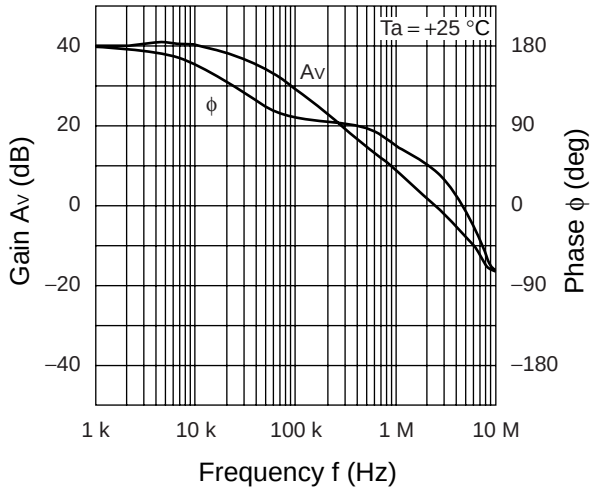


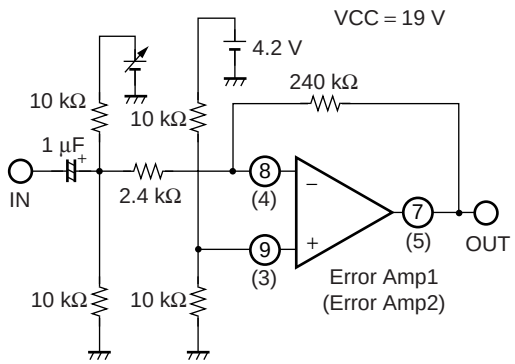
Error amplifier threshold voltage vs. Operating ambient temperature



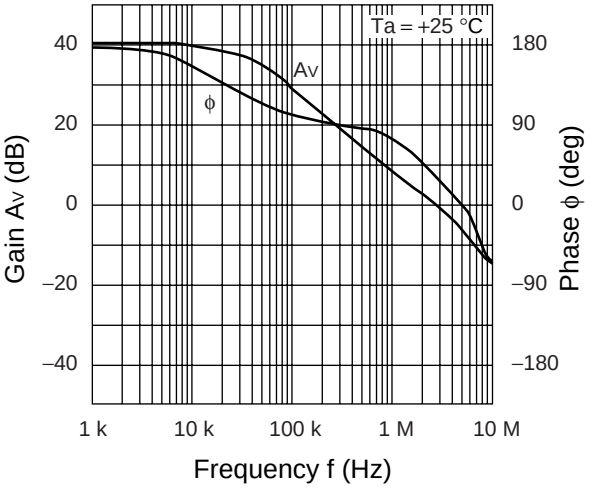
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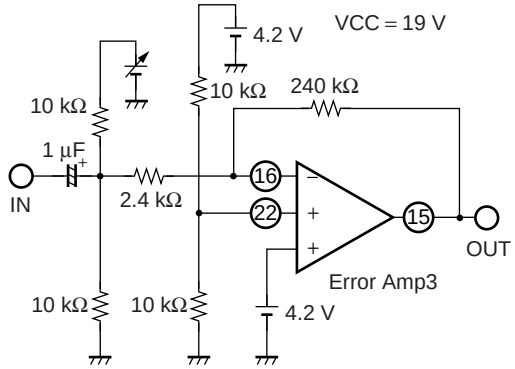
Error amplifier gain and phase vs. Frequency



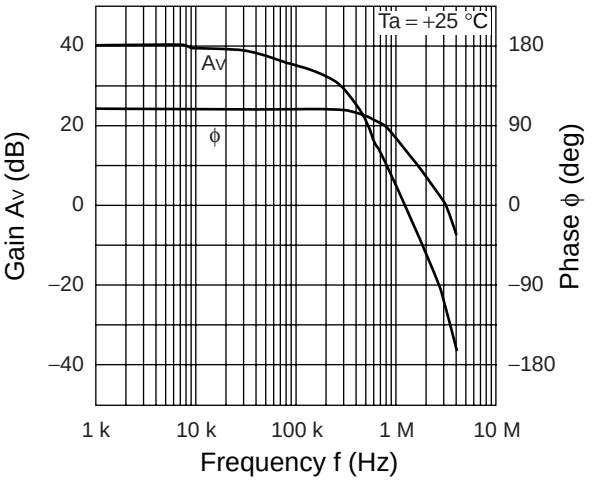


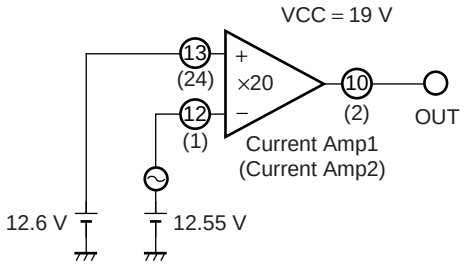
Error amplifier gain and phase vs. Frequency





Current detection amplifier gain and phase vs. Frequency

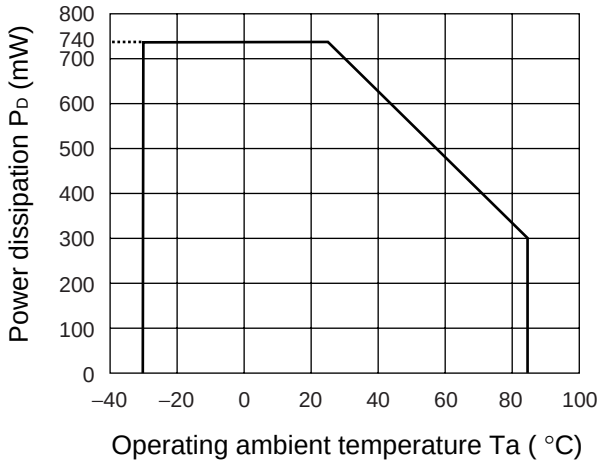




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Power dissipation vs. Operating ambient temperature



■ FUNCTIONAL DESCRIPTION

1. DC/DC Converter Unit

(1) Reference voltage block (REF)

The reference voltage generator uses the voltage supplied from the VCC terminal (pin 18) to generate a temperature-compensated, stable voltage (5.0 V Typ) used as the reference supply voltage for the IC's internal circuitry.

This terminal can also be used to obtain a load current to a maximum of 1mA from the reference voltage VREF terminal (pin 6) .

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator builds the capacitor for frequency setting into, and generates the triangular wave oscillation waveform by connecting the frequency setting resistor with the RT terminal (pin 17) .

The triangular wave is input to the PWM comparator on the IC.

(3) Error amplifier block (Error Amp1)

This amplifier detects the output signal from the current detection amplifier (Current amp1) , compares this to the +INE1 terminal (pin 9) , and outputs a PWM control signal to be used in controlling the charging current.

In addition, an arbitrary loop gain can be set up by connecting a feedback resistor and capacitor between the FB1 terminal (pin 7) and -INE1 terminal (pin 8) , providing stable phase compensation to the system.

(4) Error amplifier block (Error Amp2)

This amplifier (Error Amp2) detects voltage drop of the AC adapter and outputs a PWM control signal.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the FB2 terminal (pin 5) to the –INE2 terminal (pin 4) of the error amplifier, enabling stable phase compensation to the system.

(5) Error amplifier block (Error Amp3)

This error amplifier (Error Amp3) detects the output voltage from the DC/DC converter and outputs the PWM control signal. External output voltage setting resistors can be connected to the error amplifier inverted input terminal to set the desired level of output voltage from 1 cell to 4 cells.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the FB3 terminal (pin 15) to the –INE3 terminal (pin 16) of the error amplifier, enabling stable phase compensation to the system.

Connecting a soft-start capacitor to the CS terminal (pin 22) prevents rush currents when the IC is turned on.

Using an error amplifier for soft-start detection makes the soft-start time constant, independent of the output load.

(6) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) detects a voltage drop which occurs between both ends of the output sense resistor (R_S) due to the flow of the charge current, using the +INC1 terminal (pin 13) and –INC1 terminal (pin 12) . Then it outputs the signal amplified by 20 times to the error amplifier (Error Amp1) at the next stage.

(7) PWM comparator block (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp1 to Error Amp3) depending on their output voltage.

The PWM comparator circuit compares the triangular wave generated by the triangular wave oscillator to the error amplifier output voltage and turns on the external output transistor during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

(8) Output block (OUT)

The output circuit uses a totem-pole configuration capable of driving an external P-channel MOS FET.

The output “L” level sets the output amplitude to 6 V (Typ) using the voltage generated by the bias voltage block (VH) .

This results in increasing conversion efficiency and suppressing the withstand voltage of the connected external transistor in a wide range of input voltages.

(9) Control block (CTL)

Setting the CTL terminal (pin 14) low places the IC in the standby mode. (The supply current is 10 μA at maximum in the standby mode.)

CTL function table

CTL	Power	OUTD
L	OFF (Standby)	Hi-Z
H	ON (Active)	L

(10) Bias voltage block (VH)

The bias voltage circuit outputs V_{CC} –6 V (Typ) as the minimum potential of the output circuit. In the standby mode, this circuit outputs the potential equal to VCC.

2. Protection Functions

Under voltage lockout protection circuit (UVLO)

The transient state or a momentary decrease in supply voltage or internal reference voltage (VREF) , which occurs when the power supply (VCC) is turned on, may cause malfunctions in the control IC, resulting in breakdown or degradation of the system.

To prevent such malfunction, the under voltage lockout protection circuit detects a supply voltage or internal reference voltage drop and fixes the OUT terminal (pin 20) to the “H” level. The system restores voltage supply when the supply voltage or internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (UVLO) operation function table

When UVLO is operating (VCC or VREF voltage is lower than UVLO threshold voltage.)

OUTD	OUT	CS
Hi-Z	H	L

3. Soft-Start Function

Soft-start block (SOFT)

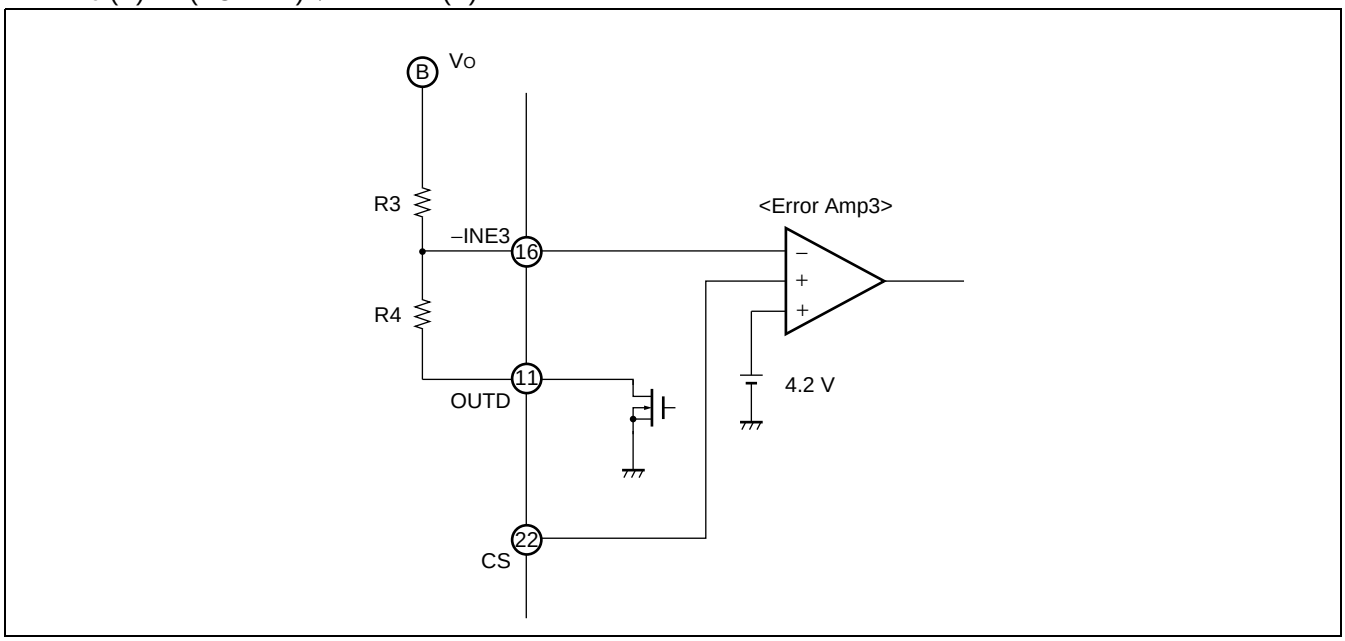
Connecting a capacitor to the CS terminal (pin 22) prevents rush currents when the IC is turned on. Using an error amplifier for soft-start detection makes the soft-start time constant, being independent of the output load of the DC/DC converter.

■ SETTING THE CHARGING VOLTAGE

The charging voltage (DC/DC output voltage) can be set by connecting external voltage setting resistors (R3, R4) to the –INE3 terminal (pin 16) . Be sure to select a resistor value that allows you to ignore the on-resistor (35 Ω, 1mA) of the internal FET connected to the OUTD terminal (pin 11) . In standby mode, the charging voltage is applied to OUTD termial. Therefore, output voltage must be adjusted so that voltage applied to OUTD terminal is 17 V or less.

Battery charging voltage : V_O

V_O (V) = (R3 + R4) / R4 × 4.2 (V)



■ METHOD OF SETTING THE CHARGING CURRENT

The charge current (output limit current) value can be set with the voltage at the +INE1 terminal (pin 9) .

If a current exceeding the set value attempts to flow, the charge voltage drops according to the set current value.

Battery charge current setting voltage : +INE1

+INE1 (V) = 20 × I1 (A) × R_S (Ω)

■ METHOD OF SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency can be set by the timing resistor (R_T) connected the RT terminal (pin 17) .

Triangular wave oscillation frequency : f_{OSC}

f_{OSC} (kHz) ≒ 13630 / R_T (kΩ)

■ METHOD OF SETTING THE SOFT-START TIME

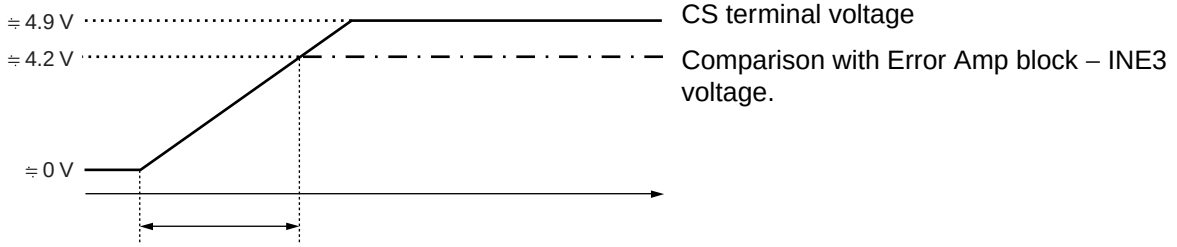
For preventing rush current upon activation of IC, the IC allows soft-start using the capacitor (Cs) connected to the CS terminal (pin 22) .

When CTL terminal (pin 14) is placed under “H” level and IC is activated ($V_{CC} \geq$ UVLO threshold voltage) , Q2 is turned off and the external soft-start capacitor (Cs) connected to the CS terminal is charged at 10 µA.

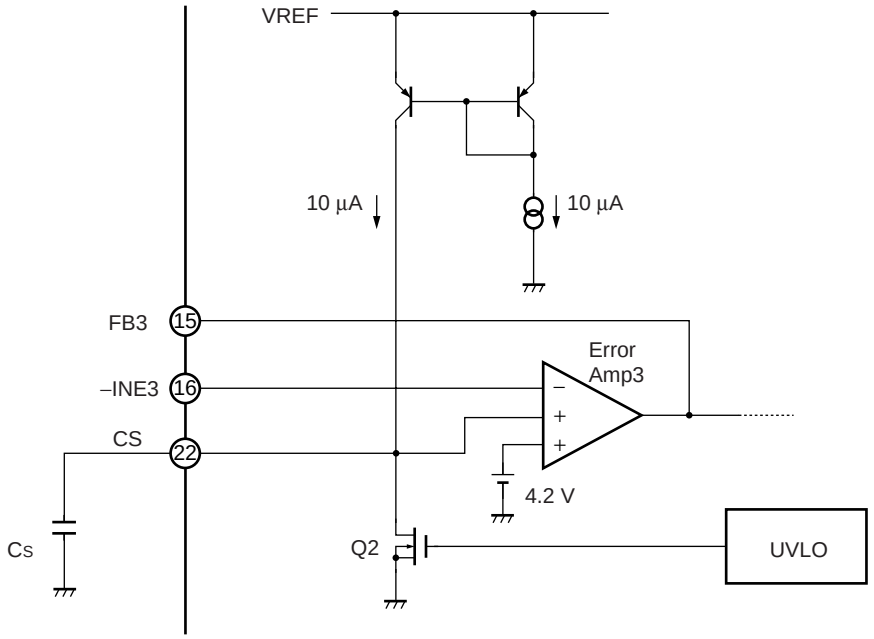
Error Amp output (FB3 terminal (pin 15)) is determined by comparison between the lower voltage of the two non-reverse input terminals (4.2 V and CS terminal voltage) and reverse input terminal voltage (–INE3 terminal (pin 16) voltage) . Within the soft-start period (CS terminal voltage < 4.2 V) , FB3 is determined by comparison between –INE3 terminal voltage and CS terminal voltage, and DC/DC converter output voltage goes up proportionately with the increase of CS terminal voltage caused by charging on the soft-start capacitor.Soft-start time is found by the following formula :

Soft-start time : ts (time to output 100 %)

t_S (s) ≒ 0.42 × C_S (µF)



Soft-start time: ts



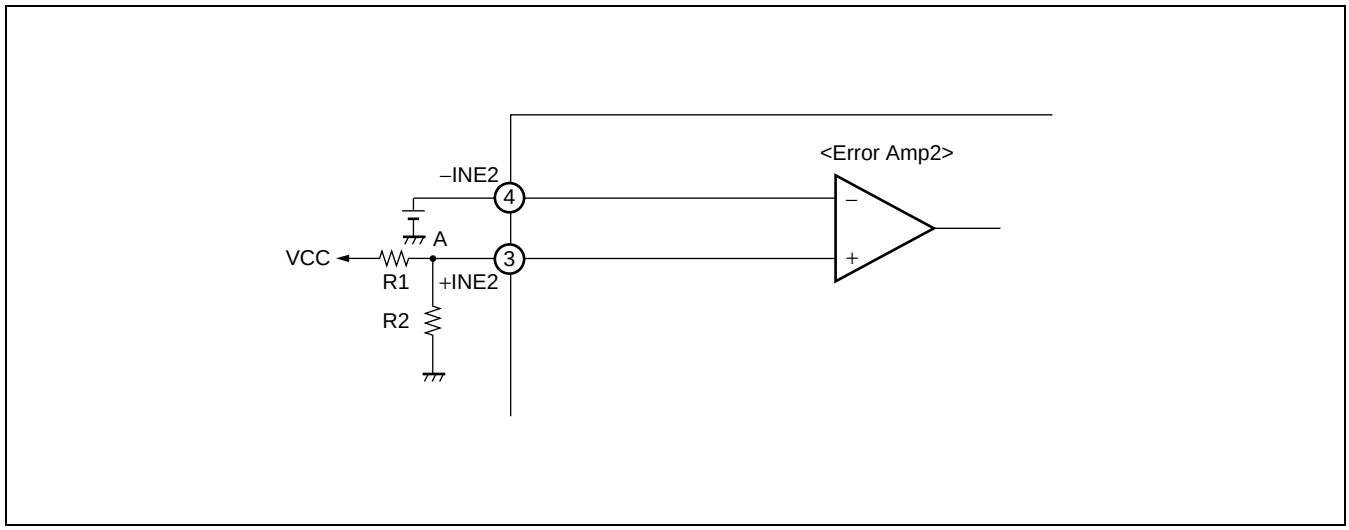
Soft-start circuit

■ AC ADAPTOR VOLTAGE DETECTION

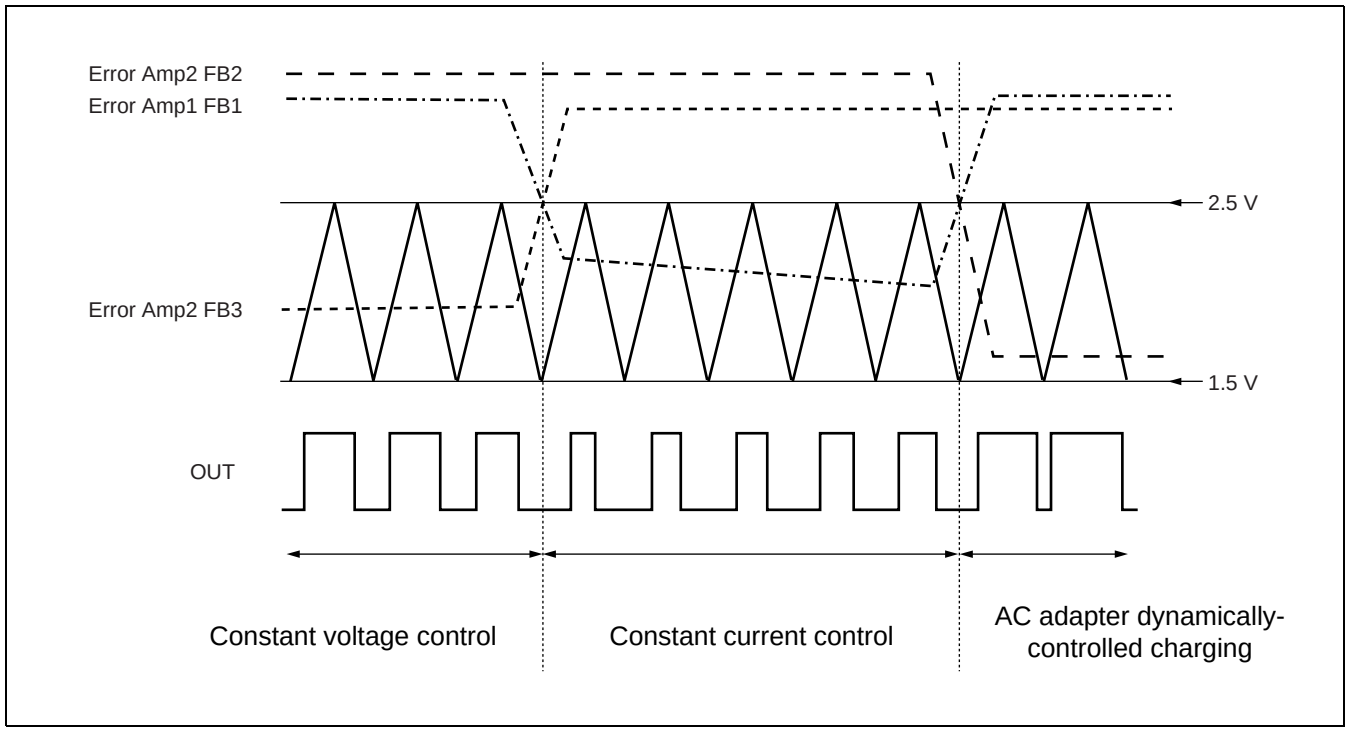
With an external resistor connected to the +INE2 terminal (pin 3) , the IC enters the dynamically-controlled charging mode to reduce the charge current to keep AC adapter power constant when the partial potential point A of the AC adapter voltage (VCC) becomes lower than the voltage at the −INE2 terminal.

AC adapter detection voltage setting : Vth

$$Vth\ (V) = (R1 + R2) / R2 \times -INE2$$

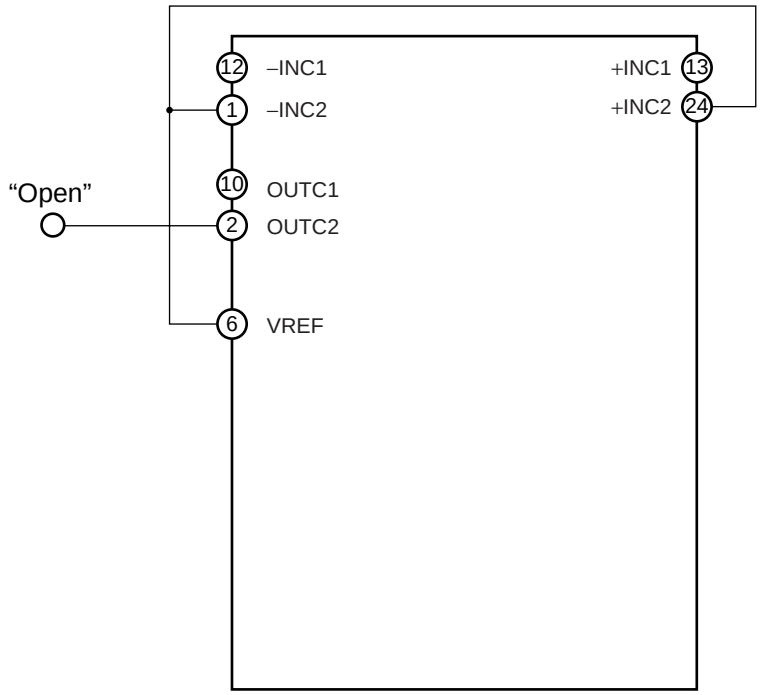


■ OPERATION TIMING DIAGRAM



■ PROCESSING WITHOUT USING THE CURRENT AMP

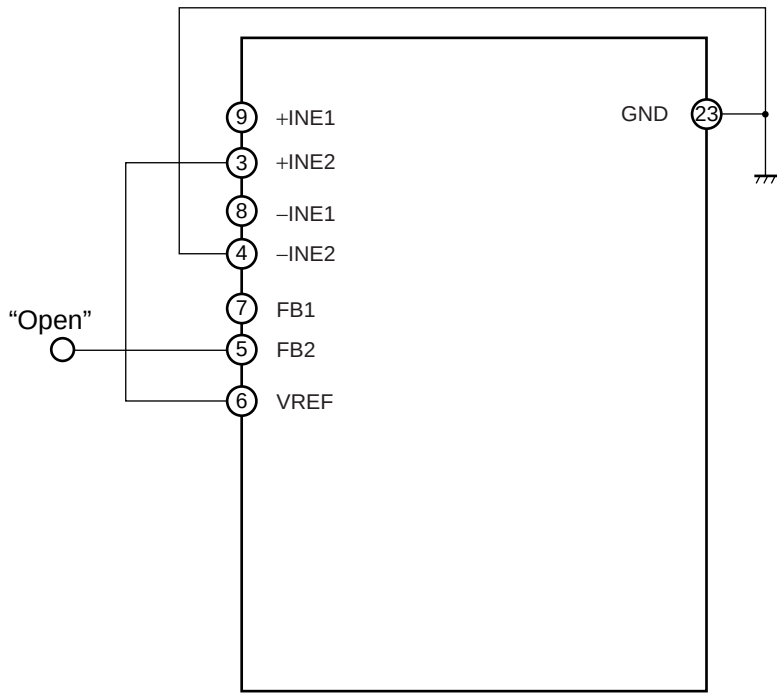
When Current Amp is not used, connect the +INC1 terminal (pin 13) , +INC2 terminal (pin 24) , –INC1 terminal (pin 12) , and –INC2 terminal (pin 1) to VREF, and then leave OUTC1 terminal (pin 10) and OUTC2 terminal (pin 2) open.



Connection when Current Amp is not used

■ PROCESSING WITHOUT USING OF THE ERROR AMP

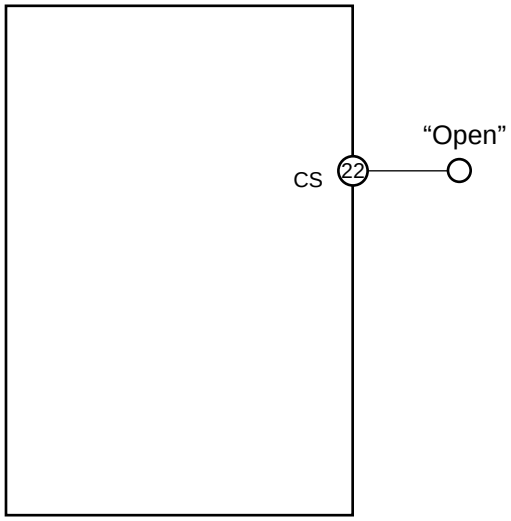
When Error Amp is not used, leave FB1 terminal (pin 7) , FB2 terminal (pin 5) open and connect the –INE1 terminal (pin 8) and –INE2 terminal (pin 4) to GND and connect +INE1 terminal (pin 9) , and +INE2 terminal (pin 3) , to VREF.



Connection when Error Amp is not used

■ PROCESSING WITHOUT USING OF THE CS TERMINAL

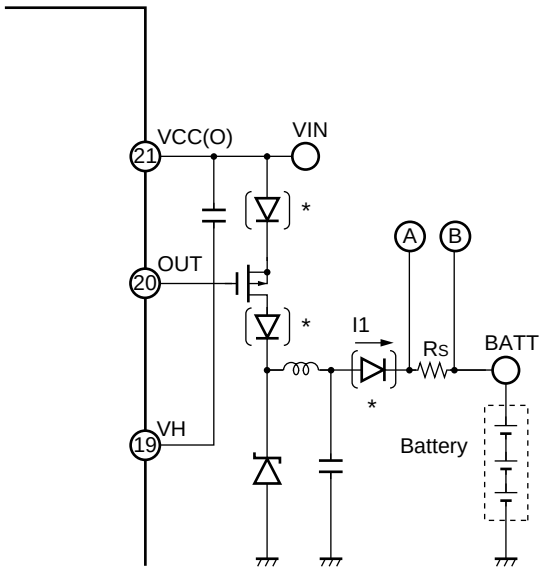
When soft-start function is not used, leave the CS terminal (pin 22) open.



Connection when soft-start time is not specified

■ NOTE ON AN EXTERNAL REVERSE-CURRENT PREVENTIVE DIODE

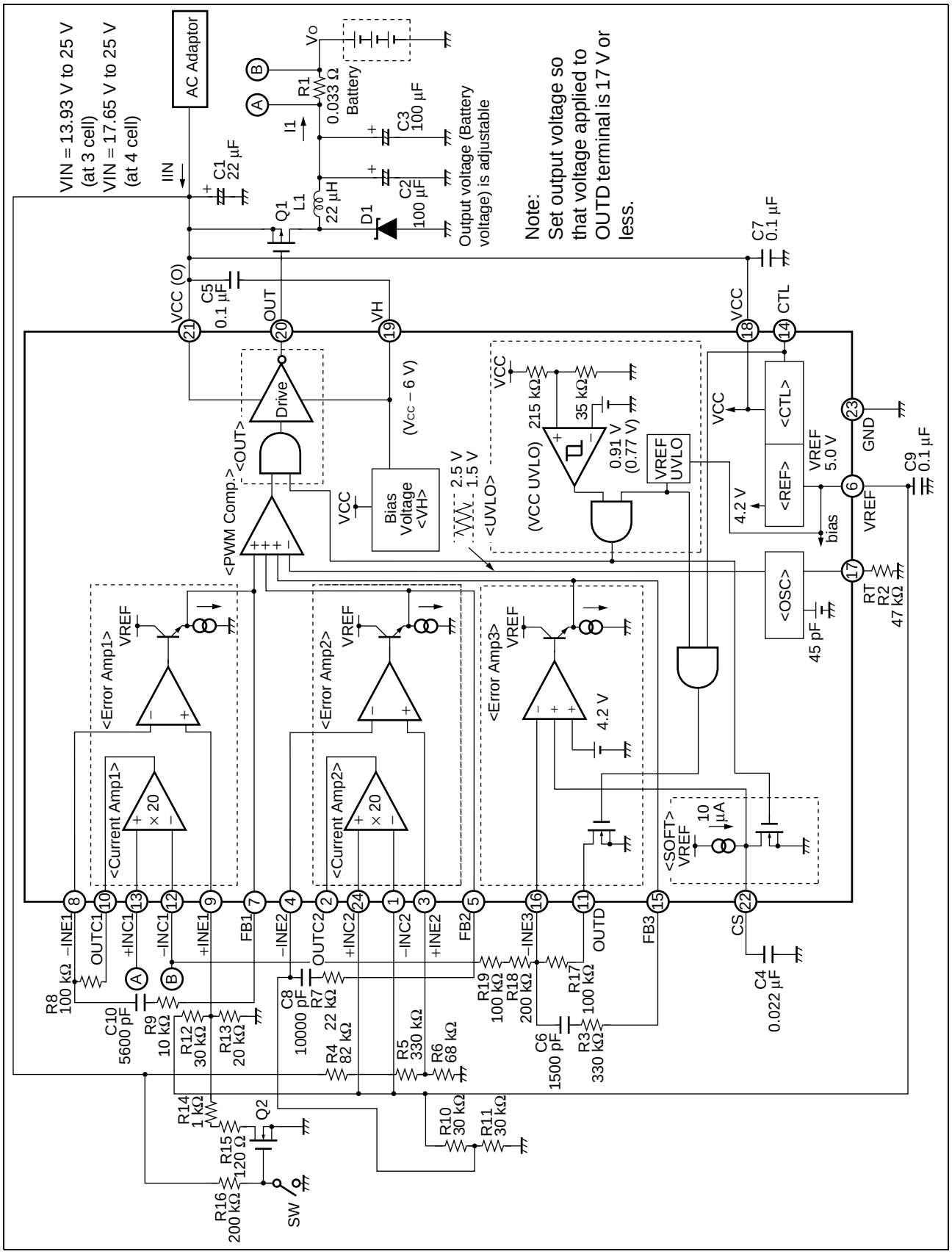
- Insert a reverse-current preventive diode at one of the three locations marked * to prevent reverse current from the battery.
- When selecting the reverse current prevention diode, be sure to consider the reverse voltage (V_R) and reverse current (I_R) of the diode.



■ THE SEQUENCE OF THE START-UP AND OFF OF THE POWER SUPPLY

Please start up and off the VCC terminal (pin 18) and VCC(O) terminal (pin 21) of the power supply terminal at the same time. No do occurrence of the bias from the VH terminal (pin 19) , when there is a period of 8 V or less in the VCC voltage after previously starting up VCC(O). At this time, there is a possibility of leading to permanent destruction of the device when the voltage of 17 V or more is impressed to the VCC(O) terminal. Moreover, when earliness VCC falls more than VCC(O) when falling, it is similar.

■ APPLICATION EXAMPLE



■ PARTS LIST

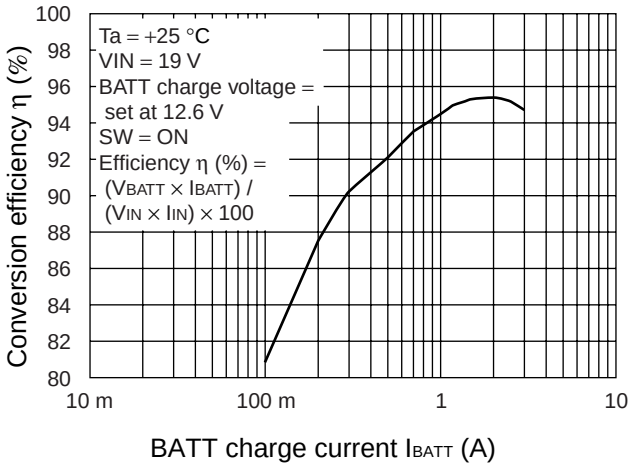
COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1	P-ch FET	VDS = –30 V, ID = ±8 A (Max)		VISHAY SILICONIX	Si4435DY
Q2	N-ch FET	VDS = 60 V, ID = 0.115 A (Max)		VISHAY SILICONIX	2N7002E
D1	Diode	VF = 0.42 V (Max) , IF = 3 A		ROHM	RB053L-30
L1	Inductor	22 µH	3.5 A, 31.6 mΩ	TDK	SLF12565T-220M3R5
C1	OS-CON™	22 µF	25 V (10 %)	SANYO	25SL22M
C2, C3	Electrolytic Condenser	100 µF	25 V (10 %)	SANYO	25CV100AX
C4	Ceramics Condenser	0.022 µF	50 V	TDK	C1608JB1H223K
C5	Ceramics Condenser	0.1 µF	16 V	KYOCERA	CM21W5R104K16
C6	Ceramics Condenser	1500 pF	10 V	MURATA	GRM39B152K10
C7	Ceramics Condenser	0.1 µF	25 V	MURATA	GRM39F104KZ25
C8	Ceramics Condenser	10000 pF	10 V	MURATA	GRM39B103K10
C9	Ceramics Condenser	0.1 µF	16 V	KYOCERA	CM21W5R104K16
C10	Ceramics Condenser	5600 pF	10 V	MURATA	GRM39B562K10
R1	Resistor	0.033 Ω	1.0 %	SEIDEN TECHNO	RK73Z1J-0D
R2	Resistor	47 kΩ	0.5 %	KOA	RK73G1J-473D
R3	Resistor	330 kΩ	0.5 %	KOA	RK73G1J-334D
R4	Resistor	82 kΩ	0.5 %	KOA	RK73G1J-823D
R5	Resistor	330 kΩ	0.5 %	KOA	RK73G1J-334D
R6	Resistor	68 kΩ	0.5 %	KOA	RK73G1J-683D
R7	Resistor	22 kΩ	0.5 %	KOA	RK73G1J-223D
R8	Resistor	100 kΩ	0.5 %	KOA	RK73G1J-104D
R9	Resistor	10 kΩ	1.0 %	KYOCERA	CR21-103-F
R10 to R12	Resistor	30 kΩ	0.5 %	KOA	RK73G1J-303D
R13	Resistor	20 kΩ	0.5 %	KOA	RK73G1J-203D
R14	Resistor	1 kΩ	0.5 %	KOA	RK73G1J-102D
R15	Resistor	120 Ω	0.5 %	ssm	RR0816P121D
R16, R18	Resistor	200 kΩ	0.5 %	KOA	RK73G1J-204D
R17, R19	Resistor	100 kΩ	0.5 %	KOA	RK73G1J-104D

Note : VISHAY SILICONIX : VISHAY Intertechnology, Inc.
ROHM : ROHM CO., LTD.
TDK : TDK Corporation
SANYO : SANYO Electric Co., Ltd.
KYOCERA : Kyocera Corporation
MURATA : Murata Manufacturing Co., Ltd.
SEIDEN TECHNO : SEIDEN TECHNO CO., LTD.
KOA : KOA Corporation
ssm : SUSUMU Co., Ltd.

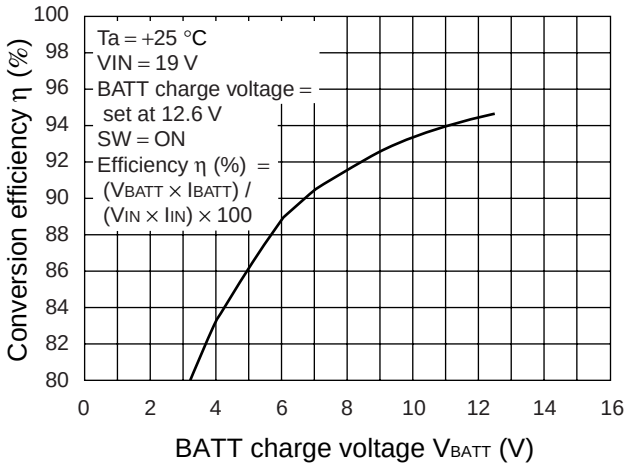
OS-CON is a trademark of SANYO Electric Co., Ltd.

■ REFERENCE DATA

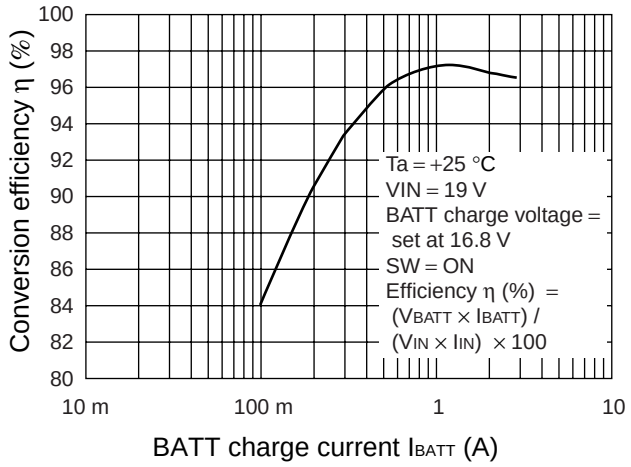
Conversion efficiency vs. Charge current
(Constant voltage mode)



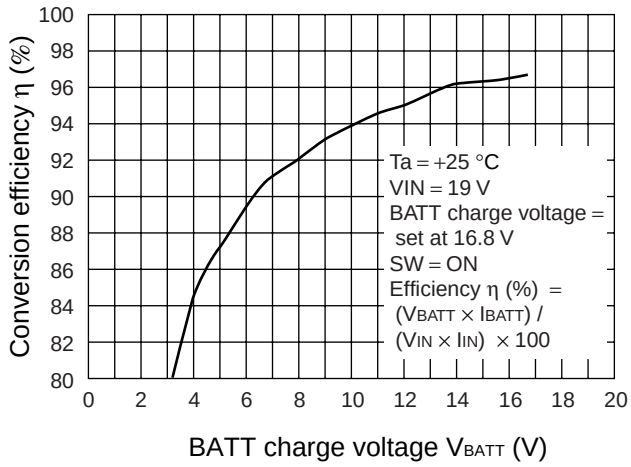
Conversion efficiency vs. Charge current
(Constant current mode)



Conversion efficiency vs. Charge current
(Constant voltage mode)

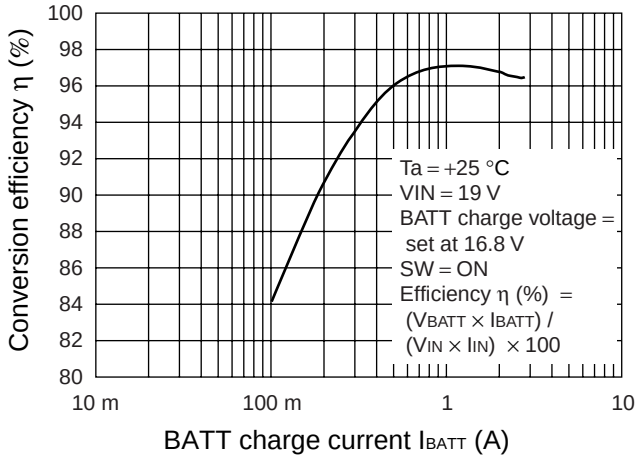


Conversion efficiency vs. Charge current
(Constant current mode)

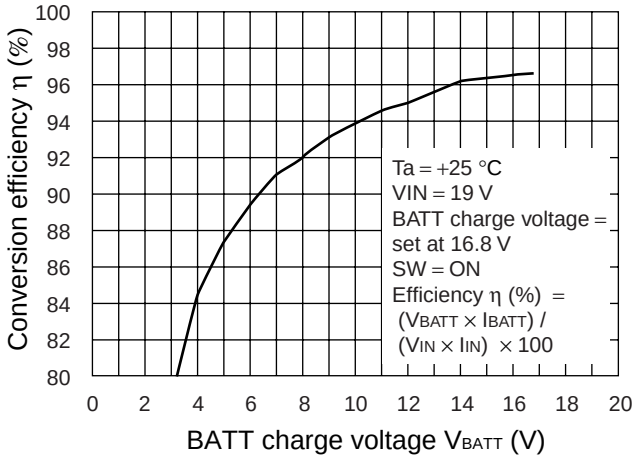


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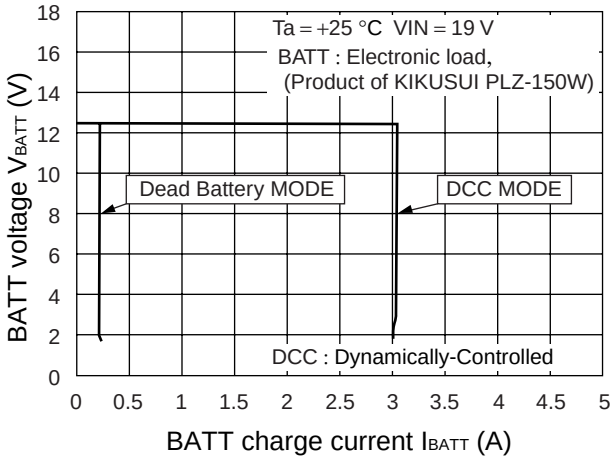
Conversion efficiency vs. Charge current
(Constant voltage mode)



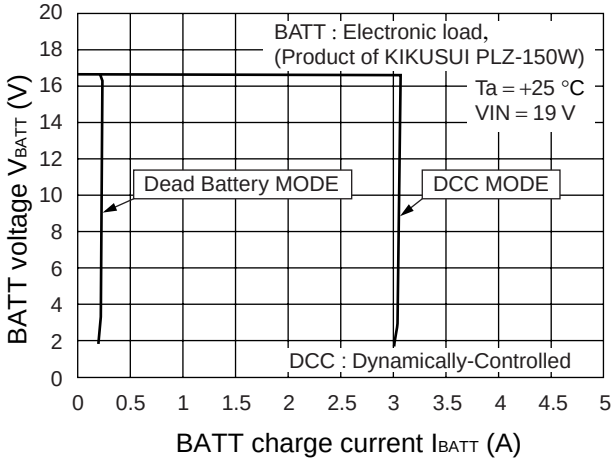
Conversion efficiency vs. Charge current
(Constant current mode)



BATT voltage vs. BATT charge current
(set at 12.6 V)

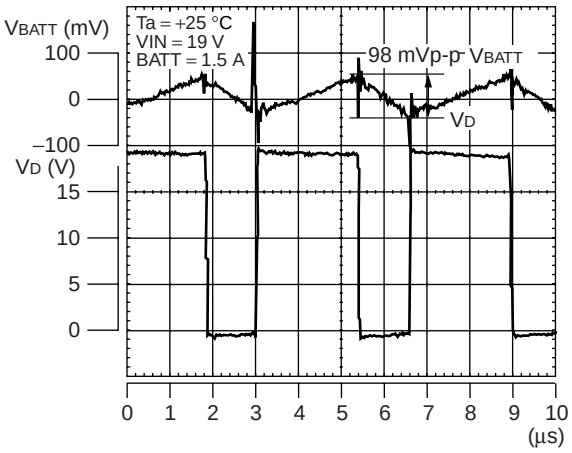


BATT voltage vs. BATT charge current
(set at 16.8 V)

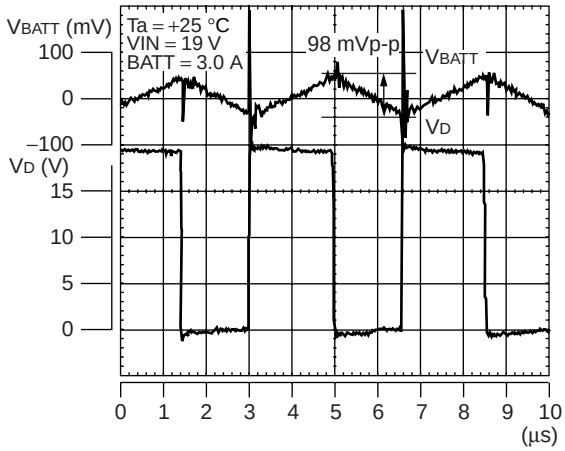


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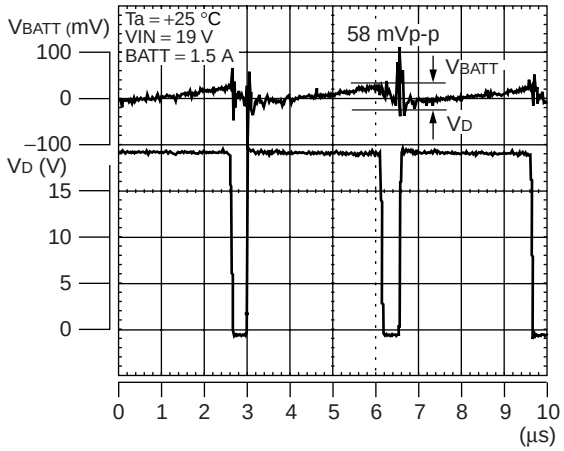
Switching waveform constant voltage mode
(set at 12.6 V)



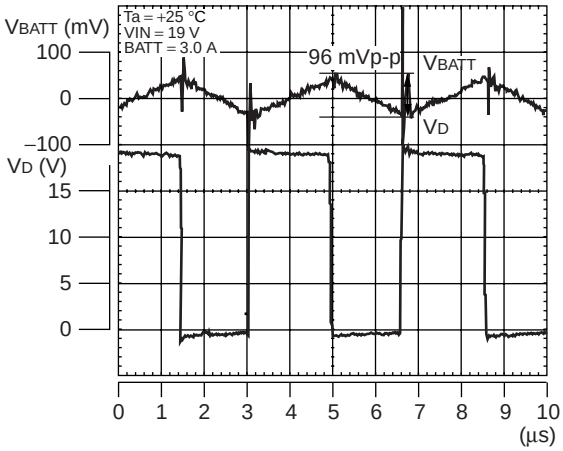
Switching waveform constant current mode
(set at 12.6 V, with 10 V)



Switching waveform constant voltage mode
(set at 16.8 V)



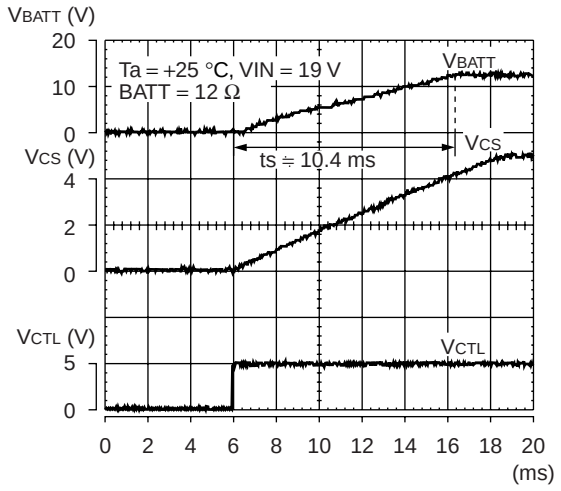
Switching waveform constant current mode
(set at 16.8 V, with 10 V)



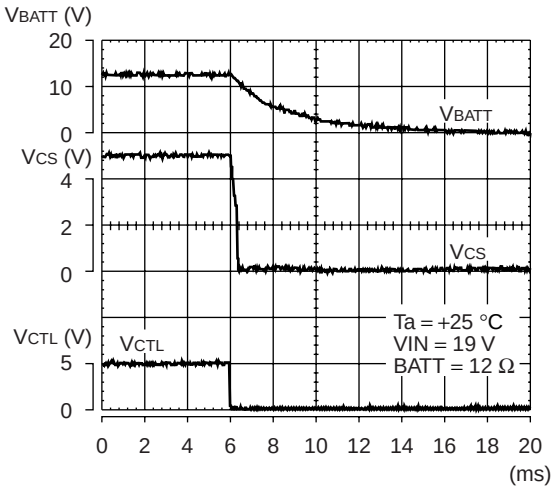
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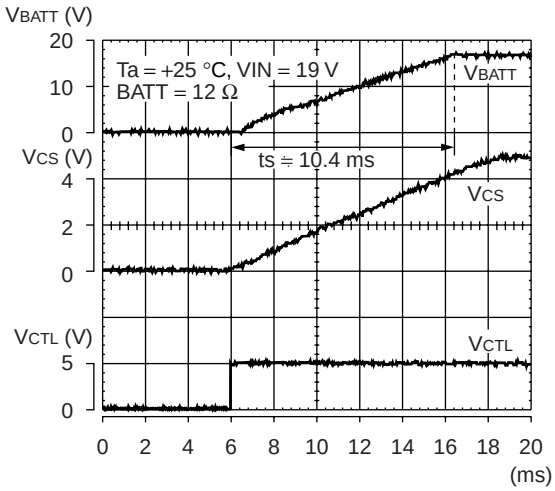
Soft-start operating waveform
constant voltage mode
(set at 12.6 V)



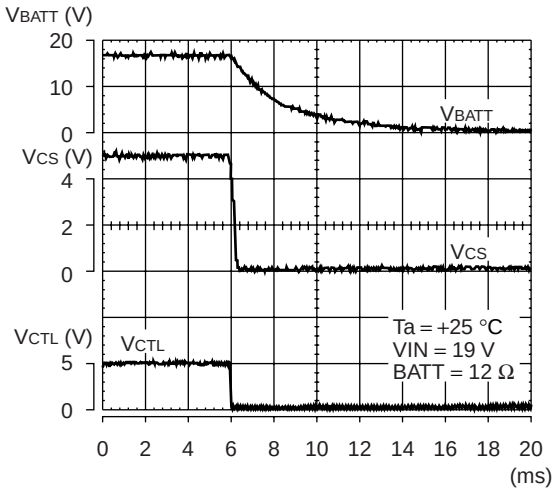
Discharge operating waveform
constant voltage mode
(set at 12.6 V)



Soft-start operating waveform
constant voltage mode
(set at 16.8 V)



Discharge operating waveform
constant voltage mode
(set at 16.8 V)



■ USAGE PRECAUTIONS

- Printed circuit board ground lines should be set up with consideration for common impedance.

- Take appropriate static electricity measures.
  - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
  - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
  - Work platforms, tools, and instruments should be properly grounded.
  - Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

- Do not apply negative voltages.
  - The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause malfunction.

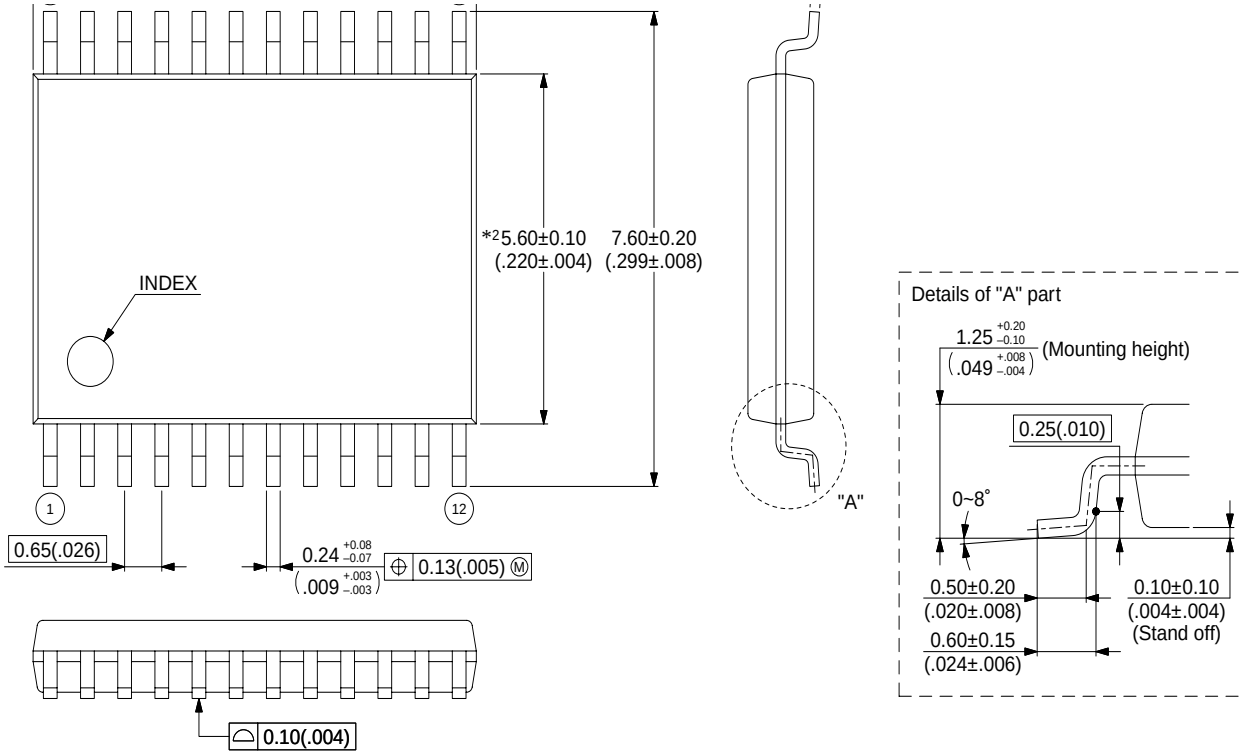
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3887PFV	24-pin plastic SSOP (FPT-24P-M03)	

■ PACKAGE DIMENSION

24-pin plastic SSOP
(FPT-24P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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