Monolithic N-Channel JFET Duals

SST404NL U401NL U406NL
SST406NL U404NL

PRODUCT SUMMARY

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$\|V_{GS1} - V_{GS2}\|$ Max (mV)
U401NL	-0.5 to -2.5	-40	1	-2	5
SST/U404NL	-0.5 to -2.5	-40	1	-2	15
SST/U406NL	-0.5 to -2.5	-40	1	-2	40

FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 2 pA
- Low Noise
- High CMRR: 102 dB

BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

- Wideband Differential Amps
- High-Speed,Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

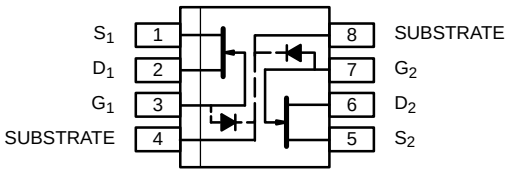
DESCRIPTION

The SST/U401NL series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. This series has a wide selection of offset and drift specifications with the U401NL featuring a 5-mV offset and 10-μV/°C drift.

Pins 4 and 8 of the SST series, and pin 4 of the U series part numbers enable the substrate to be connected to a positive polarity, external bias (V_{DD}) to avoid latchup.

The U series, hermetically sealed TO-78 package is available with full military processing. The SST series SO-8 package provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.

Narrow Body SOIC

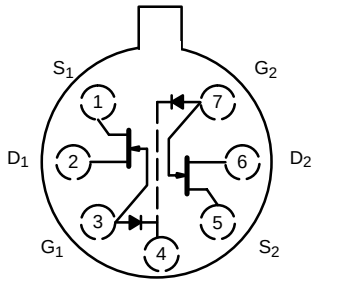


Top View

Marking Codes:

SST404NL - 404NL
SST406NL - 406NL

TO-78



Top View
U401NL
U404NL
U406NL

ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage . . . . . -40 V

Gate Current . . . . . 10 mA

Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C

Storage Temperature : U Prefix . . . . . -65 to 200°C
SST Prefix . . . . . -55 to 150°C

For applications information see AN106.

Operating Junction Temperature . . . . . -55 to 150°C

Power Dissipation : Per Side[a] . . . . . 300 mW
Total[b] . . . . . 500 mW

Notes
a. Derate 2.4 mW/°C above 25°C
b. Derate 4 mW/°C above 25°C

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

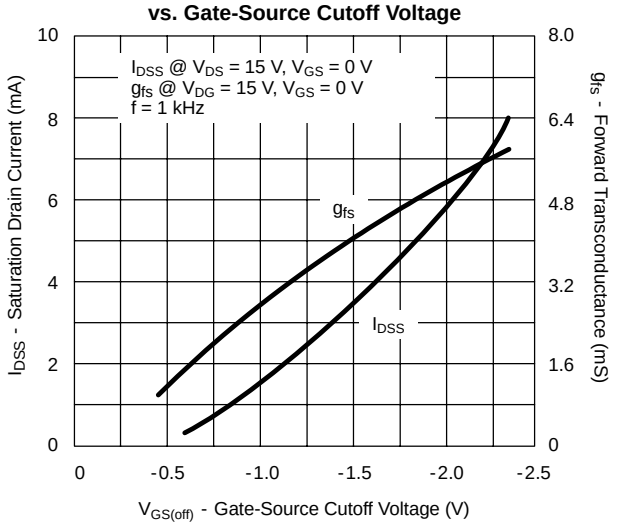
Parameter	Symbol	Test Conditions		Typ[a]	Limits U401NL Min	Limits U401NL Max	Limits SST/U404NL Min	Limits SST/U404NL Max	Limits SST/U406NL Min	Limits SST/U406NL Max	Unit
Static											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 μA, V_{DS} = 0 V		-58	-40		-40		-40		V
	$V_{(BR)G1 - G2}$	I_G = ±1 μA, V_{DS} = 0 V, V_{GS} = 0 V		±45	±30		±30		±30		
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 1 nA		-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V		-2		-25		-25		-25	pA
			T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 μA		-2		-15		-15		-15	pA
			T_A = 125°C	-0.8		-10		-10		-10	nA
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, I_D = 0.1 mA		250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 μA		-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V		0.7							
Dynamic											
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 200 μA f = 1 kHz		1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}			1.3		2		2		2	μS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz		4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}			5		30		30		30	μS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 200 μA f = 1 MHz		4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			1.5		3		3		3	
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = 15 V, I_D = 200 μA f = 10 Hz (U Only)		10		20		20		20	$\frac{nV}{\sqrt{Hz}}$
Matching											
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 200 μA				5		15		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V I_D = 200 μA T_A = -55 to 125°C	SST404NL	20							μV/°C
			SST406NL	40							
			All U			10		25		80	
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 μA		102	95		95				dB

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

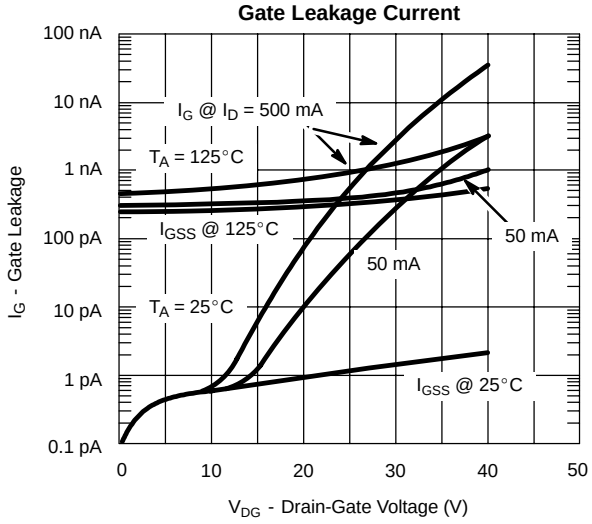
NNR

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

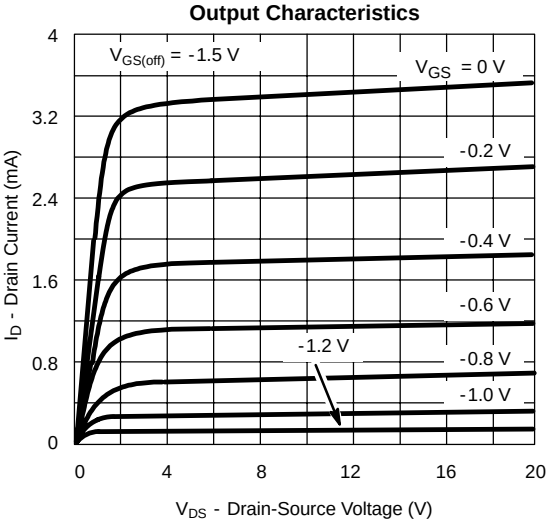
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



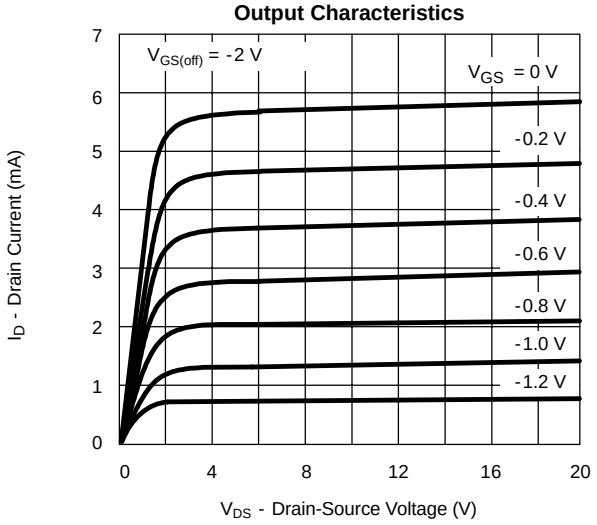
Gate Leakage Current



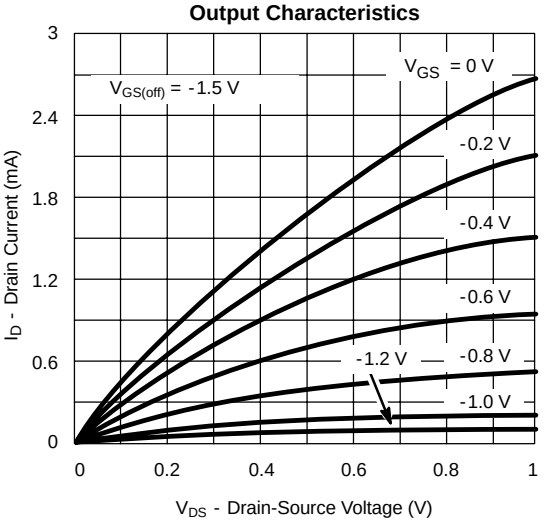
Output Characteristics



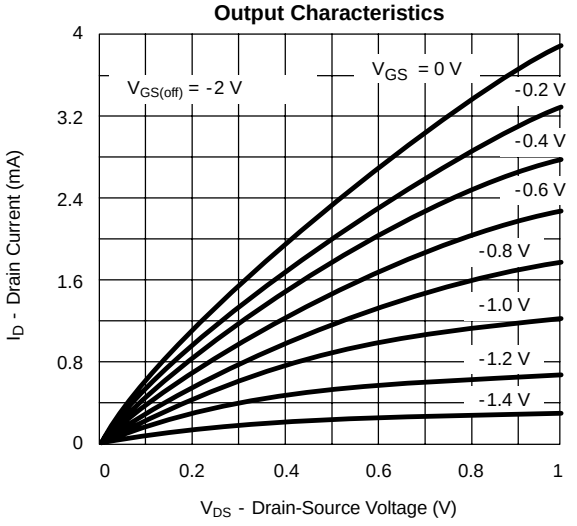
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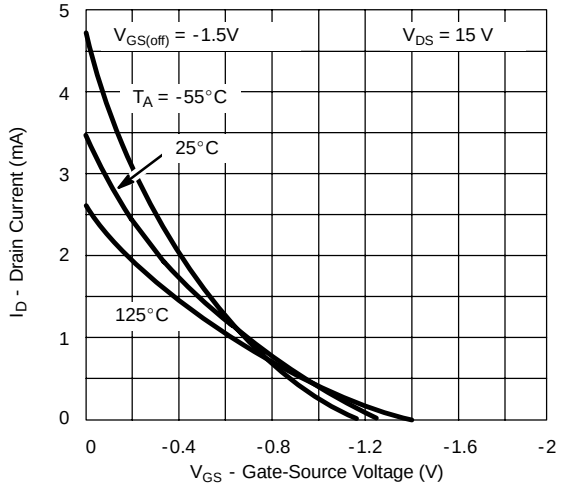


Output Characteristics

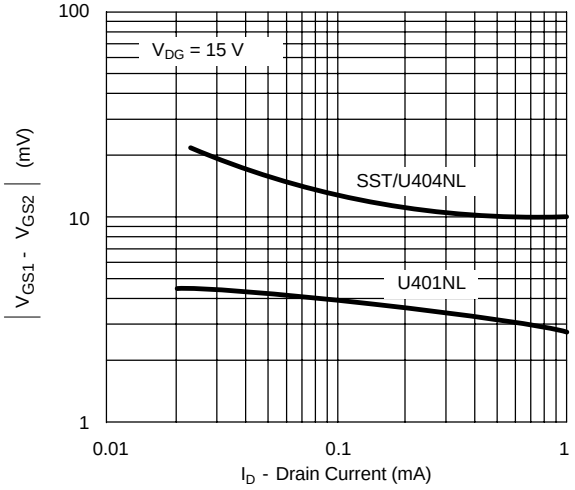


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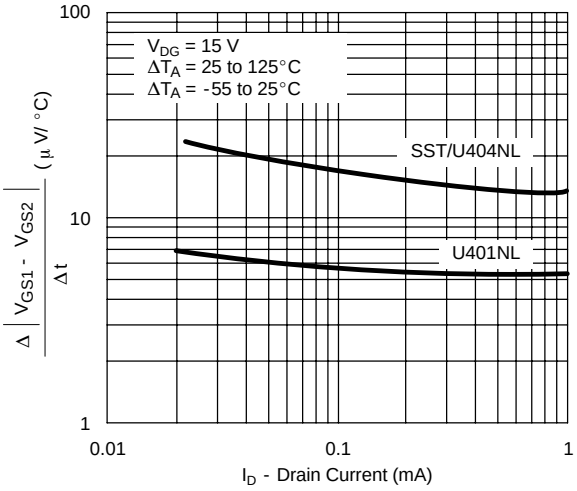
Transfer Characteristics



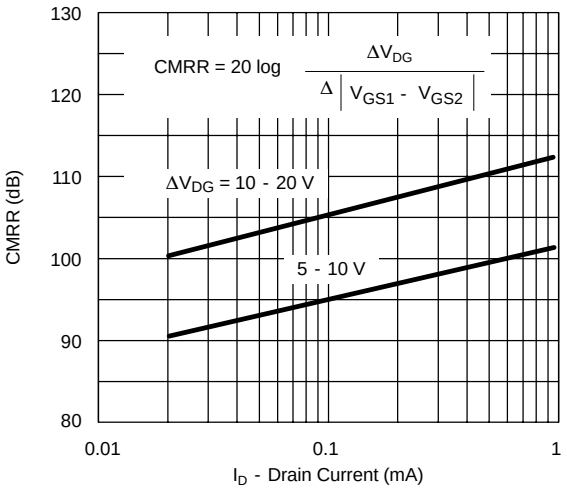
Gate-Source Differential Voltage vs. Drain Current



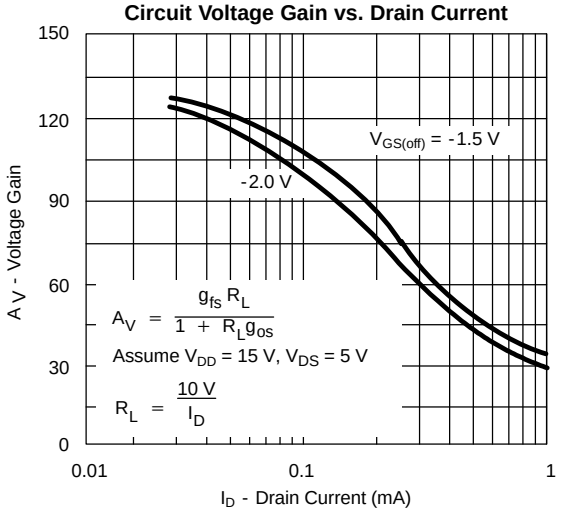
Voltage Differential with Temperature vs. Drain Current



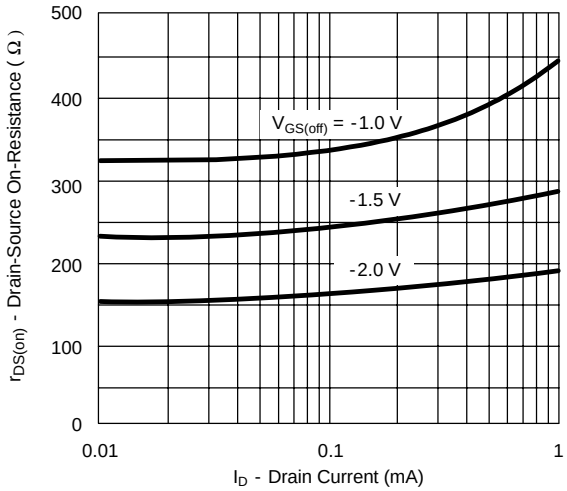
Common Mode Rejection Ratio vs. Drain Current



Circuit Voltage Gain vs. Drain Current

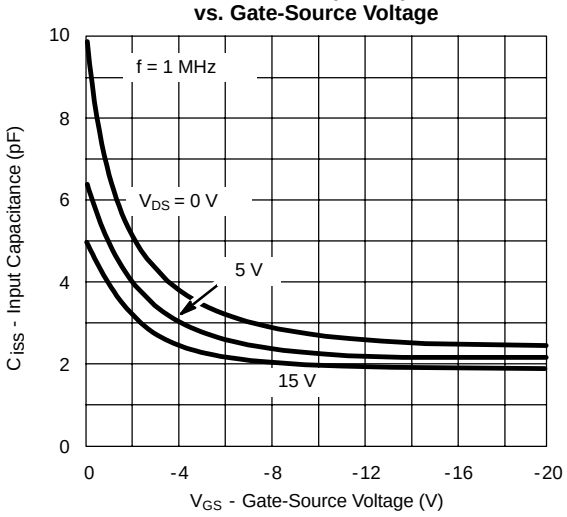


On-Resistance vs. Drain Current

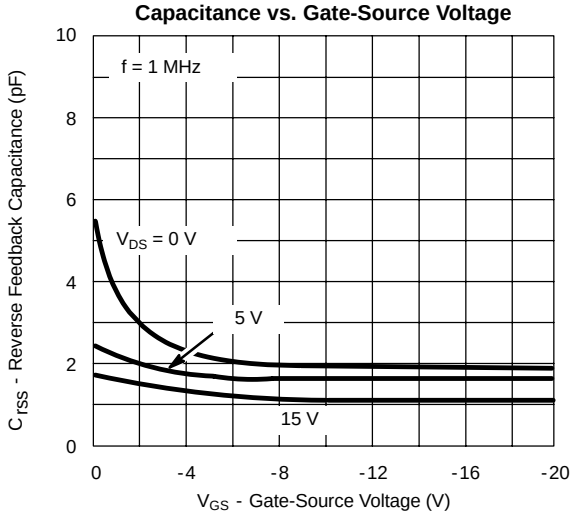


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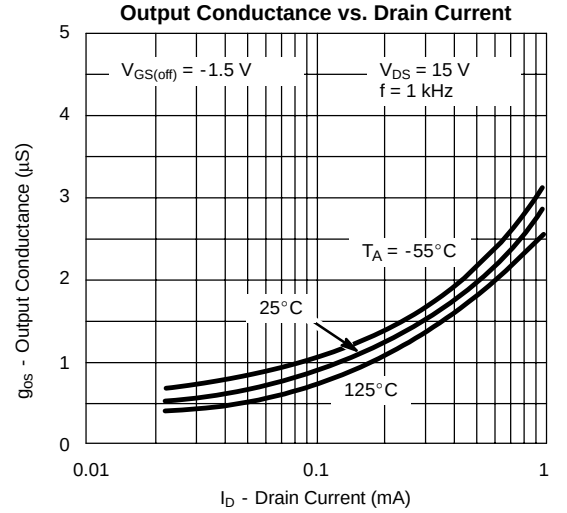
Common-Source Input Capacitance vs. Gate-Source Voltage



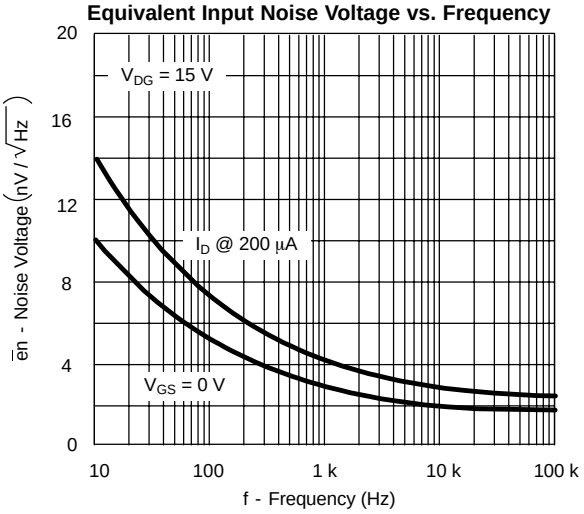
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



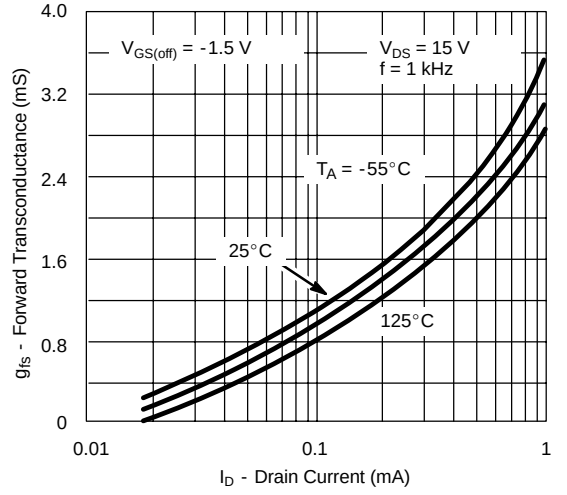
Output Conductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



Common-Source Forward Transconductance vs. Drain Current



On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage

