# 6A, 23V, 500kHz, ACOT™ Synchronous Buck Converter with LDO for System 5V

## General Description

The RT7291A/B is a synchronous Buck converter with Advanced Constant On-Time (ACOT™) mode control. The main control loop of RT7291A/B uses an ACOT™ mode control which provides a very fast transient response with no external compensators. The RT7291A/B operates from 5V to 23V input voltage, provides a 5V LDO and a 300kHz CLK to drive an external charge pump. OCP, UVP and OVP are included in the RT7291A/B. This IC also provides a 1.5ms internal soft-start function and an open-drain power good indicator.

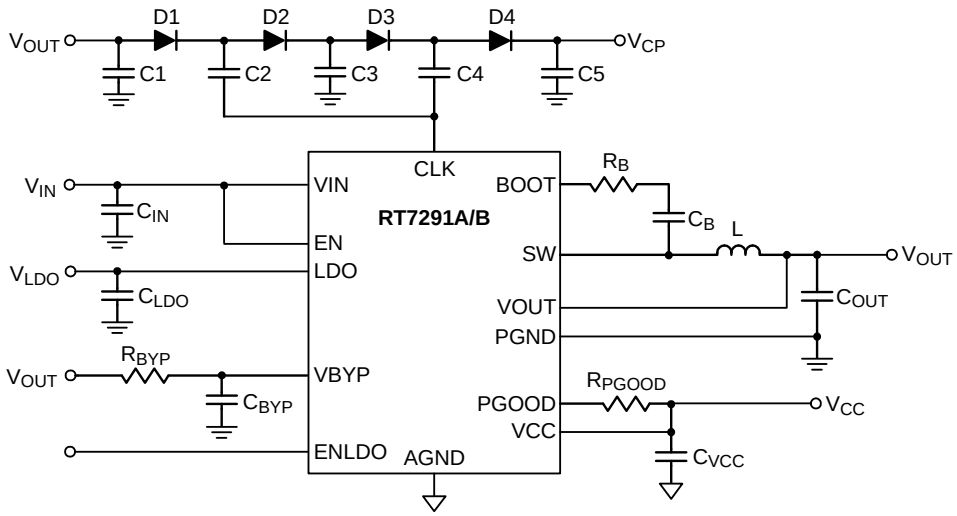
## Applications

- Laptop Computers
- Tablet PCs
- Networking Systems
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

## Features

- **5V to 23V Input Voltage Range**
- **Up to 98% Duty for 2S Battery Application**
- **PWM Frequency Fixed 500kHz**
- **ACOT™ Mode Performs Fast Transient Response**
- **Integrated MOSFETs**
  - **31mΩ of High-Side MOSFET**
  - **20mΩ of Low-Side MOSFET**
- **Support Output MLCC Stable**
- **Internal Soft-Start (1.5ms typ)**
- **Built-in OVP/UVP/OCP**
- **Power Good Indicator**
- **Fixed 300kHz VCLK to Support Charge Pump**
- **Individual EN for PWM and LDO**
- **Thermal Shutdown**

## Simplified Application Circuit




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## Ordering Information

RT7291A/B □□

- Package Type
  QUF : UQFN-16L 3x3 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Output Voltage
  A : 5V
  B : 5.1V

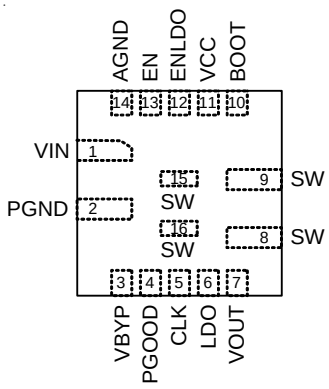
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Pin Configurations

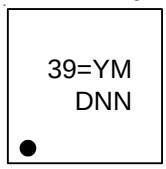
(TOP VIEW)




UQFN-16L 3x3 (FC)

## Marking Information

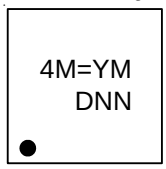
RT7291AGQUF




39= : Product Code

YMDNN : Date Code

RT7291BGQUF




4M= : Product Code

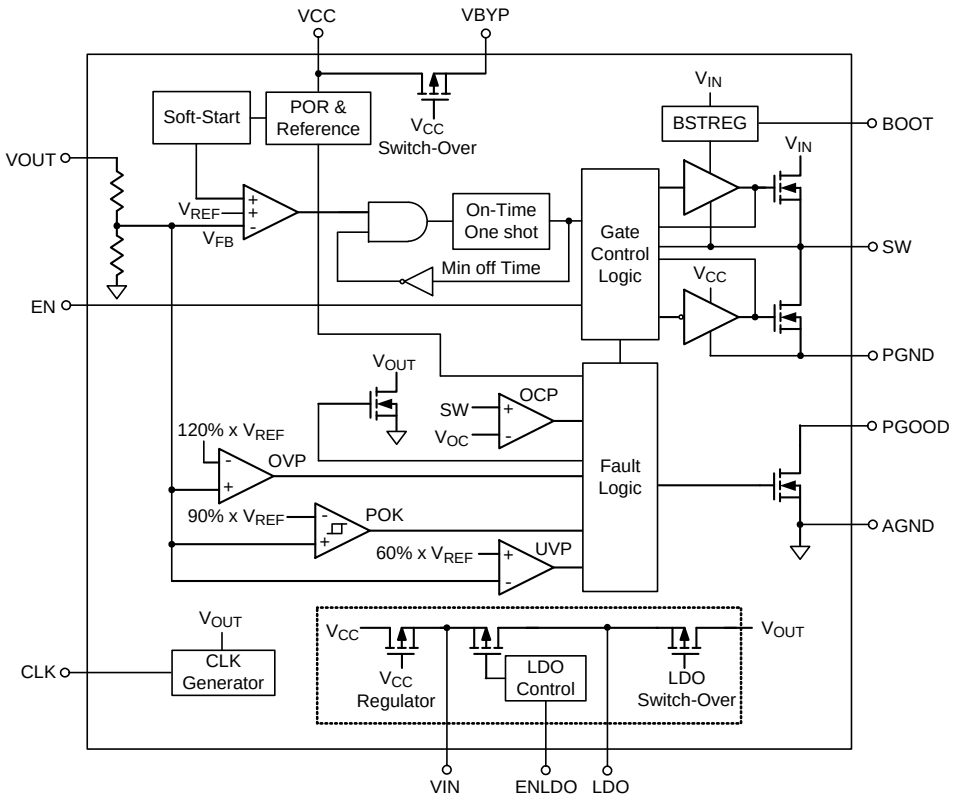
YMDNN : Date Code

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | VIN | Power Input Connect to High-Side MOSFET Drain. |
| 2 | PGND | Power Ground. |
| 3 | VBYP | Switch Over Source Voltage for VCC. A low pass filter should be connected to AGND, if VBYP is applied. If VBYP is not used, then connect to AGND. Do not connect to VCC pin. |
| 4 | PGOOD | Open-Drain Power Good Indicator Output. |
| 5 | CLK | 300kHz Clock Output to Drive the External Charge Pump. |
| 6 | LDO | 5V Linear Regulator Output. Decouple with a minimum 4.7μF ceramic capacitor. |
| 7 | VOUT | Output Voltage Sense Input. An internal discharging circuit is connected to this pin. |
| 8, 9, 15, 16 | SW | Switch Node. |
| 10 | BOOT | Bootstrap Supply for High-Side Gate Driver. A capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BOOT pins to form a floating supply across the power switch driver. |
| 11 | VCC | 5V Linear Regulator Output for Internal Control Circuit. A capacitor (typical 2.2μF) should be connected to AGND. $V_{CC}$ can only supply internal circuits. Do not connect to external loads. |
| 12 | ENLDO | Enable Control Input for Linear Regulator. This pin is internally pulled up to high by 10μA. |
| 13 | EN | Enable Control Input. Do not leave this pin floating. |
| 14 | AGND | Analog Ground. |

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## Function Block Diagram




## Operation

### Overall

The RT7291A/B is a synchronous step-down converter with advanced constant on-time control mode. Using the ACOT™ control mode can reduce the output capacitance and provide fast transient response. It can minimize the component size without additional external compensation network.

### Internal VCC Regulator

The regulator provides 5V power to supply the internal control circuit. Connecting a 2.2µF ceramic capacitor for decoupling and stability is required.

### Soft-Start

In order to prevent the converter output voltage from overshooting during the startup period, the soft-start function is necessary. The soft-start time is internal setting and the duration is around 1.5ms

### OCP

The inductor valley current is monitored via the internal switches in cycle-by-cycle. Once the output voltage drops below UV threshold, the device enters latch mode.

### Power Good

After soft-start is finished, the power good function will be activated. The PGOOD pin is an open-drain output.

### CLK Generator

Provide a 300kHz clock to drive external charge pump.

### VCC Switch-Over

The internal regulator output will switch over to VBYP if VBYP level is higher than 4.6V.

### LDO

Built-in 5V, 100mA LDO with 1% accuracy. The LDO output will switch over to VOUT once PGOOD goes high.

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## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 27V
- Switch Voltage, SW ---------- –0.3V to ($V_{IN}$ + 0.3V)
  <30ns ---------- –5V to 28V
- BOOT Switch Voltage ---------- ($V_{SW}$ – 0.3V) to ($V_{SW}$ + 6V)
- EN, ENLDO Pin Voltages ---------- –0.3V to 27V
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  UQFN-16L 3x3 (FC) ---------- 1.4W
- Package Thermal Resistance (Note 2)
  UQFN-16L 3x3 (FC), $\theta_{JA}$ ---------- 70°C/W
  UQFN-16L 3x3 (FC), $\theta_{JC}$ ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 5V to 23V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| Shutdown Current | | $V_{EN}$ = $V_{ENLDO}$ = 0V | -- | 2.5 | 5 | μA |
| Quiescent Current | | $V_{EN}$ = 2V, $V_{ENLDO}$ = 2V, No Switching | -- | 100 | 130 | μA |
| Standby Current | | $V_{EN}$ = 0V, $V_{ENLDO}$ = 2V, LDO Load Current = 0A | -- | 35 | 45 | μA |
| **Switch On-Resistance** | | | | | | |
| Switch On-Resistance | $R_{DS(ON)_H}$ | $V_{BOOT}$ – $V_{SW}$ = 5V | -- | 31 | -- | mΩ |
| | $R_{DS(ON)_L}$ | | -- | 20 | -- | |
| **Current Limit** | | | | | | |
| Current Limit | $I_{OC}$ | Valley current of low-side switch | 7.6 | -- | 11.4 | A |
| **Switching Frequency and Minimum Off Timer** | | | | | | |
| Switching Frequency | $f_{SW}$ | | 450 | 500 | 550 | kHz |
| Minimum Off-Time | $T_{OFF}$ | | -- | 200 | -- | ns |
| **Protections** | | | | | | |
| OVP Trip Threshold | $V_{OVP}$ | With respect to output voltage | 115 | 120 | 125 | % |
| OVP Propagation Delay | $T_{OVPDLY}$ | | -- | 5 | -- | μs |

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| Parameter | | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| UVP Trip Threshold | | $V_{UVP}$ | With respect to output voltage | | 55 | 60 | 65 | % |
| UVP Propagation Delay | | $T_{UVPDLY}$ | | | -- | 5 | -- | μs |
| **Reference and Soft-Start** | | | | | | | | |
| Output Voltage Valley | | $V_{OUT}$ | RT7291A | | 4.95 | 5 | 5.05 | V |
| | | | RT7291B | | 5.049 | 5.1 | 5.151 | |
| Soft-Start Time | | $T_{SS}$ | From EN high to PGOOD high | | 1 | 1.5 | 2 | ms |
| **Enable and UVLO** | | | | | | | | |
| EN Input High Voltage | | $V_{ENH}$ | RT7291A | | 1.25 | 1.35 | 1.45 | V |
| | | | RT7291B | | 1.3 | 1.4 | 1.5 | |
| EN Hysteresis | | $V_{ENHYS}$ | | | -- | 200 | -- | mV |
| EN Input Current | | $I_{EN}$ | $V_{EN}$ = 2V | | -- | 1 | -- | μA |
| | | | $V_{EN}$ = 0V | | -- | 0 | -- | |
| VCC UVLO Rising | | $V_{CCUVLO}$ | | | -- | 4.2 | -- | V |
| VCC UVLO Hysteresis | | $V_{CCHYS}$ | | | -- | 400 | -- | mV |
| **CLK Output** | | | | | | | | |
| CLK Output Voltage | High-Level | $V_{CLKH}$ | $I_{VCLK}$ = −10mA | RT7291A | -- | -- | 5.05 | V |
| | | | | RT7291B | -- | -- | 5.151 | |
| | Low-Level | $V_{CLKL}$ | $I_{VCLK}$ = 10mA | | 0 | 0.1 | 0.2 | |
| CLK Frequency | | $f_{CLK}$ | | | -- | 300 | -- | kHz |
| **LDO Regulator** | | | | | | | | |
| LDO Regulator | | $V_{LDO}$ | RT7291A | | 4.95 | 5 | 5.05 | V |
| | | | RT7291B | | 5.049 | 5.1 | 5.151 | |
| LDO Load Regulation | | | EN = GND, LDO Load Current = 5mA | | -- | 1 | -- | % |
| | | | EN = GND, LDO Load Current = 100mA | | -- | 5 | -- | |
| Switch On-Resistance | | $R_{SW}$ | | | -- | 3 | 5 | Ω |
| **VCC Regulator** | | | | | | | | |
| VCC Regulator | | $V_{VCC}$ | RT7291A | | 4.805 | 5 | 5.295 | V |
| | | | RT7291B | | 4.905 | 5.1 | 5.395 | |
| VCC Switch Over Threshold to VBYP | | | $V_{BYP}$ Rising Edge | RT7291A | 4.45 | 4.6 | 4.75 | V |
| | | | | RT7291B | 4.542 | 4.692 | 4.842 | |
| VCC Switch Over Hysteresis | | | $V_{BYP}$ Falling Edge | | -- | 200 | -- | mV |
| Switch Over On-Resistance | | | | | -- | 3 | 5 | Ω |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Good Indicator** | | | | | | |
| PGOOD Threshold From Lower | | $V_{OUT}$ Rising | 85 | 90 | 95 | % |
| PGOOD Low Hysteresis | | $V_{OUT}$ Falling | -- | –10 | -- | % |
| PGOOD Low to High Delay | $T_{PGDLY}$ | | -- | 0.5 | -- | ms |
| PGOOD Sink Current Capability | $V_{PGSINK}$ | Sink 4mA | -- | -- | 0.4 | V |
| PGOOD Leakage Current | $I_{PGLEAK}$ | $V_{PGOOD}$ = 5V | -- | -- | 100 | nA |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold | $T_{SD}$ | | 135 | 150 | -- | °C |
| Thermal Shutdown Hysteresis | | | -- | 25 | -- | °C |

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

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## Typical Application Circuit

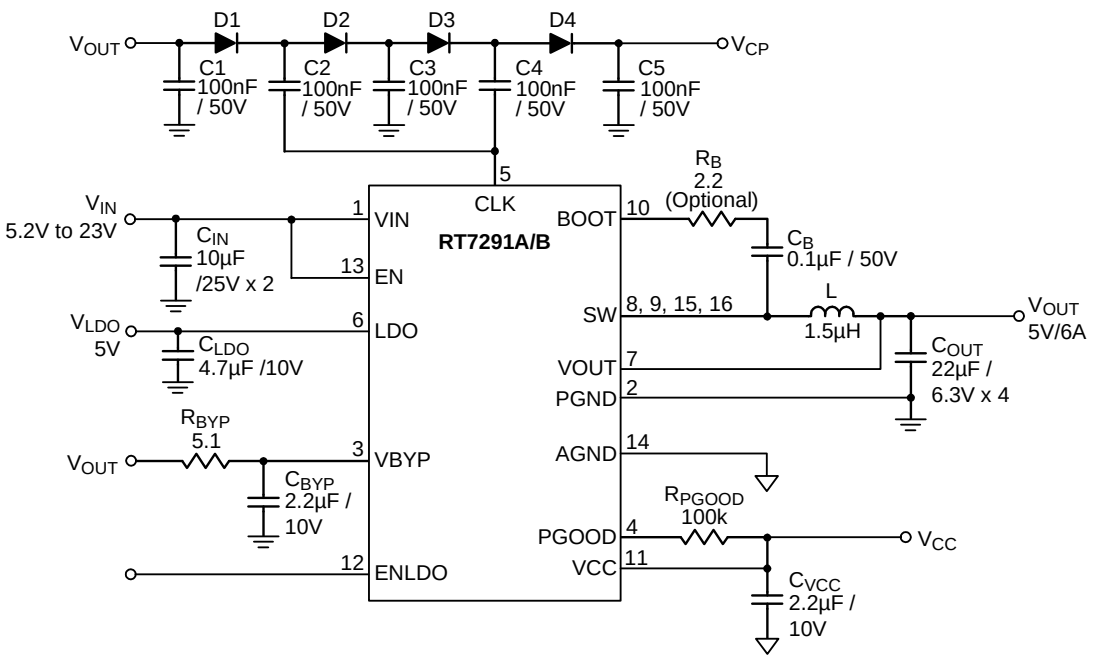
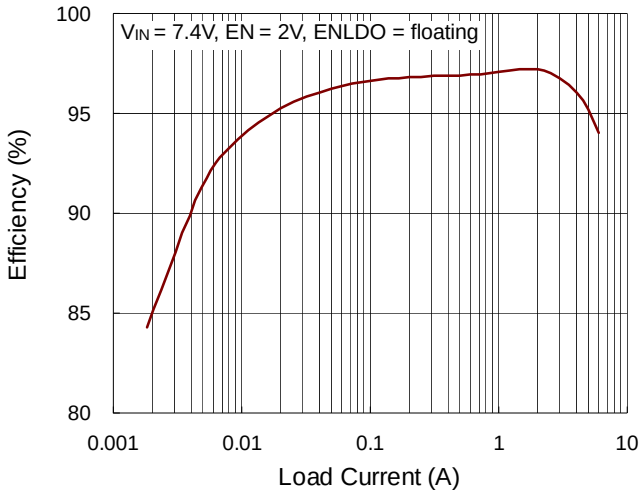



Figure 1. Typical Application Circuit with Pure MLCC Solution

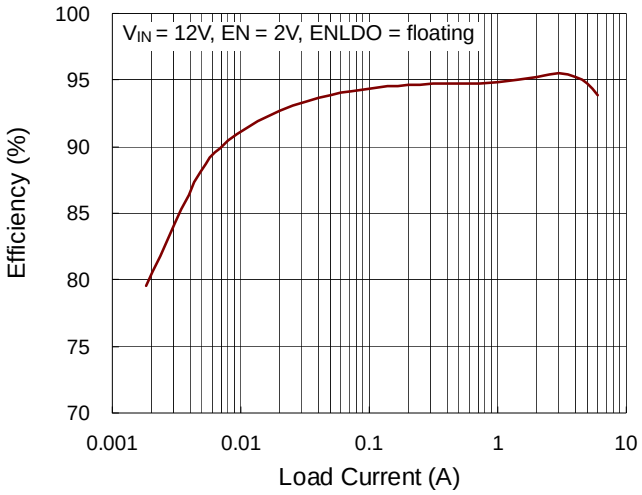
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## Typical Operating Characteristics

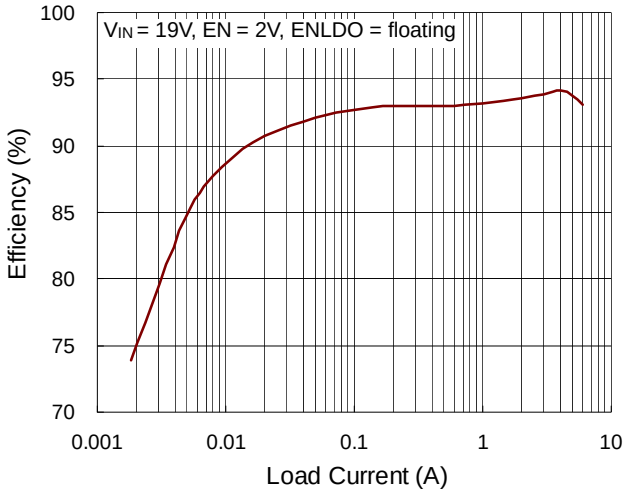
**Efficiency vs. Load Current**



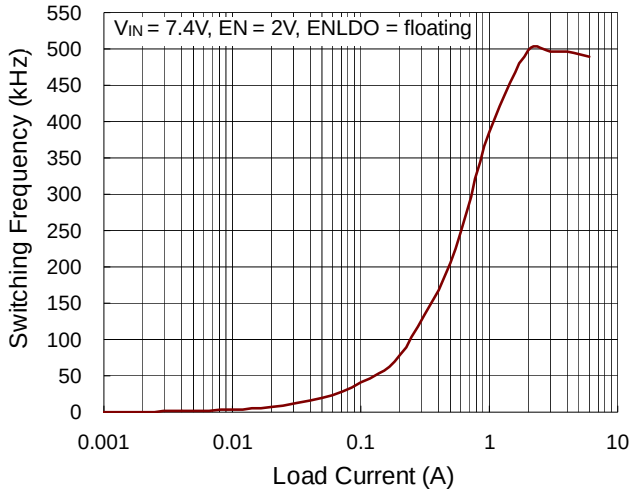

**Efficiency vs. Load Current**



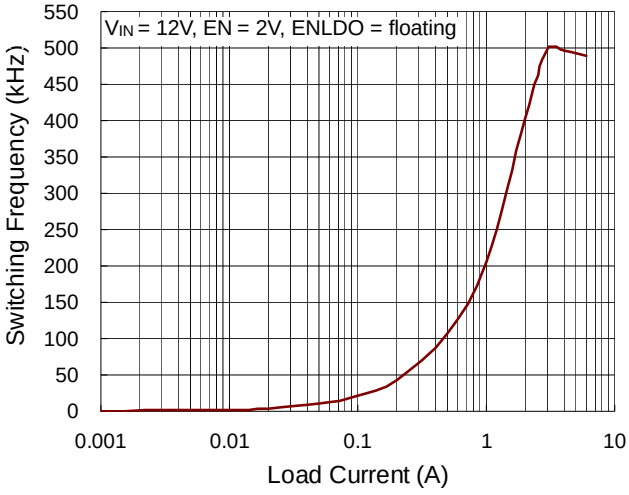

**Efficiency vs. Load Current**



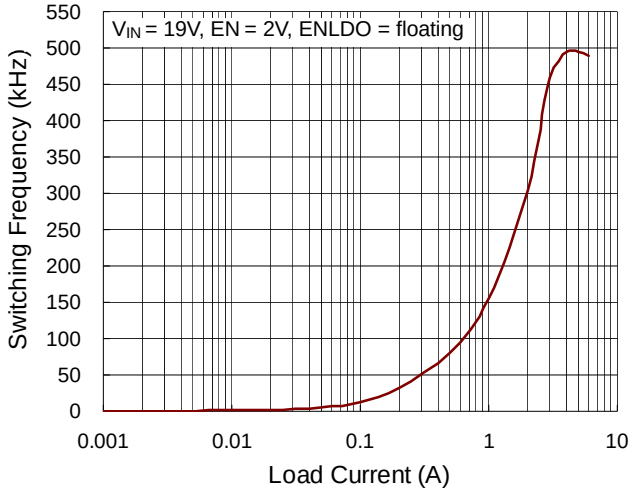

**Switching Frequency vs. Load Current**




**Switching Frequency vs. Load Current**

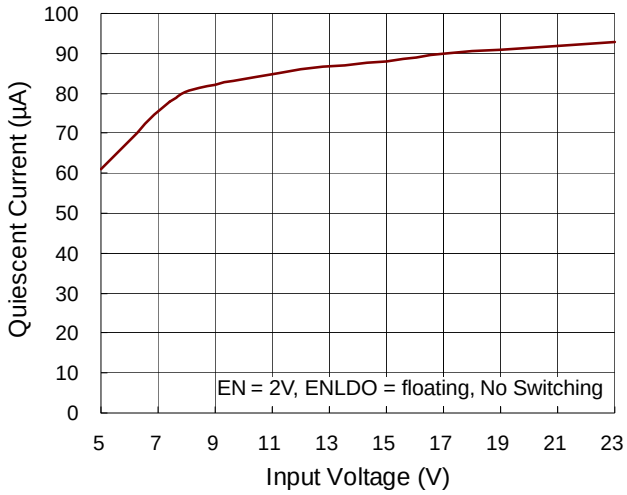



**Switching Frequency vs. Load Current**

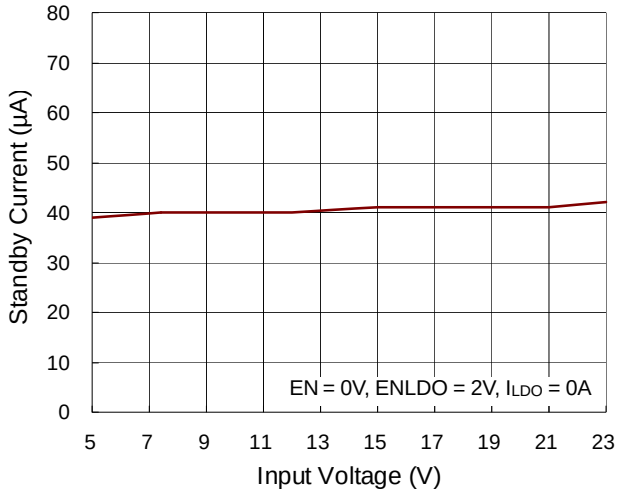



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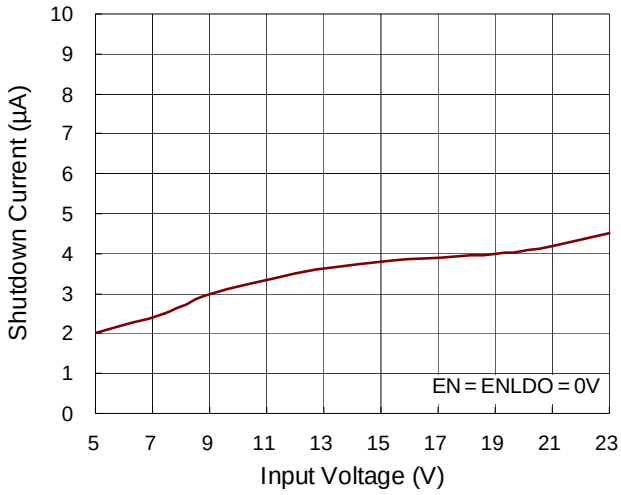
### Quiescent Current vs. Input Voltage



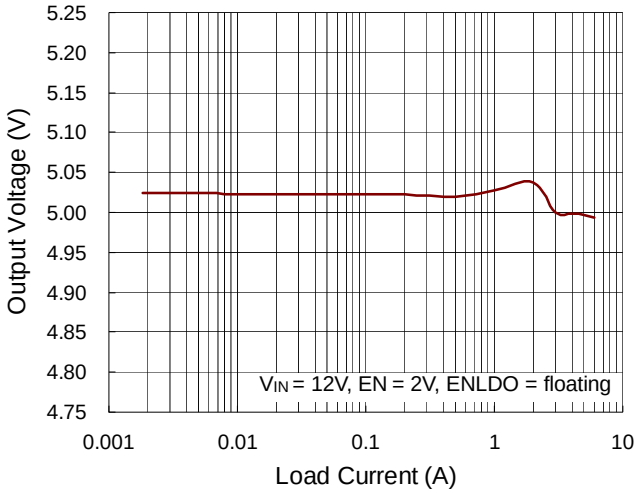

### Standby Current vs. Input Voltage



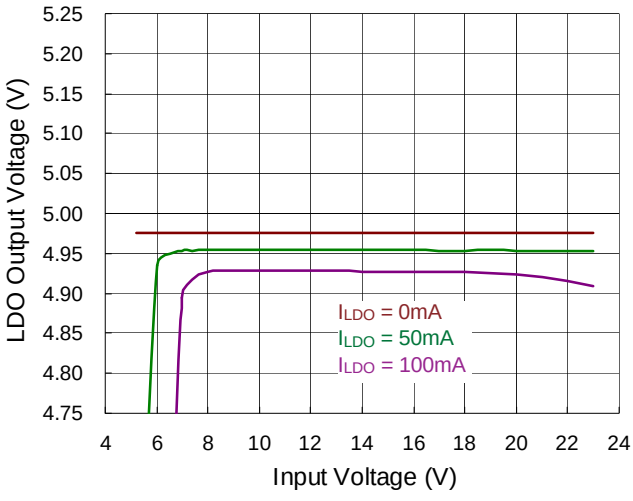

### Shutdown Current vs. Input Voltage



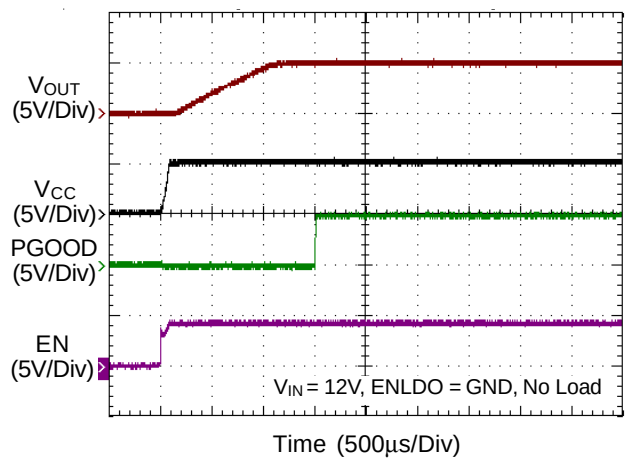

### Output Voltage vs. Load Current




### LDO Output Voltage vs. Input Voltage

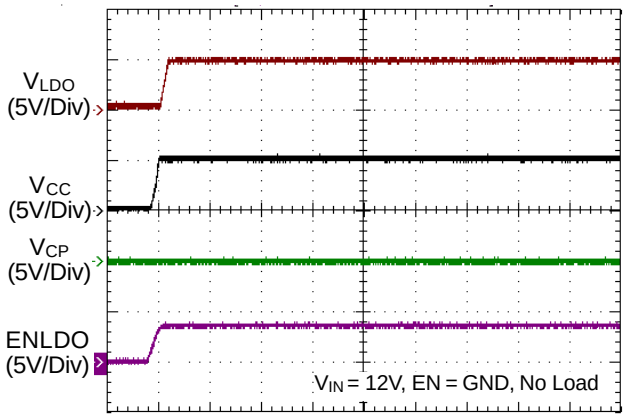



### Start Up Through EN

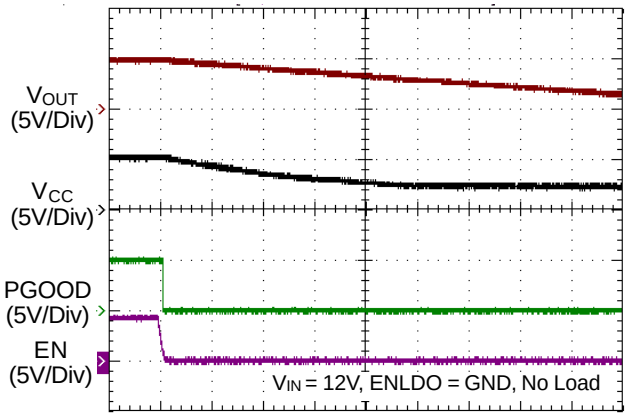



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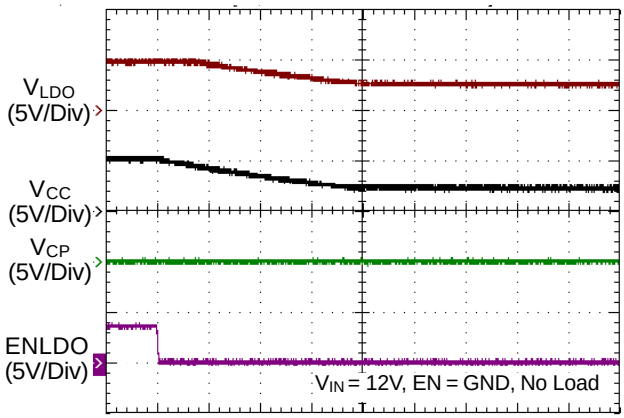
### Start Up Through ENLDO



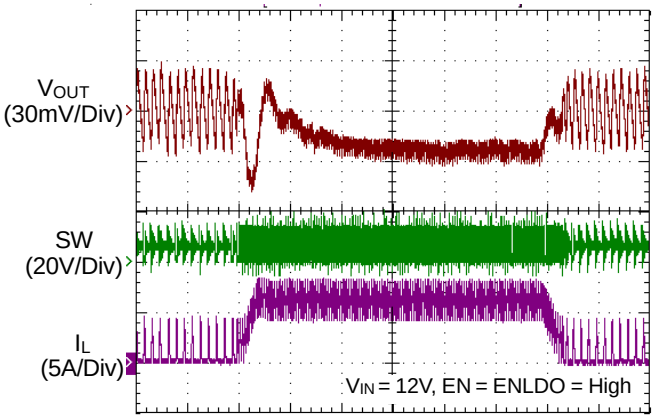

### Power Off Through EN



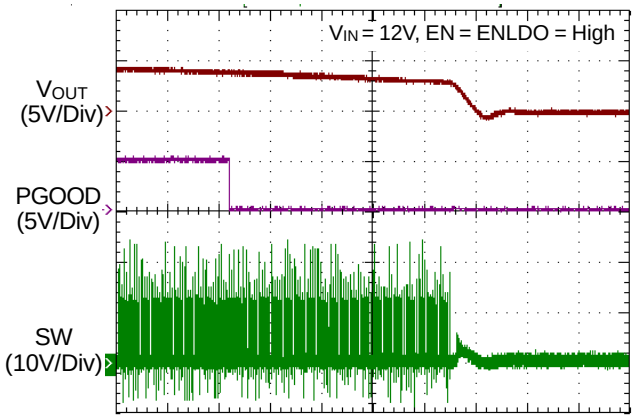

### Power Off Through ENLDO



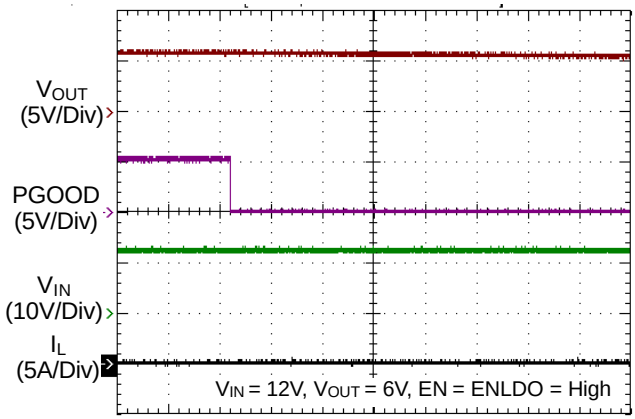

### Load Transient Response




### UVP




### OVP




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## Application Information

The RT7291A/B is high-performance 500kHz 6A step-down regulators with internal power switches and synchronous rectifiers. It features an Advanced Constant On-Time (ACOT™) control architecture that provides stable operation for ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 5V to 23V, and the output voltage is fixed 5V.

The proprietary ACOT™ control scheme improves conventional constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

### ACOT™ Control Architecture

In order to achieve good stability with low-ESR ceramic capacitors, ACOT™ uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

Making the on-time proportional to $V_{OUT}$ and inversely proportional to $V_{IN}$ is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage as sensing input and output voltage. When the load changes, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on-time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. The ACOT™ uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

### ACOT™ One-shot Operation

The RT7291A/B control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (200ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

### Diode Emulation Mode

In diode emulation mode, the RT7291A/B automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy load conditions, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the

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inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 2 and can be calculated as follows :

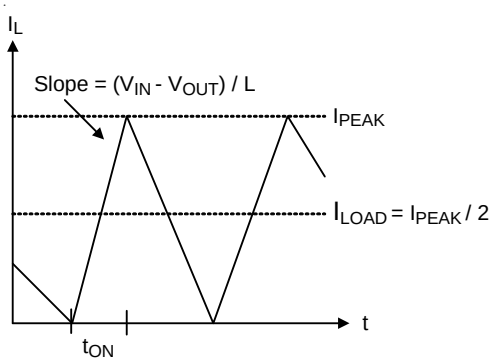



Figure 2. Boundary Condition of CCM/DEM

$$I_{LOAD} = \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where $t_{ON}$ is the on-time.

The switching waveforms may appear noisy and asynchronous when light load causes diode emulation operation. This is normal and results in high efficiency. Trade offs in DEM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

During discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially. The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for 500kHz switching and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

### Linear Regulators (LDO & VCC)

The RT7291A/B includes a 5V linear regulator (LDO). The LDO regulator can supply up to 100mA for external loads. Bypass LDO with a minimum 4.7μF ceramic capacitor. When VOUT is powered on and PGOOD is pulled high, an internal 3Ω P-MOSFET switch connects $V_{OUT}$ to the LDO pin while the internal linear regulator is simultaneously turned off.

The RT7291A/B also includes a 5V linear regulator (VCC). The VCC regulator steps down input voltage to supply both internal circuitry and gate drivers. Do not connect the VCC pin to external loads. When PGOOD is pulled high and BYP pin voltage is above 4.6V, an internal 3Ω P-MOSFET switch connects $V_{CC}$ to the BYP pin while the VCC linear regulator is simultaneously turned off.

### Current Limit

The RT7291A/B current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between Source and Drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the current limit, the on-time one-shot is inhibited until the inductor current ramps down below the current limit. Thus, only when the inductor current is well below the current limit, another on-time is permitted. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level (see next section), the IC will stop switching to avoid excessive heat.

The RT7291A/B also features a negative current limit to protect the IC against sinking excessive current and possibly damage. If the voltage across the synchronous rectifier indicates the negative current is too high, the synchronous rectifier turns off.

### Output Over-Voltage Protection and Under-Voltage Protection

The RT7291A/B features an output Over-Voltage Protection (OVP). If the output voltage rises above the regulation level, the IC stops switching and is latched off. The RT7291A/B also features an output Under-Voltage Protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 2μs (typical), the UVP

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is triggered, and the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle EN or power the IC off and then on again.

### Input Under-Voltage Lockout

In addition to the enable function, the RT7291A/B features an Under-Voltage Lockout (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

### Over-Temperature Protection

The RT7291A/B features an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP shuts down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 25°C the IC resumes normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C. Note that the VCC and LDO regulator remains on as the OTP is triggered.

### Enable and Disable

The enable input (EN) has a logic-low level of 1.15V. When $V_{EN}$ is below this level, the IC enters shutdown mode and supply current drops to less than 5μA (typical). When $V_{EN}$ exceeds its logic-high level of 1.35V, the IC is fully operational. The logics of EN and ENLDO to control the $V_{OUT}$, CLK, LDO and VCC are stated in Table 1.

**Table 1. EN/ENLDO Control Logics**

| EN | ENLDO | VOUT/CLK | LDO | VCC |
|---|---|---|---|---|
| 1 | 1 | ON | ON | ON |
| 1 | 0 | ON | ON | ON |
| 0 | 1 | OFF | ON | ON |
| 0 | 0 | OFF | OFF | OFF |

### Soft-Start

The RT7291A/B provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramp of internal reference voltage which is compared with FB signal. The typical soft-start duration is 1.5ms.

### Power Off

When $V_{EN}$ is pulled to GND or lower than the logic-low level of 1.15V, there is an internal discharging resistor to discharge the residual charge inside the output capacitors. Besides, the value of discharging resistor is about twenty ohms.

### Power Good Output (PGOOD)

The power good output is an open-drain output that requires a pull-up resistor. When the output voltage is 20% (typical) below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to 90% of its set voltage once more. During soft-start, PGOOD is actively held low and only allowed to be pulled high after soft-start is over and the output reaches 90% of its set voltage. There is a 2μs delay built into PGOOD circuitry to prevent false transition.

### External Bootstrap Capacitor ($C_{BOOT}$)

Connect a 0.22μF low ESR ceramic capacitor between the BOOT and SW pins. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-MOSFET switch.

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, and slow enough to reduce EMI. Switch turn-on is when most EMI occurs since $V_{SW}$ rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead-time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<10Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and $V_{SW}$'s rise.

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### Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response. However, they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current ($\Delta I_L$) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency ($f_{SW}$), the maximum output current ($I_{OUT(MAX)}$) and estimating a $\Delta I_L$ as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current ($\Delta I_L$) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, it will probably give fewer EMI and other noise problems.

### Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20µF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability. Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[ (1 - \frac{V_{OUT}}{V_{IN}}) \times {I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12} \right]}$$

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{IN}}{C_{IN} \times f_{SW} \times V_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The typical operating circuit is recommended to use two 10µF low ESR ceramic capacitors on the input.

### Output Capacitor Selection

The RT7291A/B is optimized for ceramic output capacitors and best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

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$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 500kHz switching frequency. However, some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} \times t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increases compensations for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Most applications never experience instantaneous full load steps and the RT7291A/B's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that over-voltage protection and under-voltage protection will not be triggered.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For UQFN-16L 3x3 (FC) package, the thermal resistance, $\theta_{JA}$, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.4W for UQFN-16L 3x3 (FC) package

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The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

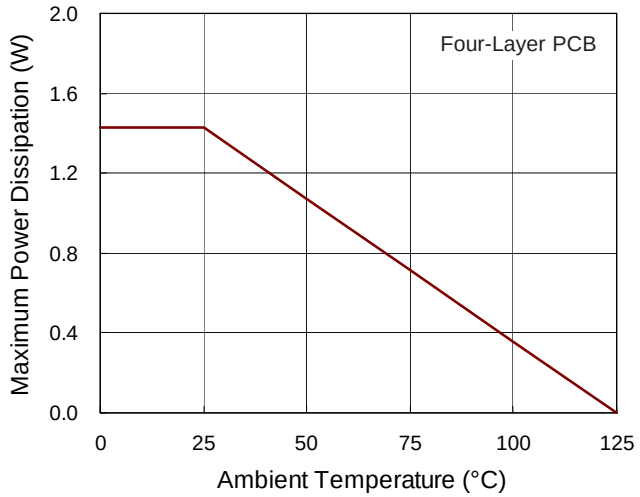



Figure 3. Derating Curve of Maximum Power Dissipation

**Layout Considerations**

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT7291A/B.

- Make traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and PGND).
- SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent stray.
- The PGND pin should be connected to a strong ground plane for heat sinking and noise protection.
- Avoid using vias in the power path connections that have switched currents (from $C_{IN}$ to PGND and $C_{IN}$ to $V_{IN}$) and the switching node (SW).

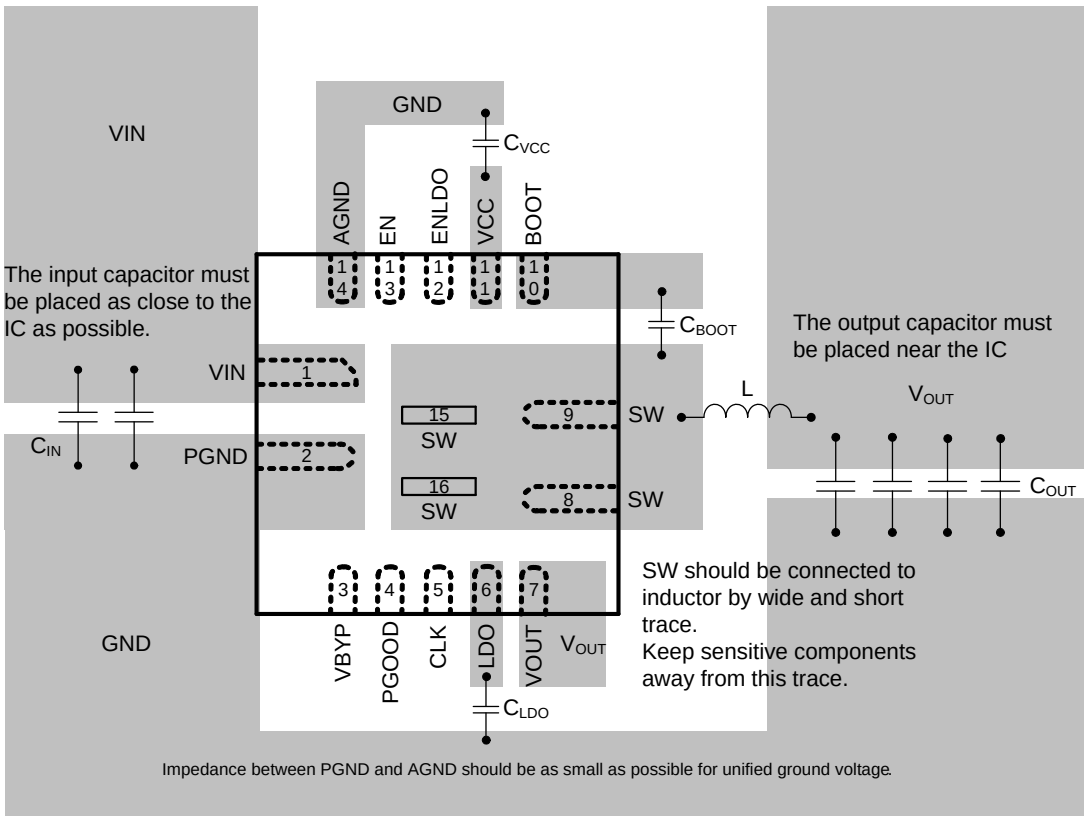
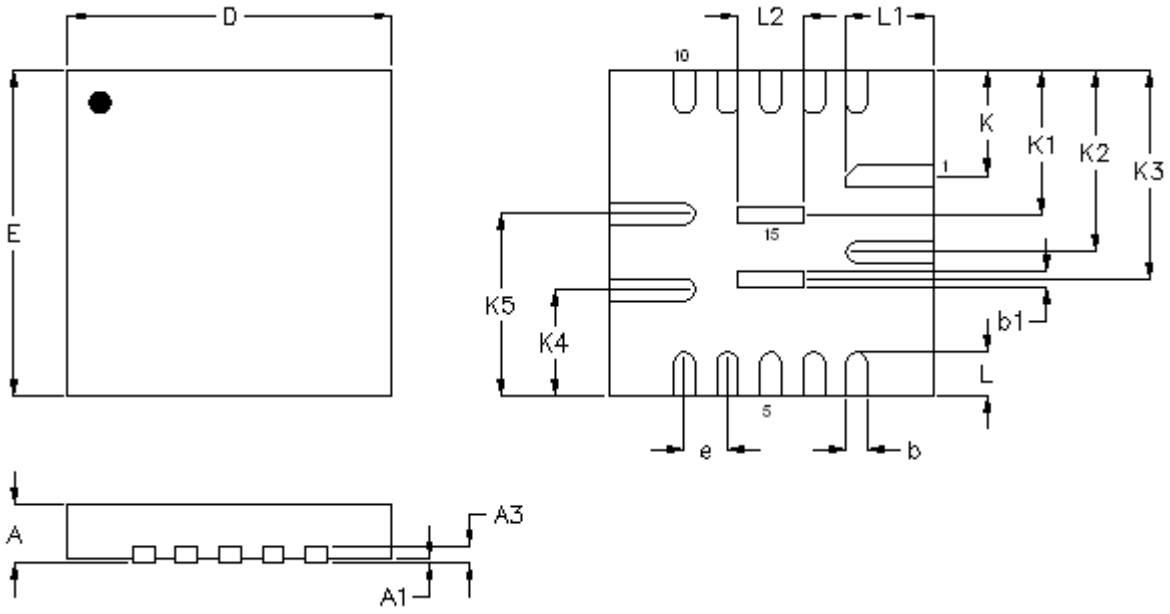



Figure 4. Layout Guide

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## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.100 | 0.175 | 0.004 | 0.007 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| b1 | 0.100 | 0.200 | 0.004 | 0.008 |
| L | 0.350 | 0.450 | 0.014 | 0.018 |
| L1 | 0.750 | 0.850 | 0.030 | 0.033 |
| L2 | 0.550 | 0.650 | 0.022 | 0.026 |
| e | 0.400 | | 0.016 | |
| K | 0.975 | | 0.038 | |
| K1 | 1.335 | | 0.053 | |
| K2 | 1.675 | | 0.066 | |
| K3 | 1.935 | | 0.076 | |
| K4 | 0.975 | | 0.038 | |
| K5 | 1.675 | | 0.066 | |

**U-Type 16L QFN 3x3 (FC) Package**

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