LOW SKEW, DUAL, 1-TO-2 DIFFERENTIAL-TO-LVDS, LVPECL FANOUT BUFFER

ICS854S204I

General Description

The ICS854S204I is a low skew, high performance dual, 1-to-2 Differential-to-LVDS, LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLKx, nCLKx pairs can accept most standard differential input levels. The ICS854S204I is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and bank skew characteristics make the ICS854S204I ideal for those clock distribution applications demanding well defined performance and repeatability.

Features

- Two differential LVDS or LVPECL output banks
- Two differential clock input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: >3GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nCLKx inputs
- Output skew: <25ps (typical) design target
- Bank skew: <50ps (typical) design target
- Propagation delay: TBD
- Additive phase jitter, RMS: 0.15ps (typical)
- Full 3.3V or 2.5V power supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

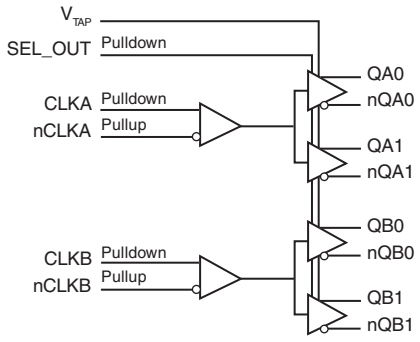
Supply Mode Operation Table

3.3V Operation	2.5V Operation
V_{DD} = 3.3V	V_{DD} = 2.5V
V_{TAP} = nc	V_{TAP} = 2.5V

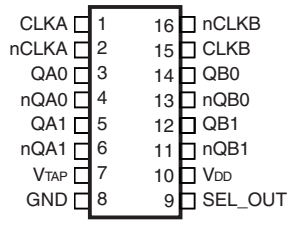
SEL_OUT Function Table

SEL_OUT	Output Level
0	LVDS
1	LVPECL

Block Diagram



Pin Assignment



ICS854S204I
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLKA	Input	Pulldown	Non-inverting differential clock input.
2	nCLKA	Input	Pullup	Inverting differential clock input.
3, 4	QA0, nQA0	Output		Differential output pair. LVDS or LVPECL interface levels.
5, 6	QA1, nQA1	Output		Differential output pair. LVDS or LVPECL interface levels.
7	V_{TAP}	Power		Power supply pin. Tie to V_{DD} for 2.5V operation.
8	GND	Power		Power supply ground.
9	SEL_OUT	Input	Pulldown	Selects between LVDS or LVPECL outputs.
10	V_{DD}	Power		Power supply pin.
11, 12	nQB1, QB1	Output		Differential output pair. LVDS or LVPECL interface levels.
13, 14	nQB0, QB0	Output		Differential output pair. LVDS or LVPECL interface levels.
15	CLKB	Input	Pulldown	Non-inverting differential clock input.
16	nCLKB	Input	Pullup	Inverting differential clock input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLKA or CLKB	nCLKA or nCLKB	QA0, QA1, QB0, QB1	nQA0, nQA1, nQB0, nQB1		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			100		mA

Table 4B. LVDS Power Supply DC Characteristics, V_{DD} = V_{TAP} = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			95		mA
I_{TAP}	Power Supply Current			5		mA

Table 4C. LVPECL Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			100		mA

Table 4D. LVPECL Power Supply DC Characteristics, V_{DD} = V_{TAP} = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			95		mA
I_{TAP}	Power Supply Current			5		mA

TABLE 4E. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR $V_{DD} = V_{TAP}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{CC} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL_OUT	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL_OUT	V_{DD} = 3.465 or 2.625V, V_{IN} = 0V	-5			µA

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR $V_{DD} = V_{TAP}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKA, CLKB	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		nCLKA, nCLKB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V			5	µA
I_{IL}	Input Low Current	CLKA, CLKB	$V_{DD} = V_{IN}$ = 3.465V or 2.625V	-5			µA
		nCLKA, nCLKB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.

TABLE 4G. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0		400		mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0		40		mV
V_{OS}	Offset Voltage	SEL_OUT = 0		1.35		V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0		50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4H. LVDS DC CHARACTERISTICS, $V_{DD} = V_{TAP}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0		370		mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0		40		mV
V_{OS}	Offset Voltage	SEL_OUT = 0		1.3		V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0		50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4I. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR $V_{DD} = V_{TAP}$ = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1	SEL_OUT = 1	V_{DD} - 1.4		V_{DD} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1	SEL_OUT = 1	V_{DD} - 2.0		V_{DD} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	SEL_OUT = 1	0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{DD} - 2V.

TABLE 5A. LVDS AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>3	GHz
t_{PD}	Propagation Delay; NOTE 1			TBD		ns
*t*sk(o)	Output Skew; NOTE 2, 4			<25 target		ps
*t*sk(b)	Bank Skew; NOTE 3, 4			<50 target		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section			0.15		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		250		ps
odc	Output Duty Cycle			50		%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. LVDS AC CHARACTERISTICS, $V_{DD} = V_{TAP}$ = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>3	GHz
t_{PD}	Propagation Delay; NOTE 1			TBD		ns
*t*sk(o)	Output Skew; NOTE 2, 4			<25 target		ps
*t*sk(b)	Bank Skew; NOTE 3, 4			<50 target		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section			0.13		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		250		ps
odc	Output Duty Cycle			50		%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. LVPECL AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>3	GHz
t_{PD}	Propagation Delay; NOTE 1			TBD		ns
*t*sk(o)	Output Skew; NOTE 2, 4			<25 target		ps
*t*sk(b)	Bank Skew; NOTE 3, 4			<50 target		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section			0.12		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		250		ps
odc	Output Duty Cycle			50		%

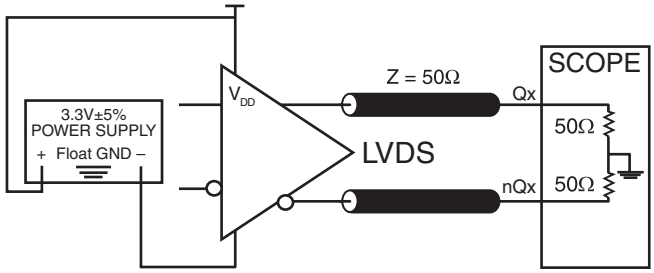
All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5D. LVPECL AC CHARACTERISTICS, V_{DD} = V_{TAP} = 2.5V ± 5%, T_A = -40°C TO 85°C

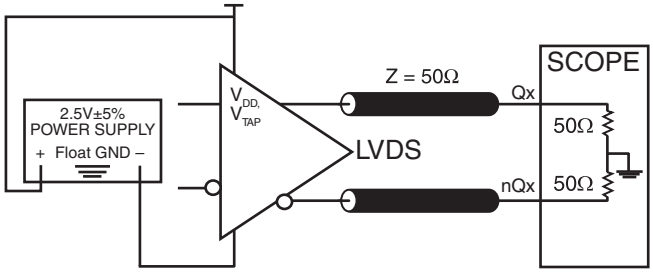
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>3	GHz
t_{PD}	Propagation Delay; NOTE 1			TBD		ns
*t*sk(o)	Output Skew; NOTE 2, 4			<25 target		ps
*t*sk(b)	Bank Skew; NOTE 3, 4			<50 target		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section			0.07		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		250		ps
odc	Output Duty Cycle			50		%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

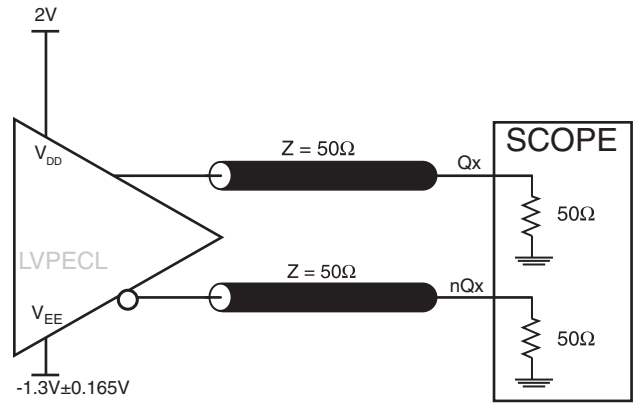
PARAMETER MEASUREMENT INFORMATION



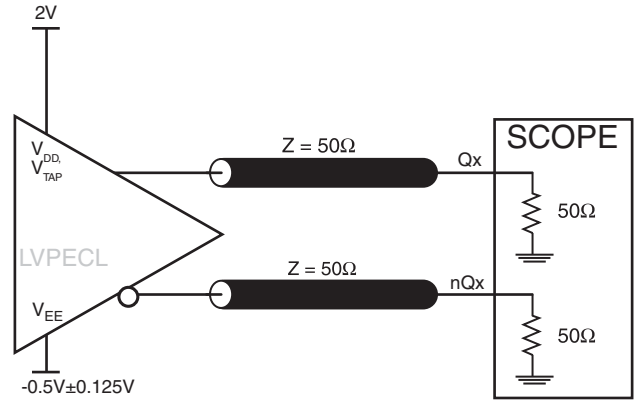
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



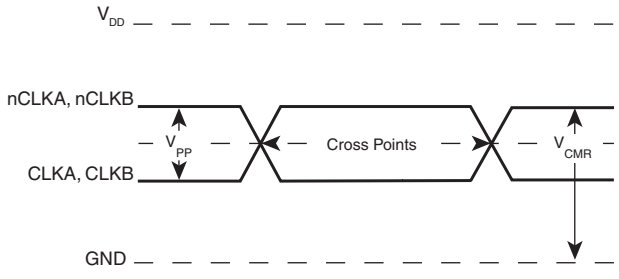
2.5V LVDS OUTPUT LOAD AC TEST CIRCUIT



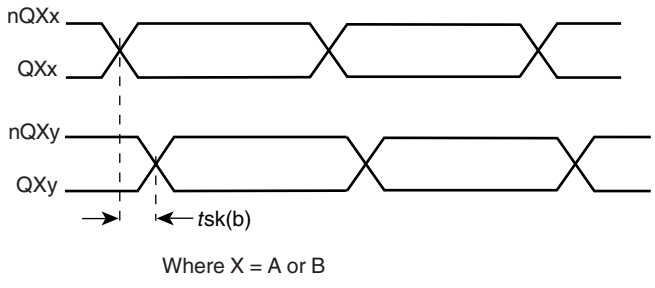
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



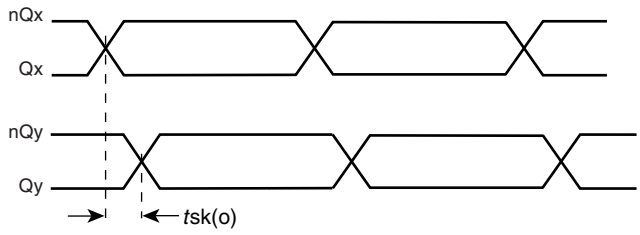
2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



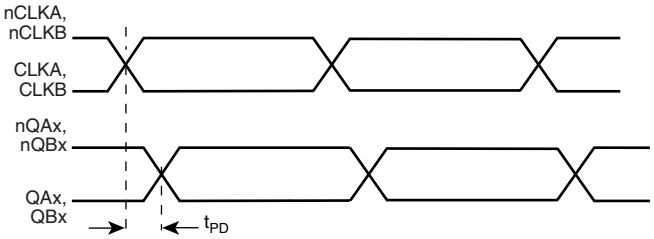
DIFFERENTIAL INPUT LEVEL



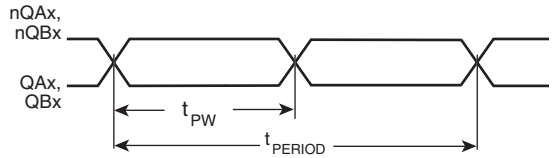
BANK SKEW



OUTPUT SKEW

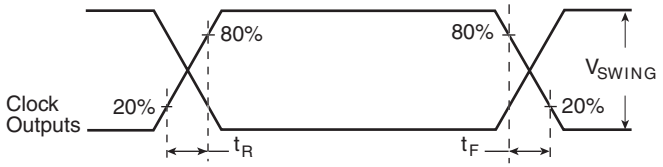


PROPAGATION DELAY

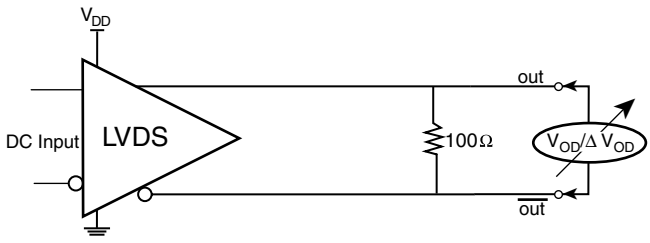


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

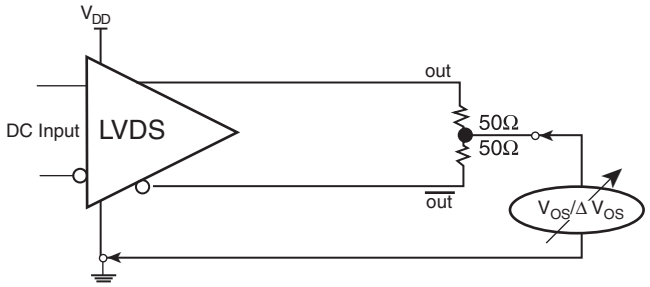
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

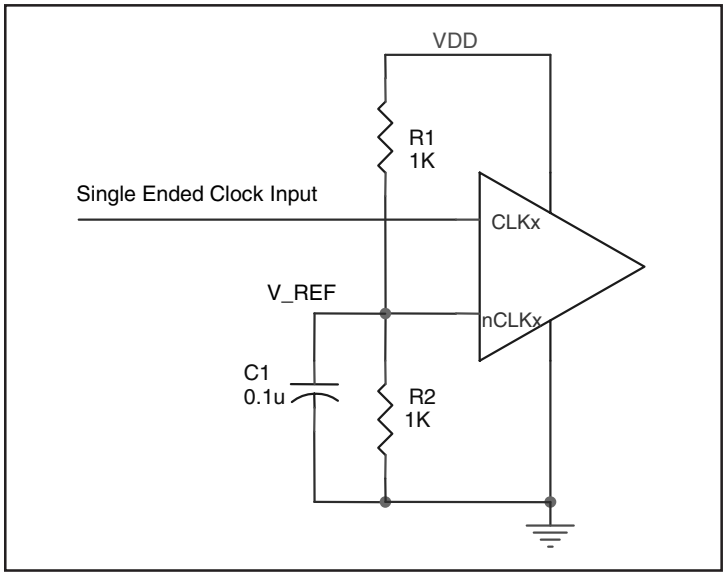


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUT:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

OUTPUTS:

LVDS OUTPUT
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

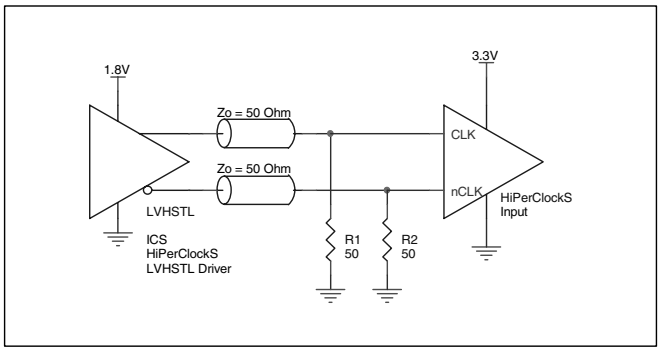


Figure 2A. HiPerClockS CLK/nCLK Input Driven by ICS HiPerClockS LVHSTL Driver

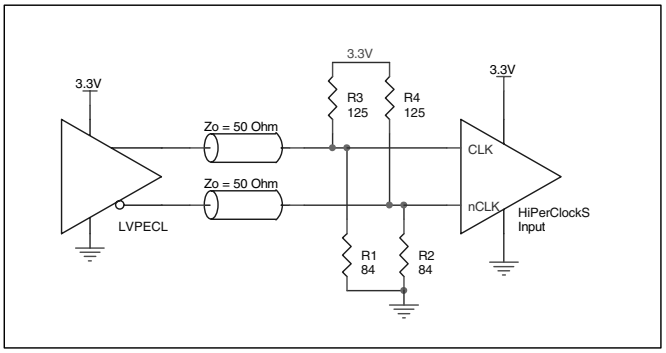


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

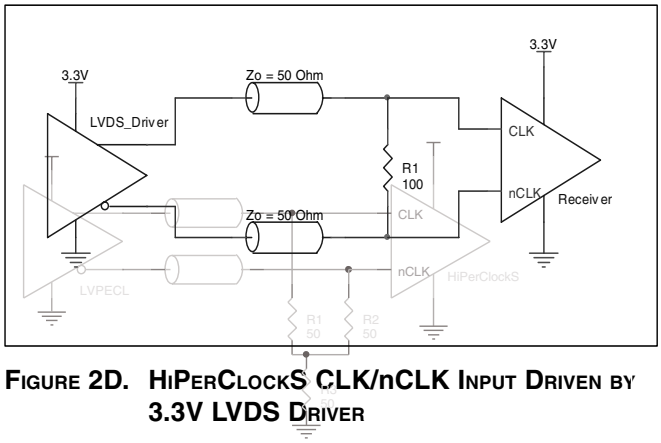


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

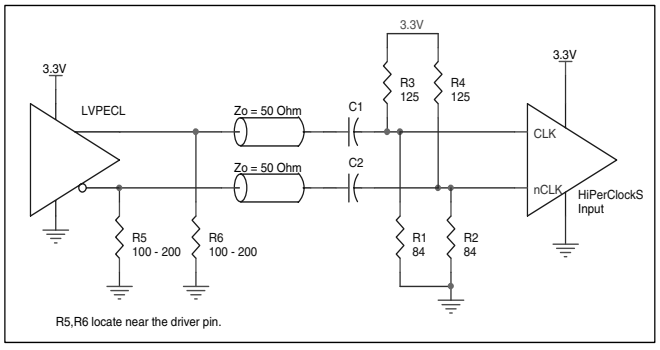


Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

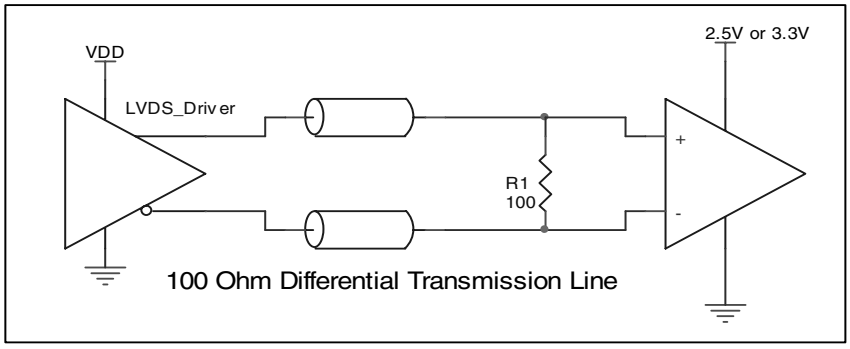


Figure 3. Typical LVDS Driver Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

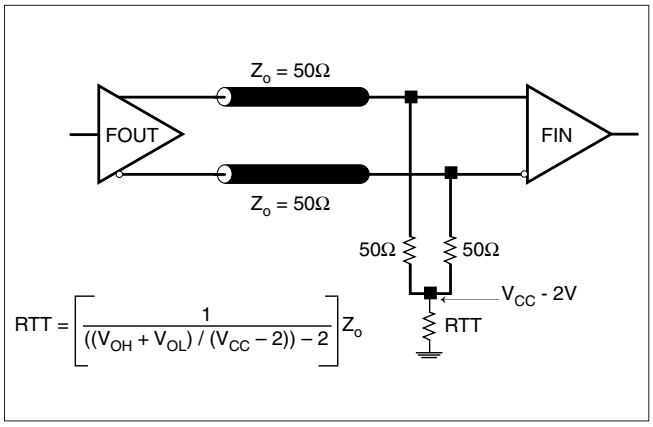


Figure 4A. LVPECL Output Termination

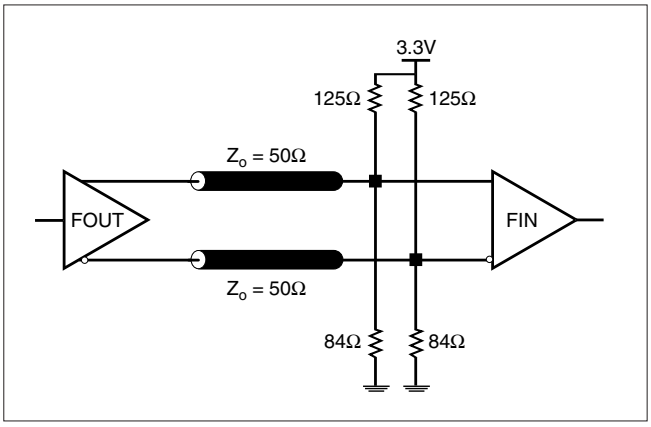


Figure 4B. LVPECL Output Termination

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

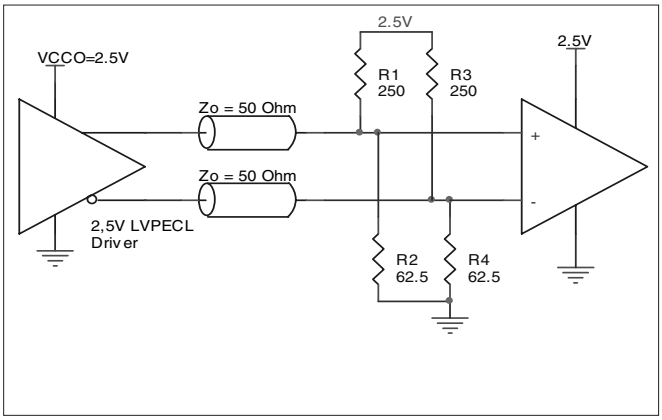


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

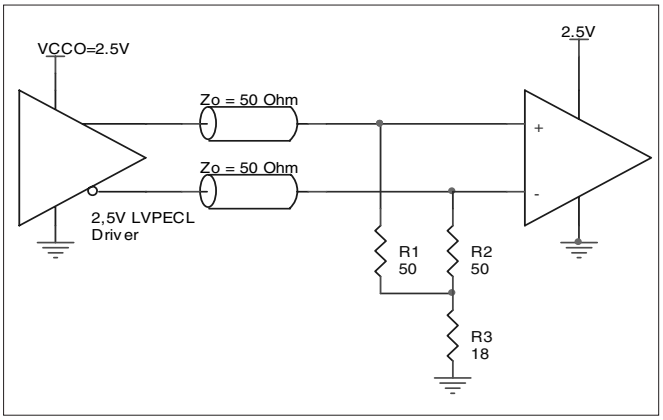


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

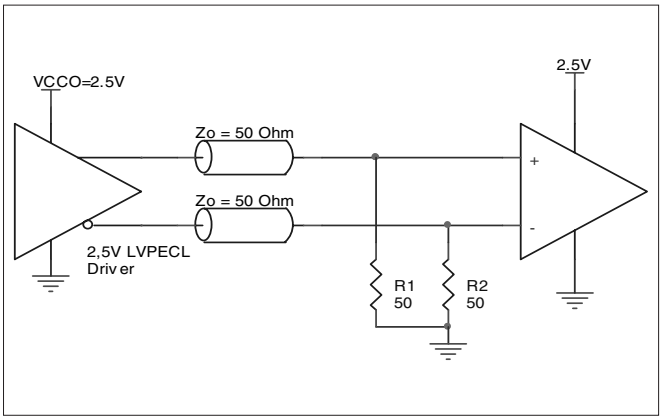


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS854S204I is: 454

Package Outline - G Suffix for 16 Lead TSSOP

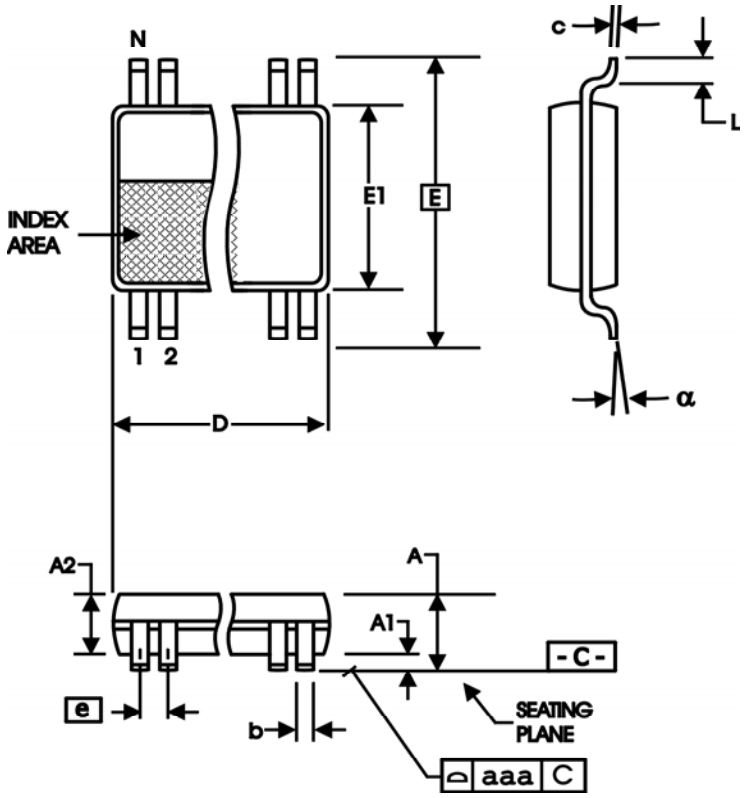


Table 7. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854S204AGI	54S204AI	16 lead TSSOP	tube	-40°C to 85°C
ICS854S204AGIT	54S204AI	16 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS854S204AGILF	4S204AIL	16 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS854S204AGILFT	4S204AIL	16 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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For Sales
800-345-7015
408-284-8200
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For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com

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