P-Channel Enhancement Mode MOSFET

MTP5103N3

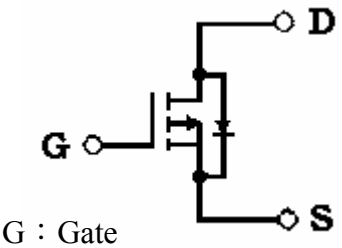
BV_{DSS}		-30V
I_D		-4.5A
$R_{DSON(TYP)}$	V_{GS}=-10V, I_D=-4.5A	41mΩ
	V_{GS}=-4.5V, I_D=-3.5A	60mΩ

Features

- Low gate charge
- Compact and low profile SOT-23 package
- Advanced trench process technology
- High density cell design for ultra low on resistance
- Pb-free lead plating and halogen-free package

Equivalent Circuit

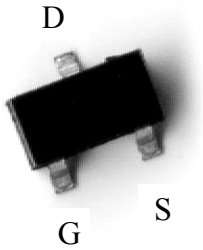
MTP5103N3



G：Gate
S：Source
D：Drain

Outline

SOT-23



Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @T_A=25°C		I_D	-4.5	A
Continuous Drain Current @T_A=70°C		I_D	-3.5	A
Pulsed Drain Current @V_{GS}=10V (Notes 1, 2)		I_{DM}	-20	A
Maximum Power Dissipation (Note 3)	T_A=25°C	P_D	1.38	W
	T_A=75°C		0.83	W
Operating Junction and Storage Temperature		Tj, Tstg	-55~+150	°C

Note : 1. Pulse width limited by maximum junction temperature.
2. Pulse width≤ 300μs, duty cycle≤2%.
3. Surface mounted on 1 in² copper pad of FR-4 board.

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient	Rth,ja	90	°C/W

Note : Surface mounted on 1 in² copper pad of FR-4 board, 270°C/W when mounted on minimum copper pad.

Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	-30	-	-	V	V_{GS}=0, I_D=-250μA
$V_{GS(th)}$	-1.0	-1.4	-2.5	V	V_{DS}=V_{GS}, I_D=-250μA
I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0
I_{DSS}	-	-	-1	μA	V_{DS}=-24V, V_{GS}=0
I_{DSS}	-	-	-10	μA	V_{DS}=-24V, V_{GS}=0, Tj=125°C
*$R_{DS(ON)}$	-	41	50	mΩ	I_D=-4.5A, V_{GS}=-10V
	-	60	70		I_D=-3.5A, V_{GS}=-4.5V
*G_{FS}	-	4.3	-	S	V_{DS}=-10V, I_D=-4.5A
Dynamic					
Ciss	-	885	-	pF	V_{DS}=-10V, V_{GS}=0, f=1MHz
Coss	-	86	-		
Crss	-	81	-		
*$t_{d(ON)}$	-	8	-	ns	V_{DS}=-15V, I_D=-1A, V_{GS}=-10V, R_D=15Ω, R_G=6Ω
*t_r	-	12	-		
*$t_{d(OFF)}$	-	30	-		
*t_f	-	23	-		
*Qg	-	15	-	nC	V_{DS}=-15V, I_D=-4.5A, V_{GS}=-10V
*Qgs	-	3	-		
*Qgd	-	7	-		
Source-Drain Diode					
*I_S	-	-	-4.5	A	
*I_{SM}	-	-	-18		
*V_{SD}	-	-	-1.2	V	V_{GS}=0V, I_S=-1A
*trr	-	32	-	ns	I_F=-4.5A, dI_F/dt=100A/μs
*Qrr	-	13.5	-	nC	

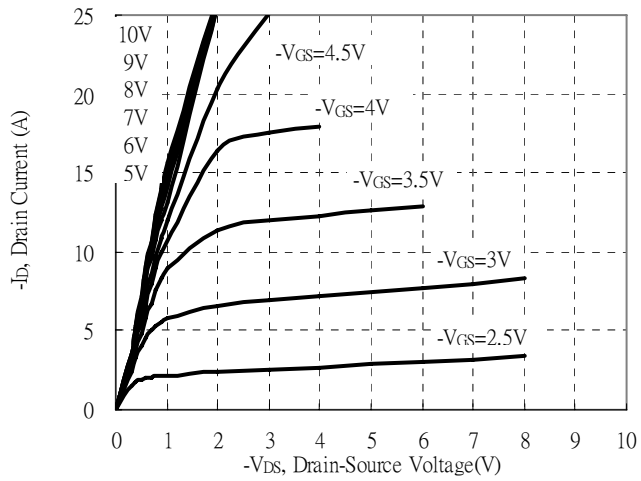
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

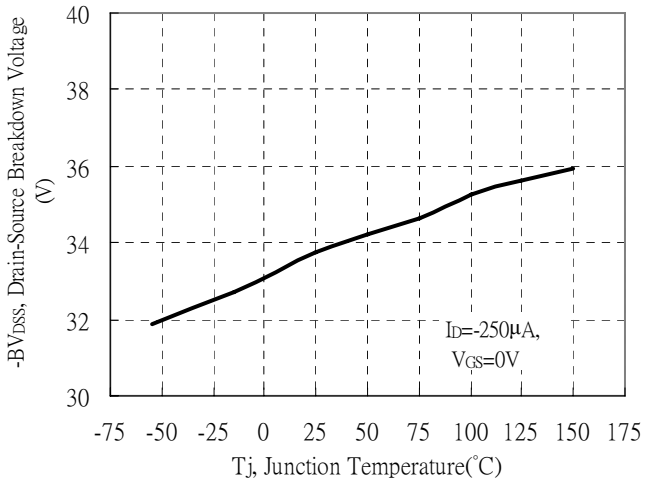
Device	Package	Shipping	Marking
MTP5103N3	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel	5103

Typical Characteristics

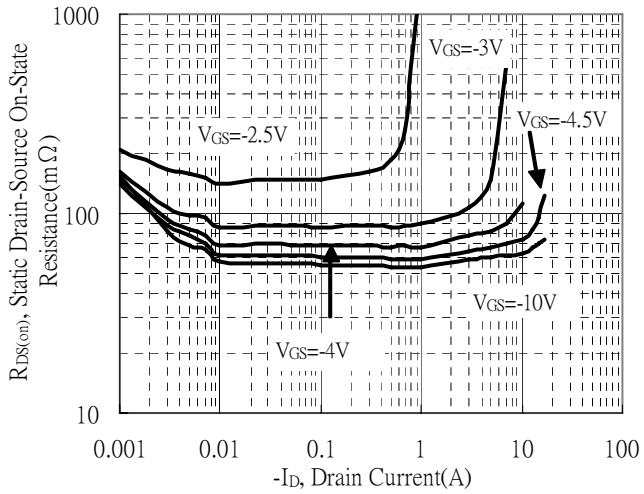
Typical Output Characteristics



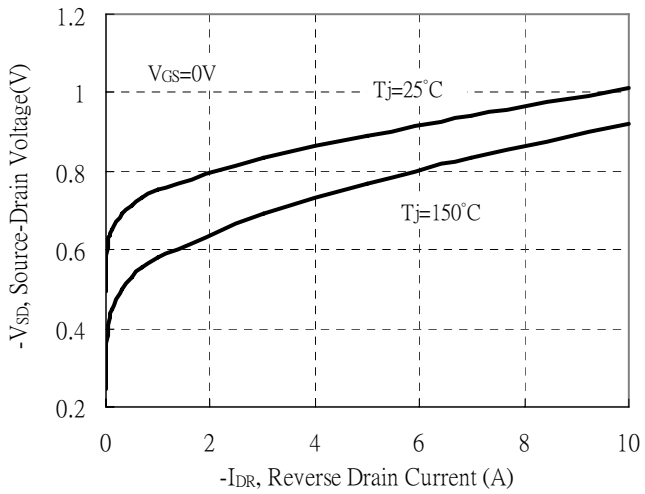
Brekdown Voltage vs Ambient Temperature



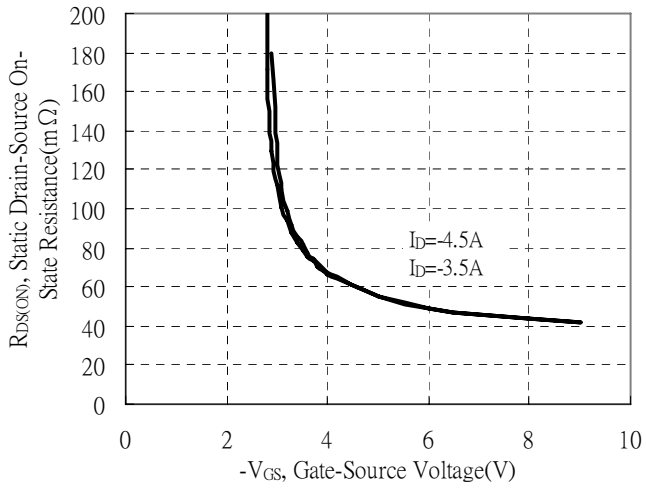
Static Drain-Source On-State resistance vs Drain Current



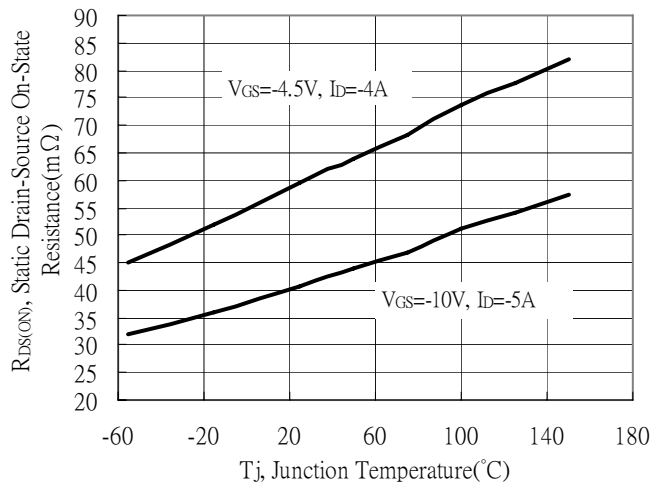
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

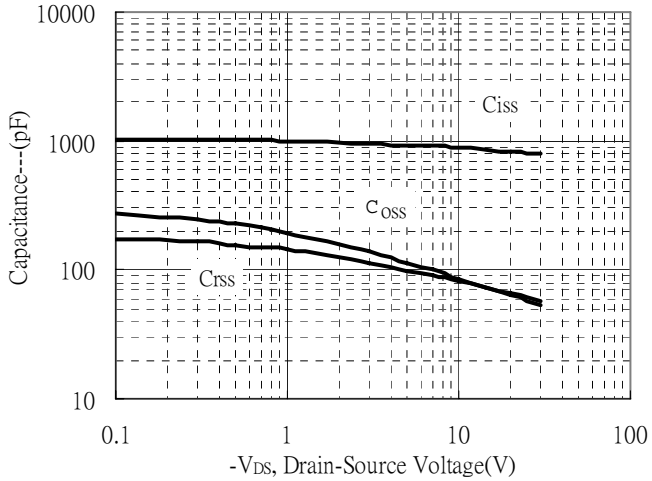


Drain-Source On-State Resistance vs Junction Tempearture

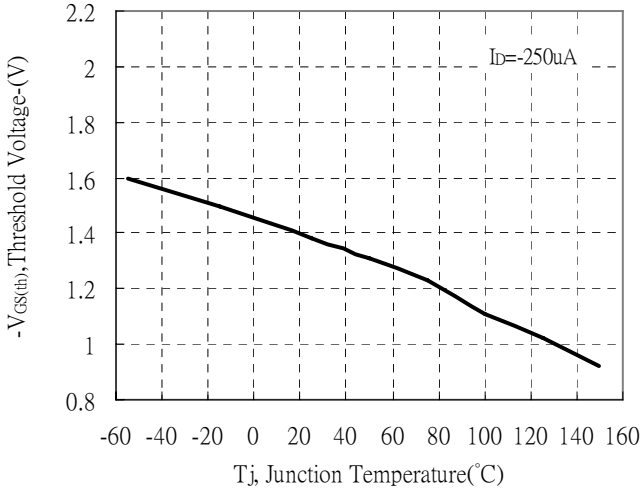


Typical Characteristics(Cont.)

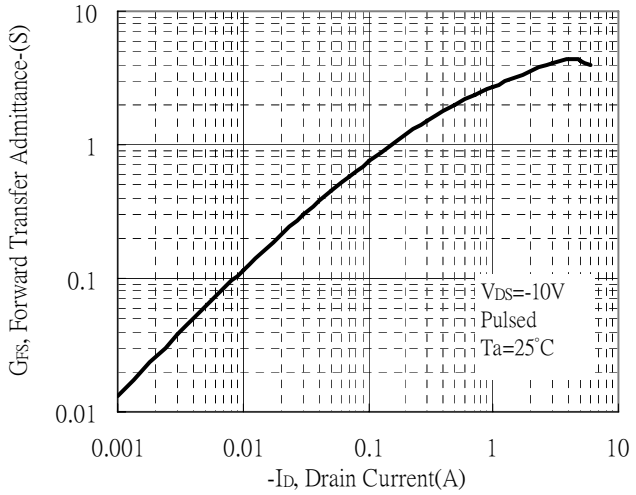
Capacitance vs Drain-to-Source Voltage



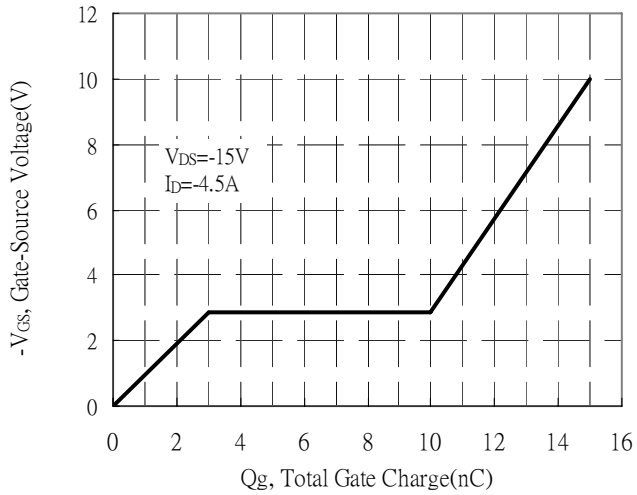
Threshold Voltage vs Junction Tempearture



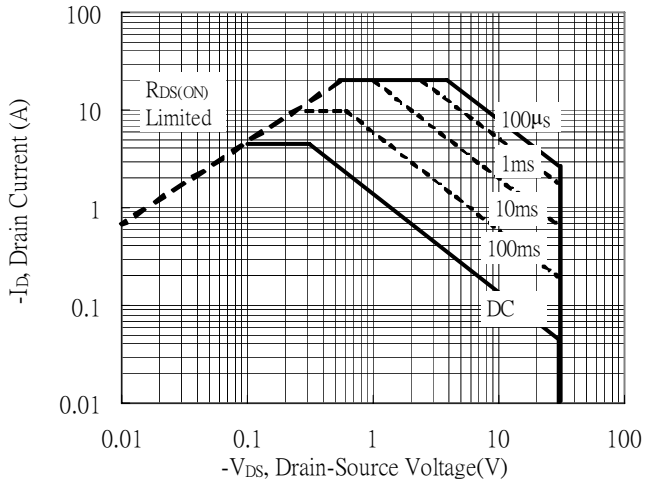
Forward Transfer Admittance vs Drain Current



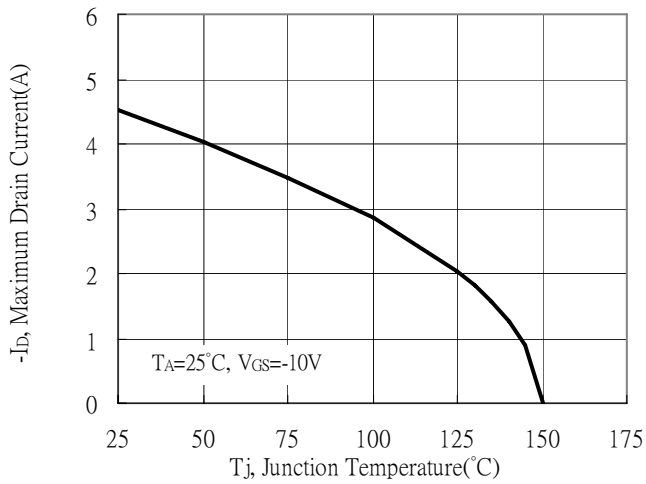
Gate Charge Characteristics



Maximum Safe Operating Area

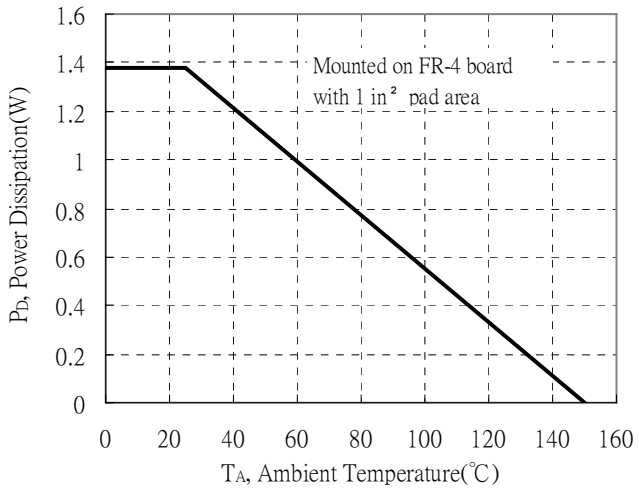


Maximum Drain Current vs JunctionTemperature

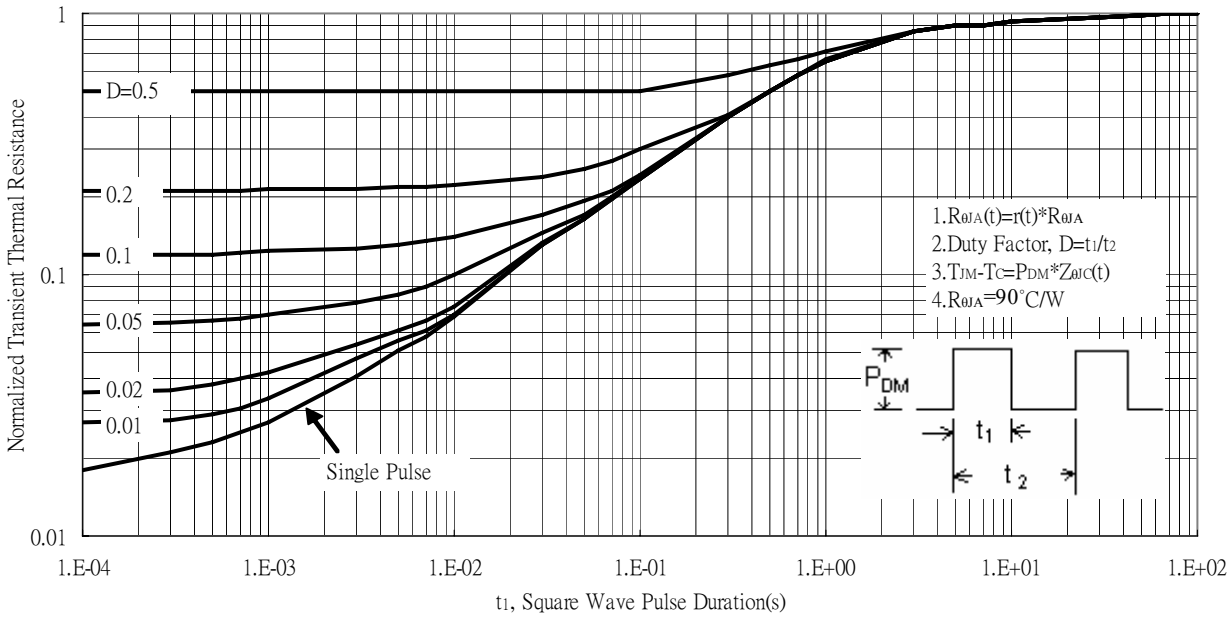


Typical Characteristics(Cont.)

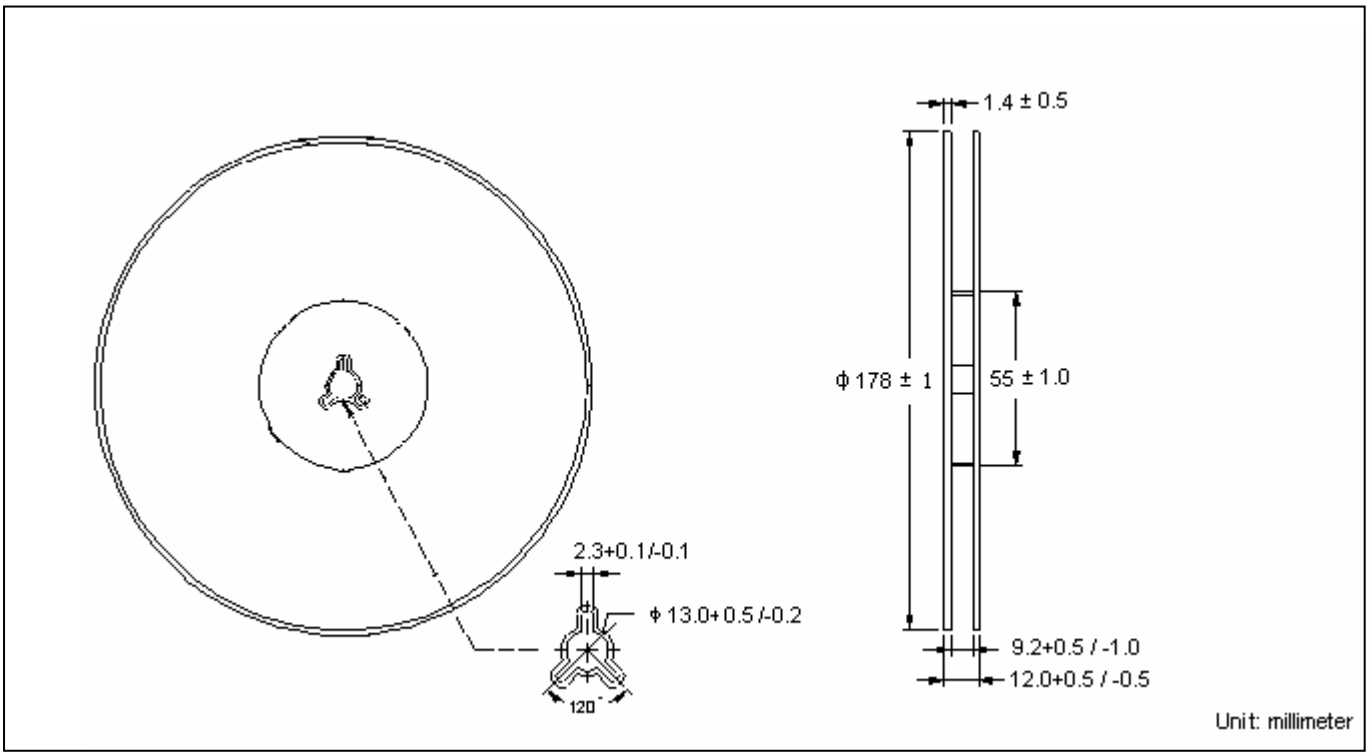
Power Derating Curve



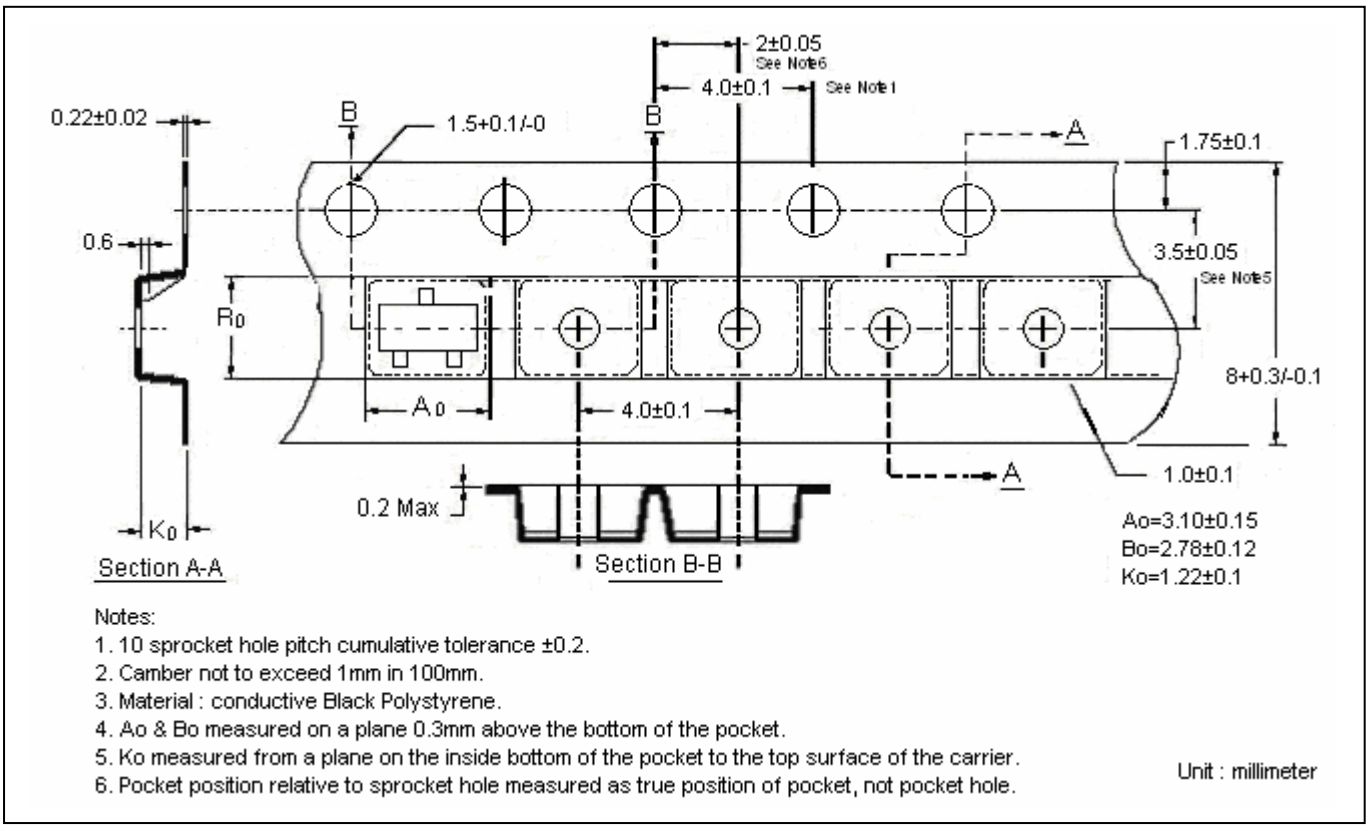
Transient Thermal Response Curves



Reel Dimension



Carrier Tape Dimension



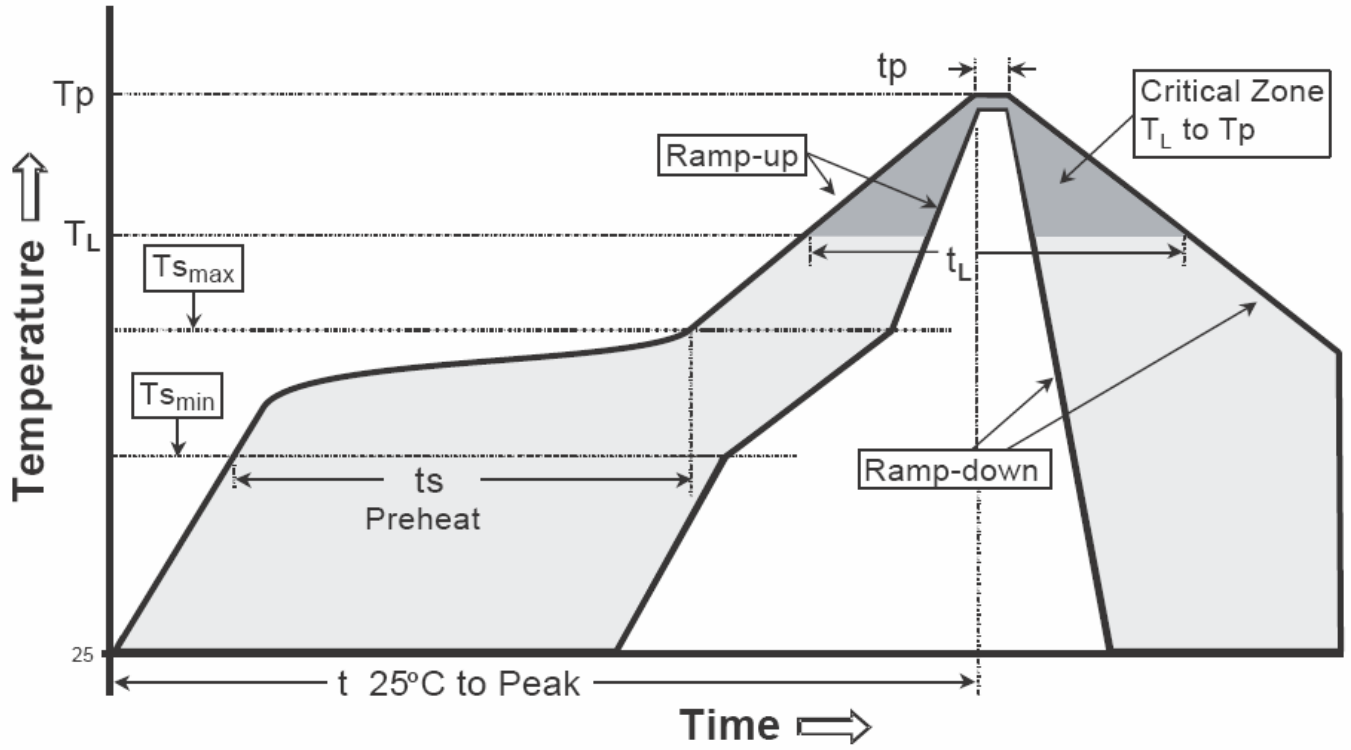
Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material : conductive Black Polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

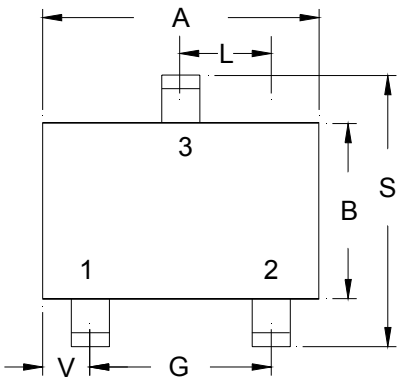
Recommended temperature profile for IR reflow

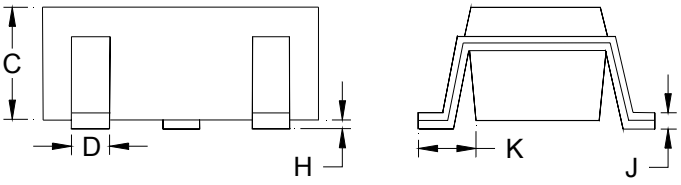


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

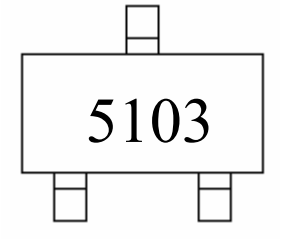
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-23 Dimension





Marking:



3-Lead SOT-23 Plastic
Surface Mounted Package
CYStek Package Code: N3

Style : Pin 1.Gate 2.Source 3.Drain

*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0035	0.0071	0.09	0.18
B	0.0472	0.0669	1.20	1.70	K	0.0276 REF		0.70 REF	
C	0.0335	0.0512	0.89	1.30	L	0.0374*		0.95*	
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0004	0.0040	0.01	0.10					

Notes : 1.Controlling dimension : millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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