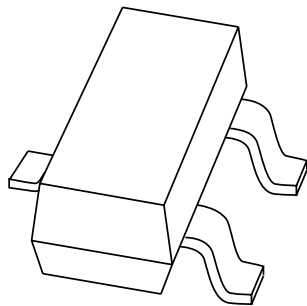


DATA SHEET



BSR17A NPN switching transistor

Product specification
Supersedes data of 1997 Jun 02

2004 Mar 24

NPN switching transistor

BSR17A

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- Switching and linear amplification.

DESCRIPTION

NPN switching transistor in a SOT23 plastic package.
PNP complement: BSR18A.

MARKING

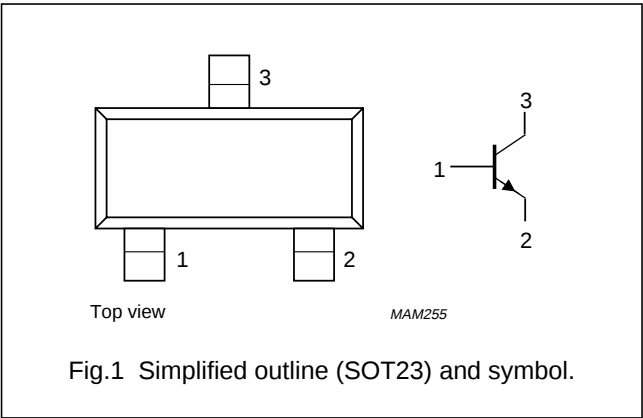
TYPE NUMBER	MARKING CODE ⁽¹⁾
BSR17A	54* or U92

Note

1. * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BSR17A	–	plastic surface mounted package; 3 leads	SOT23

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	60	V
V _{CEO}	collector-emitter voltage	open base	–	40	V
I _C	collector current (DC)		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	–	250	mW
h _{FE}	DC current gain	I _C = 10 mA; V _{CE} = 1 V	100	300	
f _T	transition frequency	I _C = 10 mA; V _{CE} = 20 V; f = 100 MHz	300	–	MHz
t _{off}	turn-off time	I _{COn} = 10 mA; I _{BOn} = 1 mA; I _{Boff} = –1 mA	–	240	ns

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	100	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	500	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

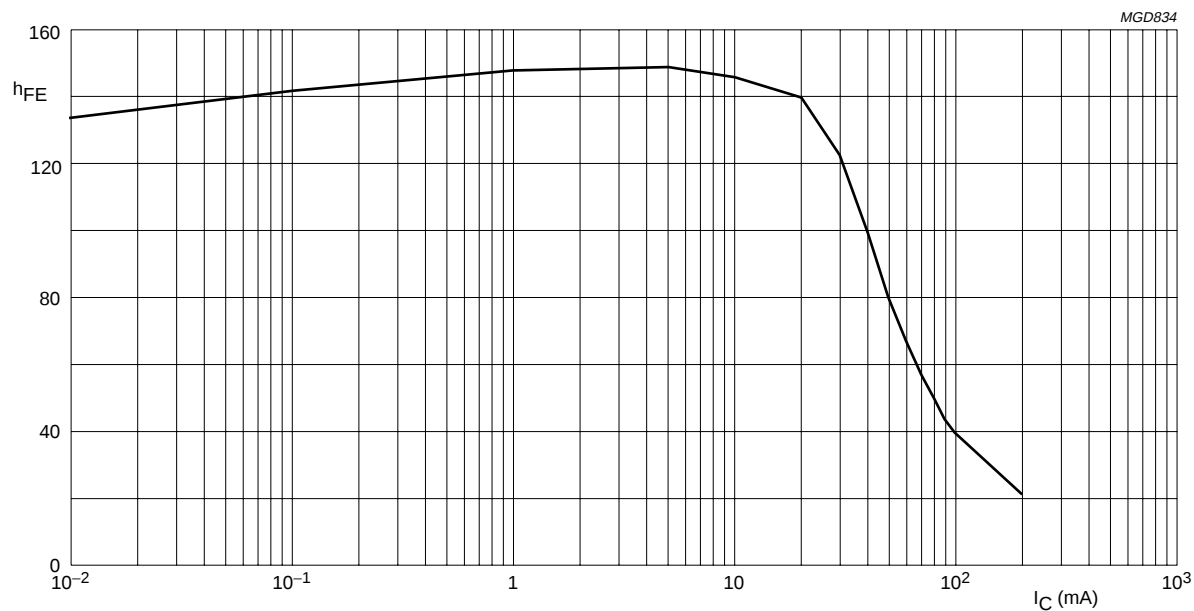
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0\text{ A}; V_{CB} = 30\text{ V}$	–	50	nA
		$I_E = 0\text{ A}; V_{CB} = 30\text{ V}; T_j = 150\text{ }^{\circ}\text{C}$	–	5	μA
I_{EBO}	emitter cut-off current	$I_C = 0\text{ A}; V_{EB} = 6\text{ V}$	–	50	nA
h_{FE}	DC current gain	$V_{CE} = 1\text{ V}$; note 1; see Fig.2			
		$I_C = 0.1\text{ mA}$	60	–	
		$I_C = 1\text{ mA}$	80	–	
		$I_C = 10\text{ mA}$	100	300	
		$I_C = 50\text{ mA}$	60	–	
		$I_C = 100\text{ mA}$	30	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 1\text{ mA}$; note 1	–	200	mV
		$I_C = 50\text{ mA}; I_B = 5\text{ mA}$; note 1	–	200	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 1\text{ mA}$; note 1	650	850	mV
		$I_C = 50\text{ mA}; I_B = 5\text{ mA}$; note 1	–	950	mV
C_c	collector capacitance	$I_E = i_e = 0\text{ A}; V_{CB} = 5\text{ V}; f = 1\text{ MHz}$	–	4	pF
C_e	emitter capacitance	$I_C = i_c = 0\text{ A}; V_{EB} = 500\text{ mV}; f = 1\text{ MHz}$	–	8	pF
f_T	transition frequency	$I_C = 10\text{ mA}; V_{CE} = 20\text{ V}; f = 100\text{ MHz}$	300	–	MHz
F	noise figure	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}; R_S = 1\text{ k}\Omega$; $f = 10\text{ Hz to }15.7\text{ kHz}$	–	5	dB
Switching times (between 10% and 90% levels); see Fig.3					
t_{on}	turn-on time	$I_{Con} = 10\text{ mA}; I_{Bon} = 1\text{ mA}; I_{Boff} = -1\text{ mA}$	–	65	ns
t_d	delay time		–	35	ns
t_r	rise time		–	35	ns
t_{off}	turn-off time		–	240	ns
t_s	storage time		–	200	ns
t_f	fall time		–	50	ns

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

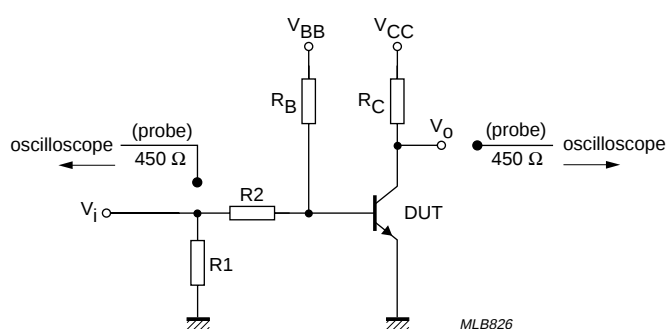
NPN switching transistor

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$V_{CE} = 1 \text{ V.}$

Fig. 2 DC current gain; typical values.



$V_i = 5 \text{ V; } T = 500 \text{ } \mu\text{s; } t_p = 10 \text{ } \mu\text{s; } t_r = t_f \leq 3 \text{ ns.}$
 $R_1 = 56 \text{ } \Omega; R_2 = 2.5 \text{ k}\Omega; R_B = 3.9 \text{ k}\Omega; R_C = 270 \text{ } \Omega.$
 $V_{BB} = -1.9 \text{ V; } V_{CC} = 3 \text{ V.}$
 Oscilloscope input impedance $Z_i = 50 \text{ } \Omega.$

Fig. 3 Test circuit for switching times.

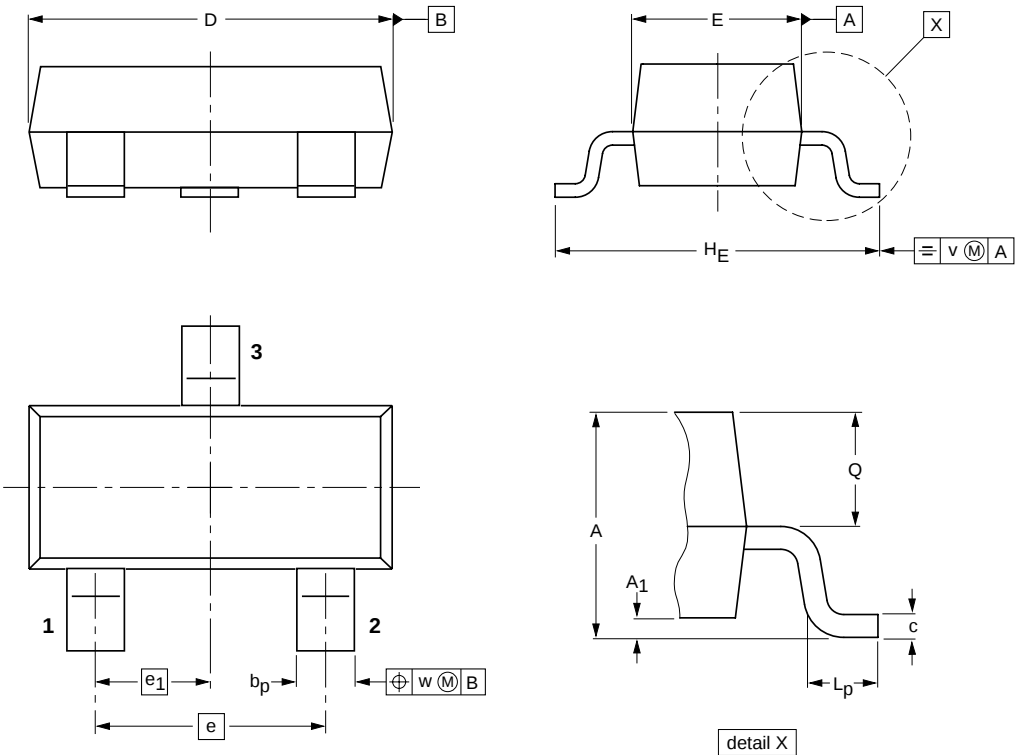
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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				97-02-28 99-09-13

NPN switching transistor

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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