TPS54332 3.5-A, 28-V, 1-MHz, Step-Down DC-DC Converter With Eco-Mode™

1 Features

- 3.5-V to 28-V Input Voltage Range
- Adjustable Output Voltage Down to 0.8 V
- Integrated 80-mΩ High-Side MOSFET Supports up to 3.5-A Continuous Output Current
- High Efficiency at Light Loads With a Pulse-Skipping Eco-Mode™
- Fixed 1-MHz Switching Frequency
- Typical 1-µA Shutdown Quiescent Current
- Adjustable Slow-Start Limits Inrush Currents
- Programmable UVLO Threshold
- Overvoltage Transient Protection
- Cycle-by-Cycle Current Limit, Frequency Foldback and Thermal Shutdown Protection
- Available in Thermally Enhanced 8-Pin SOIC PowerPAD™ Package
- Supported by WEBENCH™ Tool (http://www.ti.com/lsds/ti/analog/webench/overview.page)

2 Applications

- Consumer Applications such as Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car Audio Power Supplies
- 5-V, 12-V and 24-V Distributed Power Systems

3 Description

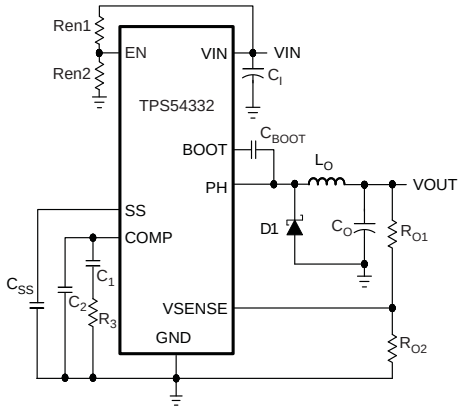
The TPS54332 is a 28-V, 3.5-A non-synchronous buck converter that integrates a low-$R_{DS(on)}$ high-side MOSFET. To increase efficiency at light loads, a pulse-skipping Eco-Mode feature is automatically activated. Furthermore, the 1-µA shutdown supply current allows the device to be used in battery-powered applications. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input undervoltage lockout. An overvoltage transient protection circuit limits voltage overshoots during start-up and transient conditions. A cycle-by-cycle current limit scheme, frequency foldback and thermal shutdown protect the device and the load in the event of an overload condition. The TPS54332 is available in an 8-pin SOIC PowerPAD™ package.

Device Information(1)

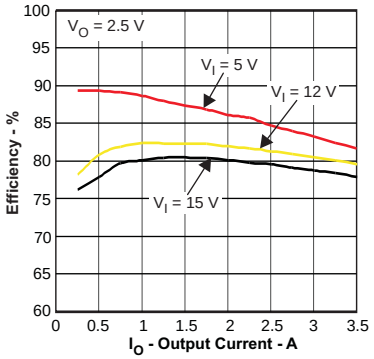
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54332	SO PowerPAD (8)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 Handling Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 6
6.7 Typical Characteristics: Characterization Curves ... 7
6.8 Typical Characteristics: Supplemental Application Curves ... 8
7 Detailed Description ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 13
8 Application and Implementation ... 14
8.1 Application Information ... 14
8.2 Typical Application ... 14
9 Power Supply Recommendations ... 24
10 Layout ... 24
10.1 Layout Guidelines ... 24
10.2 Layout Example ... 25
10.3 Estimated Circuit Area ... 25
10.4 Electromagnetic Interference (EMI) Considerations ... 25
11 Device and Documentation Support ... 26
11.1 Device Support ... 26
11.2 Trademarks ... 26
11.3 Electrostatic Discharge Caution ... 26
11.4 Glossary ... 26
12 Mechanical, Packaging, and Orderable Information ... 26

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (Feburary 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (January 2013) to Revision B — **Page**

- Deleted Swift™ from the data sheet title ... 1
- Deleted feature Item: For SWIFT™ Documentation, See the TI Website at www.ti.com/swift ... 1

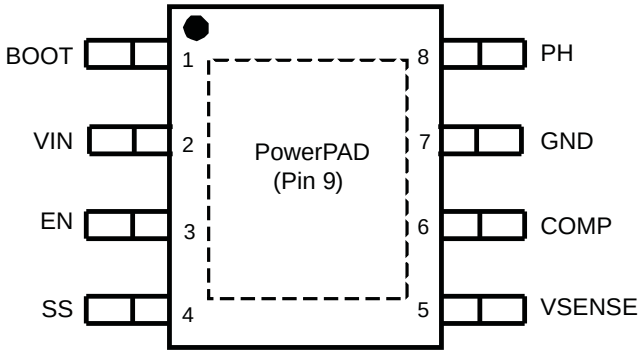
Copyright © 2009–2014, Texas Instruments Incorporated

Changes from Original (March 2007) to Revision A **Page**

- Changed the ABSOLUTE MAXIMUM RATINGS table, Input Voltage - EN pin max value From: 5V to 6V 4

5 Pin Configuration and Functions

DDA PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A 0.1-µF bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed.
VIN	2	I	Input supply voltage, 3.5 V to 28 V.
EN	3	I	Enable pin. Pull below 1.25 V to disable. Float to enable. Programming the input undervoltage lockout with two resistors is recommended.
SS	4	I	Slow-start pin. An external capacitor connected to this pin sets the output rise time.
VSENSE	5	I	Inverting node of the gm error amplifier.
COMP	6	O	Error amplifier output, and input to the PWM comparator. Connect frequency compensation components to this pin.
GND	7	-	Ground.
PH	8	O	The source of the internal high-side power MOSFET.
PowerPAD	9	-	GND pin must be connected to the exposed pad for proper operation.

Copyright © 2009–2014, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	30	V
	EN	–0.3	6	
	BOOT		38	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	SS	–0.3	3	
Output Voltage	BOOT-PH		8	V
	PH	–0.6	30	
	PH (10 ns transient from ground to negative peak)		–5	
Source Current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH		9.25	A
Sink Current	VIN		9.25	A
	COMP		100	µA
	SS		200	
Operating Junction Temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maxmium Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage Temperature		–65	150	°C
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating Input Voltage on (VIN pin)	3.5	28	V
Operating junction temperature, T_J	–40	150	°C

Copyright © 2009–2014, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		TPS54332 HSOP 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	25.3	
ψ_{JT}	Junction-to-top characterization parameter	8.4	
ψ_{JB}	Junction-to-board characterization parameter	25.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2009–2014, Texas Instruments Incorporated

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 3.5 V to 28 V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	Rising and Falling			3.5	V
Shutdown supply current	EN = 0 V, VIN = 12 V, –40°C to 85°C		1	4	µA
Operating – non switching supply current	VSENSE = 0.85 V		82	120	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising and Falling		1.25	1.35	V
Input current	Enable threshold – 50 mV		-1		µA
Input current	Enable threshold + 50 mV		-4		µA
VOLTAGE REFERENCE					
Voltage reference		0.772	0.8	0.828	V
HIGH-SIDE MOSFET					
On resistance	BOOT-PH = 3 V, VIN = 3.5 V		115	200	mΩ
	BOOT-PH = 6 V, VIN = 12 V		80	150	
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2 µA < I_{COMP} < 2 µA, V(COMP) = 1 V		92		µmhos
Error amplifier DC gain(1)	VSENSE = 0.8 V		800		V/V
Error amplifier unity gain bandwidth(1)	5 pF capacitance from COMP to GND pins		2.7		MHz
Error amplifier source/sink current	$V_{(COMP)}$ = 1.0 V, 100-mV overdrive		±7		µA
Switch current to COMP transconductance	VIN = 12 V		12		A/V
PULSE-SKIPPING ECO-MODE					
Pulse-skipping Eco-Mode switch current threshold			160		mA
CURRENT LIMIT					
Current limit threshold	VIN = 12 V	4.2	6.5		A
THERMAL SHUTDOWN					
Thermal Shutdown			165		°C
SLOW-START (SS PIN)					
Charge current	$V_{(SS)}$ = 0.4 V		2		µA
SS to VSENSE matching	$V_{(SS)}$ = 0.4 V		10		mV

(1) Specified by design

6.6 Switching Characteristics

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS54332 Switching Frequency	VIN = 12 V, 25°C	800	1000	1200	kHz
Minimum controllable on time	VIN = 12 V, 25°C		110	135	ns
Maximum controllable duty ratio(1)	BOOT-PH = 6 V	90%	93%		

(1) Specified by design

Copyright © 2009–2014, Texas Instruments Incorporated

6.7 Typical Characteristics: Characterization Curves

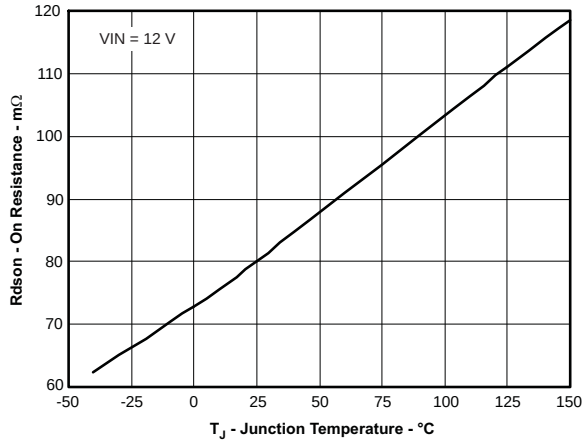


Figure 1. On Resistance vs Junction Temperature

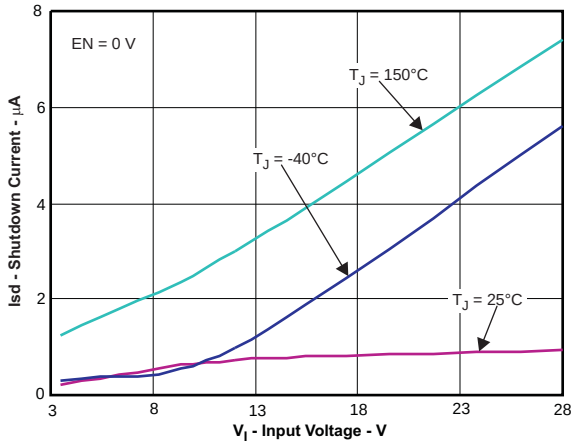


Figure 2. Shutdown Quiescent Current vs Input Voltage

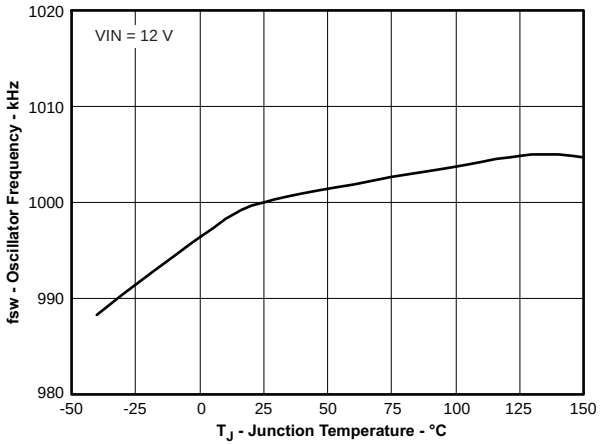


Figure 3. Switching Frequency vs Junction Temperature

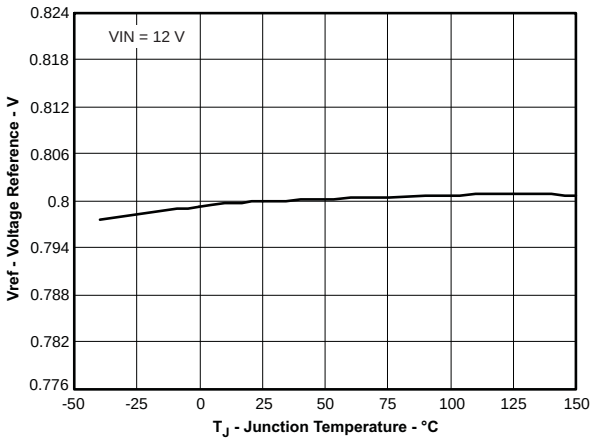


Figure 4. Voltage Reference vs Junction Temperature

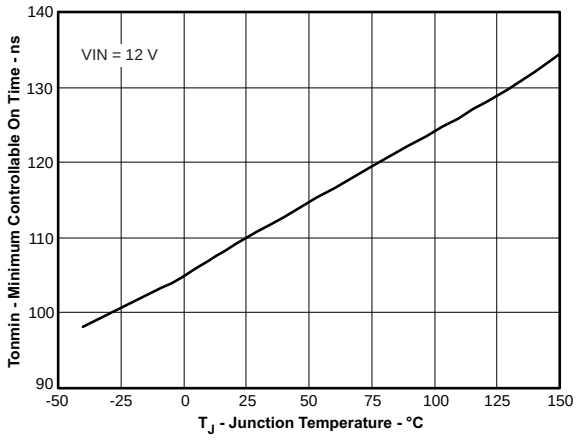


Figure 5. Minimum Controllable on Time vs Junction Temperature

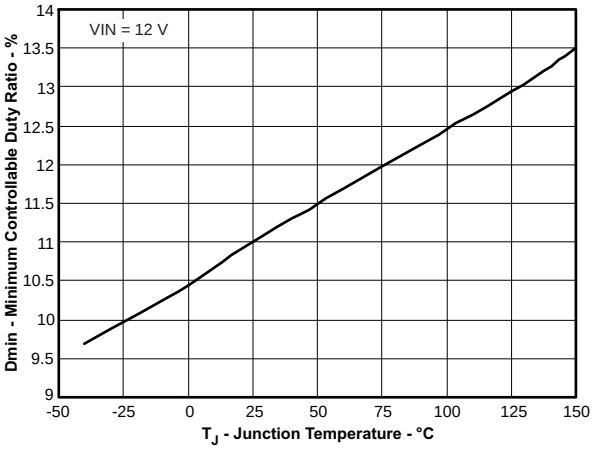


Figure 6. Minimum Controllable Duty Ratio vs Junction Temperature

Copyright © 2009–2014, Texas Instruments Incorporated

Typical Characteristics: Characterization Curves (continued)

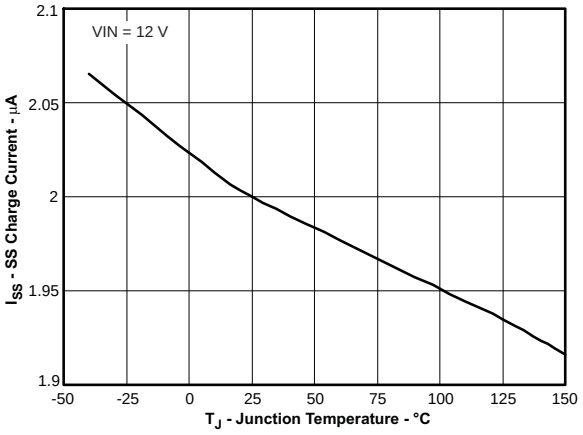


Figure 7. SS Charge Current vs Junction Temperature

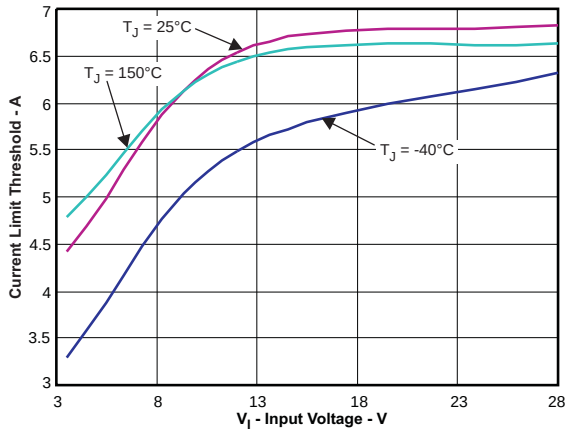


Figure 8. Current Limit Threshold vs Input Voltage

6.8 Typical Characteristics: Supplemental Application Curves

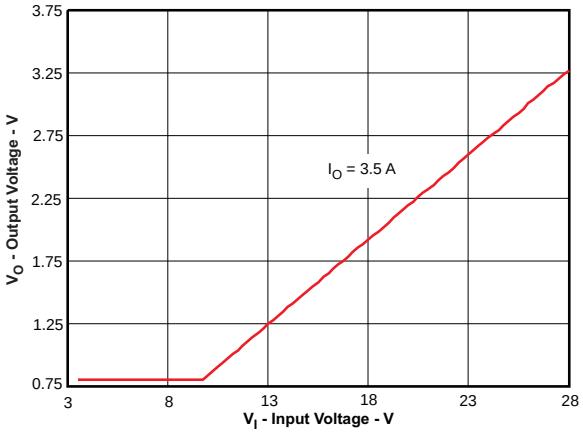


Figure 9. Typical Minimum Output Voltage vs Input Voltage

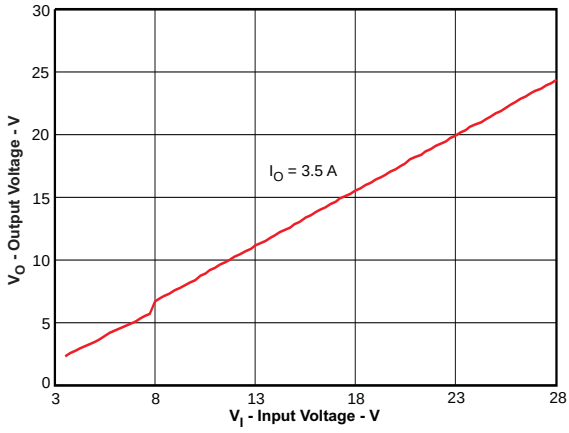


Figure 10. Typical Maximum Output Voltage vs Input Voltage

Copyright © 2009–2014, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The TPS54332 is a 28-V, 3.5-A, step-down (buck) converter with an integrated high-side, N-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current mode control, which reduces output capacitance and simplifies external frequency compensation design. The TPS54332 has a pre-set switching frequency of 1 MHz.

The TPS54332 needs a minimum input voltage of 3.5 V to operate normally. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The operating current is 82 μA typically when not switching and under no load. When the device is disabled, the supply current is 1 μA typically.

The integrated 80-mΩ high-side MOSFET allows for high-efficiency power supply designs with continuous output currents up to 3.5 A.

The TPS54332 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically. The output voltage can be stepped down to as low as the reference voltage.

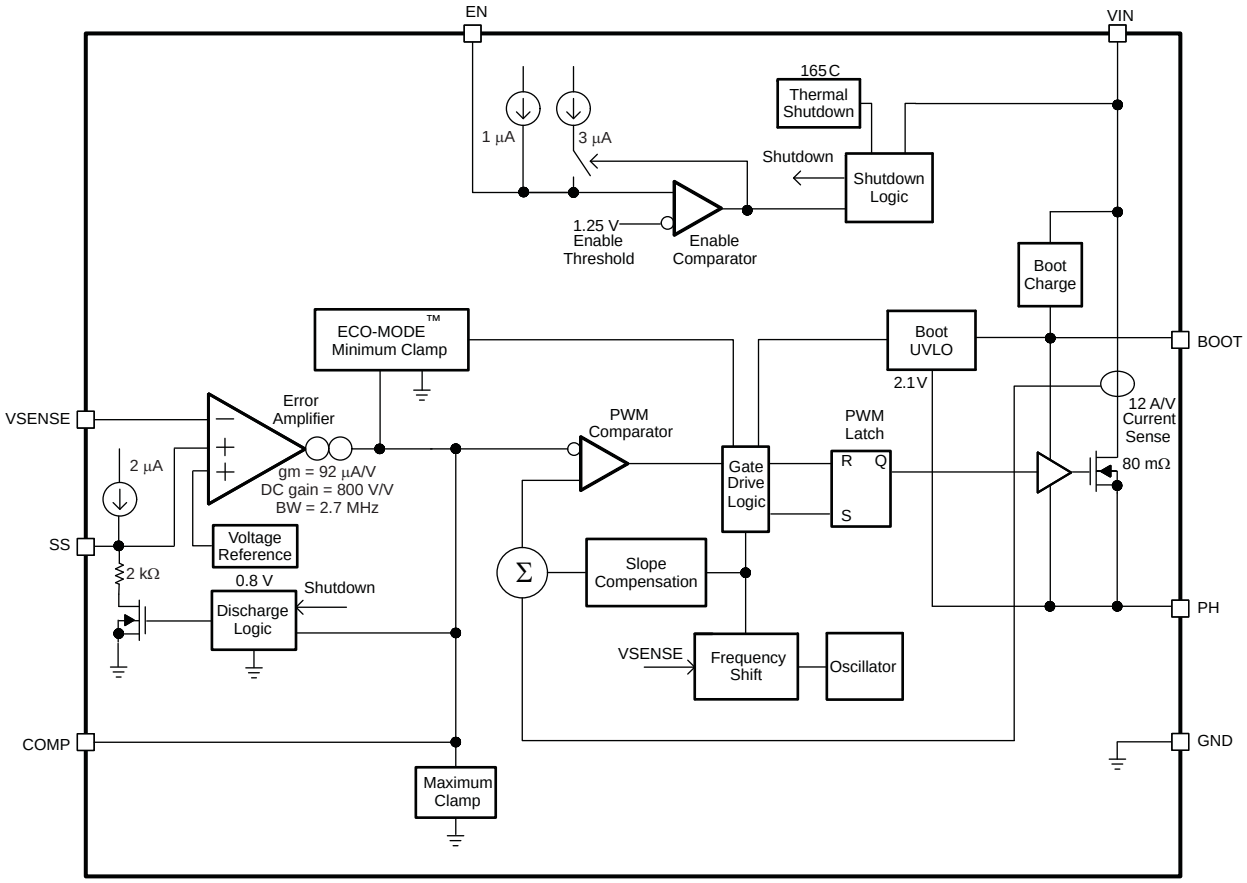
By adding an external capacitor, the slow-start time of the TPS54332 can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the TPS54332 enters a special pulse-skipping Eco-Mode when the peak inductor current drops below 160 mA typically.

The frequency foldback reduces the switching frequency during start-up and over current conditions to help control the inductor current. The thermal shutdown gives the additional protection under fault conditions.

Copyright © 2009–2014, Texas Instruments Incorporated

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54332 uses a fixed-frequency, peak-current mode control. The internal switching frequency of the TPS54332 is fixed at 1 MHz.

7.3.2 Voltage Reference (V_{ref})

The voltage reference system produces a ±2% initial accuracy voltage reference (±3.5% over temperature) by scaling the output of a temperature stable band-gap circuit. The typical voltage reference is designed at 0.8 V.

7.3.3 Bootstrap Voltage (BOOT)

The TPS54332 has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve dropout, the TPS54332 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1 V typically.

7.3.4 Enable and Adjustable Input Undervoltage Lockout (VIN UVLO)

The EN pin has an internal pullup current source that provides the default condition of the TPS54332 operating when the EN pin floats.

Copyright © 2009–2014, Texas Instruments Incorporated

Feature Description (continued)

The TPS54332 is disabled when the VIN pin voltage falls below internal VIN UVLO threshold. TI recommends using an external VIN UVLO to add Hysteresis unless VIN is greater than (V_{OUT} + 2 V). To adjust the VIN UVLO with Hysteresis, use the external circuitry connected to the EN pin as shown in Figure 11. Once the EN pin voltage exceeds 1.25 V, an additional 3 µA of hysteresis is added. Use Equation 1 and Equation 2 to calculate the resistor values needed for the desired VIN UVLO threshold voltages. The V_{START} is the input start threshold voltage, the V_{STOP} is the input stop threshold voltage and the V_{EN} is the enable threshold voltage of 1.25 V. The V_{STOP} should always be greater than 3.5 V.

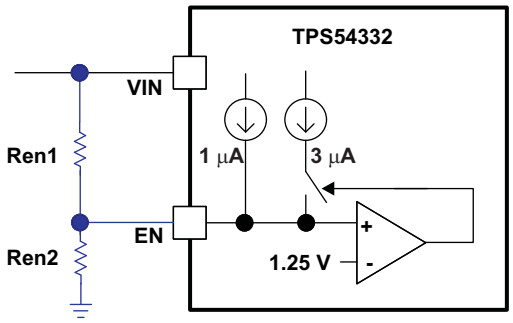


Figure 11. Adjustable Input Undervoltage Lockout

$$Ren1 = \frac{V_{START} - V_{STOP}}{3\ \mu A} \quad (1)$$

$$Ren2 = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{Ren1} + 1\ \mu A} \quad (2)$$

7.3.5 Programmable Slow-Start Using SS Pin

TI highly recommends programing the slow-start time externally because no slow-start time is implemented internally. The TPS54332 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power supply's reference voltage fed into the error amplifier and will regulate the output accordingly. A capacitor (C_{SS}) on the SS pin-to-ground implements a slow-start time. The TPS54332 has an internal pullup current source of 2 µA that charges the external slow-start capacitor. The equation for the slow-start time (10% to 90%) is shown in Equation 3 . The V_{ref} is 0.8V and the I_{SS} current is 2 µA.

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{ref}(V)}{I_{SS}(\mu A)} \quad (3)$$

The slow-start time should be set between 1 ms to 10 ms to ensure good start-up behavior. The slow-start capacitor should be no more than 27 nF.

If during normal operation, the input voltage drops below the VIN UVLO threshold, or the EN pin is pulled below 1.25 V, or a thermal shutdown event occurs, the TPS54332 stops switching.

7.3.6 Error Amplifier

The TPS54332 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 µA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

7.3.7 Slope Compensation

In order to prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS54332 adds a built-in slope compensation which is a compensating ramp to the switch current signal.

Copyright © 2009–2014, Texas Instruments Incorporated

Feature Description (continued)

7.3.8 Current Mode Compensation Design

To simplify design efforts using the TPS54332, the typical designs for common applications are listed in Table 1. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when doing the stability analysis. This is because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. Advanced users may refer to the *Detailed Design Procedure* in the *Application and Implementation* section for the detailed guidelines, or use the WEBENCH tool (http://www.ti.com/lsds/ti/analog/webench/overview.page).

Table 1. Typical Designs (Referring to Simplified Schematic on Page 1)

VIN (V)	V_{OUT} (V)	F_{sw} (kHz)	L_o (µH)	C_o	R_{O1} (kΩ)	R_{O2} (kΩ)	C_2 (pF)	C_1 (pF)	R_3 (kΩ)
12	5	1000	3.3	Ceramic 22-µF	10	1.91	18	470	24.9
12	3.3	1000	2.7	Ceramic 22-µF x 2	10	3.24	18	1800	39.2
12	5	1000	3.3	Aluminum 330-µF / 160-mohm	10	1.91	22	47	10
12	3.3	1000	2.7	Aluminum 330-µF / 160-mohm	10	3.24	39	100	29.4

7.3.9 Overcurrent Protection and Frequency Shift

The TPS54332 implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. Every cycle, the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limit the output current.

The TPS54332 provides robust protection during short circuits. There is potential for overcurrent runaway in the output inductor during a short circuit at the output. The TPS54332 solves this issue by increasing the off-time during short circuit conditions by lowering the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is shown in Table 2.

Table 2. Switching Frequency Conditions

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
1 MHz	VSENSE ≥ 0.6 V
1 MHz / 2	0.6 V > VSENSE ≥ 0.4 V
1 MHz / 4	0.4 V > VSENSE ≥ 0.2 V
1 MHz / 8	0.2 V > VSENSE

7.3.10 Overvoltage Transient Protection

The TPS54332 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × V_{ref}, the high-side MOSFET will be forced off. When the VSENSE pin voltage falls below 107% × V_{ref}, the high-side MOSFET will be enabled again.

7.3.11 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 165°C, the device reinitiates the power-up sequence.

Copyright © 2009–2014, Texas Instruments Incorporated

7.4 Device Functional Modes

7.4.1 Operation With VIN < 3.5 V

The device is recommended to operate with input voltages above 3.5 V. The typical VIN UVLO threshold is not specified and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device will not switch. If EN is externally pulled up or left floating, when VIN passes the UVLO threshold the device will become active. Switching will commenced when the soft-start sequence is initiated.

7.4.2 Operation With EN Control

The enable threshold voltage is 1.25 V typical. With EN held below that voltage the device is disabled and switching is inhibited even if VIN is above its UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage is increased above the threshold while VIN is above its UVLO threshold, the device becomes active. Switching is enabled, and the slow-start sequence is initiated.

7.4.3 Eco-Mode

The device is designed to operate in pulse-skipping Eco-Mode at light-load currents to boost light-load efficiency. When the peak inductor current is lower than pulse skip threshold, the COMP pin voltage falls to 0.5 V (typical) and the device enters Eco-Mode . When the device is in Eco-Mode, the COMP pin voltage is clamped at 0.5 V internally which prevents the high-side integrated MOSFET from switching. The peak inductor current must rise above 160 mA for the COMP pin voltage to rise above 0.5 V and exit Eco-Mode. Because the integrated current comparator catches the peak inductor current only, the average load current entering Eco-Mode varies with the applications and external output filters.

Copyright © 2009–2014, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54332 is typically used as step down converters, which convert a voltage from 3.5 V - 28 V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits.

	TPS54231	TPS54232	TPS54233	TPS54331	TPS54332
I_O(Max)	2 A	2 A	2 A	3 A	3.5 A
Input Voltage Range	3.5 V - 28 V	3.5 V - 28 V	3.5 V - 28 V	3.5 V - 28 V	3.5 V - 28 V
Switching Freq. (Typ)	570 kHz	1000 kHz	285 kHz	570 kHz	1000 kHz
Switch Current Limit (Min)	2.3 A	2.3 A	2.3 A	3.5 A	4.2 A
Pin/Package	8/SOIC	8/SOIC	8/SOIC	8/SOIC	8/SO PowerPAD™

8.2 Typical Application

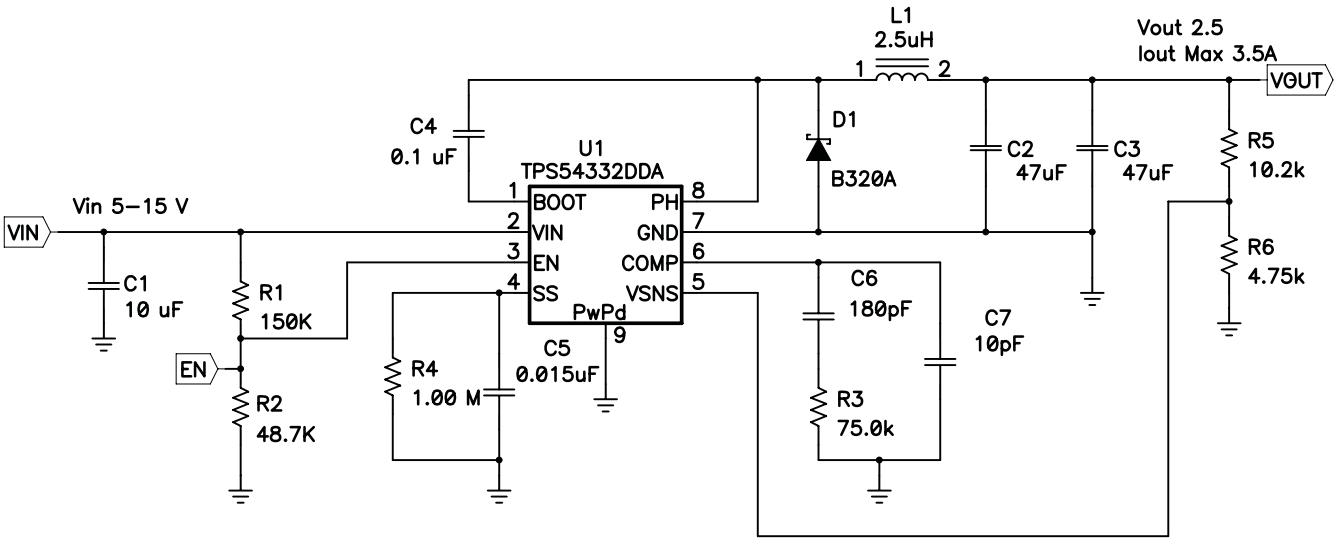


Figure 12. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the following as the input parameters:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5 V to 15 V
Output voltage	2.5 V
Input ripple voltage	200 mV
Output ripple voltage	20 mV
Output current rating	3.5 A
Operating Frequency	1 MHz

Copyright © 2009–2014, Texas Instruments Incorporated

8.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54332. Alternately, the WEBENCH Tool may be used to generate a complete design. The WEBENCH Tool uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2.2.1 Switching Frequency

The switching frequency for the TPS54332 is fixed at 1 MHz.

8.2.2.2 Output Voltage Set Point

The output voltage of the TPS54332 is externally adjustable using a resistor divider network. In the application circuit of Figure 12, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by Equation 4 and Equation 5.

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT} - V_{REF}} \tag{4}$$

$$V_{OUT} = V_{REF} \times \left[\frac{R5}{R6} + 1\right] \tag{5}$$

Choose R5 to be approximately 10 kΩ. Slightly increasing or decreasing R5 can result in closer output voltage matching when using standard value resistors. In this design, R4 = 10.2 kΩ and R = 4.75 kΩ, resulting in a 2.5-V output voltage.

8.2.2.3 Input Capacitors

The TPS54332 requires an input decoupling capacitor and depending on the application, a bulk-input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value may be used as long as all other requirements are met; however 10 µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54332 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design, a single 10-µF capacitor is used for the input decoupling capacitor. It is X5R dielectric rated for 25 V. The equivalent series resistance (ESR) is approximately 3 mΩ, and the current rating is 3 A.

This input ripple voltage can be approximated by Equation 6.

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \tag{6}$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency (derated by a factor of 0.8), C_{BULK} is the bulk capacitor value and ESR_{MAX} is the maximum series resistance of the bulk capacitor.

The maximum RMS imput ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 7.

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \tag{7}$$

In this case, the input ripple voltage would be 98 mV and the RMS ripple current would be 1.75 A. It is also important to note that the actual input voltage ripple will be greatly affected by parasitic associated with the layout and the output impedance of the voltage source. The actual input voltage ripple for this circuit is shown in *Design Parameters* and is larger than the calculated value. This measured value is still below the specified input limit of 200 mV. The maximum voltage across the input capacitors would be VIN max plus ΔVIN/2. The chosen bypass capacitor is rated for 25 V and the ripple current capacity is greater than 3 A, providing ample margin. It is important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Copyright © 2009–2014, Texas Instruments Incorporated

8.2.2.4 Output Filter Components

Two components need to be selected for the output filter, the output inductor L1 and the output capacitance. Since the TPS54332 is an externally compensated device, a wide range of filter component types and values can be supported.

8.2.2.5 Inductor Selection

To calculate the minimum value of the output inductor, use Equation 8.

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW} \times 0.8} \quad (8)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.4 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated to be 2.48 µH. For this design, a l 2.5-µH inductor is chosen.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The peak-to-peak inductor current is calculated using Equation 9.

$$I_{LPP} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \quad (9)$$

The RMS inductor current can be found from Equation 10.

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \quad (10)$$

And the peak inductor current can be determined with Equation 11.

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (11)$$

(12)

For this design, the RMS inductor current is 3.51 A and the peak inductor current is 4.15 A. The chosen inductor is a Coilcraft MSS1038-252NX_ 2.5-µH. It has a saturation current rating of 7.62 A and an RMS current rating of 6.55 A, meeting these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wishes to allow so long as the other design requirements are met. Larger value inductors will have lower AC current and result in lower output voltage ripple, while smaller inductor values will increase ac current and output voltage ripple. In general, inductor values for use with the TPS54332 are in the range of 1 µH to 47 µH.

8.2.2.6 Capacitor Selection

The important design factors for the output capacitor are DC voltage rating, ripple current rating, and equivalent series resistance (ESR). The DC voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed-loop crossover frequency at less than 1/5 of the switching frequency. With high-switching frequencies such as the 1 MHz frequency of this design, internal circuit limitations of the TPS54332 limit the practical maximum crossover frequency to about 75 kHz. In general, the closed-loop crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

Copyright © 2009–2014, Texas Instruments Incorporated

$$C_{O_MIN} = 1/(2 \times \pi \times R_O \times F_{CO_MAX}) \quad (13)$$

Where R_O is the output load impedance (V_O/I_O) and f_{CO} is the desired crossover frequency. For a desired maximum crossover of 75 kHz the minimum value for the output capacitor is around 3.2 µF. This may not satisfy the output ripple voltage requirement. The output ripple voltage consists of two components; the voltage change due to the charge and discharge of the output filter capacitance and the voltage change due to the ripple current times the ESR of the output filter capacitor. The output ripple voltage can be estimated by:

$$V_{OPP} = I_{LPP}\left[\frac{(D - 0.5)}{4 \times F_{SW} \times C_O} + R_{ESR}\right] \quad (14)$$

Where C_O is the total effective output capacitance.

The maximum ESR of the output capacitor can be determined from the amount of allowable output ripple as specified in the initial design parameters. The contribution to the output ripple voltage due to ESR is the inductor ripple current times the ESR of the output filter, so the maximum specified ESR as listed in the capacitor data sheet is given by Equation 15.

$$ESR_{max} = \frac{V_{OPPMAX}}{I_{LPP}} - \frac{(D - 0.5)}{4 \times F_{SW} \times C_O} \quad (15)$$

Where V_{OPPMAX} is the desired maximum peak-to-peak output ripple. The maximum RMS ripple current in the output capacitor is given by Equation 16.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C}\right) \quad (16)$$

The minimum switching frequency should be used in the above equations (derated by a factor of 0.8). For this design example, two 47-µF ceramic output capacitors are chosen for C2 and C3. These are rated at 10 V with a maximum ESR of 3 mΩ and a ripple current rating in excess of 3 A. The calculated total RMS ripple current is 300 mA (150 mA each) and the total ESR required is 20 mΩ or less. These output capacitors exceed the requirements by a wide margin and will result in a reliable, high-performance design. it is important to note that the actual capacitance in circuit may be less than the catalog value when the output is operating at the desired output of 2.5 V. 10-V rated capacitors are used to minimize the this reduction in capacitance due to dc voltage on the output. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus ½ the ripple voltage. Any derating amount must also be included. Other capacitor types work well with the TPS54332, depending on the needs of the application.

8.2.2.7 Compensation Components

The external compensation used with the TPS54332 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses ceramic X5R dielectric output capacitors, but other types are supported.

A Type II compensation scheme is recommended for the TPS54332. The compensation components are chosen to set the desired closed-loop crossover frequency and phase margin for output filter components. The type II compensation has the following characteristics; a DC gain component, a low-frequency pole, and a mid-frequency zero or pole pair.

The DC gain is determined by Equation 17.

$$G_{DC} = \frac{V_{ggm} \times V_{REF}}{V_O} \quad (17)$$

Where:

V_{ggm} = 800
V_{REF} = 0.8 V

The low-frequency pole is determined by Equation 18.

Copyright © 2009–2014, Texas Instruments Incorporated

$$F_{PO} = 1/(2 \times \pi \times R_{OO} \times C_Z) \quad (18)$$

R_{OA} = 8.696 MΩ.

The mid-frequency zero is determined by Equation 19.

$$F_{Z1} = 1/(2 \times \pi \times R_Z \times C_Z) \quad (19)$$

And, the mid-frequency pole is given by Equation 20.

$$F_{P1} = 1/(2 \times \pi \times R_Z \times C_P) \quad (20)$$

The first step is to choose the closed-loop crossover frequency. The closed-loop crossover frequency should be less than 1/8 of the minimum operating frequency, but for the TPS54332 it is recommended that the maximum closed-loop crossover frequency be not greater than 75 kHz. Next, the required gain and phase boost of the crossover network needs to be calculated. By definition, the gain of the compensation network must be the inverse of the gain of the modulator and output filter. For this design example, where the ESR zero is much higher than the closed-loop crossover frequency, the gain of the modulator and output filter can be approximated by Equation 21.

$$\text{Gain} = -20 \log(2 \times \pi \times R_{SENSE} \times F_{CO} \times C_O) \quad (21)$$

Where:

R_{SENSE} = 1 Ω / 12
F_{CO} = Closed-loop crossover frequency
C_O = Output capacitance

The phase loss is given by Equation 22.

$$PL = a\tan(2 \times \pi \times F_{CO} \times R_{ESR} \times C_O) - a\tan(2 \times \pi \times F_{CO} \times R_O \times C_O) - 10\text{dB} \quad (22)$$

Where:

R_{ESR} = Equivalent series resistance of the output capacitor
$R_O = V_O/I_O$

The measured overall loop response for the circuit is given in Figure 20. Note that the actual closed-loop crossover frequency is higher than intended at about 25 kHz. This is primarily due to variation in the actual values of the output filter components and tolerance variation of the internal feed-forward gain circuitry. Overall the design has greater than 60 degrees of phase margin and will be completely stable over all combinations of line and load variability.

Now that the phase loss is known the required amount of phase boost to meet the phase margin requirement can be determined. The required phase boost is given by Equation 23.

$$PB = (PM - 90\,\text{DEG}) - PL \quad (23)$$

Where PM = the desired phase margin.

A zero / pole pair of the compensation network will be placed symmetrically around the intended closed-loop frequency to provide maximum phase boost at the crossover point. The amount of separation can be determined by Equation 24 and the resultant zero and pole frequencies are given by Equation 25 and Equation 26.

$$k = \text{TAN}\left(\frac{PB}{2} + 45\,\text{DEG}\right) \quad (24)$$

$$F_{Z1} = \frac{F_{CO}}{k} \quad (25)$$

$$F_{P1} = F_{CO} \times k \quad (26)$$

Copyright © 2009–2014, Texas Instruments Incorporated

The low-frequency pole is set so that the gain at the crossover frequency is equal to the inverse of the gain of the modulator and output filter. Due to the relationships established by the pole and zero relationships, the value of R_Z can be derived directly by Equation 27 .

$$R_Z = \frac{2 \times \pi \times F_{CO} \times V_O \times C_O \times R_{OA}}{GM_{ICOMP} \times V_{ggm} \times V_{REF}} \quad (27)$$

Where:

V_O = Output voltage
C_O = Output capacitance
F_{CO} = Desired crossover frequency
R_{OA} = 8.696 MΩ
GM_{COMP} = 12 A/V
V_{ggm} = 800
V_{REF} = 0.8 V

With R_Z known, C_Z and C_P can be calculated using Equation 28 and Equation 29.

$$C_Z = \frac{1}{2 \times \pi \times F_{Z1} \times R_z} \quad (28)$$

$$C_P = \frac{1}{2 \times \pi \times F_{P1} \times R_z} \quad (29)$$

For this design, the two 47-µF output capacitors are used. For ceramic capacitors, the actual output capacitance is less than the rated value when the capacitors have a DC bias voltage applied. This is the case in a dc/dc converter. The actual output capacitance may be as low as 54 µF. The combined ESR is approximately .001 Ω.

Using Equation 21 and Equation 22, the output stage gain and phase loss are equivalent as:

Gain = –6.94 dB

and

PL - –93.94 degrees

For 70 degrees of phase margin, Equation 23 requires 63.64 degrees of phase boost.

Equation 24, Equation 25, and Equation 26 are used to find the zero and pole frequencies of:

F_{Z1} = 11.57 kHz

And

F_{P1} = 216 kHz

R_Z, C_Z, and C_P are calculated using Equation 27, Equation 28, and Equation 29.

$$Rz = \frac{2 \times \pi \times 50000 \times 2.5 \times 82 \times 10^{-6} \times 8.696 \times 10^{6}}{12 \times 800 \times 0.8} = 72.92\ k\Omega \quad (30)$$

$$Cz = \frac{1}{2 \times \pi \times 11570 \times 75000} = 183\ pF \quad (31)$$

$$Cp = \frac{1}{2 \times \pi \times 216000 \times 75000} = 9.8\ pF \quad (32)$$

Using standard values for R3, C6, and C7 in the application schematic of Figure 12.

R3 = 75 kΩ

C6 = 180 pF

C7 = 10 pF

Copyright © 2009–2014, Texas Instruments Incorporated

8.2.2.8 Bootstrap Capacitor

Every TPS54332 design requires a bootstrap capacitor, C4. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT pin. The bootstrap capacitor should be a high-quality, ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.9 Catch Diode

The TPS54332 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is Vin(max) + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak-to-peak inductor current. Forward-voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A is chosen, with a reverse voltage of 40 V, forward current of 3 A, and a forward voltage drop of 0.5 V.

8.2.2.10 Output Voltage Limitations

Due to the internal design of the TPS54332, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 91% and is given by Equation 33.

$$V_{O(max)} = 0.91 \times ((V_{IN(min)} - I_{O(max)} \times R_{DS(on)\,max}) + V_D) - (I_{O(max)} \times R_L) - V_D \quad (33)$$

Where:

$V_{IN(min)}$ = Minimum input voltage
$I_{O(max)}$ = Maximum load current
V_D = Catch diode forward voltage
R_L = Output inductor series resistance

The equation assumes maximum on resistance for the internal high-side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 130 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by Equation 32.

$$V_{O(min)} = 0.118 \times ((V_{IN(max)} - I_{Omin} \times R_{DS(on)\,max}) + V_D) - I_{O(min)} \times R_L) - V_D \quad (34)$$

Where:

$V_{IN(max)}$ = Maximum input voltage
$I_{O(min)}$ = Minimum load current
V_D = Catch diode forward voltage
R_L = Output inductor series resistance

This equation assumes nominal on-resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

8.2.2.11 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse-skipping Eco-Mode.

The device power dissipation includes:

1. Conduction loss: $P_{con} = I_{out}^2 \times R_{DS(on)} \times V_{OUT}/VIN$
2. Switching loss: $P_{sw} = 0.55 \times 10^{-9} \times VIN^2 \times I_{OUT} \times F_{sw}$
3. Gate charge loss: $P_{gc} = 22.8 \times 10^{-9} \times F_{sw}$
4. Quiescent current loss: $P_q = 0.082 \times 10^{-3} \times VIN$

Where:

I_{OUT} is the output current (A).

Copyright © 2009–2014, Texas Instruments Incorporated

$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
V_{OUT} is the output voltage (V).
VIN is the input voltage (V).
Fsw is the switching frequency (Hz).
So

Ptot = Pcon + Psw + Pgc + Pq

For given T_A , $T_J = T_A + Rth \times Ptot$.

For given T_{JMAX} = 150°C, $T_{AMAX} = T_{JMAX} – Rth \times Ptot$.

Where:

Ptot is the total device power dissipation (W).

T_A is the ambient temperature (°C).

T_J is the junction temperature (°C) .

Rth is the thermal resistance of the package (°C/W).

T_{JMAX} is maximum junction temperature (°C).

T_{AMAX} is maximum ambient temperature (°C).

Copyright © 2009–2014, Texas Instruments Incorporated

8.2.3 Application Curves

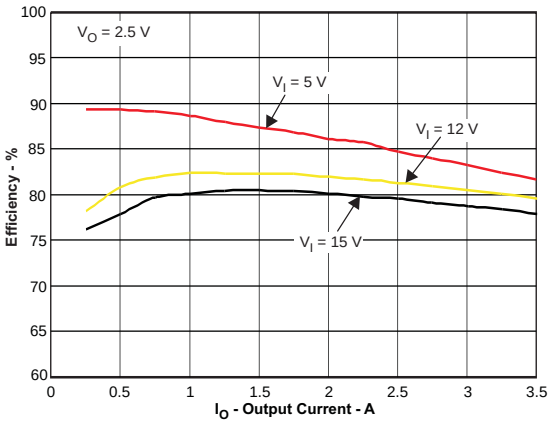


Figure 13. TPS54332 Efficiency

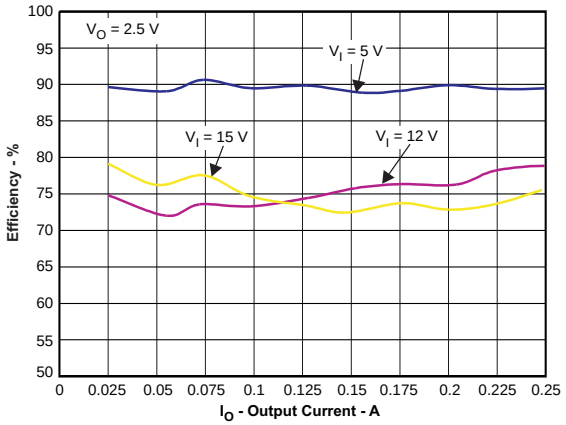


Figure 14. TPS54332 Low-Current Efficiency

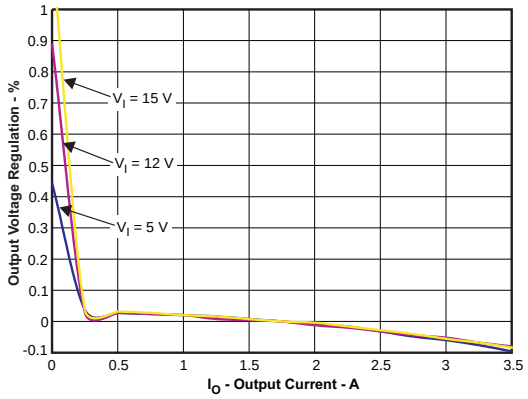


Figure 15. TPS54332 Load Regulation

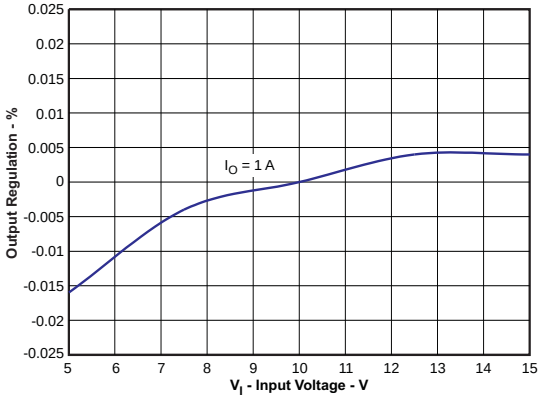


Figure 16. TPS54332 Line Regulation

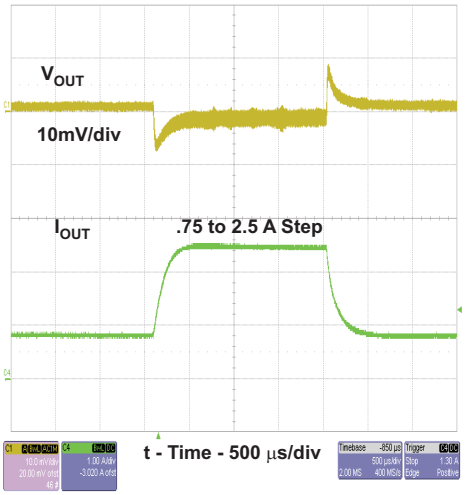


Figure 17. TPS54332 Transient Response

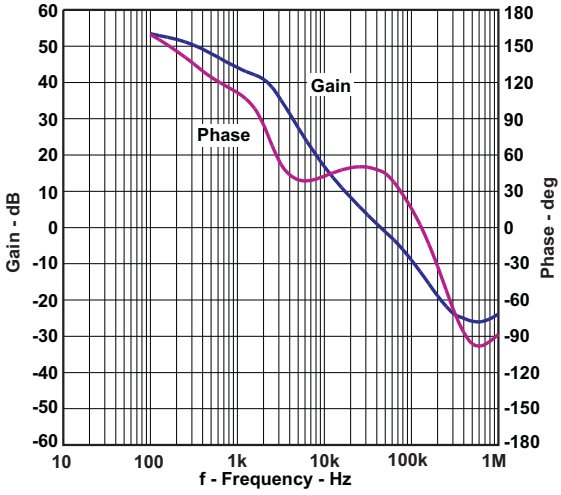


Figure 18. TPS54332 Loop Response

Copyright © 2009–2014, Texas Instruments Incorporated

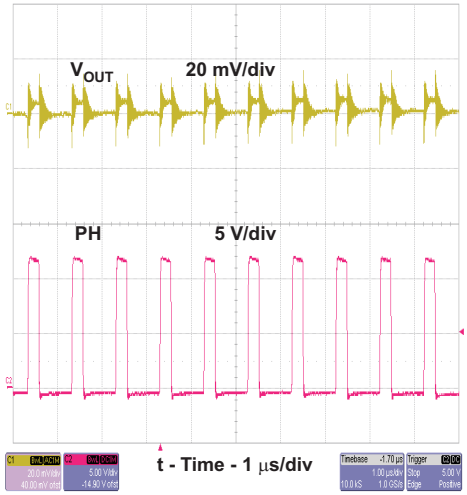


Figure 19. TPS54332 Output Ripple

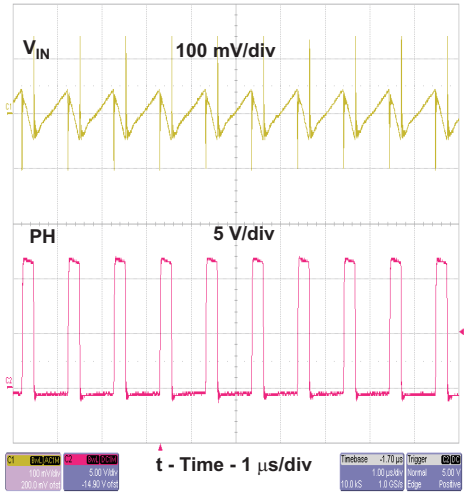


Figure 20. TPS54332 Input Ripple

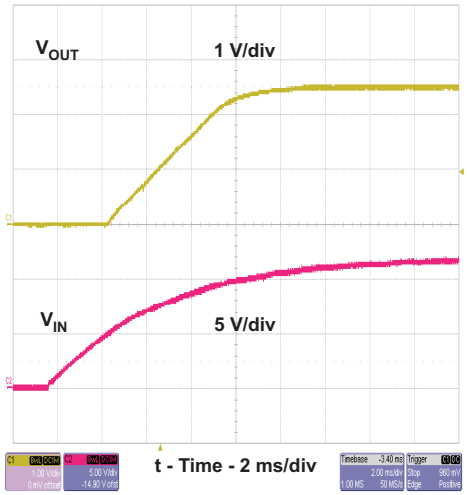


Figure 21. TPS54332 Start-Up

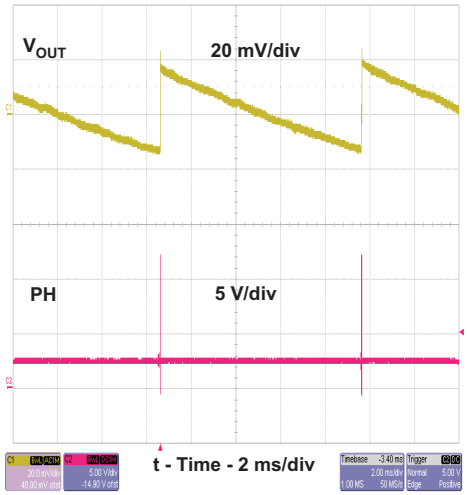


Figure 22. TPS54332 Output Ripple during Eco-Mode Operation

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 28 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR, ceramic bypass capacitor. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. See Figure 23 for a PCB layout example. The GND D pin should be tied to the PCB ground plane at the pin of the IC. The source of the low-side MOSFET should be connected directly to the top-side PCB ground area used to tie together the ground sides of the input and output capacitors, as well as the anode of the catch diode. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top-side ground area must provide adequate heat dissipating area. The TPS54332 uses a fused lead frame so that the GND pin acts as a conductive path for heat dissipation from the die. Many applications have larger areas of internal or back side ground plane available, and the top-side ground area can be connected to these areas using multiple vias under or adjacent to the device to help dissipate heat. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

Copyright © 2009–2014, Texas Instruments Incorporated

10.2 Layout Example

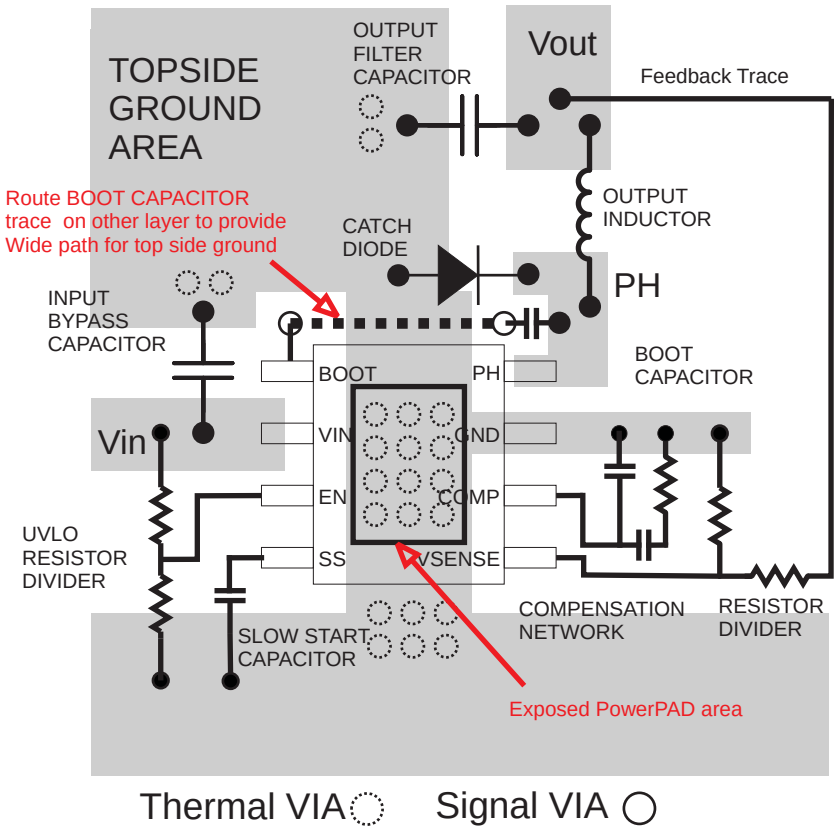


Figure 23. TPS54332 Board Layout

10.3 Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 12 is 0.58 in^2. This area does not include test points or connectors.

10.4 Electromagnetic Interference (EMI) Considerations

As EMI becomes a rising concern in more and more applications, the internal design of the TPS54332 takes measures to reduce the EMI. The high-side MOSFET gate-drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the *Detailed Design Procedure* to prevent potential EMI issues.

Copyright © 2009–2014, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For the WEBENCH Tool, go to http://www.ti.com/lsds/ti/analog/webench/overview.page.

11.2 Trademarks

Eco-Mode, PowerPAD, WEBENCH are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

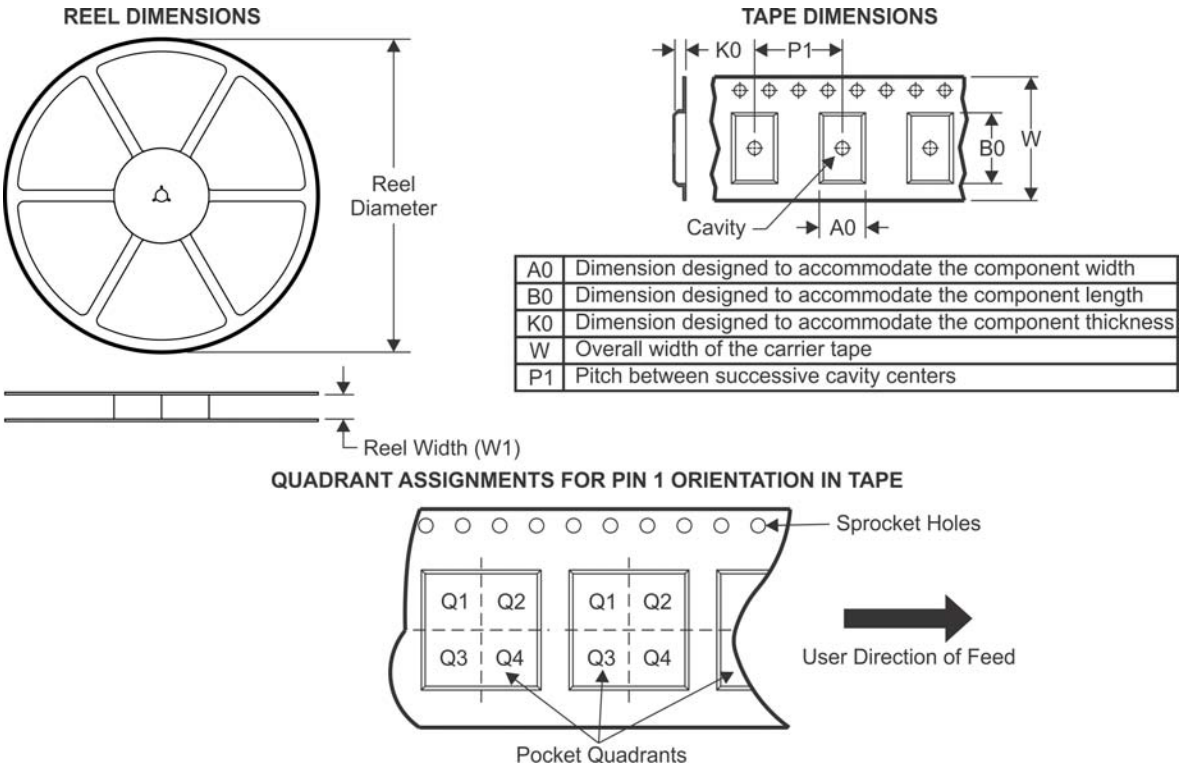
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2009–2014, Texas Instruments Incorporated

TAPE AND REEL INFORMATION

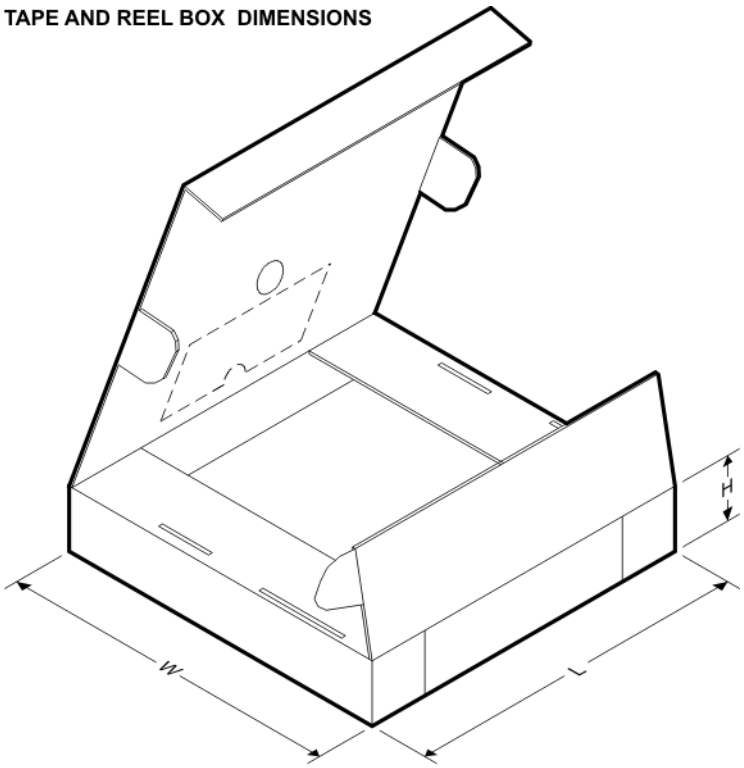


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54332DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

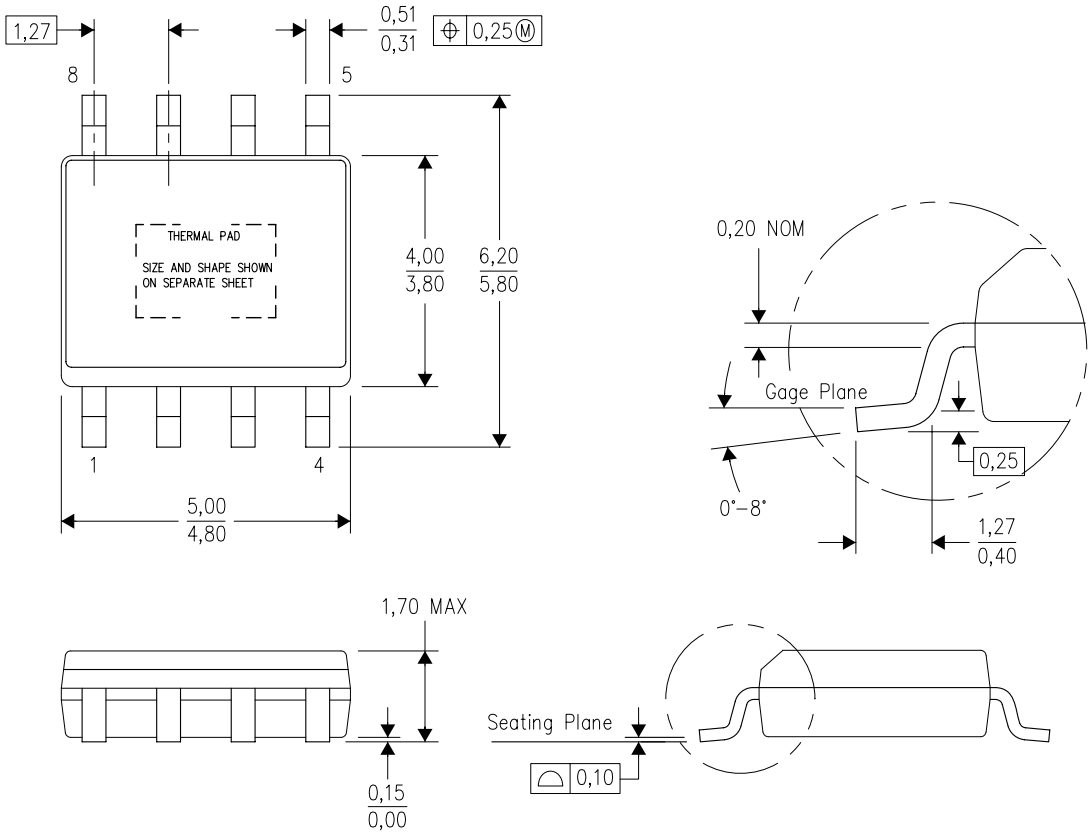
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54332DDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

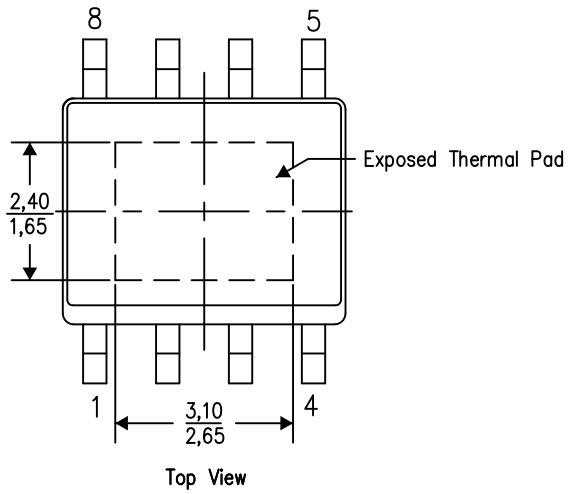
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



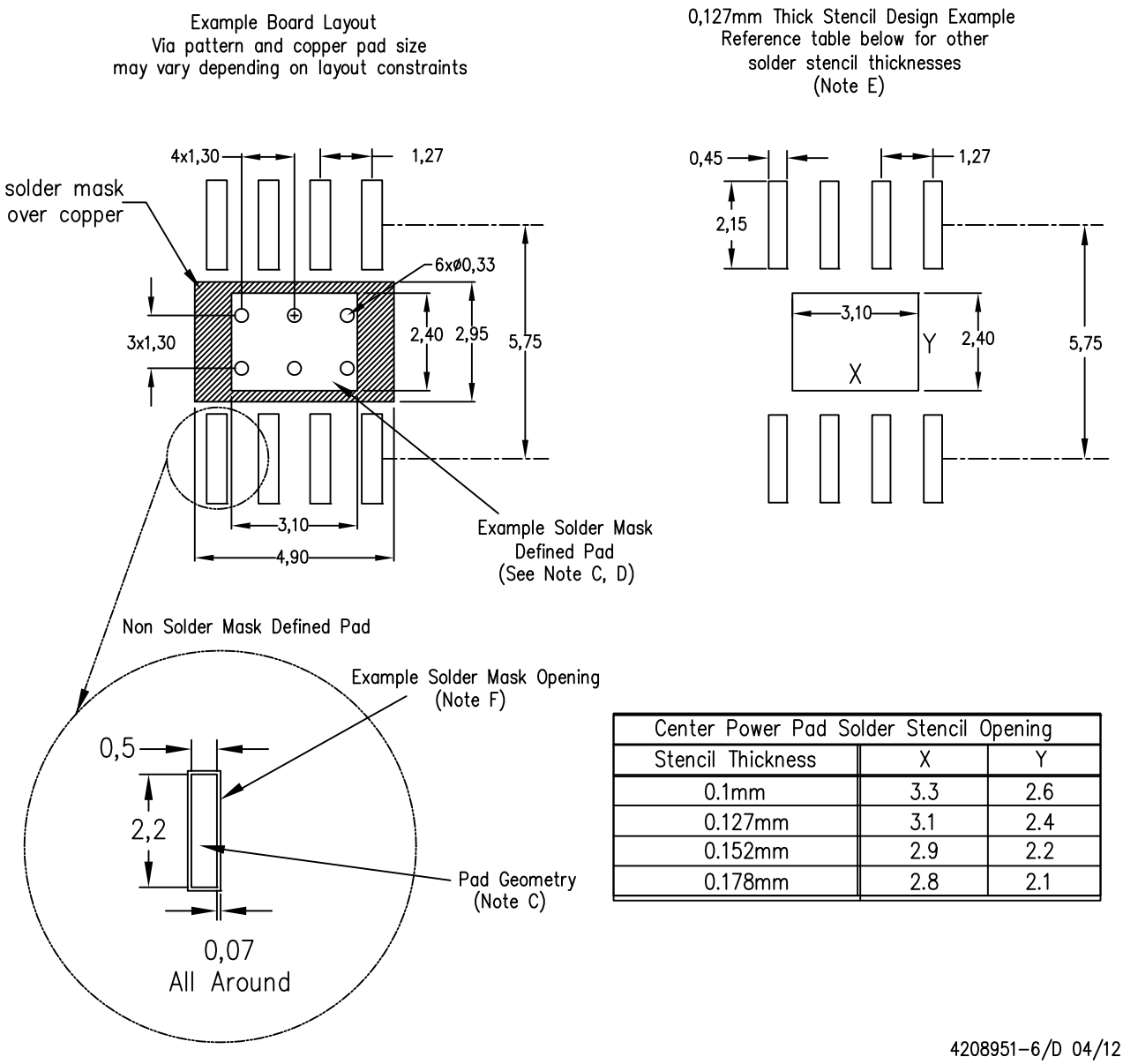
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951–6/D 04/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

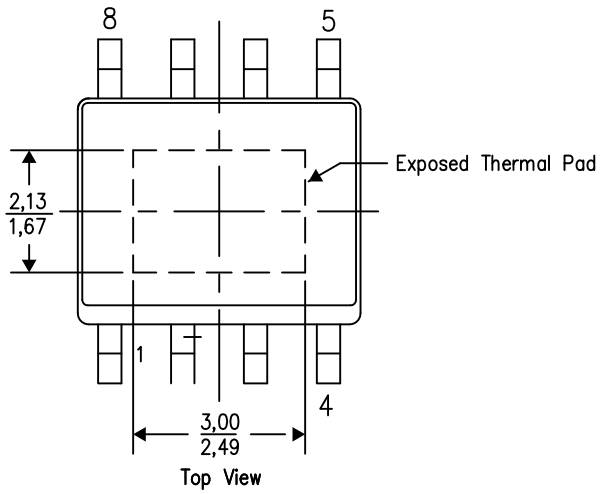
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



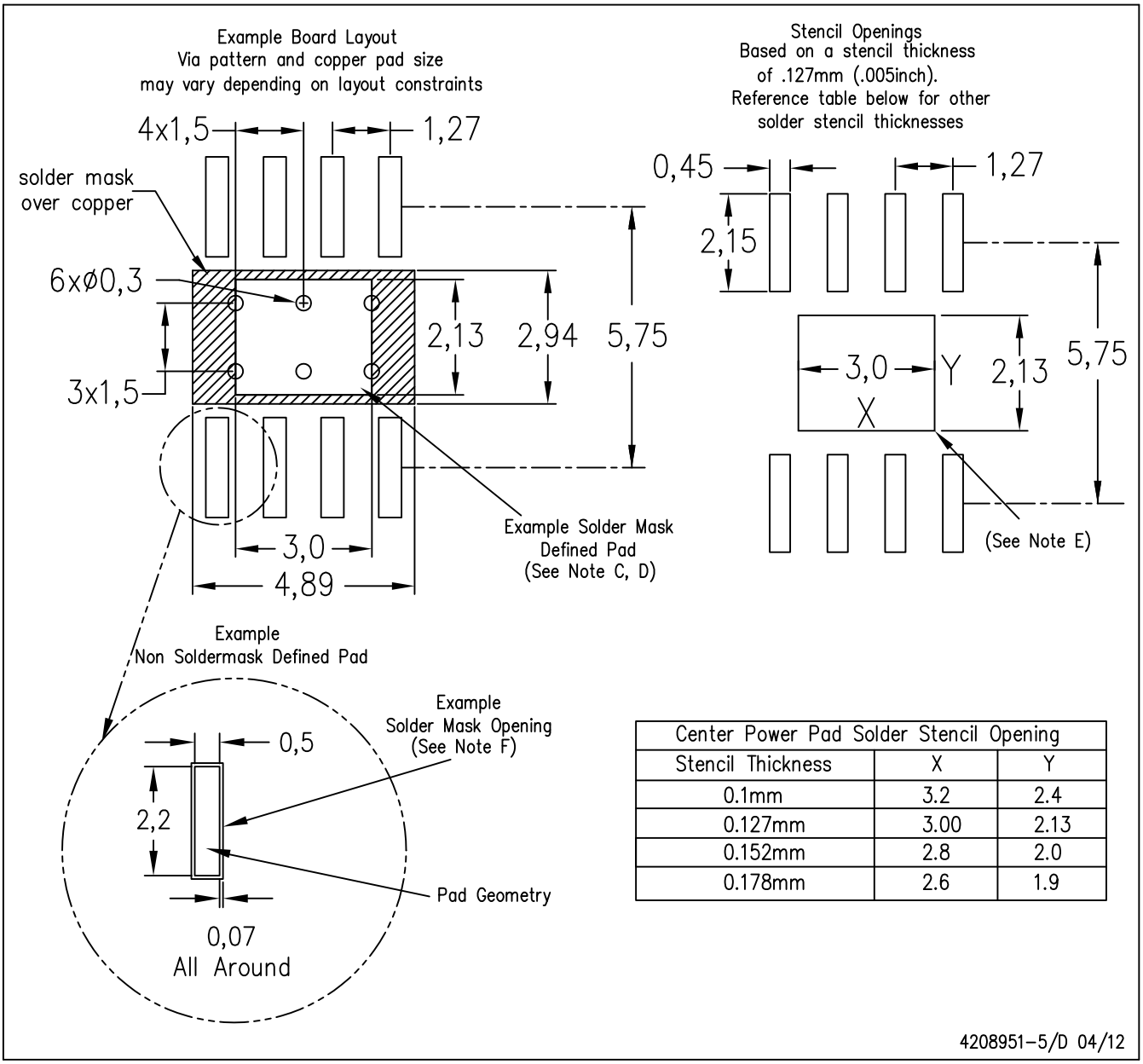
Exposed Thermal Pad Dimensions

4206322–5/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	2.4
0.127mm	3.00	2.13
0.152mm	2.8	2.0
0.178mm	2.6	1.9

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated