# SMF05T1

# Quad Array for ESD Protection

## ESD Protection Diodes with Low Clamping Voltage

This quad monolithic silicon voltage suppressor is designed for applications requiring transient overvoltage protection capability. It is intended for use in voltage and ESD sensitive equipment such as computers, printers, business machines, communication systems, medical equipment, and other applications. Its quad junction common anode design protects four separate lines using only one package. These devices are ideal for situations where board space is at a premium.

**Specification Features**

- Low Clamping Voltage
- Stand Off Voltage 5 V
- Low Leakage < 5 μA @ 5 V
- SC−88A Package Allows Four Separate Unidirectional Configurations
- IEC6100−4−2 Level 4 ESD Protection
- Pb−Free Packages are Available*

**Mechanical Characteristics**

- Void Free, Transfer−Molded, Thermosetting Plastic Case
- Corrosion Resistant Finish, Easily Solderable
- Package Designed for Optimal Automated Board Assembly
- Small Package Size for High Density Applications

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Peak Power Dissipation @ 8 X 20 μs @$T_A \le$ 25°C | $P_{pk}$ | 200 | W |
| Steady State Power − 1 Diode (Note 1) | $P_D$ | 385 | mW |
| Thermal Resistance Junction−to−Ambient<br>Above 25°C, Derate | $R_{\theta JA}$ | <br>325<br>3.1 | <br>°C/W<br>mW/°C |
| Maximum Junction Temperature | $T_{Jmax}$ | 150 | °C |
| Operating Junction and Storage Temperature Range | $T_J$ $T_{stg}$ | −55 to +150 | °C |
| ESD Discharge<br>IEC61000−4−2, Air Discharge<br>IEC61000−4−2, Contact Discharge | | <br>30<br>30 | kV |
| Lead Solder Temperature (10 seconds duration) | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

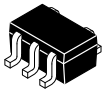
1. Only 1 diode under power. For all 4 diodes under power, $P_D$ will be 25%. Mounted on FR−4 board with min pad.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

See Application Note AND8308/D for further description of survivability specs.

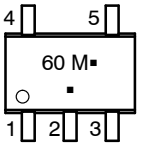
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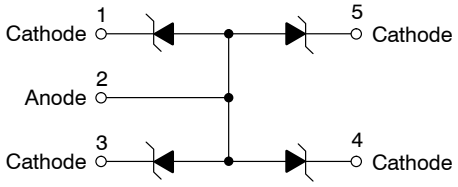


**SC−88A/SOT−323**
**CASE 419A**
**STYLE 5**

**MARKING DIAGRAM**




60 = Device Marking
M = One Digit Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)




**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| SMF05T1 | SC−88A | 3000/Tape & Reel |
| SMF05T1G | SC−88A (Pb−Free) | 3000/Tape & Reel |
| SMF05T2G | SC−88A (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

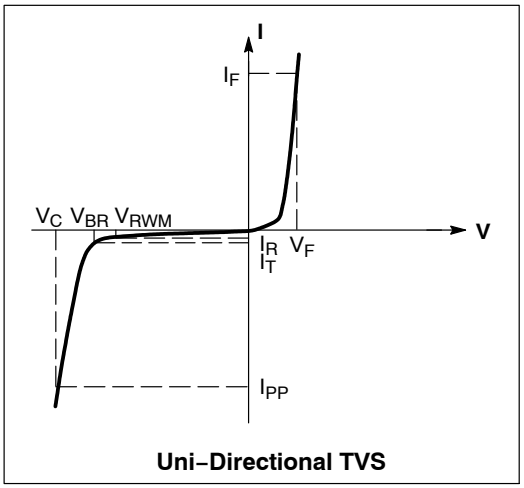
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## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Reverse Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Working Peak Reverse Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $I_F$ | Forward Current |
| $V_F$ | Forward Voltage @ $I_F$ |
| $P_{pk}$ | Peak Power Dissipation |
| C | Capacitance @ $V_R$ = 0 and f = 1.0 MHz |

*See Application Note AND8308/D for detailed explanations of datasheet parameters.




**Uni−Directional TVS**

## ELECTRICAL CHARACTERISTICS

| Device | Breakdown Voltage $V_{BR}$ @ 1 mA (V) | | Leakage Current $I_R$ @ $V_{RWM}$ = 5 V (μA) | Capacitance @ 0 V Bias (pF) | Max $V_F$ @ $I_F$ = 200 mA (V) | Max Clamping Voltage ($V_C$) @ $I_{PP}$ (Note 2) | | Max Clamping Voltage ($V_C$) @ $I_{PP}$ (Note 2) | | $V_C$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Max | Max | | $I_{PP}$ (A) | $V_C$ (V) | $I_{PP}$ (A) | $V_C$ (V) | Per IEC61000−4−2 (Note 3) |
| SMF05 | 6.0 | 7.2 | 5.0 | 90 | 1.25 | 1.0 | 9.5 | 12 | 12.5 | Figures 1 and 2 See Below |

2. Non−repetitive current per Figure 5. Derate per Figure 6.
3. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

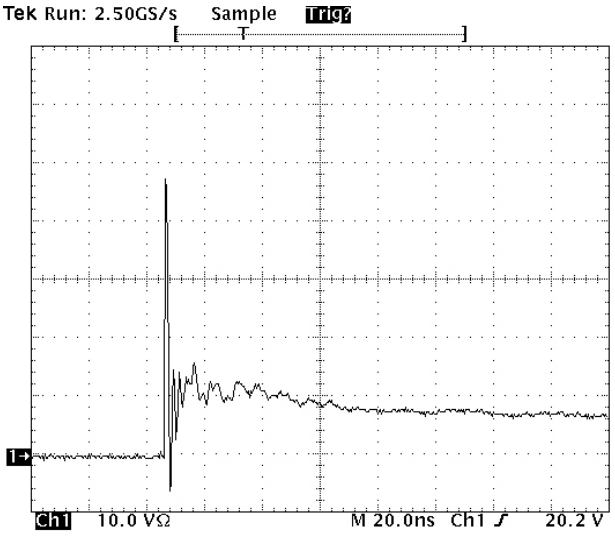



**Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2**

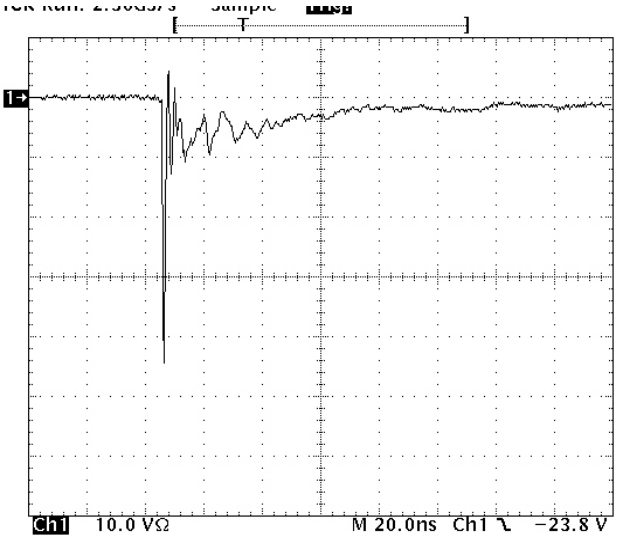



**Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2**

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

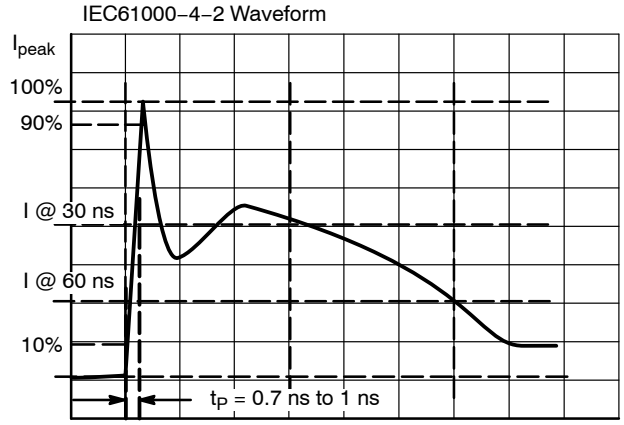



**Figure 3. IEC61000−4−2 Spec**

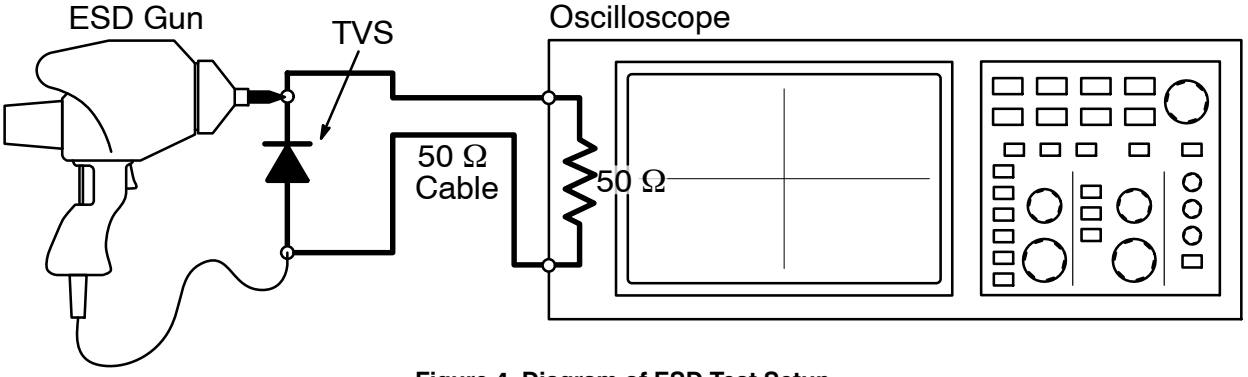



**Figure 4. Diagram of ESD Test Setup**

**The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.**

**ESD Voltage Clamping**

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

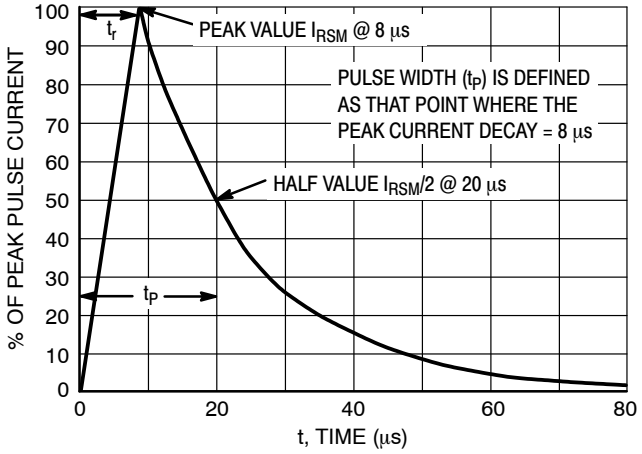



**Figure 5. 8 X 20 μs Pulse Waveform**

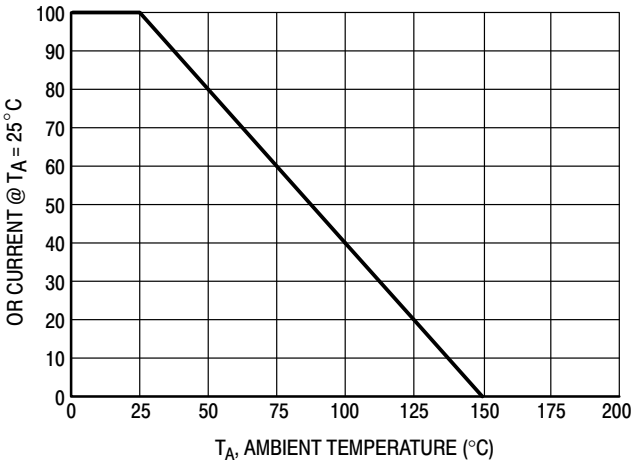



**Figure 6. Pulse Derating Curve**

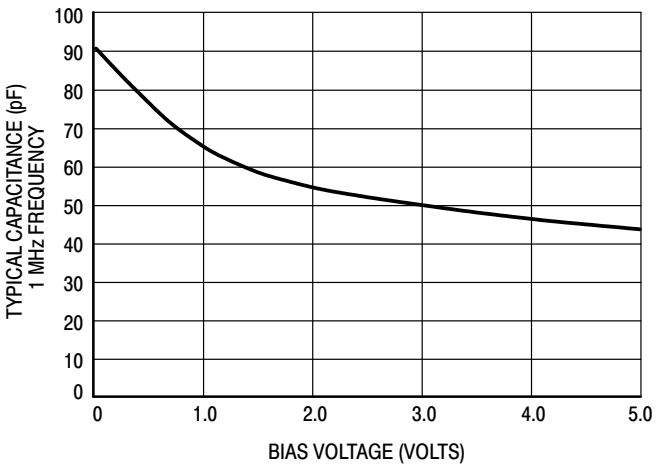



**Figure 7. Capacitance**

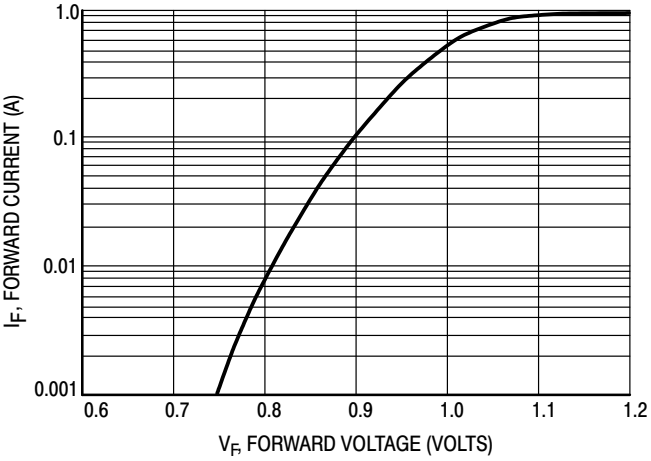



**Figure 8. Forward Voltage**

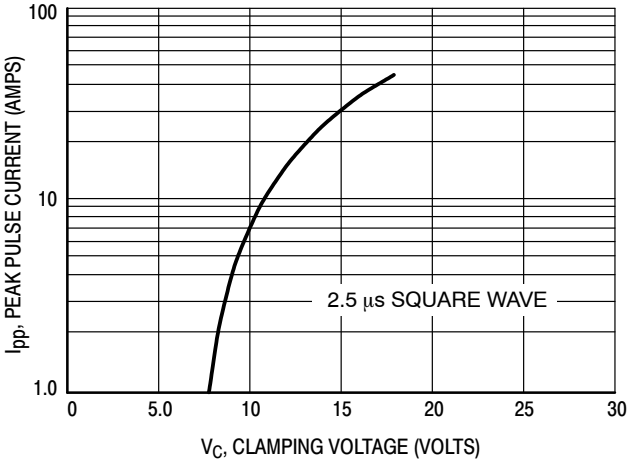



**Figure 9. Clamping Voltage versus Peak Pulse Current (Reverse Direction)**

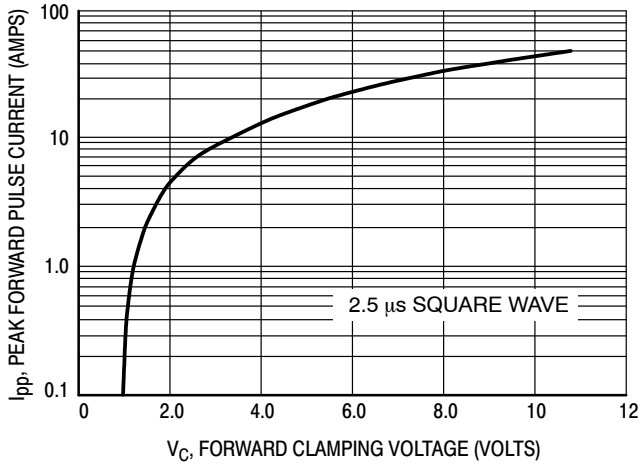



**Figure 10. Clamping Voltage versus Peak Pulse Current (Forward Direction)**

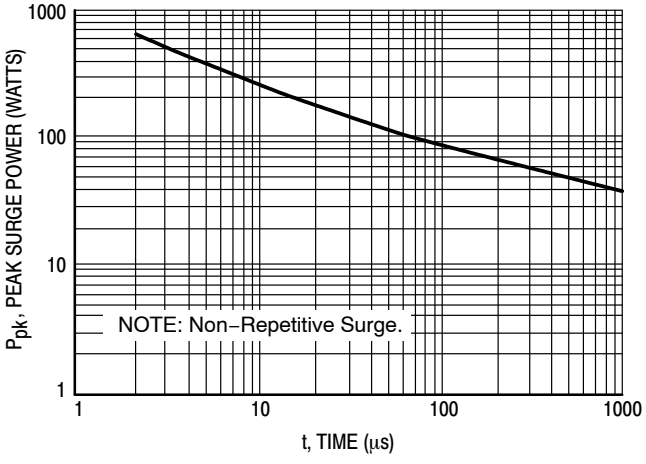
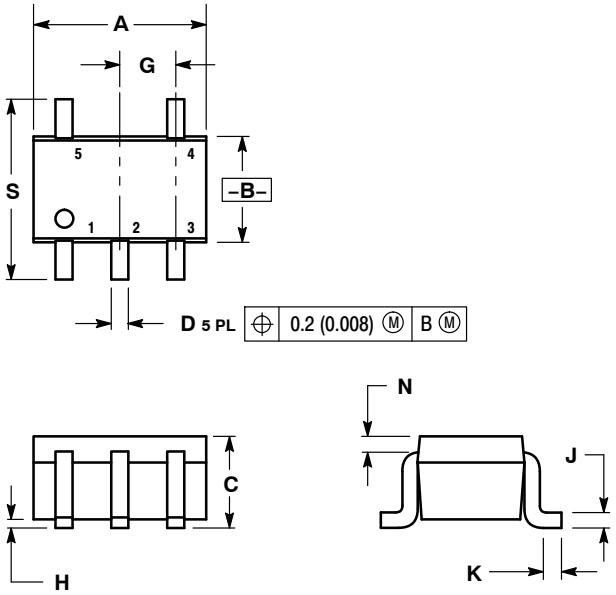



**Figure 11. Pulse Width**

## PACKAGE DIMENSIONS

**SC−88A/SOT−353/SC−70**
5−LEAD PACKAGE
CASE 419A−02
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

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