Multiphase PWM Regulator for IMVP-6.5™ Mobile CPUs

ISL62883, ISL62883B

The ISL62883 is a multiphase PWM buck regulator for miroprocessor core power supply. The multiphase buck converter uses interleaved phase to reduce the total output voltage ripple with each phase carrying a portion of the total load current, providing better system performance, superior thermal management, lower component cost, reduced power dissipation, and smaller implementation area. The ISL62883 uses two integrated gate drivers and an external gate driver to provide a complete solution. The PWM modulator is based on Intersil's Robust Ripple Regulator (R^3) technology™. Compared with traditional modulators, the R^3™ modulator commands variable switching frequency during load transients, achieving faster transient response. With the same modulator, the switching frequency is reduced at light load, increasing the regulator efficiency.

The ISL62883 is fully compliant with IMVP-6.5™ specifications. It responds to PSI# and DPRSLPVR signals by adding or dropping PWM3 and Phase-2 respectively, adjusting overcurrent protection threshold accordingly, and entering/exiting diode emulation mode. It reports the regulator output current through the IMON pin. It senses the current by using either a discrete resistor or inductor DCR whose variation over temperature can be thermally compensated by a single NTC thermistor. It uses differential remote voltage sensing to accurately regulate the processor die voltage. The adaptive body diode conduction time reduction function minimizes the body diode conduction loss in diode emulation mode. User-selectable overshoot reduction function offers an option to aggressively reduce the output capacitors as well as the option to disable it for users concerned about increased system thermal stress. In 2-Phase configuration, the ISL62883 offers the FB2 function to optimize 1-Phase performance.

The ISL62883B has the same functions as the ISL62883, but comes in a different package.

Features

- Precision Multiphase Core Voltage Regulation
  - 0.5% System Accuracy Over-Temperature
  - Enhanced Load Line Accuracy
- Microprocessor Voltage Identification Input
  - 7-Bit VID Input, 0.300V to 1.500V in 12.5mV Steps
  - Supports VID Changes On-The-Fly
- Supports Multiple Current Sensing Methods
  - Lossless Inductor DCR Current Sensing
  - Precision Resistor Current Sensing
- Supports PSI# and DPRSLPVR modes
- Superior Noise Immunity and Transient Response
- Current Monitor and Thermal Monitor
- Differential Remote Voltage Sensing
- High Efficiency Across Entire Load Range
- Programmable 1-, 2- or 3-Phase Operation
- Two Integrated Gate Drivers
- Excellent Dynamic Current Balance Between Phases
- FB2 Function in 2-Phase Configuration to Optimize 1-Phase Performance
- Adaptive Body Diode Conduction Time Reduction
- User-selectable Overshoot Reduction Function
- Small Footprint 40 Ld 5x5 or 48 Ld 6x6 TQFN Package
- Pb-Free (RoHS Compliant)

Applications

- Notebook Computers

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

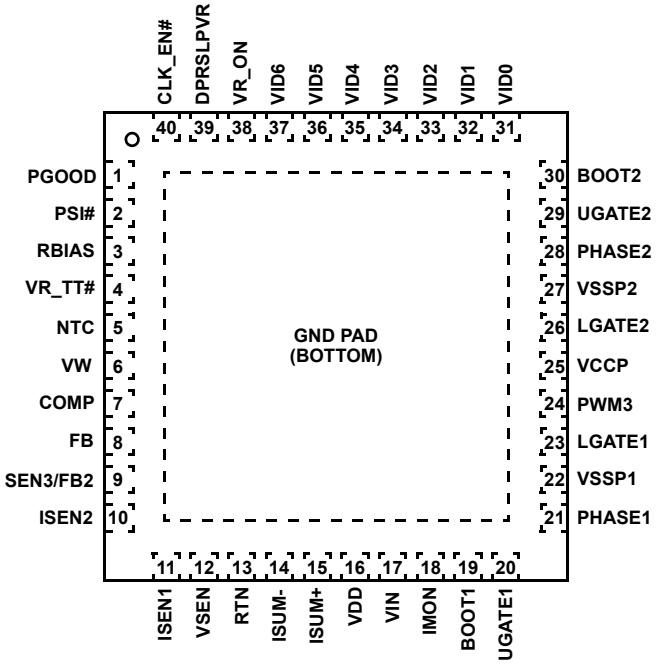
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL62883HRTZ	62883 HRTZ	-10 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL62883IRTZ	62883 IRTZ	-40 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL62883BHRTZ	62883 BHRTZ	-10 to +100	48 Ld 6x6 TQFN	L48.6x6

NOTES:

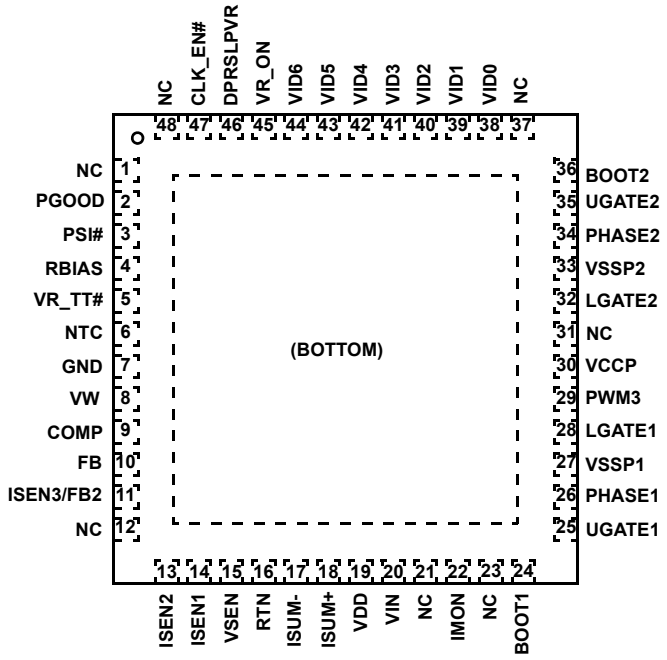
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL62883, ISL62883B. For more information on MSL please see techbrief TB363.

Pin Configurations

ISL62883
(40 LD TQFN)
TOP VIEW



ISL62883B
(48 LD TQFN)
TOP VIEW



Pin Function Descriptions

GND

Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

PGOOD

Power-Good open-drain output indicating when the regulator is able to supply regulated voltage. Pull-up externally with a 680Ω resistor to VCCP or 1.9kΩ to 3.3V.

PSI#

Low load current indicator input. When asserted low, indicates a reduced load-current condition. For ISL62883, when PSI# is asserted low, PWM3 will be disabled.

RBIAS

147k resistor to GND sets internal current reference.

VR_TT#

Thermal overload output indicator.

NTC

Thermistor input to VR_TT# circuit.

VW

A resistor from this pin to COMP programs the switching frequency (8kΩ gives approximately 300kHz).

COMP

This pin is the output of the error amplifier. Also, a resistor across this pin and GND adjusts the overcurrent threshold.

FB

This pin is the inverting input of the error amplifier.

ISEN3/FB2

When the ISL62883 is configured in 3-phase mode, this pin is ISEN3. ISEN3 is the individual current sensing for phase 3. When the ISL62883 is configured in 2-phase mode, this pin is FB2. There is a switch between the FB2 pin and the FB pin. The switch is on in 2-phase mode and is off in 1-phase mode. The components connecting to FB2 are used to adjust the compensation in 1-phase mode to achieve optimum performance.

ISEN2

Individual current sensing for Phase-2. When ISEN2 is pulled to 5V VDD, the controller will disable Phase-2 and allow other phases to operate.

ISEN1

Individual current sensing for Phase-1.

VSEN

Remote core voltage sense input. Connect to microprocessor die.

RTN

Remote voltage sensing return. Connect to ground at microprocessor die.

ISUM- and ISUM+

Droop current sense input.

VDD

5V bias power.

VIN

Battery supply voltage, used for feed-forward.

IMON

An analog output. IMON outputs a current proportional to the regulator output current.

BOOT1

Connect an MLCC capacitor across the BOOT1 and the PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT1 pin, each time the PHASE1 pin drops below VCCP minus the voltage dropped across the internal boot diode.

UGATE1

Output of the Phase-1 high-side MOSFET gate driver. Connect the UGATE1 pin to the gate of the Phase-1 high-side MOSFET.

PHASE1

Current return path for the Phase-1 high-side MOSFET gate driver. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase-1.

VSSP1

Current return path for the Phase-1 low-side MOSFET gate driver. Connect the VSSP1 pin to the source of the Phase-1 low-side MOSFET through a low impedance path, preferably in parallel with the trace connecting the LGATE1 pin to the gate of the Phase-1 low-side MOSFET.

LGATE1

Output of the Phase-1 low-side MOSFET gate driver. Connect the LGATE1 pin to the gate of the Phase-1 low-side MOSFET.

PWM3

PWM output for Channel 3. When PWM3 is pulled to 5V VDD, the controller will disable Phase-3 and allow other phases to operate.

VCCP

Input voltage bias for the internal gate drivers. Connect +5V to the VCCP pin. Decouple with at least 1µF of an MLCC capacitor to VSSP1 and VSSP2 pins respectively.

LGATE2

Output of the Phase-2 low-side MOSFET gate driver. Connect the LGATE2 pin to the gate of the Phase-2 low-side MOSFET.

VSSP2

Current return path for the Phase-2 converter low-side MOSFET gate driver. Connect the VSSP2 pin to the source of the Phase-2 low-side MOSFET through a low impedance path, preferably in parallel with the trace connecting the LGATE2 pin to the gate of the Phase-2 low-side MOSFET.

PHASE2

Current return path for the Phase-2 high-side MOSFET gate driver. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase-2.

UGATE2

Output of the Phase-2 high-side MOSFET gate driver. Connect the UGATE2 pin to the gate of the Phase-2 high-side MOSFET.

BOOT2

Connect an MLCC capacitor across the BOOT2 and the PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT2 pin, each time the PHASE2 pin drops below VCCP minus the voltage dropped across the internal boot diode.

VID0, VID1, VID2, VID3, VID4, VID5, VID6

VID input with VID0 = LSB and VID6 = MSB.

VR_ON

Voltage regulator enable input. A high level logic signal on this pin enables the regulator.

DPRSLPVR

Deeper sleep enable signal. A high level logic signal on this pin indicates that the microprocessor is in deeper sleep mode.

CLK_EN#

Open drain output to enable system PLL clock. It goes low 13 switching cycles after V_{core} is within 10% of V_{boot}.

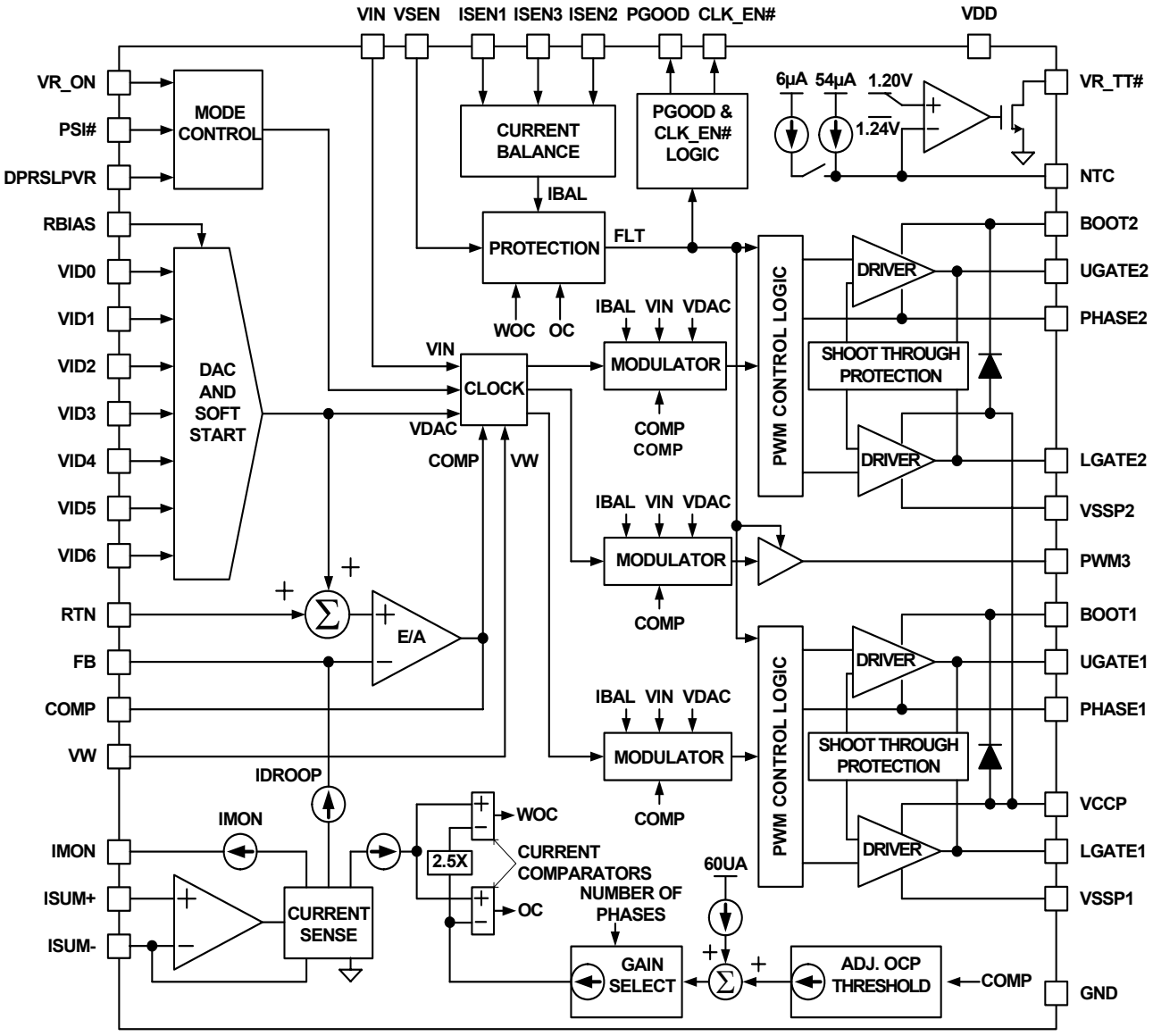
NC

No Connect.

BOTTOM (on ISL62883B)

The bottom pad of ISL62883B is electrically connected to the GND pin inside the IC.

Block Diagram



Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3V to +7V
Battery Voltage, VIN . . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE) . . . . . -0.3V to +7V(DC)
. . . . . -0.3V to +9V(<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE - 0.3V (DC) to BOOT
. . . . . PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage (LGATE) . . . . . -0.3V (DC) to VDD + 0.3V
. . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
All Other Pins . . . . . -0.3V to (VDD +0.3V)
Open Drain Outputs, PGOOD, VR_TT#,
CLK_EN# . . . . . -0.3V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld TQFN Package (Notes 4, 5)	32	3
48 Ld TQFN Package (Notes 4, 5)	29	2

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, VDD . . . . . +5V ±5%
Battery Voltage, VIN . . . . . +4.5V to 25V
Ambient Temperature
ISL62883HRTZ, ISL62883BHRTZ . . . . . -10°C to +100°C
ISL62883IRTZ . . . . . -40°C to +100°C
Junction Temperature
ISL62883HRTZ, ISL62883BHRTZ . . . . . -10°C to +125°C
ISL62883IRTZ . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VDD = 5V, T_A = -40°C to +100°C, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 1V		4	**4.6**	mA
		VR_ON = 0V			**1**	µA
Battery Supply Current	I_{VIN}	VR_ON = 0V			**1**	µA
V_{IN} Input Resistance	R_{VIN}	VR_ON = 1V		900		kΩ
Power-On-Reset Threshold	POR_r	V_{DD} rising		4.35	**4.5**	V
	POR_f	V_{DD} falling	**4.00**	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	HRTZ %Error (V_{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.50V	**-0.5**		**+0.5**	%
		VID = 0.5V to 0.7375V	**-8**		**+8**	mV
		VID = 0.3V to 0.4875V	**-15**		**+15**	mV
	IRTZ %Error (V_{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.50V	**-0.8**		**+0.8**	%
		VID = 0.5V to 0.7375V	**-10**		**+10**	mV
		VID = 0.3V to 0.4875V	**-18**		**+18**	mV
V_{BOOT}			**1.0945**	1.100	**1.1055**	V
Maximum Output Voltage	$V_{CC_CORE(max)}$	VID = [0000000]		1.500		V
Minimum Output Voltage	$V_{CC_CORE(min)}$	VID = [1100000]		0.300		V
R_{BIAS} Voltage		R_{BIAS} = 147kΩ	**1.45**	1.47	**1.49**	V

Electrical Specifications Operating Conditions: VDD = 5V, T_A = -40°C to +100°C, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CHANNEL FREQUENCY						
Nominal Channel Frequency	$f_{SW(nom)}$	Rfset = 7kΩ, 3 channel operation, V_{COMP} = 1V	**285**	300	**315**	kHz
Adjustment Range			**200**		**500**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset		I_{FB} = 0A	**-0.15**		**+0.15**	mV
Error Amp DC Gain	A_{V0}			90		dB
Error Amp Gain-Bandwidth Product	GBW	C_L= 20pF		18		MHz
ISEN						
Imbalance Voltage		Maximum of ISENs - Minimum of ISENs			**1**	mV
Input Bias Current				20		nA
POWER GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.26	**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	**-1**		**1**	µA
PGOOD Delay	tpgd	CLK_EN# LOW to PGOOD HIGH	**6.3**	7.6	**8.9**	ms
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA Source Current		1.0	**1.5**	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance	R_{UGPD}	250mA Sink Current		1.0	**1.5**	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA Source Current		1.0	**1.5**	Ω
LGATE Source Current	I_{LGSRC}	LGATE - VSSP = 2.5V		2.0		A
LGATE Sink Resistance	R_{LGPD}	250mA Sink Current		0.5	**0.9**	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - VSSP = 2.5V		4.0		A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load		23		ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load		28		ns
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 2mA		0.58		V
Reverse Leakage	I_R	V_R = 25V		0.2		µA
PROTECTION						
Overvoltage Threshold	OV_H	VSEN rising above setpoint for >1ms	**150**	195	**240**	mV
Severe Overvoltage Threshold	OV_{HS}	VSEN rising for >2µs	**1.525**	1.55	**1.575**	V
OC Threshold Offset at Rcomp = Open Circuit		3-phase configuration, ISUM- pin current	**28.4**	30.3	**32.2**	µA
		2-phase configuration, ISUM- pin current	**18.3**	20.2	**22.1**	µA
		1-phase configuration, ISUM- pin current	**8.2**	10.1	**12.0**	µA
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
Undervoltage Threshold	UV_f	VSEN falling below setpoint for >1.2ms	**-355**	-295	**-235**	mV
LOGIC THRESHOLDS						
VR_ON Input Low	$V_{IL(1.0V)}$				**0.3**	V

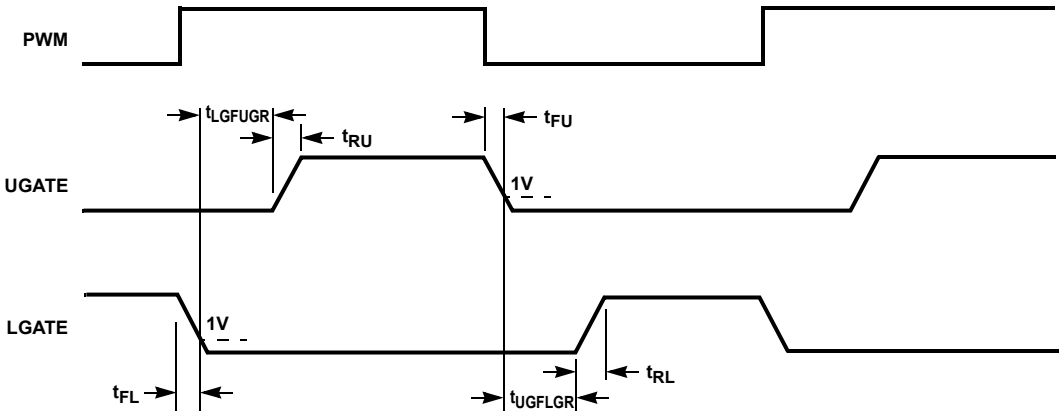
Electrical Specifications Operating Conditions: VDD = 5V, T_A = -40°C to +100°C, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
VR_ON Input High	HRTZ $V_{IH(1.0V)}$		**0.7**			V
	IRTZ $V_{IH(1.0V)}$		**0.75**			V
VID0-VID6, PSI#, and DPRSLPVR Input Low	$V_{IL(1.0V)}$				**0.3**	V
VID0-VID6, PSI#, and DPRSLPVR Input High	$V_{IH(1.0V)}$		**0.7**			V
PWM						
PWM3 Output Low	$V_{OL(5.0V)}$	Sinking 5mA			**1.0**	V
PWM3 Output High	$V_{OH(5.0V)}$	Sourcing 5mA	**3.5**			V
PWM Tri-State Leakage		PWM = 2.5V		2		µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	**53**	60	**67**	µA
Over-Temperature Threshold		V (NTC) falling	**1.18**	1.2	**1.22**	V
VR_TT# Low Output Resistance	R_{TT}	I = 20mA		6.5	**9**	Ω
CLK_EN# OUTPUT LEVELS						
CLK_EN# Low Output Voltage	V_{OL}	I = 4mA		0.26	**0.4**	V
CLK_EN# Leakage Current	I_{OH}	CLK_EN# = 3.3V	**-1**		**1**	µA
CURRENT MONITOR						
IMON Output Current	I_{IMON}	ISUM- pin current = 20µA	**108**	120	**132**	µA
		ISUM- pin current = 10µA	**51**	60	**69**	µA
		ISUM- pin current = 5µA	**22**	30	**37.5**	µA
IMON Clamp Voltage	$V_{IMONCLAMP}$			1.1	**1.15**	V
Current Sinking Capability				275		µA
INPUTS						
VR_ON Leakage Current	I_{VR_ON}	VR_ON = 0V	**-1**	0		µA
		VR_ON = 1V		0	**1**	µA
VIDx Leakage Current	I_{VIDx}	VIDx = 0V	**-1**	0		µA
		VIDx = 1V		0.45	**1**	µA
PSI# Leakage Current	$I_{PSI\#}$	PSI# = 0V	**-1**	0		µA
		PSI# = 1V		0.45	**1**	µA
DPRSLPVR Leakage Current	$I_{DPRSLPVR}$	DPRSLPVR = 0V	**-1**	0		µA
		DPRSLPVR = 1V		0.45	**1**	µA
SLEW RATE						
Slew Rate (For VID Change)	SR		**5**		**6.5**	mV/µs

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Gate Driver Timing Diagram



Simplified Application Circuits

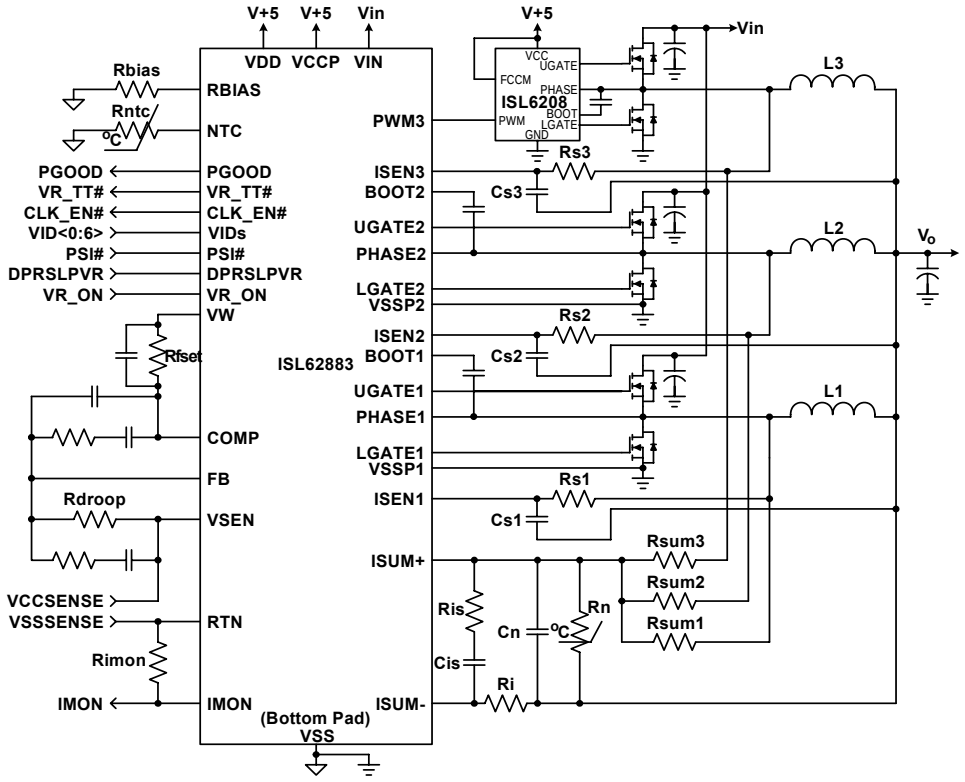


FIGURE 1. TYPICAL APPLICATION CIRCUIT USING DCR SENSING

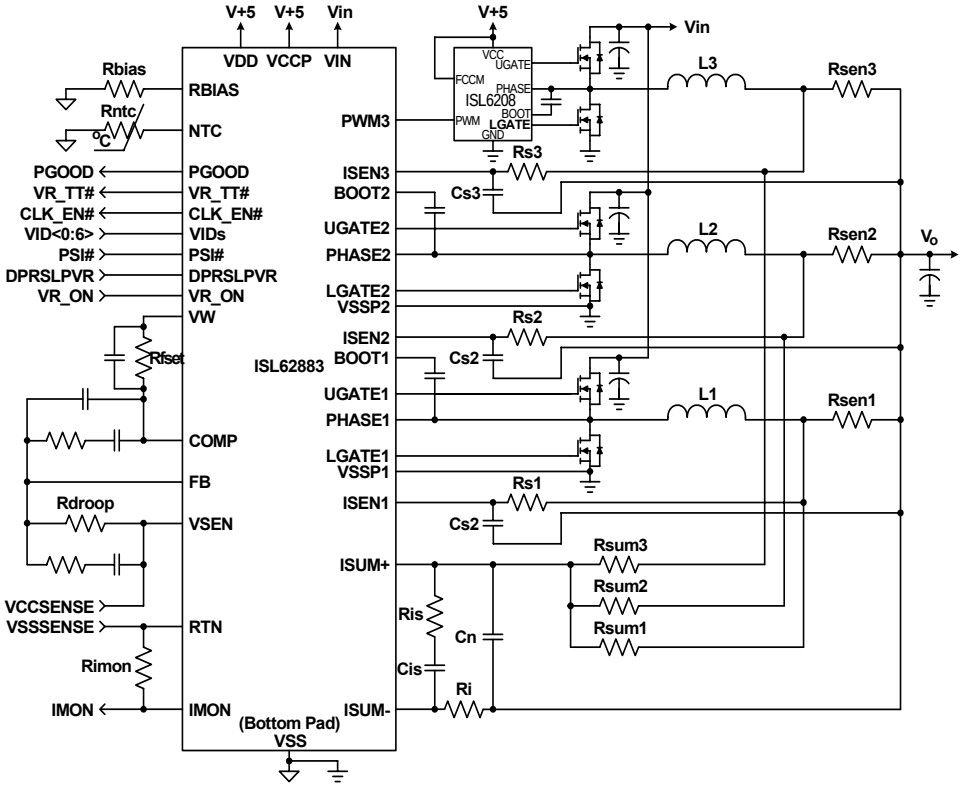


FIGURE 2. TYPICAL APPLICATION CIRCUIT USING RESISTOR SENSING

Theory of Operation

Multiphase R^3 ™ Modulator

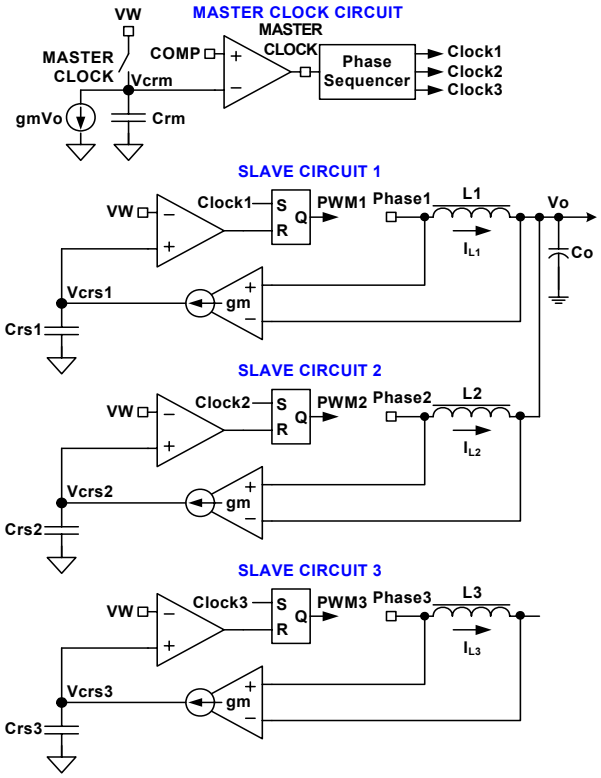


FIGURE 3. R^3™ MODULATORCIRCUIT

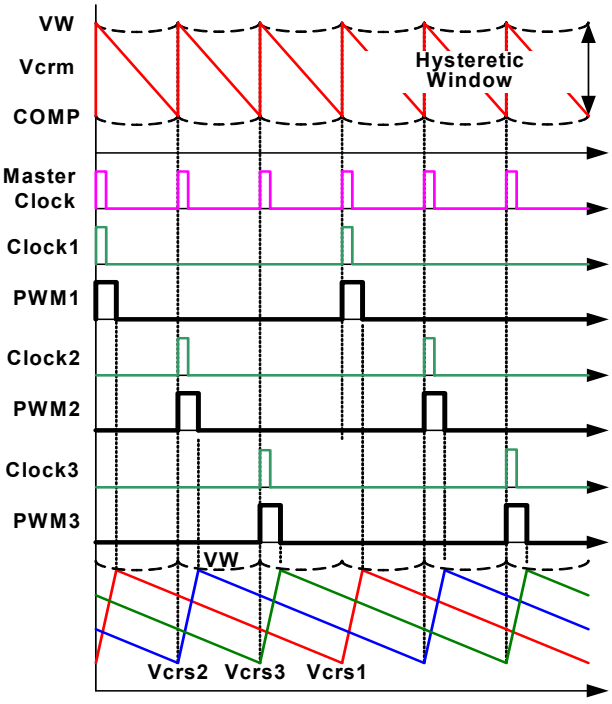


FIGURE 4. R^3™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

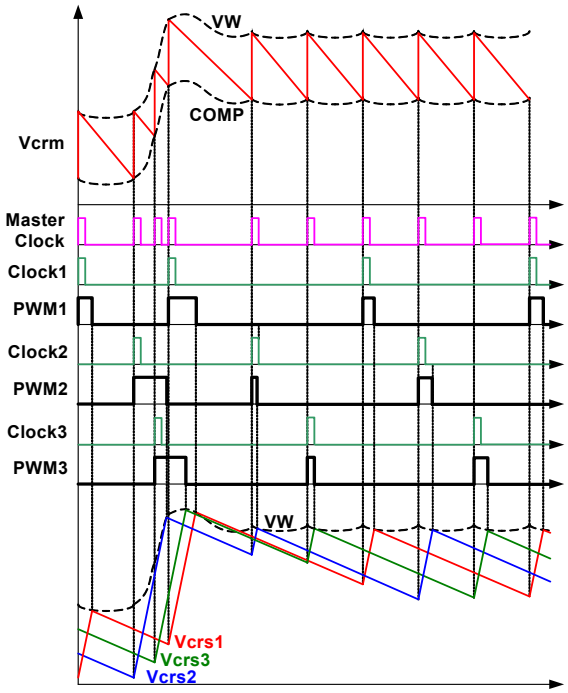


FIGURE 5. R^3™ MODULATOROPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

The ISL62883 is a multiphase regulator, which implements Intel™ IMVP-6.5™ protocol. It can be programmed for 1-, 2- or 3-phase operation for microprocessor core applications. It uses Intersil patented R^3™ (Robust Ripple Regulator™) modulator. The R^3™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 3 conceptually shows the ISL62883 multiphase R^3™ modulator circuit, and Figure 4 shows the operation principles.

A current source flows from the VW pin to the COMP pin, creating a voltage window set by the resistor between the two pins. This voltage window is called VW window in the following discussion.

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to g_mV_o, where g_m is a gain factor. C_{rm} voltage V_{crm} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If the ISL62883 is in 3-phase mode, the master clock signal will be distributed to the three phases, and the Clock1~3 signals will be 120° out-of-phase. If the ISL62883 is in 2-phase mode, the master clock signal will be distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If the ISL62883 is in 1-phase mode, the master clock signal will be distributed to Phases 1 only and be the Clock1 signal.

Each slave circuit has its own ripple capacitor C_{rs}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{rs}. When C_{rs}

voltage V_{Crs} hits VW, the slave circuit turns off the PWM pulse, and the current source discharges C_{rs}.

Since the ISL62883 works with V_{crs}, which are large-amplitude and noise-free synthesized signals, the ISL62883 achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL62883 has an error amplifier that allows the controller to maintain a 0.5% output voltage accuracy.

Figure 5 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency, which allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the VW voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL62883 excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

Diode Emulation and Period Stretching

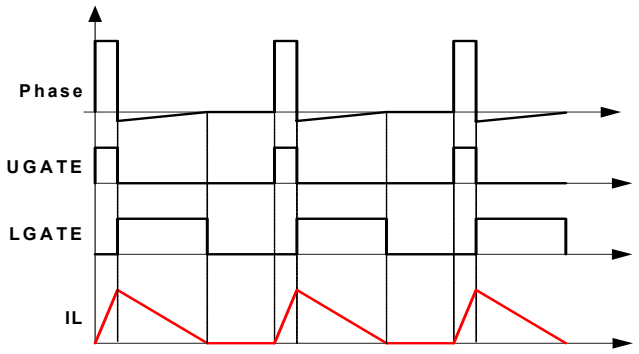


FIGURE 6. DIODE EMULATION

ISL62883 can operate in diode emulation (DE) mode to improve light load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and doesn't not allow reverse current, emulating a diode. As Figure 6 shows, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL62883 monitors the current through monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 6 shows, the inductor current will reach and stay at zero before the next phase node pulse, and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator is in CCM although the controller is in DE mode.

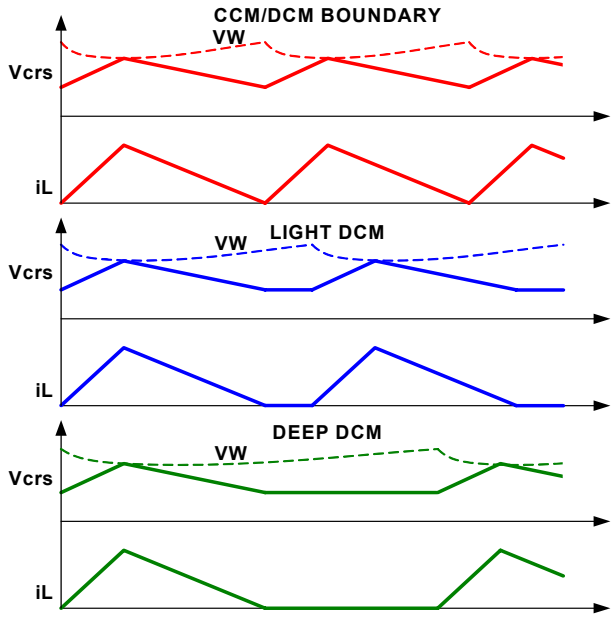


FIGURE 7. PERIOD STRETCHING

Figure 7 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore is the same, making the inductor current triangle the same in the three cases. The ISL62883 clamps the ripple capacitor voltage V_{crs} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{crs}, naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light load efficiency.

Start-up Timing

With the controller's V_{DD} voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic high threshold. The ISL62883 uses digital soft start to ramp up DAC to the boot voltage of 1.1V at about 2.5mV/µs. Once the output voltage is within 10% of the boot voltage for 13 PWM cycles (43µs for frequency = 300kHz), CLK_EN# is pulled low and DAC slews at 5mV/µs to the voltage set by the VID pins. PGOOD is asserted high in approximately 7ms. Figure 8 shows the typical start-up timing. Similar results occur if VR_ON is tied to V_{DD}, with the soft-start sequence starting 120µs after V_{DD} crosses the POR threshold.

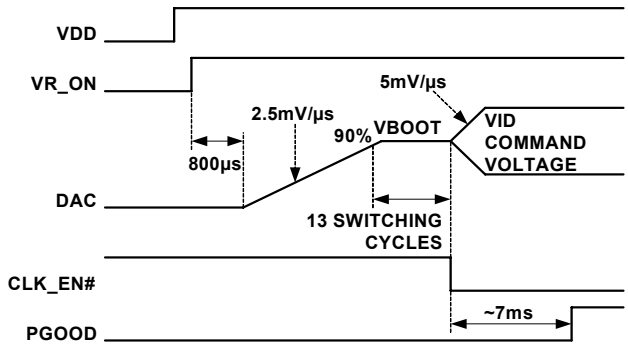


FIGURE 8. SOFT-START WAVEFORMS

Voltage Regulation and Load Line Implementation

After the start sequence, the ISL62883 regulates the output voltage to the value set by the VID inputs per Table 1. The ISL62883 will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.5V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

TABLE 1. VID TABLE

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_O (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625

TABLE 1. VID TABLE (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_O (V)
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250

TABLE 1. VID TABLE (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_O (V)
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000

TABLE 1. VID TABLE (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_O (V)
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

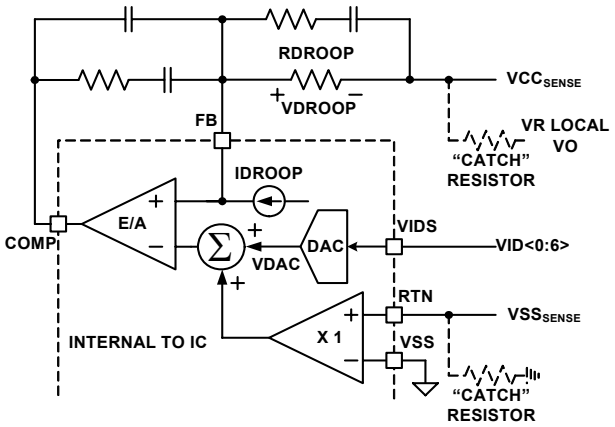


FIGURE 9. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to the load current to achieve the load line. The ISL62883 can sense the inductor current through the intrinsic DC Resistance (DCR) resistance of the inductors Figure 1 shows on page 10 or through resistors in series with the inductors as Figure 2 shows also on page 10. In both methods, capacitor C_n voltage represents the inductor total currents. A droop amplifier converts C_n voltage into an internal current source with the gain set by resistor R_i. The current source is used for load line implementation, current monitor and overcurrent protection.

Figure 9 shows the load line implementation. The ISL62883 drives a current source I_{droop} out of the FB pin, described by Equation 1.

$$I_{droop} = \frac{2xV_{Cn}}{R_i} \quad \text{(EQ. 1)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus sustaining the load line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop of:

$$V_{droop} = R_{droop} \times I_{droop} \quad \text{(EQ. 2)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can both change the load line slope. Since I_{droop} also sets the overcurrent protection level, it is recommended to first scale I_{droop} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Sensing

Figure 9 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and add it to the DAC output. The error amplifier regulates the inverting and the non-inverting input voltages to be equal as shown in Equation 3:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 3)}$$

Rewriting Equation 3 and substitution of Equation 2 gives:

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 4)}$$

Equation 4 is the exact equation required for load line implementation.

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback will be open circuit in the absence of the processor. As shown in Figure 9, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without a processor installed.

Phase Current Balancing

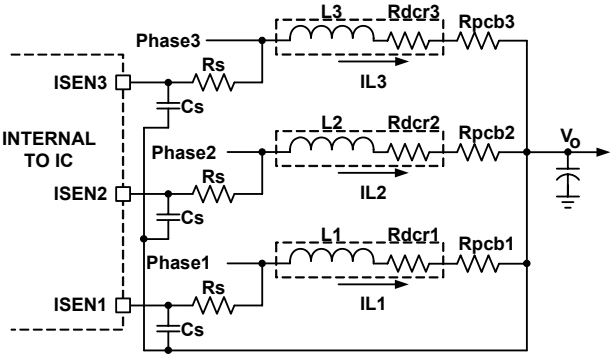


FIGURE 10. CURRENT BALANCING CIRCUIT

The ISL62883 monitors individual phase average current by monitoring the ISEN1, ISEN2, and ISEN3 voltages. Figure 10 shows the current balancing circuit recommended for ISL62883. Each phase node voltage is averaged by a low-pass filter consisting of R_S and C_S, and presented to the corresponding ISEN pin. R_S should be routed to inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 5 thru 7 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 5)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 6)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 7)}$$

where R_{dcr1}, R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2} and I_{L3} are inductor average currents.

The ISL62883 will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when there are $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using same components for L1, L2 and L3 will provide a good match of R_{dcr1}, R_{dcr2} and R_{dcr3}. Board layout will determine R_{pcb1}, R_{pcb2} and R_{pcb3}. It is recommended to have symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

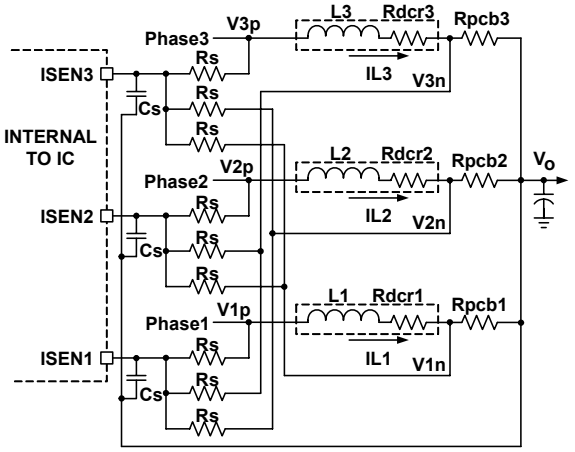


FIGURE 11. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes, it is difficult to implement symmetrical layout. For the circuit shown in Figure 10, asymmetric layout causes different R_{pcb1}, R_{pcb2} and R_{pcb3} thus current imbalance. Figure 11 shows a differential-sensing current balancing circuit recommended for ISL62883. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own phase inductor phase-node pad, and the other two phases inductor output side pads. Equations 8 thru 10 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad \text{(EQ. 8)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 9)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 10)}$$

The ISL62883 will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as in:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 11)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 12)}$$

Rewriting Equation 11 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 13)}$$

and rewriting Equation 12 gives:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 14)}$$

Combining Equations 13 and 14 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 15)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 16)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) will be achieved when there is $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2} and R_{pcb3} will not have any effect.



FIGURE 12. ISL62883 EVALUATION BOARD CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: IL1, CH2: I_{LOAD}, CH3: IL2, CH4: IL3

Since the slave ripple capacitor voltages mimic the inductor currents, R^{3}™ modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 12 shows current balancing performance of the ISL62883 evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at low rep rate, but cannot keep up when the rep rate gets into the hundred-kHz range, where it's out of the control loop bandwidth. The controller achieves excellent current balancing in all cases.

CCM Switching Frequency

The R_{fset} resistor between the COMP and the VW pins sets the sets the VW windows size, therefore sets the switching frequency. When the ISL62883 is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the R^{3}™ modulator. As explained in the Multiphase R^{3}™ Modulator section, the effective switching frequency will increase during load insertion and will decrease during load release to achieve fast response. On the other hand, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 15% and doesn't have any significant effect on output voltage ripple magnitude. Equation 17 gives an estimate of the frequency-setting resistor R_{fset} value. 8kΩ R_{fset} gives approximately 300kHz switching frequency. Lower resistance gives higher switching frequency.

$$R_{fset}(k\Omega) = (Period(\mu s) - 0.29) \times 2.65 \quad \text{(EQ. 17)}$$

Phase Count Configurations

The ISL62883 can be configured for 3-, 2- or 1-phase operation.

For 2-phase configuration, tie the PWM3 pin to 5V. Phase-1 and Phase-2 PWM pulses are 180° out-of-phase. In this configuration, the ISEN3/FB2 pin (pin 9) serves the FB2 function.

For 1-phase configuration, tie the PWM3 and ISEN2 pins to 5V. In this configuration, only Phase-1 is active. The ISEN3/FB2, ISEN2, and ISEN1 pins are not used because there is no need for either current balancing or FB2 function.

Modes of Operation

TABLE 2. ISL62883 MODES OF OPERATION

CONFIGURATION	PSI#	DPRSLPVR	OPERATIONAL MODE
3-phase Configuration	0	0	2-phase CCM
	0	1	1-phase DE
	1	0	3-phase CCM
	1	1	1-phase DE
2-phase Configuration	0	0	1-phase CCM
	0	1	1-phase DE
	1	0	2-phase CCM
	1	1	1-phase DE
1-phase Configuration	0	0	1-phase CCM
	0	1	1-phase DE
	1	0	1-phase CCM
	1	1	1-phase DE

Table 2 shows the ISL62883 operational modes, programmed by the logic status of the PSI# and the DPRSLPVR pins. In 3-phase configuration, the ISL62883 enters 2-phase CCM for (PSI# = 0 and DPRSLPVR = 0) by dropping PWM3 and operating phases 1 and 2 180° out-of-phase. It also reduces the overcurrent and the way-overcurrent protection levels to 2/3 of the initial values. The ISL62883 enters 1-phase DE mode when DPRSLPVR = 1. It drops phases 2 and 3, and reduces the overcurrent and the way-overcurrent protection levels to 1/3 of the initial values.

In 2-phase configuration, the ISL62883 enters 1-phase CCM for (PSI# = 0 and DPRSLPVR = 0). It drops Phase-2 and reduces the overcurrent and the way-overcurrent protection levels to 1/2 of the initial values. The ISL62883 enters 1-phase DE mode when DPRSLPVR = 1 by dropping phase 2.

In 1-phase configuration, the ISL62883 does not change the operational mode when the PSI# signal changes status. It enters 1-phase DE mode when DPRSLPVR = 1.

Dynamic Operation

The ISL62883 responds to VID changes by slewing to the new voltage at 5mV/µs slew rate. As the output approaches the VID command voltage, the dv/dt moderates to prevent overshoot. Geyserville-III transitions commands one LSB VID step (12.5mV) every 2.5µs, controlling the effective dv/dt at 5mv/µs. The ISL62883 is capable of 5mV/µs slew rate.

When the ISL62883 is in DE mode, it will actively drive the output voltage up when the VID changes to a higher value. It'll resume DE mode operation after reaching the new voltage level. If the load is light enough to warrant DCM, it will enter DCM after the inductor current has crossed zero for four consecutive cycles. The ISL62883 will remain in DE mode when the VID changes to a lower value. The output voltage will decay to the new value and the load will determine the slew rate.

During load insertion response, the Fast Clock function increases the PWM pulse response speed. The ISL62883 monitors the VSEN pin voltage and compares it to 100ns - filtered version. When the unfiltered version is 20mV below the filtered version, the controller knows there is a fast voltage dip due to load insertion, hence issues an additional master clock signal to deliver a PWM pulse immediately.

The R^{3}™ modulator intrinsically has voltage feed forward. The output voltage is insensitive to a fast slew rate input voltage change.

Protections

The ISL62883 provides overcurrent, current-balance, undervoltage, overvoltage, and over-temperature protections.

The ISL62883 determines overcurrent protection (OCP) by comparing the average value of the droop current I_{droop} with an internal current source threshold. It declares OCP when I_{droop} is above the threshold for 120µs. A resistor R_{comp} from the COMP pin to GND programs the OCP current source threshold, as Table 3 shows. It is recommended to use the nominal R_{comp} value. The ISL62883 detects the R_{comp} value at the beginning of start up, and sets the internal OCP threshold accordingly. It remembers the R_{comp} value until the VR_ON signal drops below the POR threshold.

TABLE 3. ISL62883 OCP THRESHOLD

R_{comp}			OCP THRESHOLD (µA)		
MIN. (kΩ)	NOMINAL (kΩ)	MAX. (kΩ)	1-PHASE MODE	2-PHASE MODE	3-PHASE MODE
	none	none	20	40	60
320	400	480	22.7	45.3	68
210	235	260	20.7	41.3	62
155	165	175	18	36	54
104	120	136	20	37.33	56
78	85	92	22.7	38.7	58
62	66	70	20.7	42.7	64
45	50	55	18	44	66

The default OCP threshold is the value when R_{comp} is not populated. It is recommended to scale the droop current I_{droop} such that the default OCP threshold gives approximately the desired OCP level, then use R_{comp} to fine tune the OCP level if necessary.

For overcurrent conditions above 2.5 times the OCP level, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection. This protection is also referred to as way-overcurrent protection or fast-overcurrent protection, for short-circuit protections.

The ISL62883 monitors the ISEN pin voltages to determine current-balance protection. If the ISEN pin voltage difference is greater than 9mV for 1ms, the controller will declare a fault and latch off.

The ISL62883 will declare undervoltage (UV) fault and latch off if the output voltage is less than the VID set value by 300mV or more for 1ms. It'll turn off the PWM outputs and dessert PGOOD.

The ISL62883 has two levels of overvoltage protections. The first level of overvoltage protection is referred to as PGOOD overvoltage protection. If the output voltage exceeds the VID set

value by +200mV for 1ms, the ISL62883 will declare a fault and dessert PGOOD.

The ISL62883 takes the same actions for all of the above fault protections: desertion of PGOOD and turn-off of the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes. These fault conditions can be reset by bringing VR_ON low or by bringing V_{DD} below the POR threshold. When VR_ON and V_{DD} return to their high operating levels, a soft-start will occur.

The second level of overvoltage protection is different. If the output voltage exceeds 1.55V, the ISL62883 will immediately declare an OV fault, dessert PGOOD, and turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below 0.85V when all power MOSFETs are turned off. If the output voltage rises above 1.55V again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground. Resetting VR_ON cannot clear the 1.55V OVP. Only resetting V_{DD} will clear it. The 1.55V OVP is active all the time when the controller is enabled, even if one of the other faults have been declared. This ensures that the processor is protected against high-side power MOSFET leakage while the MOSFETs are commanded off.

The ISL62883 has a thermal throttling feature. If the voltage on the NTC pin goes below the 1.18V OT threshold, the VR_TT# pin is pulled low indicating the need for thermal throttling to the system. No other action is taken within the ISL62883 in response to NTC pin voltage.

Table 4 summarizes the fault protections.

TABLE 4. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Way-Overcurrent (2.5xOC)	<2µs		
Overvoltage +200mV	1ms		
Undervoltage -300mV			
Phase Current Unbalance			
Overvoltage 1.55V	Immediately	Low-side MOSFET on until V_{core} <0.85V, then PWM tri-state, PGOOD latched low.	VDD toggle
Over-Temperature		1ms	N/A

Current Monitor

The ISL62883 provides the current monitor function. The IMON pin outputs a high-speed analog current source that is 3 times of the droop current flowing out of the FB pin. Thus Equation 18:

$$I_{IMON} = 3 \times I_{droop} \quad \text{(EQ. 18)}$$

As Figures 1 and 2 show, a resistor R_{imon} is connected to the IMON pin to convert the IMON pin current to voltage. A capacitor can be paralleled with R_{imon} to filter the voltage information. The IMVP-6.5™ specification requires that the IMON voltage information be referenced to VSSSENSE.

The IMON pin voltage range is 0V to 1.1V. A clamp circuit prevents the IMON pin voltage from going above 1.1V.

FB2 Function

The FB2 function is only available when the ISL62883 is in 2-phase configuration, when pin 9 serves the FB2 function instead of the ISEN3 function.

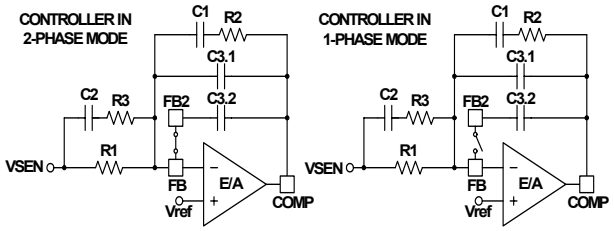


FIGURE 13. FB2 FUNCTION IN 2-PHASE MODE

Figure 13 shows the FB2 function. A switch (called FB2 switch) turns on to short the FB and the FB2 pins when the controller is in 2-phase mode. Capacitors C3.1 and C3.2 are in parallel, serving as part of the compensator. When the controller enters 1-phase mode, the FB2 switch turns off, removing C3.2 and leaving only C3.1 in the compensator. The compensator gain will increase with the removal of C3.2. By properly sizing C3.1 and C3.2, the compensator cab be optimal for both 2-phase mode and 1-phase mode.

When the FB2 switch is off, C3.2 is disconnected from the FB pin. However, the controller still actively drives the FB2 pin voltage to follow the FB pin voltage such that C3.2 voltage always follows C3.1 voltage. When the controller turns on the FB2 switch, C3.2 will be reconnected to the compensator smoothly.

The FB2 function ensures excellent transient response in both 2-phase mode and 1-phase mode. If one decides not to use the FB2 function, simply populate C3.1 only.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET R_{dson} voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero-crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it'll flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it'll flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase

comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns to minimize the body diode-related loss.

Overshoot Reduction Function

The ISL62883 has an optional overshoot reduction function. Using R_{BIAS} = 47kΩ enables this function and using R_{BIAS} = 147kΩ disables this function.

When a load release occurs, the energy stored in the inductors will dump to the output capacitor, causing output voltage overshoot. The inductor current freewheels through the low-side MOSFET during this period of time. The overshoot reduction function turns off the low-side MOSFET during the output voltage overshoot, forcing the inductor current to freewheel through the low-side MOSFET body diode. Since the body diode voltage drop is much higher than MOSFET R_{dson} voltage drop, more energy is dissipated on the low-side MOSFET therefore the output voltage overshoot is lower.

If the overshoot reduction function is enabled, the ISL62883 monitors the COMP pin voltage to determine the output voltage overshoot condition. The COMP voltage will fall and hit the clamp voltage when the output voltage overshoots. The ISL62883 will turn off LGATE1 and LGATE2, and tri-state PWM3 when COMP is being clamped. All the low-side MOSFETs in the power stage will be turned off. When the output voltage has reached its peak and starts to come down, the COMP voltage starts to rise and is no longer clamped. The ISL62883 will resume normal PWM operation.

When PSI# is low, indicating a low power state of the CPU, the controller will disable the overshoot reduction function as large magnitude transient event is not expected and overshoot is not a concern.

While the overshoot reduction function reduces the output voltage overshoot, energy is dissipated on the low-side MOSFET, causing additional power loss. The more frequent transient event, the more power loss dissipated on the low-side MOSFET. The MOSFET may face severe thermal stress when transient events happen at a high repetitive rate. User discretion is advised when this function is enabled.

Key Component Selection

R_{BIAS}

The ISL62883 uses a resistor (1% or better tolerance is recommended) from the RBIAS pin to GND to establish highly accurate reference current sources inside the IC. Using R_{BIAS} = 47kΩ enables the overshoot reduction function and using R_{BIAS} = 147kΩ disables this function. Do not connect any other components to this pin. Do not connect any capacitor to the RBIAS pin as it will create instability.

Care should be taken in layout that the resistor is placed very close to the RBIAS pin and that a good quality signal ground is connected to the opposite side of the R_{BIAS} resistor.

R_{is} and C_{is}

As Figures 1 and 2, show, the ISL62883 needs the R_{is} - C_{is} network across the ISUM+ and the ISUM- pins to stabilize the droop amplifier. The preferred values are R_{is} = 82.5Ω and C_{is} = 0.01µF. Slight deviations from the recommended values are acceptable. Large deviations may result in instability.

Inductor DCR Current-Sensing Network

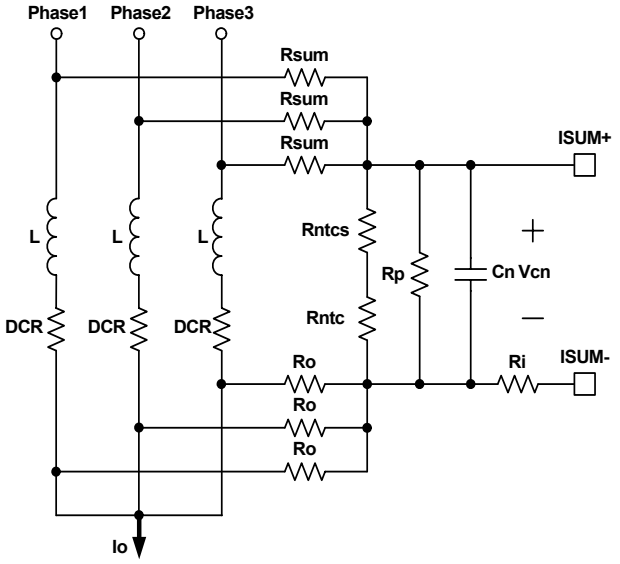


FIGURE 14. DCR CURRENT-SENSING NETWORK

Figure 14 shows the inductor DCR current-sensing network for a 3-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown, and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to temperature-compensate the inductor DCR change.

The inductor output side pads are electrically shorted in the schematic, but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use 1Ω~10Ω R_o to create quality signals. Since R_o value is much smaller than the rest of the current sensing circuit, the following analysis will ignore it for simplicity.

The summed inductor current information is presented to the capacitor C_n. Equations 19 thru 23 describe the frequency-domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 19)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 20)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 21)}$$

where N is the number of phases.

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 22)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 23)}$$

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC R_{ntc} values decreases as its temperature decreases. Proper selections of R_{sum}, R_{ntcs}, R_p and R_{ntc} parameters ensure that V_{Cn} represent the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of V_{cn} to the inductor DCR voltage, so the droop circuit has higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current-sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole ω_{sns} and a zero ω_L. One needs to match ω_L and ω_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing ω_L equal to ω_{sns} and solving for the solution, Equation 24 solves for the value of Cn.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 24)}$$

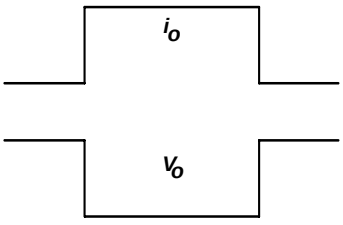


FIGURE 15. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

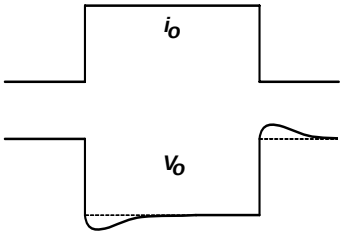


FIGURE 16. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

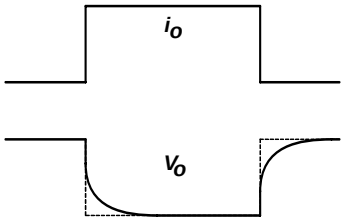


FIGURE 17. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ and L = 0.36µH, Equation 24 gives C_n = 0.406µF.

Assuming the compensator design is correct, Figure 15 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{core} also has a square response.

If C_n value is too large or too small, $V_{Cn}(s)$ will not accurately represent real-time $I_o(s)$ and will worsen the transient response. Figure 16 shows the load transient response when C_n is too small. V_{core} will sag excessively upon load insertion and may create a system failure. Figure 17 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.

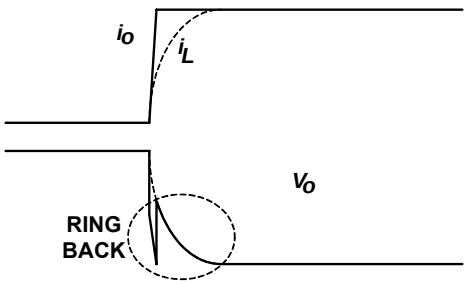


FIGURE 18. OUTPUT VOLTAGE RING BACK PROBLEM

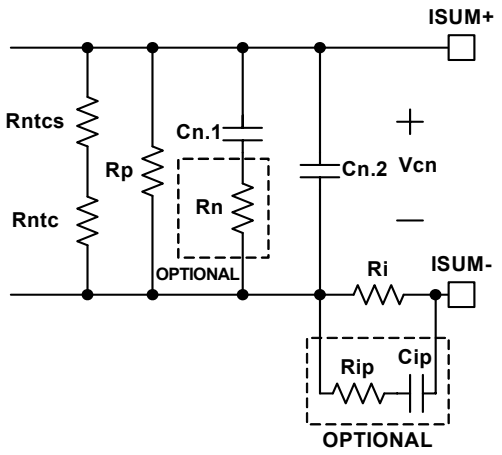


FIGURE 19. OPTIONAL CIRCUITS FOR RING BACK REDUCTION

Figure 18 shows the output voltage ring back problem during load transient response. The load current i_o has a fast step change, but the inductor current i_L cannot accurately follow. Instead, i_L responds in first order system fashion due to the nature of current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_o dip quickly upon load current change. However, the controller regulates V_o according to the droop current i_{droop}, which is a real-time representation of i_L; therefore it pulls V_o back to the level dictated by i_L, causing the ring back problem. This phenomenon is not observed when the output capacitor have very low ESR and ESL, such as all ceramic capacitors.

Figure 19 shows two optional circuits for reduction of the ring back. R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of i_o change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L, and V_o will not ring back. The recommended value for R_{ip} is100Ω. C_{ip} should be determined through tuning the load transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF.

C_n is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 19 shows that two capacitors $C_{n.1}$ and $C_{n.2}$ are in parallel. Resistor R_n is an optional component to reduce the V_o ring back. At steady state, $C_{n.1}$+$C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As explained in Figure 16, V_o tends to dip when C_n is too small, and this effect will reduce the V_o ring back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. R_n value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and R_n values should be determined through tuning the load transient response waveforms on an actual board.

Resistor Current-Sensing Network

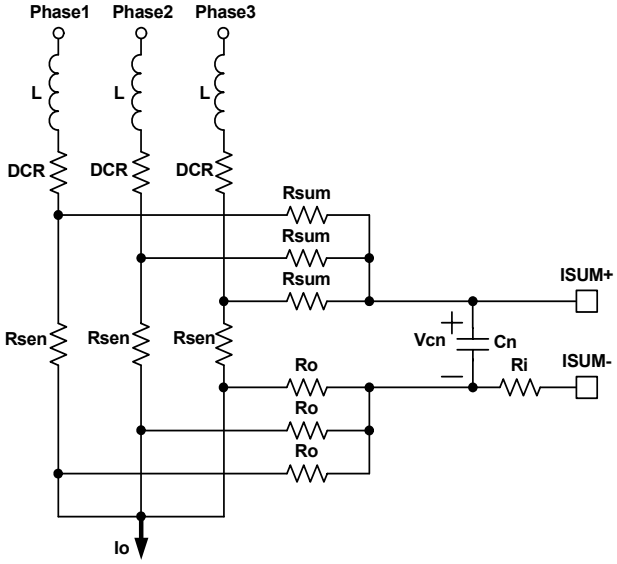


FIGURE 20. RESISTOR CURRENT-SENSING NETWORK

Figure 20 shows the resistor current-sensing network for a 3-phase solution. Each inductor has a series current-sensing resistor R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a a filter for noise attenuation. Equations 25 thru 27 give $V_{Cn}(s)$ expression:

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 25)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 26)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 27)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor R_{sen} value will not have significant variation over temperature, so there is no need for the NTC network.

The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

Overcurrent Protection

Refer to Equation 1 and Figures 9, 14 and 20; resistor R_i sets the droop current I_{droop}. Table 3 shows the internal OCP threshold. It is recommended to design I_{droop} without using the R_{comp} resistor.

For example, the OCP threshold is 60µA for 3-phase solution. We will design I_{droop} to be 38.8µA at full load, so the OCP trip level is 1.55 times of the full load current.

For inductor DCR sensing, Equation 28 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 28)}$$

Substitution of Equation 28 into Equation 1 gives Equation 29:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 29)}$$

Therefore:

$$R_i = \frac{2R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N}\right) \times I_{droop}} \quad \text{(EQ. 30)}$$

Substitution of Equation 20 and application of the OCP condition in Equation 30 gives Equation 31:

$$R_i = \frac{2 \times \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N}\right) \times I_{droopmax}} \quad \text{(EQ. 31)}$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ, I_{omax} = 51A and $I_{droopmax}$ = 40.9µA, Equation 31 gives R_i = 606Ω.

For resistor sensing, Equation 32 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 32)}$$

Substitution of Equation 32 into Equation 1 gives Equation 33:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 33)}$$

Therefore:

$$R_i = \frac{2R_{sen} \times I_o}{N \times I_{droop}} \quad \text{(EQ. 34)}$$

Substitution of Equation 34 and application of the OCP condition in Equation 30 gives:

$$R_i = \frac{2R_{sen} \times I_{omax}}{N \times I_{droopmax}} \quad \text{(EQ. 35)}$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sen} = 1mΩ, I_{omax} = 51A and $I_{droopmax}$ = 40.9µA, Equation 35 gives R_i = 831Ω.

A resistor from COMP to GND can adjust the internal OCP threshold, providing another dimension of fine-tune flexibility. Table 3 shows the detail. It is recommended to scale I_{droop} such that the default OCP threshold gives approximately the desired OCP level, then use R_{comp} to fine tune the OCP level if necessary.

Load Line Slope

Refer to Figure 9.

For inductor DCR sensing, substitution of Equation 29 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \quad \text{(EQ. 36)}$$

For resistor sensing, substitution of Equation 33 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{sen} \times R_{droop}}{N \times R_i} \quad \text{(EQ. 37)}$$

Substitution of Equation 30 and rewriting Equation 36, or substitution of Equation 34 and rewriting Equation 37 gives the same result in Equation 38:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad \text{(EQ. 38)}$$

One can use the full load condition to calculate R_{droop}. For example, given I_{omax} = 51A, $I_{droopmax}$ = 40.9µA and LL = 1.9mΩ, Equation 38 gives R_{droop} = 2.37kΩ.

It is recommended to start with the R_{droop} value calculated by Equation 38, and fine tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Current Monitor

Refer to Equation 18 for the IMON pin current expression.

Refer to Figures 1 and 2, the IMON pin current flows through R_{imon}. The voltage across R_{imon} is expressed in Equation 39:

$$V_{Rimon} = 3 \times I_{droop} \times R_{imon} \quad \text{(EQ. 39)}$$

Rewriting Equation 38 gives Equation 40:

$$I_{droop} = \frac{I_o}{R_{droop}} \times LL \quad \text{(EQ. 40)}$$

Substitution of Equation 40 into Equation 39 gives Equation 41:

$$V_{Rimon} = \frac{3I_o \times LL}{R_{droop}} \times R_{imon} \quad \text{(EQ. 41)}$$

Rewriting Equation 41 and application of full load condition gives Equation 42:

$$R_{imon} = \frac{V_{Rimon} \times R_{droop}}{3I_o \times LL} \quad \text{(EQ. 42)}$$

For example, given LL = 1.9mΩ, R_{droop} = 2.37kΩ, V_{Rimon} = 963mV at I_{omax} = 51A, Equation 42 gives R_{imon} = 7.85kΩ.

A capacitor C_{imon} can be paralleled with R_{imon} to filter the IMON pin voltage. The $R_{imon}C_{imon}$ time constant is the user's choice. It is recommended to have a time constant long enough such that switching frequency ripples are removed.

Compensator

Figure 15 shows the desired load transient response waveforms. Figure 21 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e. constant output impedance, in the entire frequency range, V_o will have square response when I_o has a square change.

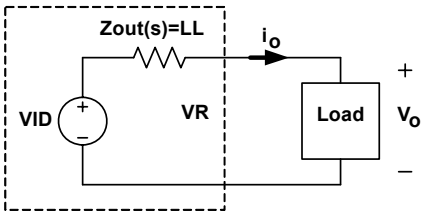


FIGURE 21. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network, so the VR achieves constant output impedance as a stable system. Please contact Intersil Application support at www.intersil.com/design/. Figure 24 shows a screenshot of the spreadsheet.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 22 conceptually shows T1(s) measurement set-up and Figure 23 conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. T(1) is measured after the summing node, and T2(s) is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can be actually measured on an ISL62883 regulator.

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s) and has more meaning of system stability.

T2(s) is the voltage loop gain with closed droop loop. It has more meaning of output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin, and output impedance equal or smaller than the load line slope.

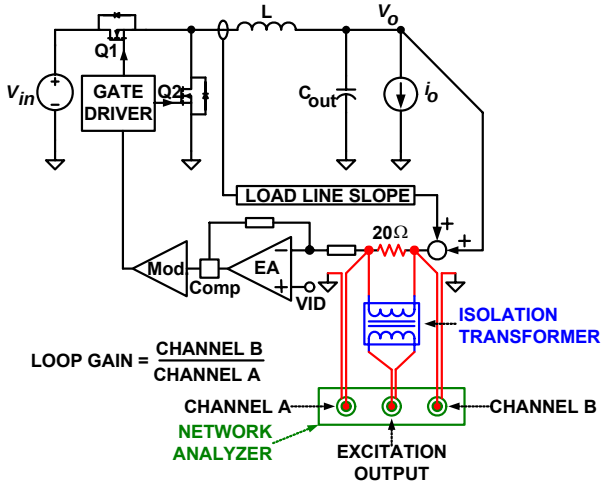


FIGURE 22. LOOP GAIN T1(s) MEASUREMENT SET-UP

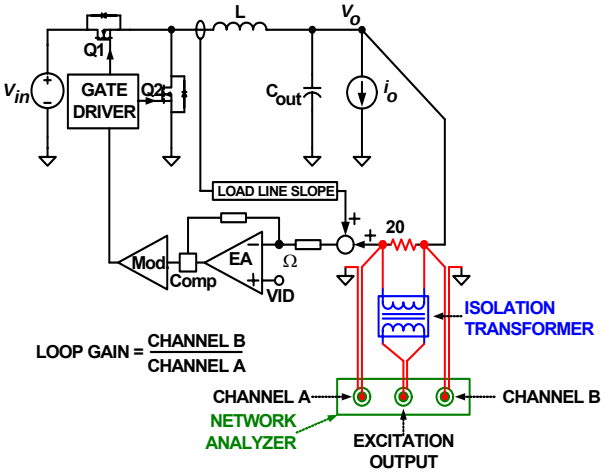


FIGURE 23. LOOP GAIN T2(s) MEASUREMENT SET-UP

Compensation & Current Sensing Network Design for Intersil Multiphase R^3 Regulators for IMVP-6.5

Jia Wei, jwei@intersil.com, 919-405-3605

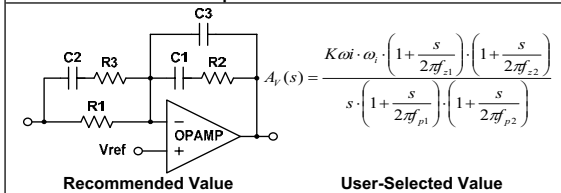
Attention: 1. "Analysis ToolPak" Add-in is required. To turn on, go to Tools--Add-Ins, and check "Analysis ToolPak"

2. Green cells require user input

Operation Parameters

Controller Part Number:	ISL6288x	
Phase Number:	3	
Vin:	12	volts
Vo:	1.15	volts
Full Load Current:	51	Amps
Estimated Full-Load Efficiency:	87	%
Number of Output Bulk Capacitors:	4	
Capacitance of Each Output Bulk Capacitor:	270	uF
ESR of Each Output Bulk Capacitor:	4.5	mΩ
ESL of Each Output Bulk Capacitor:	0.6	nH
Number of Output Ceramic Capacitors:	24	
Capacitance of Each Output Ceramic Capacitor:	10	uF
ESR of Each Output Ceramic Capacitor:	3	mΩ
ESL of Each Output Ceramic Capacitor:	3	nH
Switching Frequency:	300	kHz
Inductance Per Phase:	0.36	uH
CPU Socket Resistance:	0.9	mΩ
Desired Load-Line Slope:	1.9	mΩ
Desired ISUM- Pin Current at Full Load:	40.9	uA
(This sets the over-current protection level)		

Compensator Parameters



$$A_V(s) = \frac{K\omega i \cdot \omega_i \cdot \left(1+\frac{s}{2\pi f_{z1}}\right)\cdot\left(1+\frac{s}{2\pi f_{z2}}\right)}{s\cdot\left(1+\frac{s}{2\pi f_{p1}}\right)\cdot\left(1+\frac{s}{2\pi f_{p2}}\right)}$$

	Recommended Value		User-Selected Value	
R1	2.369	kΩ	2.37	kΩ
R2	338.213	kΩ	324	kΩ
R3	0.530	kΩ	0.536	kΩ
C1	148.140	pF	150	pF
C2	455.369	pF	390	pF
C3	40.069	pF	39	pF

Use User-Selected Value (Y/N)? N

Performance and Stability

T1 Bandwidth:	212kHz	T2 Bandwidth:	66kHz
T1 Phase Margin:	58.9°	T2 Phase Margin:	89.3°

Changing the settings in red requires deep understanding of control loop design

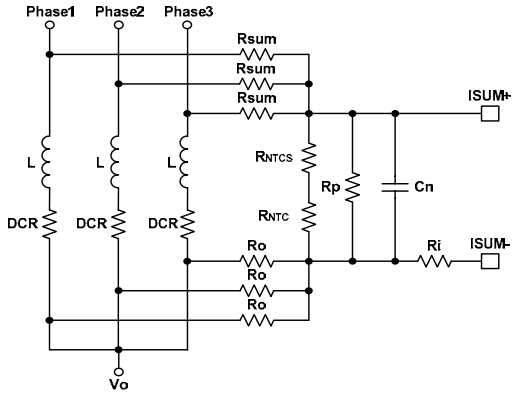
Place the 2nd compensator pole fp2 at: 2.2 **xfs** (Switching Frequency)

Tune Kωi to get the desired loop gain bandwidth

Tune the compensator gain factor Kωi: 1.3

(Recommended Kωi range is 0.8~2)

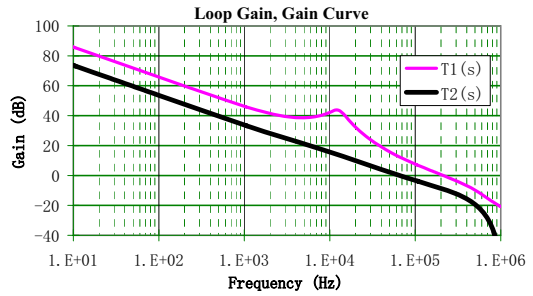
Current Sensing Network Parameters

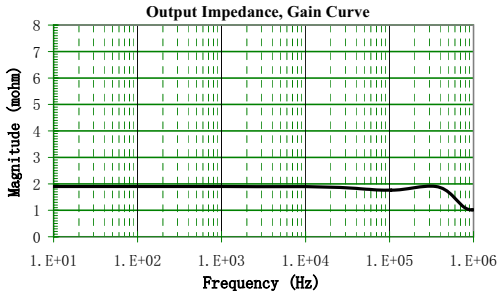


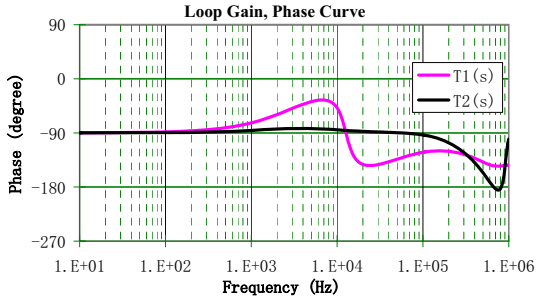
Operation Parameters

Inductor DCR	0.88	mΩ
Rsum	3.65	kΩ
Rntc	10	kΩ
Rntcs	2.61	kΩ
Rp	11	kΩ

	Recommended Value		User Selected Value	
Cn	0.406	uF	0.406	uF
Ri	606.036	Ω	604	Ω







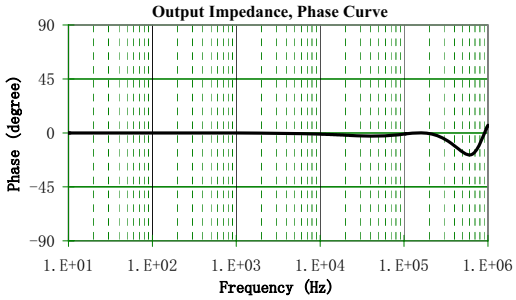


FIGURE 24. SCREENSHOT OF THE COMPENSATOR DESIGN SPREADSHEET

Optional Slew Rate Compensation Circuit For 1-Tick VID Transition

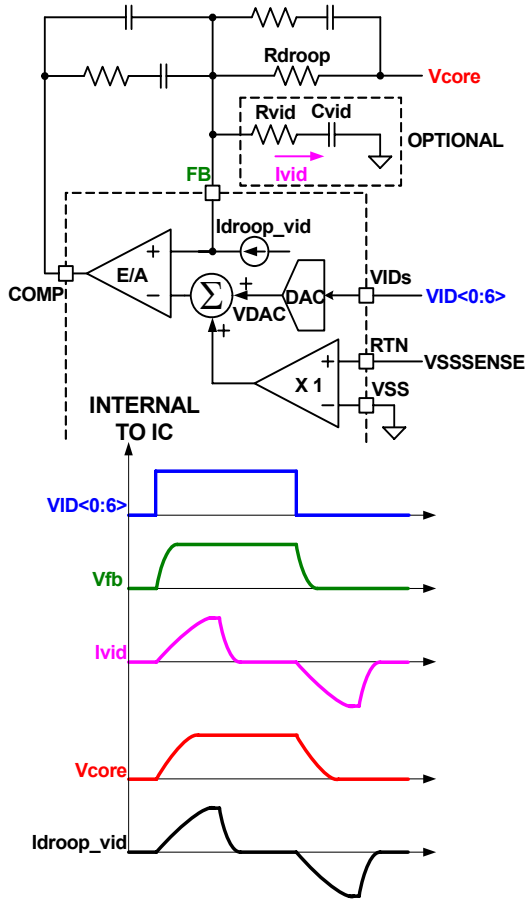


FIGURE 25. OPTIONAL SLEW RATE COMPENSATION CIRCUIT FOR1-TICK VID TRANSITION

During a large VID transition, the DAC steps through the VIDs at a controlled slew rate of 2.5µs per tick (12.5mV), controlling output voltage V_{core} slew rate at 5mV/µs.

Figure 25 shows the waveforms of 1-tick VID transition. During 1-tick VID transition, the DAC output changes at approximately 15mV/µs slew rate, but the DAC cannot step through multiple VIDs to control the slew rate. Instead, the control loop response speed determines V_{core} slew rate. Ideally, V_{core} will follow the FB pin voltage slew rate. However, the controller senses the inductor current increase during the up transition, as the I_{droop_vid} waveform shows, and will droop the output voltage V_{core} accordingly, making V_{core} slew rate slow. Similar behavior occurs during the down transition.

To control V_{core} slew rate during 1-tick VID transition, one can add the R_{vid}-C_{vid} branch, whose current I_{vid} cancels I_{droop_vid}.

When V_{core} increases, the time domain expression of the induced I_{droop} change is expressed in Equation 43:

$$I_{droop}(t) = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \times \left(1 - e^{\frac{-t}{C_{out} \times LL}}\right) \quad \text{(EQ. 43)}$$

where C_{out} is the total output capacitance.

In the mean time, the R_{vid}-C_{vid} branch current I_{vid} time domain expression is shown in Equation 44:

$$I_{vid}(t) = C_{vid} \times \frac{dV_{fb}}{dt} \times \left(1 - e^{\frac{-t}{R_{vid} \times C_{vid}}}\right) \quad \text{(EQ. 44)}$$

It is desired to let $I_{vid}(t)$ cancel $I_{droop_vid}(t)$. So there are:

$$C_{vid} \times \frac{dV_{fb}}{dt} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \quad \text{(EQ. 45)}$$

and:

$$R_{vid} \times C_{vid} = C_{out} \times LL \quad \text{(EQ. 46)}$$

The result is expressed in Equation 47:

$$R_{vid} = R_{droop} \quad \text{(EQ. 47)}$$

and:

$$C_{vid} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{\frac{dV_{core}}{dt}}{\frac{dV_{fb}}{dt}} \quad \text{(EQ. 48)}$$

For example: given LL = 1.9mΩ, R_{droop} = 2.37kΩ, C_{out} = 1320µF, dV_{core}/dt = 5mV/us and dV_{fb}/dt = 15mV/µs, Equation 47 gives R_{vid} = 2.37kΩ and Equation 48 gives C_{vid} = 350pF.

It's recommended to select the calculated R_{vid} value and start with the calculated C_{vid} value and tweak it on the actual board to get the best performance.

During normal transient response, the FB pin voltage is held constant, therefore is virtual ground in small signal sense. The R_{vid}-C_{vid} network is between the virtual ground and the real ground, and hence has no effect on transient response.

Voltage Regulator Thermal Throttling

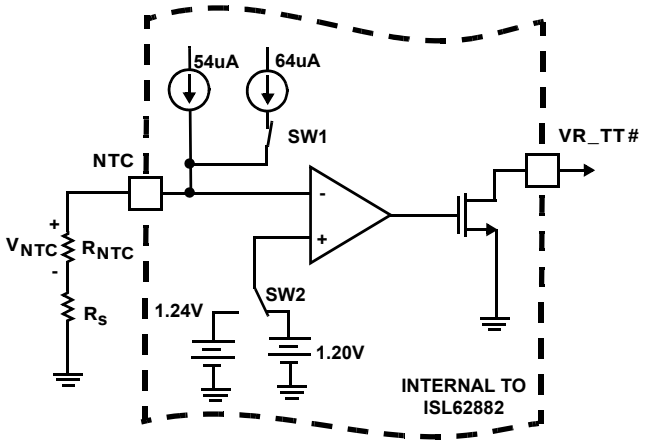


FIGURE 26. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE OF THE ISL62882

Figure 26 shows the thermal throttling feature with hysteresis. An NTC network is connected between the NTC pin and GND. At low temperature, SW1 is on and SW2 connects to the 1.20V side. The total current flowing out of the NTC pin is 60µA. The voltage on NTC pin is higher than threshold voltage of 1.20V and the comparator output is low. VR_TT# is pulled up by the external resistor.

When temperature increases, the NTC thermistor resistance decreases so the NTC pin voltage drops. When the NTC pin voltage drops below 1.20V, the comparator changes polarity and turns SW1 off and throws SW2 to 1.24V. This pulls VR_TT# low and sends the signal to start thermal throttle. There is a 6µA current reduction on NTC pin and 40mV voltage increase on threshold voltage of the comparator in this state. The VR_TT# signal will be used to change the CPU operation and decrease the power consumption. When the temperature drops down, the NTC thermistor voltage will go up. If NTC voltage increases to above 1.24V, the comparator will flip back. The external resistance difference in these two conditions is expressed in Equation 49:

$$\frac{1.24V}{54\mu A} - \frac{1.20V}{60\mu A} = 2.96k \quad \text{(EQ. 49)}$$

One needs to properly select the NTC thermistor value such that the required temperature hysteresis correlates to 2.96kΩ resistance change. A regular resistor may need to be in series with the NTC thermistor to meet the threshold voltage values.

For example, given Panasonic NTC thermistor with B = 4700, the resistance will drop to 0.03322 of its nominal at +105°C, and drop to 0.03956 of its nominal at +100°C. If the required temperature hysteresis is +105°C to +100°C, the required resistance of NTC will be:

$$\frac{2.96k\Omega}{(0.03956 - 0.03322)} = 467k\Omega \quad \text{(EQ. 50)}$$

Therefore a larger value thermistor, such as 470k NTC should be used.

At +105°C, 470kΩ NTC resistance becomes (0.03322×470kΩ) = 15.6kΩ. With 60µA on the NTC pin, the voltage is only (15.6kΩ×60µA) = 0.937V. This value is much lower than the threshold voltage of 1.20V. Therefore, a regular resistor needs to be in series with the NTC. The required resistance can be calculated by Equation 51:

$$\frac{1.20V}{60\mu A} - 15.6k\Omega = 4.4k\Omega \quad \text{(EQ. 51)}$$

4.42k is a standard resistor value. Therefore, the NTC branch should have a 470k NTC and 4.42k resistor in series. The part number for the NTC thermistor is ERTJ0EV474J. It is a 0402 package. The NTC thermistor will be placed in the hot spot of the board.

Current Balancing

Refer to Figures 1 and 2. The ISL62883 achieves current balancing through matching the ISEN pin voltages. R_S and C_S form filters to remove the switching ripple of the phase node voltages. It is recommended to use rather long R_SC_S time constant such that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are R_S = 10kΩ and C_S = 0.22µF.

Layout Guidelines

Table 5 shows the layout considerations. The designators refer to the reference design shown in Figure 27.

TABLE 5. LAYOUT CONSIDERATION

PIN	NAME	LAYOUT CONSIDERATION
EP	GND	Create analog ground plane underneath the controller and the analog signal processing components. Don't let the power ground plane overlap with the analog ground plane. Avoid noisy planes/traces (e.g.: phase node) from crossing over/overlapping with the analog plane.
1	PGOOD	No special consideration
2	PSI#	No special consideration
3	RBIAS	Place the Rbias resistor (R16) in general proximity of the controller. Low impedance connection to the analog ground plane.
4	VR_TT#	No special consideration
5	NTC	The NTC thermistor (R9) needs to be placed close to the thermal source that is monitor to determine thermal throttling. Usually it's placed close to Phase-1 high-side MOSFET.
6	VW	Place the capacitor (C4) across VW and COMP in close proximity of the controller
7	COMP	Place the compensator components (C3, C6 R7, R11, R10 and C11) in general proximity of the controller.
8	FB	
9	ISEN3/FB2	A capacitor (C7) decouples it to VSUM-. Place it in general proximity of the controller. An optional capacitor is placed between this pin and COMP. (It's only used when the controller is configured 2-phase). Place it in general proximity of the controller.
10	ISEN2	A capacitor (C9) decouples it to VSUM-. Place it in general proximity of the controller.
11	ISEN1	A capacitor (C10) decouples it to VSUM-. Place it in general proximity of the controller.
12	VSEN	Place the VSEN/RTN filter (C12, C13) in close proximity of the controller for good decoupling.
13	RTN	

TABLE 5. LAYOUT CONSIDERATION (Continued)

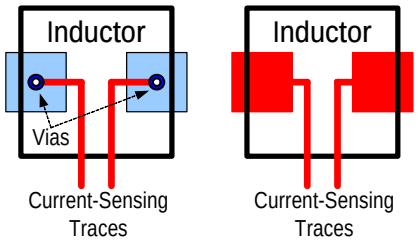
PIN	NAME	LAYOUT CONSIDERATION
14	ISUM-	Place the current sensing circuit in general proximity of the controller. Place C82 very close to the controller. Place NTC thermistors R42 next to Phase-1 inductor (L1) so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUM+ and VSUM- signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. Route R63 and R71 to the Phase-1 side pad of inductor L1. Route R88 to the output side pad of inductor L1. Route R65 and R72 to the Phase-2 side pad of inductor L2. Route R90 to the output side pad of inductor L2. Route R67 and R73 to the Phase-3 side pad of inductor L3. Route R92 to the output side pad of inductor L3. If possible. Route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. 
15	ISUM+	
16	VDD	A capacitor (C16) decouples it to GND. Place it in close proximity of the controller.
17	VIN	A capacitor (C17) decouples it to GND. Place it in close proximity of the controller.
18	IMON	Place the filter capacitor (C21) close to the CPU.
19	BOOT1	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
20	UGATE1	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE1 trace to the Phase-1 high-side MOSFET (Q2 and Q8) source pins instead of general Phase-1 node copper.
21	PHASE1	
22	VSSP1	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing VSSP1 to the Phase-1 low-side MOSFET (Q3 and Q9) source pins instead of general power ground plane for better performance.
23	LGATE1	
24	PWM3	No special consideration.

TABLE 5. LAYOUT CONSIDERATION (Continued)

PIN	NAME	LAYOUT CONSIDERATION
25	VCCP	A capacitor (C22) decouples it to GND. Place it in close proximity of the controller.
26	LGATE2	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing VSSP2 to the Phase-2 low-side MOSFET (Q5 and Q1) source pins instead of general power ground plane for better performance.
27	VSSP2	
28	PHASE2	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE2 trace to the Phase-2 high-side MOSFET (Q4 and Q10) source pins instead of general Phase-2 node copper.
29	UGATE2	
30	BOOT2	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
31~37	VID0~6	No special consideration.
38	VR_ON	No special consideration.
39	DPRSLPVR	No special consideration.
40	CLK_EN#	No special consideration.
Other	Phase Node	Minimize phase node copper area. Don't let the phase node copper overlap with/getting close to other sensitive traces. Cut the power ground plane to avoid overlapping with phase node copper.
Other		Minimize the loop consisting of input capacitor, high-side MOSFETs and low-side MOSFETs (e.g.: C27, C33, Q2, Q8, Q3 and Q9).

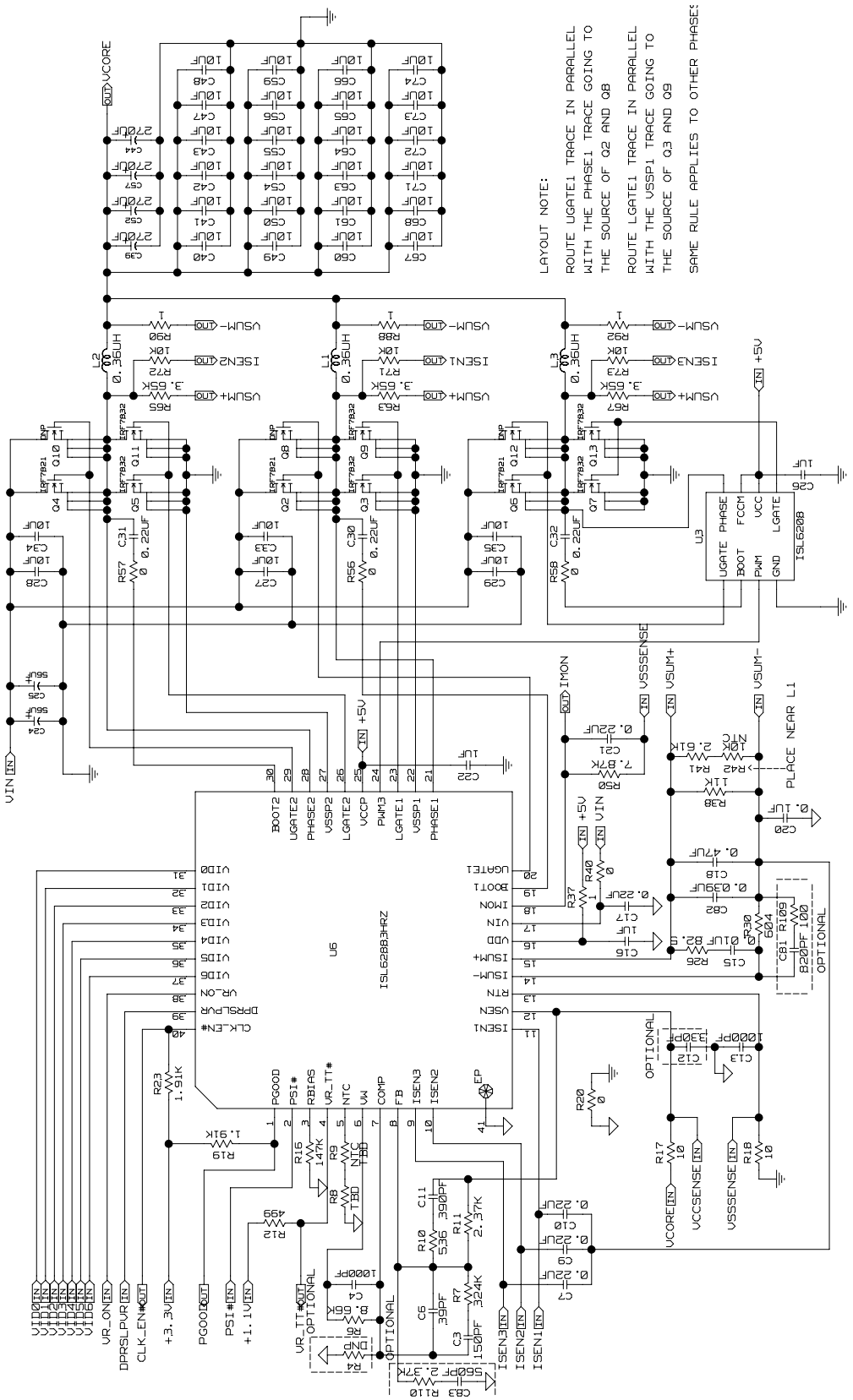


FIGURE 27. 3-PHASE REFERENCE DESIGN

Reference Design Bill of Materials

QTY	REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER	PACKAGE
1	C11	390pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00391-16V10	SM0603
1	C12	330pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00331-16V10	SM0603
1	C13	1000pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00102-16V10	SM0603
1	C15	0.01µF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00103-16V10	SM0603
3	C16, C22, C26	1µF	Multilayer Cap, 16V, 20%	GENERIC	H1045-00105-16V20	SM0603
1	C18	0.47µF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00474-16V10	SM0603
1	C20	0.1µF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00104-16V10	SM0603
8	C21, C7, C9, C10, C17, C30, C31, C32	0.22µF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00224-16V10	SM0603
2	C24, C25	56µF	Radial SP Series Cap, 25V, 20%	SANYO	25SP56M	CASE-CC
6	C27, C28, C29, C33, C34, C35	10µF	Multilayer Cap, 25V, 20%	GENERIC	H1065-00106-25V20	SM1206
1	C3	150pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00151-16V10	SM0603
4	C39, C44, C52, C57	270µF	SPCAP, 2V, 4.5MOHM POLYMER CAP, 2.5V, 4.5mΩ	PANASONIC KEMET	EEFSX0D471E4 T520V477M2R5A(1)E4R5	
1	C4	1000pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00102-16V10	SM0603
24	C40-C43, C47-C50, C53-C56, C59-C69, C78	10µF	Multilayer Cap, 6.3V, 20%	MURATA PANASONIC TDK	GRM21BR61C106KE15L ECJ2FB0J106K C2012X5R0J106K	SM0805
1	C6	39pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00390-16V10	SM0603
1	C81	820pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00821-16V10	SM0603
1	C82	0.039µF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00393-16V10	SM0603
1	C83	560pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00561-16V10	SM0603
3	L1, L2, L3	0.36µH	Inductor, Inductance 20%, DCR 5%	NEC-TOKIN PANASONIC	MPCH1040LR36 ETQP4LR36AFC	10mmx10mm
3	Q2, Q4, Q6		N-Channel Power MOSFET	IR	IRF7821	PWRPAKSO8
6	Q3, Q5, Q7, Q9, Q11, Q13		N-Channel Power MOSFET	IR	IRF7832	PWRPAKSO8
3	Q8, Q10, Q12	DNP				
1	R10	536	Thick Film Chip Resistor, 1%	GENERIC	H2511-05360-1/16W1	SM0603
1	R109	100	Thick Film Chip Resistor, 1%	GENERIC	H2511-01000-1/16W1	SM0603
1	R11	2.37k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02371-1/16W1	SM0603
1	R110	2.37k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02371-1/16W1	SM0603
1	R12	499	Thick Film Chip Resistor, 1%	GENERIC	H2511-04990-1/16W1	SM0603
1	R16	147k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01473-1/16W1	SM0603
2	R17, R18	10	Thick Film Chip Resistor, 1%	GENERIC	H2511-00100-1/16W1	SM0603
4	R19, R71, R72, R73	10k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01002-1/16W1	SM0603
1	R23	1.91k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01911-1/16W1	SM0603
1	R26	82.5	Thick Film Chip Resistor, 1%	GENERIC	H2511-082R5-1/16W1	SM0603
5	R20, R40, R56, R57, R58	0	Thick Film Chip Resistor, 1%	GENERIC	H2511-00R00-1/16W1	SM0603
1	R30	604	Thick Film Chip Resistor, 1%	GENERIC	H2511-06040-1/16W1	SM0603

Reference Design Bill of Materials (Continued)

QTY	REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER	PACKAGE
4	R37, R88, R90, R92	1	Thick Film Chip Resistor, 1%	GENERIC	H2511-01R00-1/16W1	SM0603
1	R38	11k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01102-1/16W1	SM0603
1	R4	DNP				
1	R41	2.61k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02611-1/16W1	SM0603
1	R42	10k NTC	Thermistor, 10k NTC	PANASONIC	ERT-J1VR103J	SM0603
1	R50	7.87k	Thick Film Chip Resistor, 1%	GENERIC	H2511-07871-1/16W1	SM0603
1	R6	8.66k	Thick Film Chip Resistor, 1%	GENERIC	H2511-08662-1/16W1	SM0603
3	R63, R65, R67	3.65k	Thick Film Chip Resistor, 1%	GENERIC	H2511-03651-1/16W1	SM0805
2	R8, R9	DNP				
1	R7	324k	Thick Film Chip Resistor, 1%	GENERIC	H2511-03243-1/16W1	SM0603
1	U3		Synchronous Rectified MOSFET Driver	INTERSIL	ISL6208CBZ	SOIC8_150_50
1	U6		IMVP-6.5 PWM Controller	INTERSIL	ISL62883HRTZ	QFN-40

Typical Performance

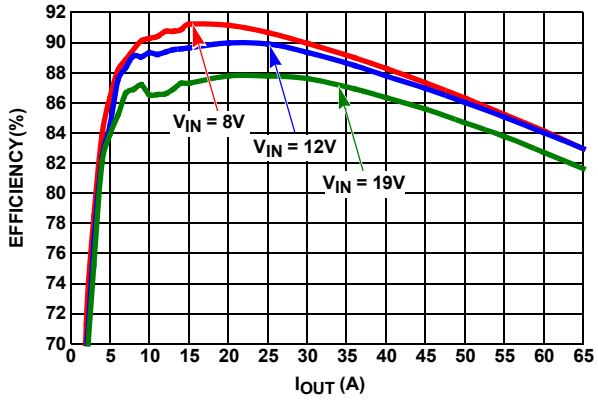


FIGURE 28. 3-PHASE CCM EFFICIENCY, VID = 1.075V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

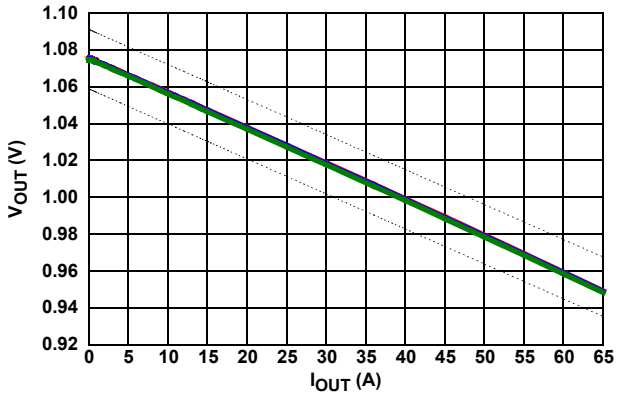


FIGURE 29. 3-PHASE CCM LOAD LINE, VID = 1.075V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

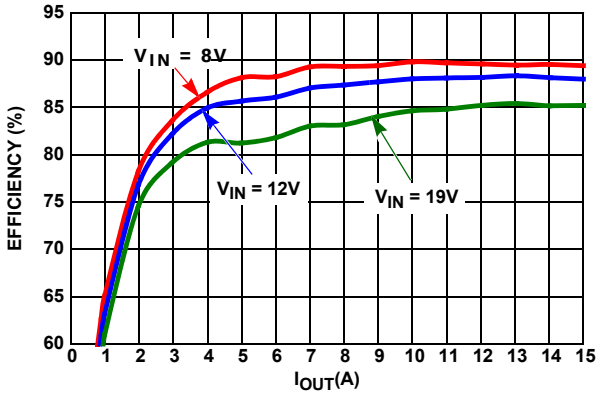


FIGURE 30. 2-PHASE CCM EFFICIENCY, VID = 0.875V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

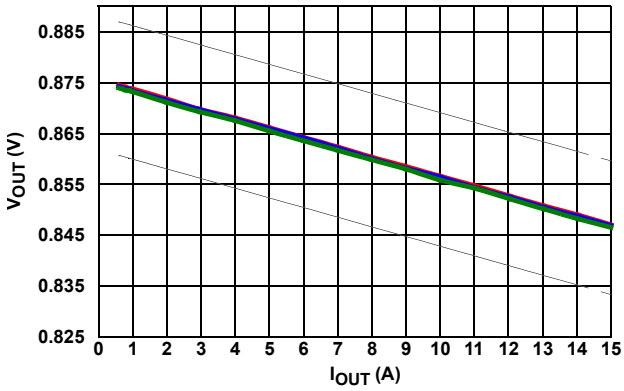


FIGURE 31. 2-PHASE CCM LOAD LINE, VID = 0.875V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

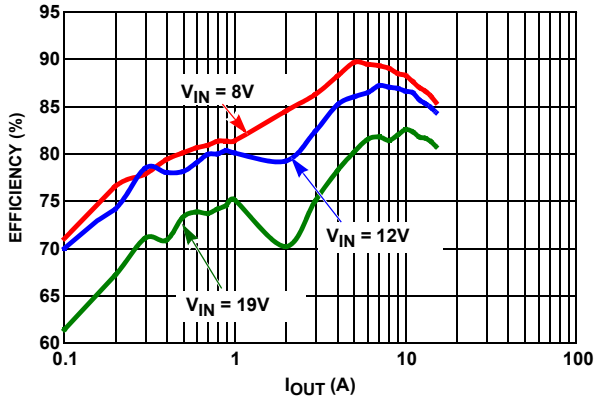


FIGURE 32. 1-PHASE DEM EFFICIENCY, VID = 0.875V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

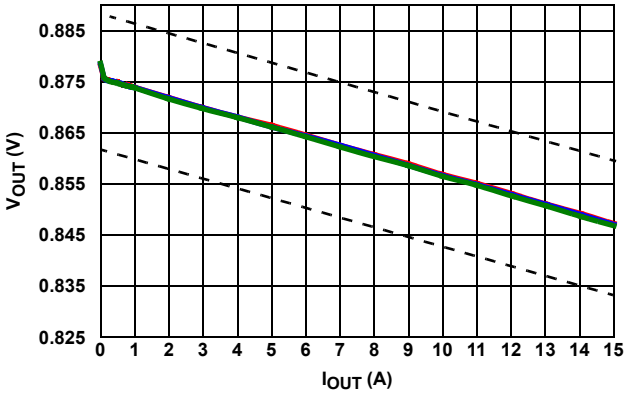


FIGURE 33. 1-PHASE DEM LOAD LINE, VID = 0.875V, V_{IN1} = 8V, V_{IN2} = 12.6V AND V_{IN3} = 19V

Typical Performance (Continued)

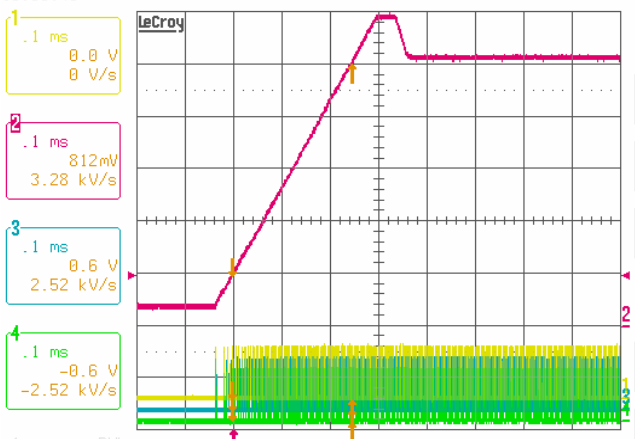


FIGURE 34. SOFT-START, V_{IN} = 19V, I_O = 0A, VID = 0.95V, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

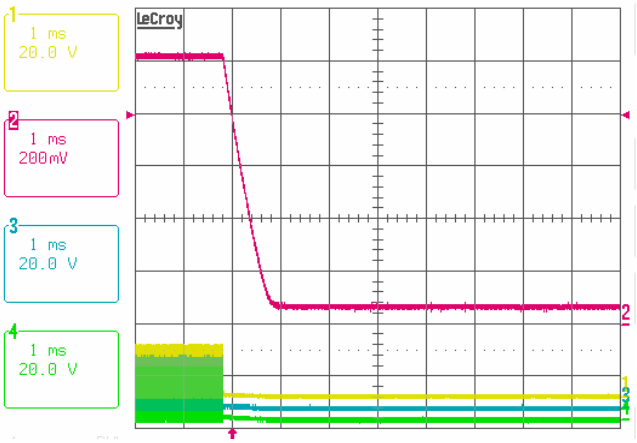


FIGURE 35. SHUT DOWN, V_{IN} = 19V, I_O = 1A, VID = 0.95V, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

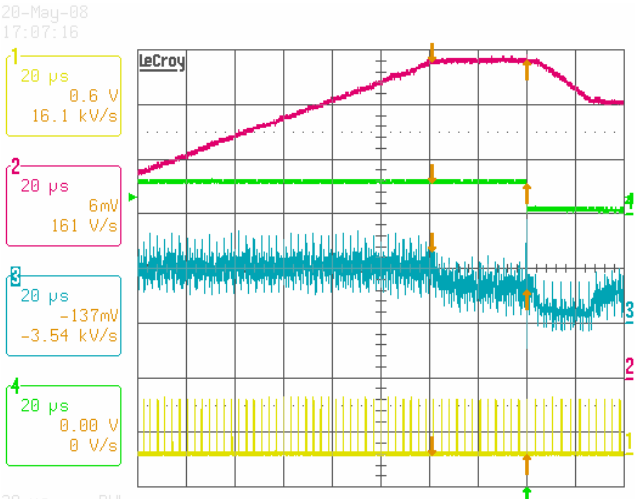


FIGURE 36. CLK_EN# DELAY, V_{IN} = 19V, I_O = 2A, VID = 1.5V, Ch1: PHASE1, Ch2: V_O, Ch3: IMON, Ch4: CLK_EN#

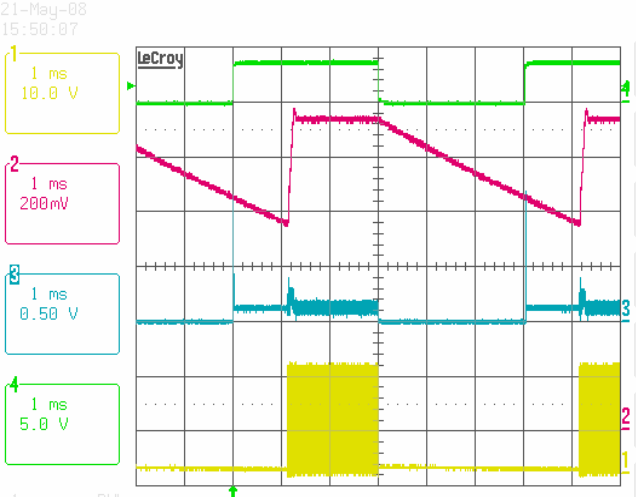


FIGURE 37. PRE-CHARGED START UP, V_{IN} = 19V, VID = 0.95V, Ch1: PHASE1, Ch2: V_O, Ch3: IMON, Ch4: VR_ON

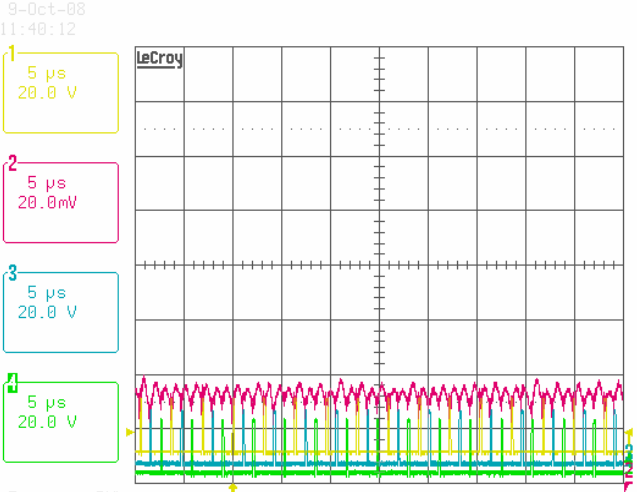


FIGURE 38. STEADY STATE, V_{IN} = 19V, I_O = 51A, VID = 0.95V, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

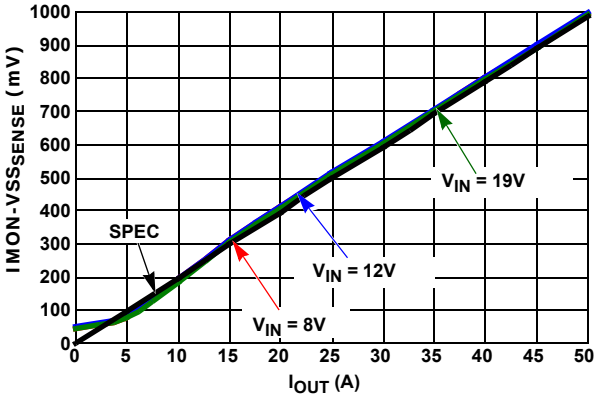


FIGURE 39. IMON, VID = 1.075V

Typical Performance (Continued)

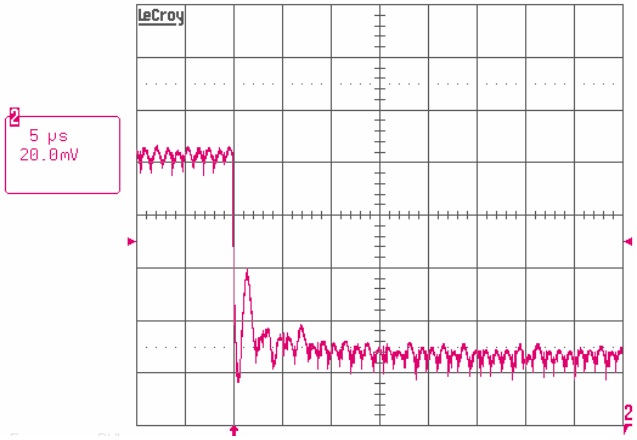


FIGURE 40. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, V_{IN} = 12V, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, I_O = 12A/51A, di/dt = "FASTEST", LL = 1.9mΩ

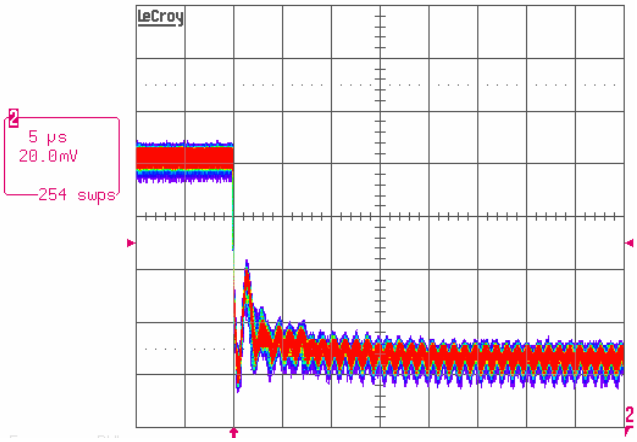


FIGURE 41. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, V_{IN} = 12V, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, I_O = 12A/51A, di/dt = "FASTEST", LL = 1.9mΩ

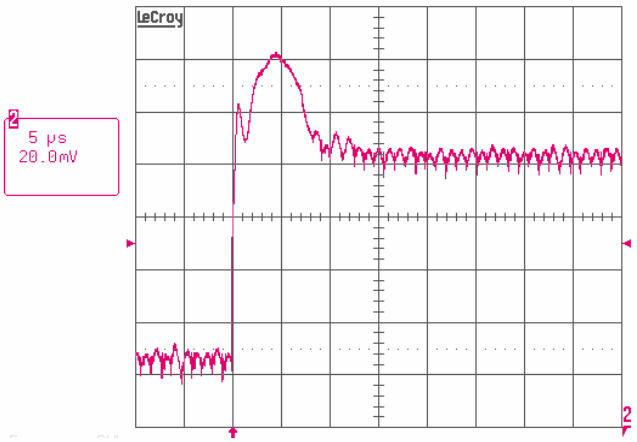


FIGURE 42. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, V_{IN} = 12V, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, I_O = 12A/51A, di/dt = "FASTEST", LL = 1.9mΩ

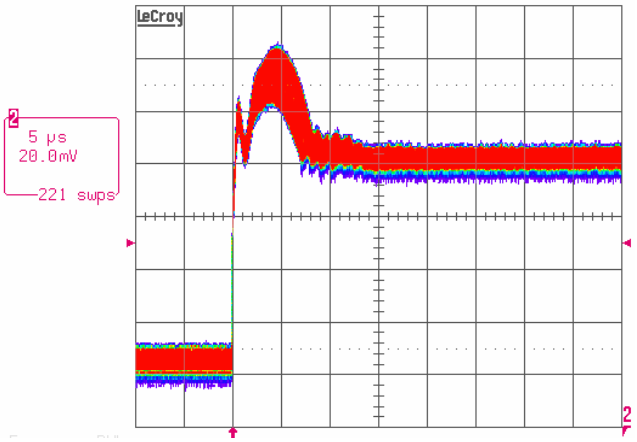


FIGURE 43. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, V_{IN} = 12V, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, I_O = 12A/51A, di/dt = "FASTEST", LL = 1.9mΩ

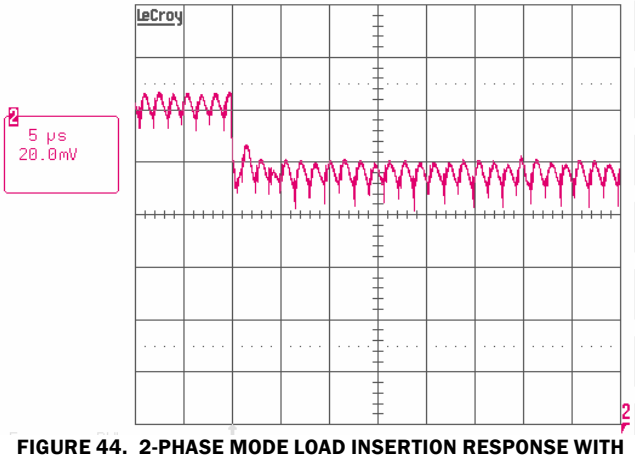


FIGURE 44. 2-PHASE MODE LOAD INSERTION RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, 3-PHASE CONFIGURATION, PSI# = 0, DPRSLPVR = 0, V_{IN} = 12V, VID = 0.875V, I_O = 4A/17A, di/d = "FASTEST

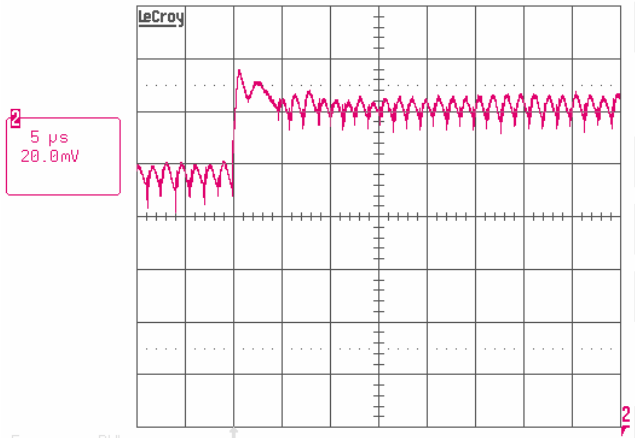


FIGURE 45. 2-PHASE MODE LOAD INSERTION RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, 3-PHASE CONFIGURATION, PSI# = 0, DPRSLPVR=0, V_{IN} = 12V, VID = 0.875V, I_O = 4A/17A, di/dt = "FASTEST"

Typical Performance (Continued)

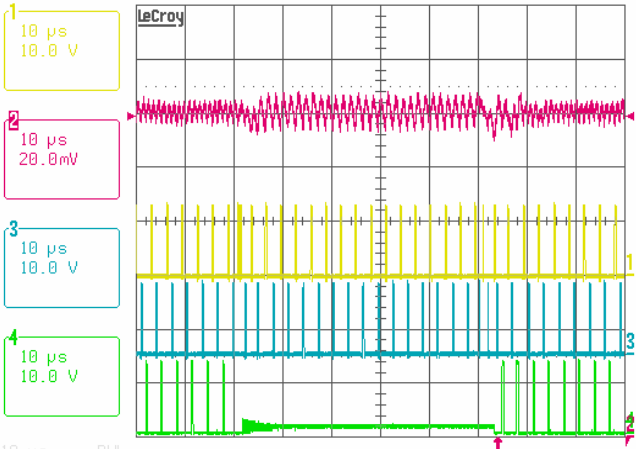


FIGURE 46. PHASE ADDING/DROPPING (PSI# TOGGLE), I_O = 15A, VID = 1.075V, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

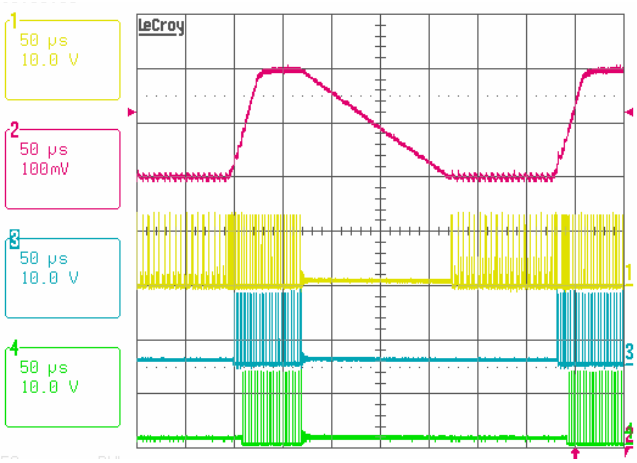


FIGURE 47. DEEPER SLEEP MODE ENTRY/EXIT, I_O = 1.5A, HFM VID = 1.075V, LFM VID = 0.875V, DEEPER SLEEP VID = 0.875V, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

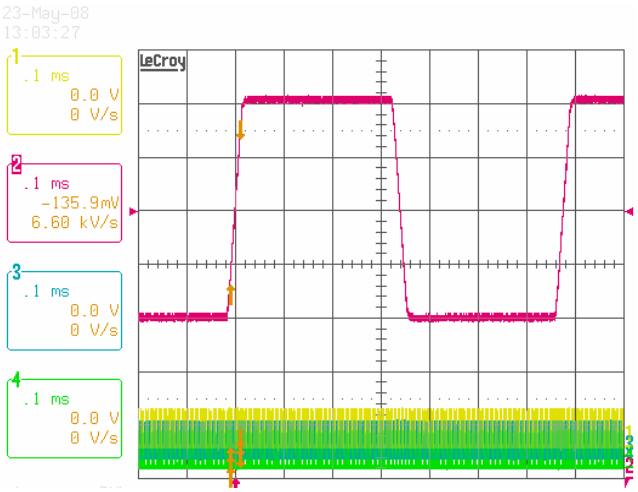


FIGURE 48. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI#=1, DPRSLPVR=0, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

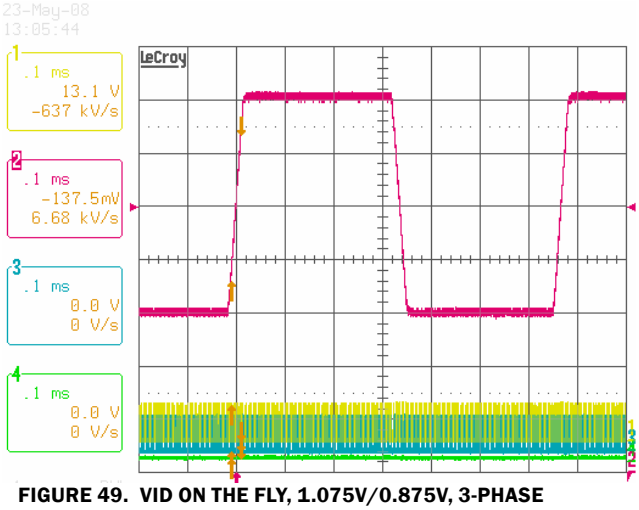


FIGURE 49. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI#=0, DPRSLPVR=0, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

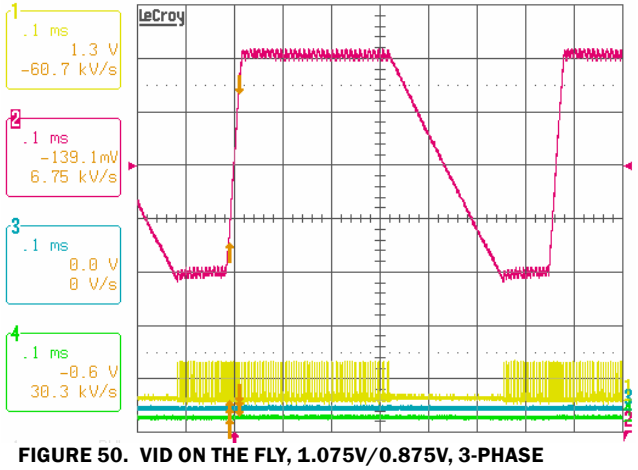


FIGURE 50. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI# = 0, DPRSLPVR = 1, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

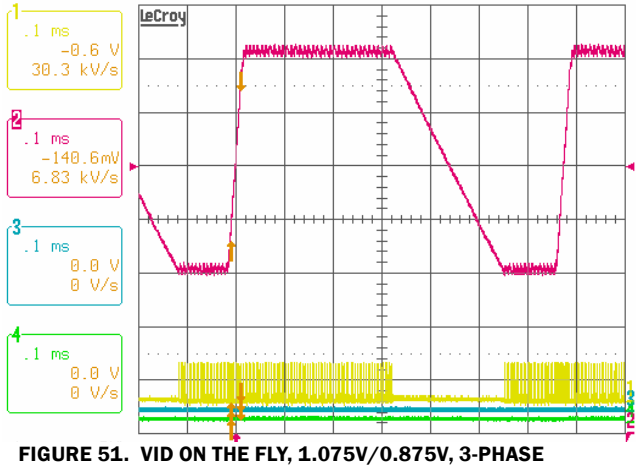


FIGURE 51. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI# = 1, DPRSLPVR = 1, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

Typical Performance (Continued)

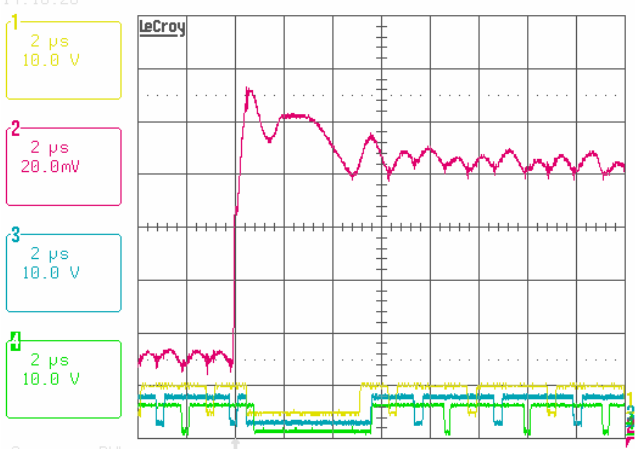


FIGURE 52. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION ENABLED, V_{IN} = 12V, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, I_O = 12A/51A, di/dt = "FASTEST", LL = 1.9mΩ, Ch1: LGATE1, Ch2: V_O, Ch3: LGATE2, Ch4: ISL6208 LGATE

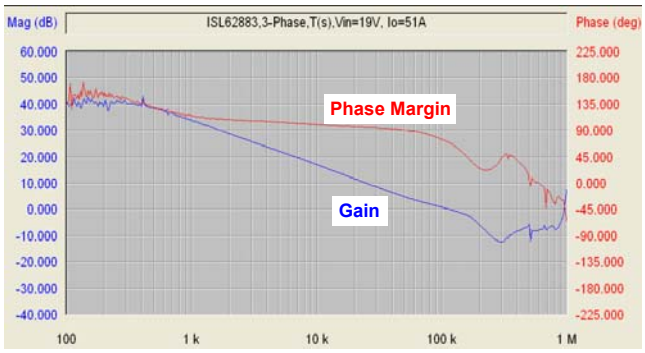


FIGURE 53. REFERENCE DESIGN LOOP GAIN T2(s) MEASUREMENT RESULT

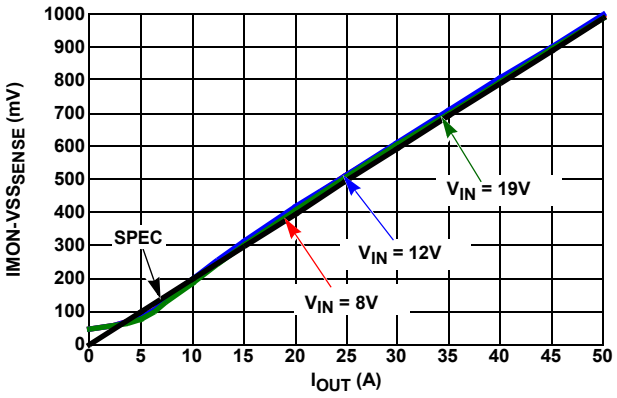


FIGURE 54. IMON, VID = 1.075V

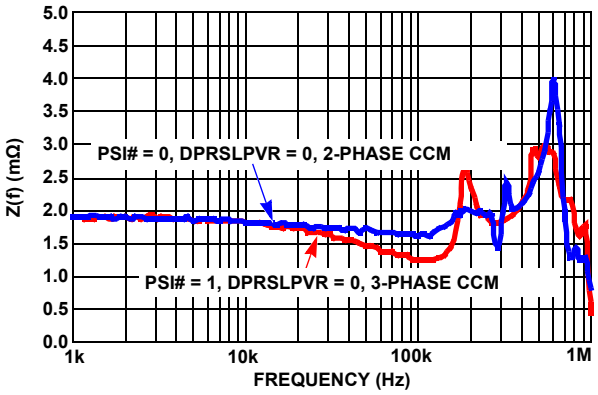


FIGURE 55. REFERENCE DESIGN FDIM RESULT

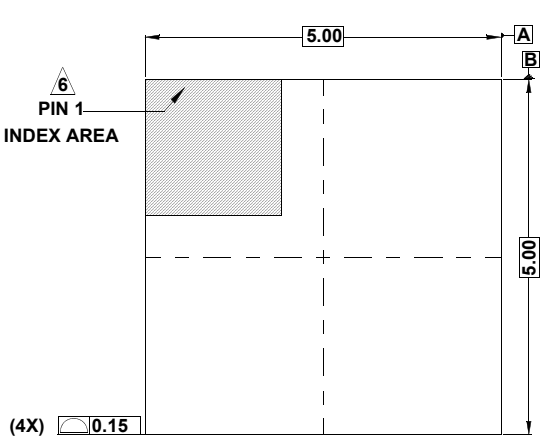
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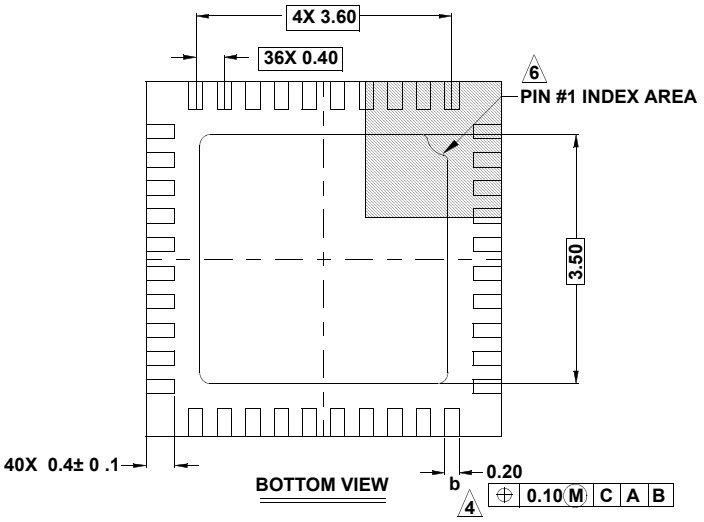
Package Outline Drawing

L40.5x5

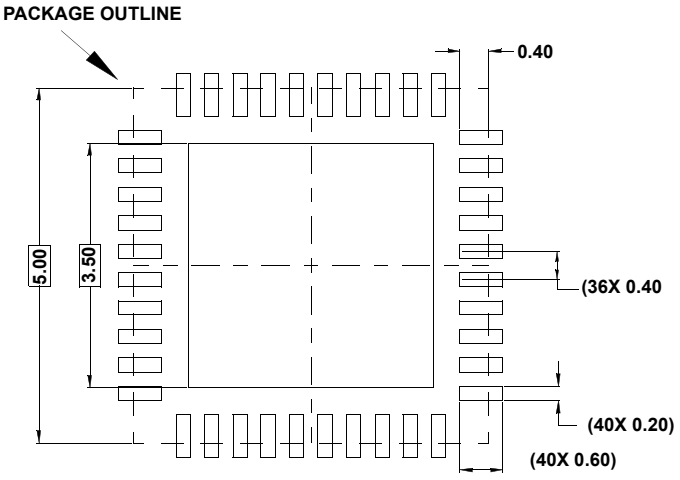
40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 9/10



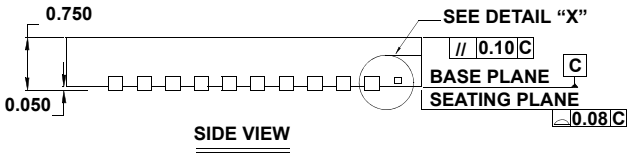
TOP VIEW



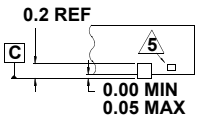
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

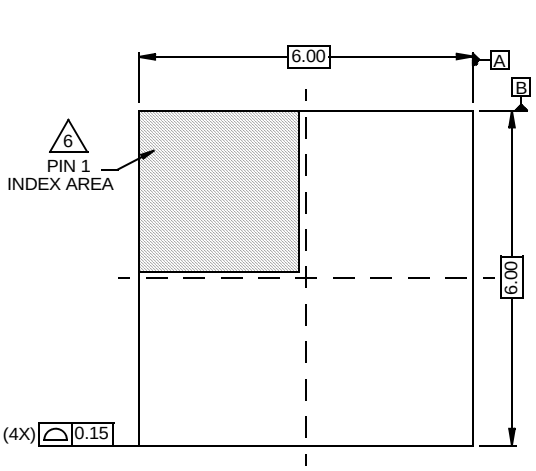
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1

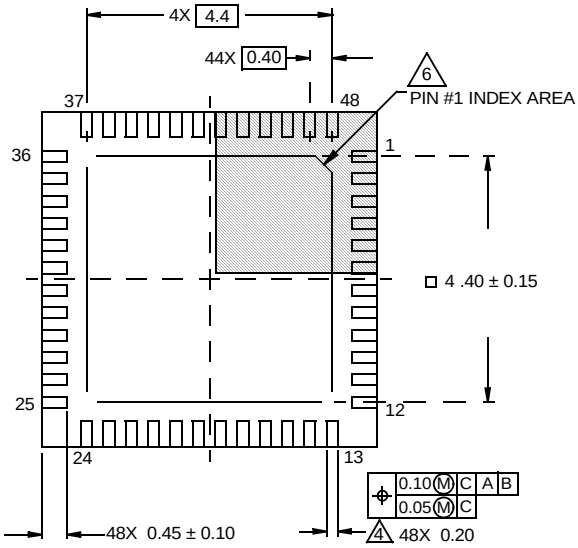
Package Outline Drawing

L48.6x6

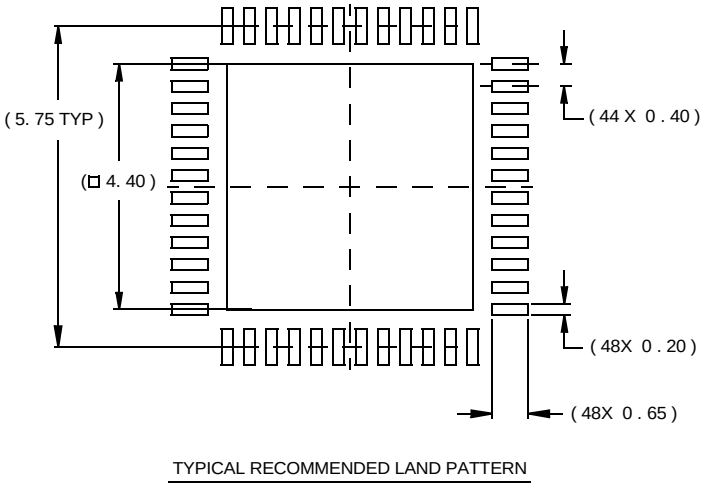
48 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 4/07



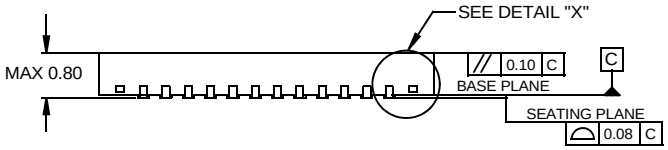
TOP VIEW



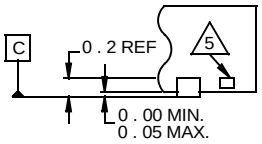
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.