# 1MHz, High-Efficiency, Step-Up Converter with Load Disconnection

## Features

- **Wide 0.8V to $V_{OUT}$ Input Voltage Range**
- **Low 1.05V (typical) Start-Up Voltage**
- **Low 40mA No Load Bias Current**
- **100mA Output from a Single AA Cell Input**
- **250mA Output from a Dual AA Cell Input**
- **Internal Synchronous Rectifier**
- **Up to 92% Efficiency**
- **<1mA Quiescent Current during Shutdown**
- **Current-Mode Operation with Internal Compensation**
  - **Stable with Ceramic Output Capacitors**
  - **Fast Line Transient Response**
- **Fixed 1MHz Oscillator Frequency**
- **1.2A Current-Limit Protection**
- **Built-In Soft-Start**
- **Over-Temperature Protection with Hysteresis**
- **Available in a 2mmx2mm TDFN2x2-8 and TSOT-23-6A Packages**
- **Halogen and Lead Free Available (RoHS Compliant)**

## Applications

- **Cell Phone and Smart Phone**
- **PDA, PMP, and MP3**
- **Digital Camera**
- **Boost Regulator**

## General Description

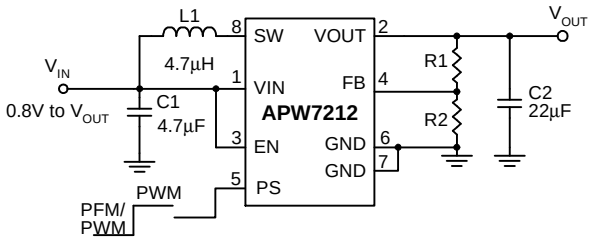
The APW7212 is a synchronous rectifier, fixed switching frequency (1MHz typical), and current-mode step-up regulator. The device allows use of small inductors and output capacitors for portable devices. The current-mode control scheme provides fast transient response and good output voltage accuracy.

At light loads, the APW7212 will automatically enter in pulse frequency modulation(PFM) operation to reduce the dominant switching losses. During PFM operation, the IC consumes very low quiescent current and maintains high efficiency over the complete load range. The device has a 1.05V start-up voltage and can operate with input voltage down to 0.8V after start-up.

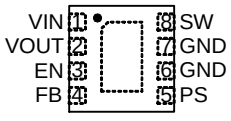
The APW7212 also includes current-limit and over-temperature shutdown to prevent damage in the event of an output overload.

The APW7212 is available in 2mmx2mm TDFN2x2-8 and TSOT-23-6A packages.

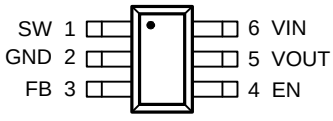
## Simplified Application Circuit




## Pin Configuration




**TDFN2x2-8**
**(Top View)**




**TSOT-23-6A**
**(Top View)**

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

| | |
|---|---|
| APW7212 □□□-□□□<br>Assembly Material<br>Handling Code<br>Temperature Range<br>Package Code | Package Code<br>QB : TDFN2x2-8 CT : TSOT-23-6A<br>Operating Ambient Temperature Range<br>I : -40 to 85°C<br>Handling Code<br>TR : Tape & Reel<br>Assembly Material<br>G: Halogen and Lead Free Device |
| APW7212 QB: 7212 / • X | X - Date Code |
| APW7212 CT: W12X / • | X - Date Code |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | VIN Supply Voltage (VIN to GND) | -0.3 ~ 7 | V |
| $V_{OUT}$ | VOUT to GND Voltage | -0.3 ~ 7 | V |
| $V_{SW}$ | SW to GND Voltage | -0.3 ~ 7 | V |
| | FB, EN and PS to GND Voltage | -0.3 ~ 7 | V |
| $T_J$ | Maximum Junction Temperature | 150 | °C |
| $T_{STG}$ | Storage Temperature | -65 ~ 150 | °C |
| $T_{SDR}$ | Maximum Lead Soldering Temperature, 10 Seconds | 260 | °C |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

| Symbol | Parameter | Typical Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance -Junction to Ambient (Note 2)<br>TDFN2x2-8<br>TSOT-23-6A | <br>85<br>220 | °C/W |

Note 2: $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

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## Recommended Operating Conditions (Note 3)

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $V_{IN}$ | VIN Input Voltage | 0.8 ~ $V_{OUT}$ | V |
| | EB, EN and PS to GND Voltage | -0.3 ~ $V_{OUT}$ +0.3 | V |
| L | Inductor | 1.5 ~ 10 | µH |
| $C_{IN}$ | Input Capacitor | 4.7 ~ | µF |
| $C_{OUT}$ | Output Capacitor | 3.7 ~ | µF |
| $T_A$ | Ambient Temperature | -40 ~ 85 | °C |
| $T_J$ | Junction Temperature | -40 ~ 125 | °C |

Note 3: Refer to the application circuit for further information.

## Electrical Characteristics

Refer to the typical application circuits. These specifications apply over $V_{IN}$ = 1.2V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 0mA, $T_A$ = -40°C to 85°C, unless otherwise noted. Typical values are at $T_A$ = 25°C.

| Symbol | Parameter | Test Conditions | APW7212 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **SUPPLY VOLTAGE AND CURRENT** | | | | | | |
| $V_{IN}$ | Minimum Start-up Voltage | $R_L$ = 3kΩ | - | 1.05 | 1.15 | V |
| | Minimum Operating Voltage after Stat-up | $V_{EN}$ = $V_{IN}$ | - | 0.8 | 0.9 | |
| $V_{OUT}$ | Output Voltage Range | | 1.8 | - | 5.5 | V |
| $I_{DD1}$ | No Switching Quiescent Current | Measured form VOUT, $V_{FB}$ = 1.3V, $V_{OUT}$ = 3.3V, $T_A$=25°C | - | 40 | 60 | µA |
| $I_{DD2}$ | VIN Quiescent Current | Measured from VIN, $V_{IN}$ = 1.2V, $T_A$=25°C | - | 0.5 | 1 | |
| $I_{SD}$ | Shutdown Current | $V_{EN}$ = GND, $V_{IN}$ = 1.2V | - | 0.1 | 1 | µA |
| **REFERENCE AND OUTPUT VOLTAGES** | | | | | | |
| $V_{REF}$ | Regulated Feedback Voltage | $T_A$ = 0 ~ 85°C | -1.5% | 1.23 | +1.5% | V |
| | | $T_A$ = -40 ~ 85°C | -2% | - | +2% | |
| $I_{FB}$ | FB Input Current | $V_{FB}$ = 1.3V | -50 | - | 50 | nA |
| **INTERNAL POWER SWITCH** | | | | | | |
| $F_{SW}$ | Switching Frequency | FB = GND | 0.75 | 1 | 1.25 | MHz |
| $R_{N-FET}$ | N-FET Switch On Resistance | $V_{OUT}$ = 3.3V | - | 0.35 | - | Ω |
| | | $V_{OUT}$ = 5V | - | 0.3 | - | |
| $R_{P-FET}$ | P-FET Switch On Resistance | $V_{OUT}$ = 3.3V | - | 0.6 | - | Ω |
| | | $V_{OUT}$ = 5V | - | 0.55 | - | |
| | N-FET Switch Leakage Current | $V_{SW}$ = 5V | - | 0.05 | 1 | µA |
| | P-FET Switch Leakage Current | $V_{SW}$ = 0V, $V_{OUT}$ = 5V | - | 0.05 | 1 | µA |
| $I_{LIM}$ | N-FET Switch Current-Limit | | 0.9 | 1.2 | - | A |
| | Dead-Time (Note 4) | | - | 10 | - | ns |
| $D_{MAX}$ | SW Maximum Duty Cycle | | 80 | 85 | 95 | % |

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## Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over $V_{IN}$ = 1.2V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 0mA, $T_A$ = -40°C to 85°C, unless otherwise noted. Typical values are at $T_A$ = 25°C.

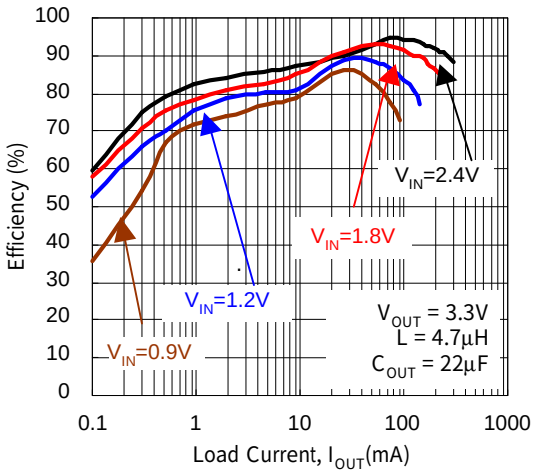
| Symbol | Parameter | Test Conditions | APW7212 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **CONTROL STAGE** | | | | | | |
| EN | EN Input Low Threshold | | - | - | 0.4 | V |
| | EN Input High Threshold | | 1 | - | - | |
| PS | PS Input Low Threshold | | - | - | 0.4 | V |
| | PS Input High Threshold | | 1 | - | - | |
| $I_{EN}$ | EN Input Leakage Current | $V_{EN}$ = 5V or GND | - | 0.4 | 1 | µA |
| $I_{PS}$ | PS Input Leakage Current | $V_{PS}$ = 5V or GND | - | 0.1 | 1 | µA |
| **OVER-TEMPERATURE PROTECTION** | | | | | | |
| $T_{OTP}$ | Over-Temperature Protection (Note 4) | $T_J$ Rising | - | 150 | - | °C |
| | Over-Temperature Protection Hysteresis (Note 4) | | - | 30 | - | °C |

Note 4: Guaranteed by design, not production tested.

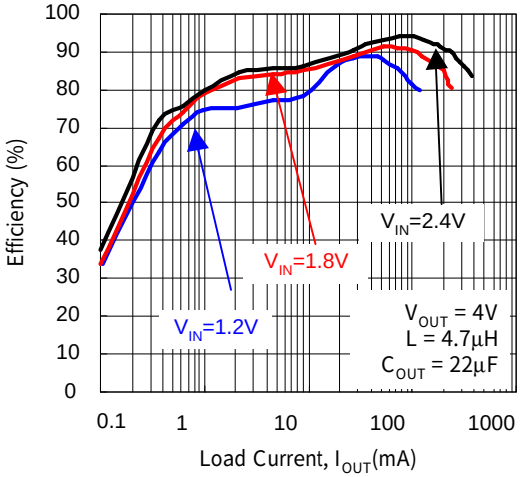
## Typical Operating Characteristics

(Refer to the application circuit in the section"Typical Application Circuits", $V_{IN}$=1.5V, $V_{OUT}$=3.3V, $T_A$=25°C unless otherwise specified )

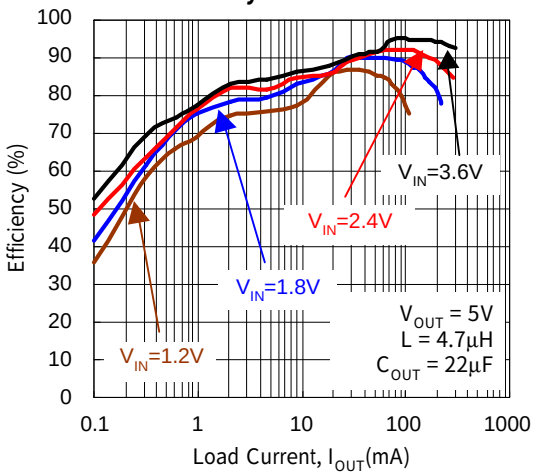
**Efficiency vs. Load Current**



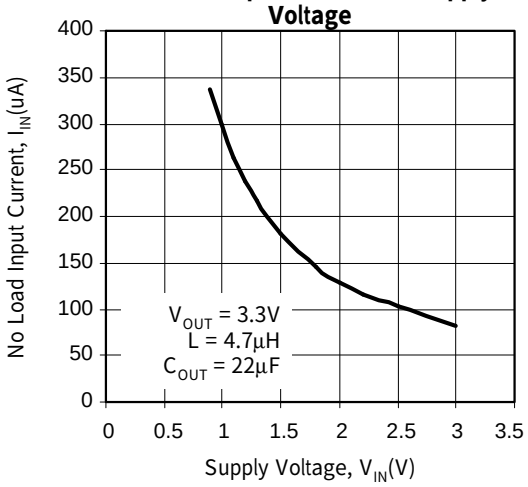

**Efficiency vs. Load Current**



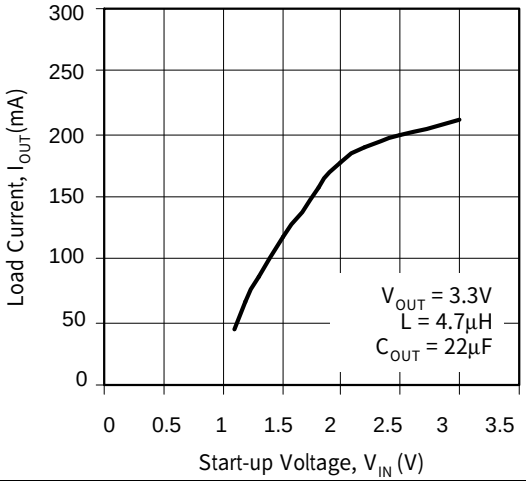

**Efficiency vs. Load Current**




**No Load Input Current vs. Supply Voltage**



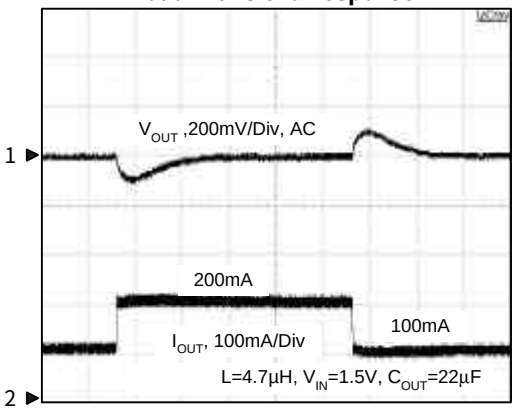

**Start-up Voltage vs. Load Current**



## Operating Waveforms

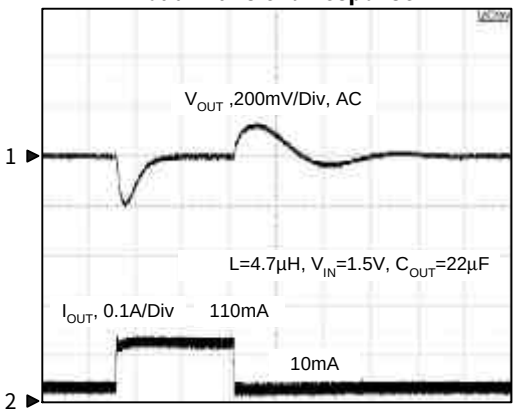
(Refer to the application circuit in the section "Typical Application Circuits", $V_{IN}$=1.5V, $V_{OUT}$=3.3V,$T_A$=25°C unless otherwise specified)

**Load Transient Response**



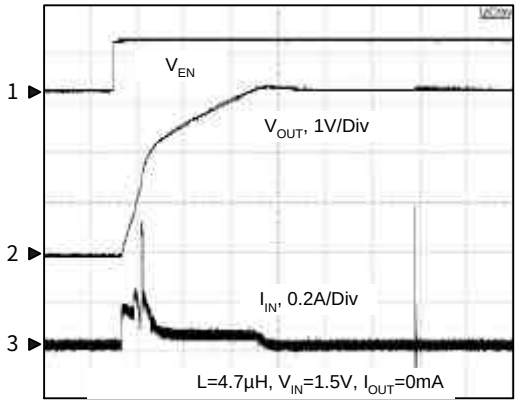

Time: 100µs/Div

**Load Transient Response**



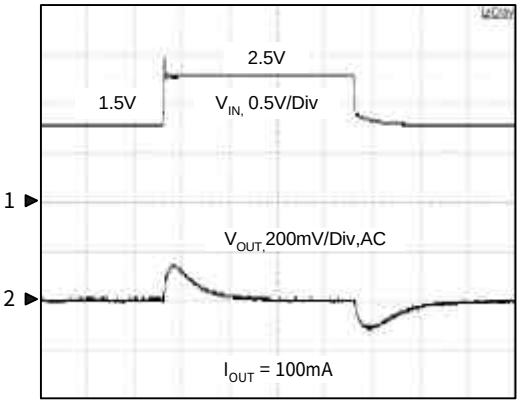

Time: 100µs/Div

**No Load Start-up**



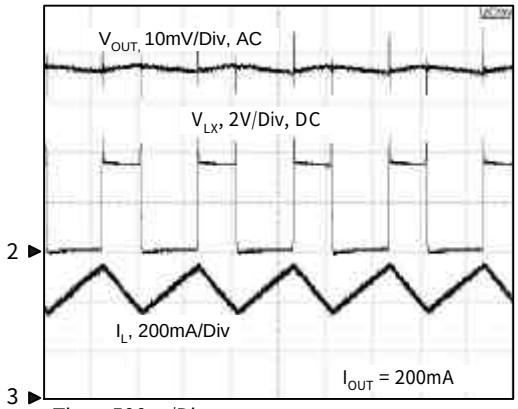

Time: 500µs/Div

**Line Transient Response**



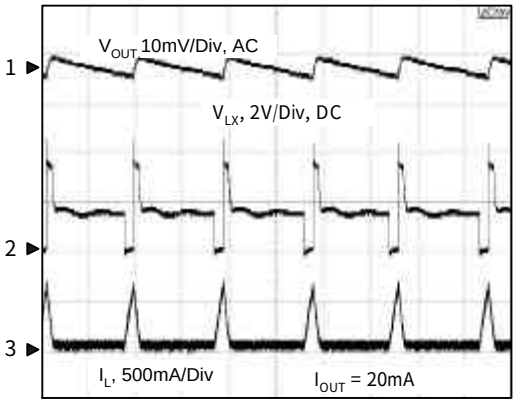

Time: 100µs/Div

**Normal Operating Waveform**




Time: 500ns/Div

**Normal Operating Waveform**




Time: 10µs/Div

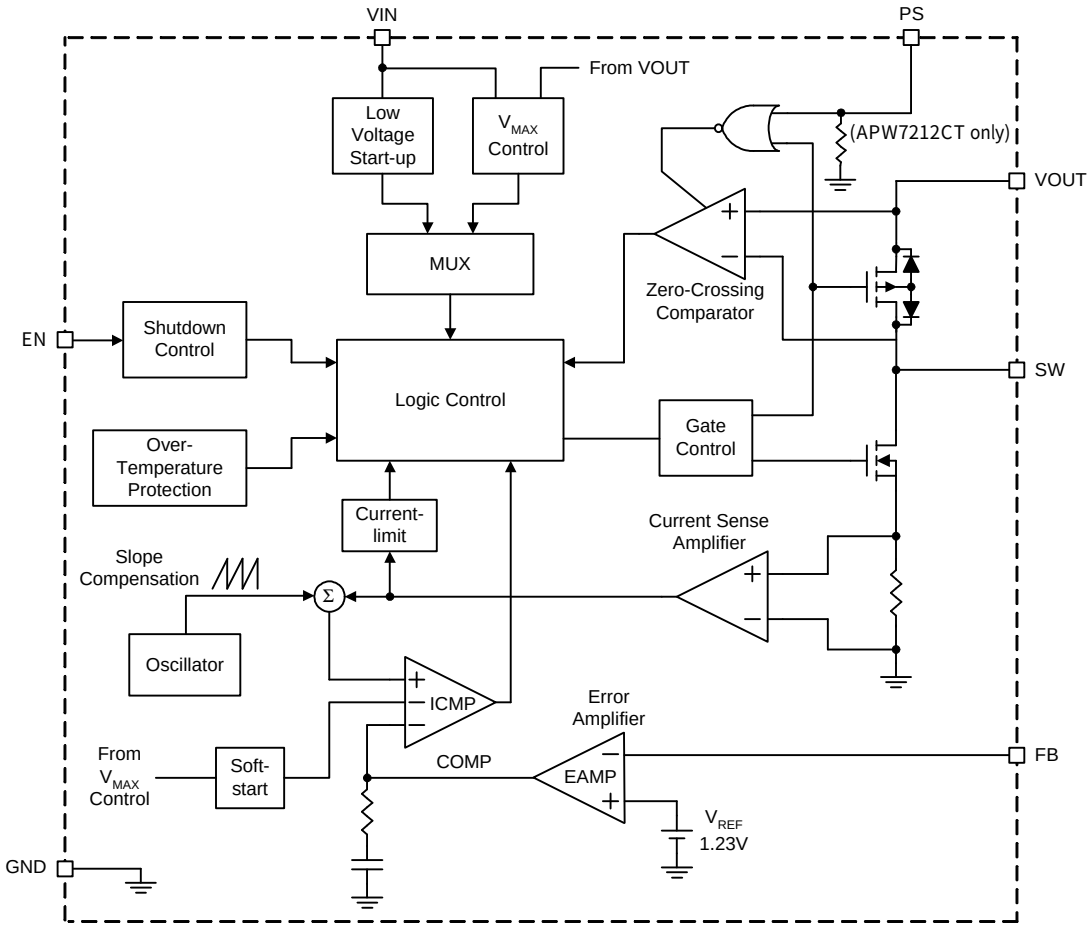
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## Pin Description

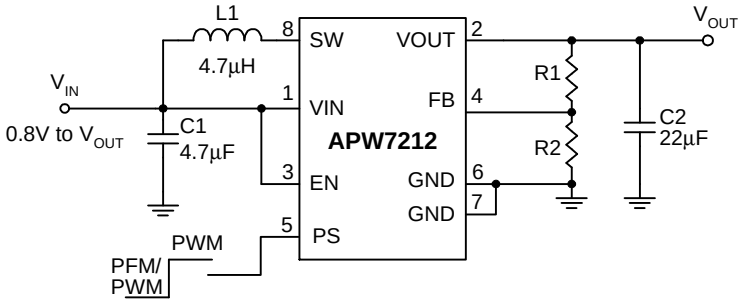
| PIN | | | FUNCTION |
|---|---|---|---|
| NO. | | NAME | |
| TDFN2x2-8 | TSOT-23-6A | | |
| 1 | 6 | VIN | Supply Voltage Input Pin. |
| 2 | 5 | VOUT | Converter output and control circuitry bias supply pin. |
| 3 | 4 | EN | Enable Control Input. Forcing this pin above 1.0V enables the device. Forcing this pin below 0.4V to shut it down. In shutdown, all functions are disabled to decrease the supply current below 1μA. |
| 4 | 3 | FB | Feedback Input. The device senses feedback voltage via FB and regulate the voltage at 1.23V. Connecting FB with a resistor-divider from the output set the output voltage in the range from 1.8 to 5.5V. |
| 5 | - | PS | Pulse Skipping Mode Selection. Pulling this pin to logic high to force boost converter enter PWM mode. Pulling it low to automatic switch under PFM (Pulse Frequency Mode) and PWM mode. Do not leave this pin floating. This pin internally connects to GND for TSOT-23-6 package. |
| 6, 7 | 2 | GND | Power and signal ground pin. |
| 8 | 1 | SW | Switch pin. Connect this pin to inductor. |
| - | - | Exposed PAD | Connected this pad to GND. |

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## Block Diagram




## Typical Application Circuit



## Function Description

### Main Control Loop

The APW7212 is a constant frequency, synchronous rectifier, and current-mode switching regulator. In normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and turned off when an internal comparator (ICMP) resets the latch. The peak inductor current which ICMP resets the RS latch is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external resistive divider connected between $V_{OUT}$ and ground allows the EAMP to receive an output feedback voltage $V_{FB}$ at FB pin. When the load current increases, it causes a slightly decrease in $V_{FB}$ relative to the 1.23V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

### Start-up

A start-up oscillator circuit is integrated in the APW7212. When the device enables, the circuit pumps the output voltage high. Once the output voltage reaches 1.6V (typ), the main DC-DC circuitry turns on and boosts the output voltage to the final regulation voltage.

### Automatic PFM/PWM mode Switch

The APW7212 is a fixed frequency PWM peak current modulation control step-up converter. At light loads, the APW7212 will automatically enter in pulse frequency modulation operation to reduce the dominant switching losses. In PFM operation, the inductor current may reach zero or reverse on each pulse. A zero current comparator turns off the P-channel synchronous MOSFET, forcing DCM(Discontinuous Current Mode) operation at light load. These controls get very low quiescent current, help to maintain high efficiency over the complete load range.

### Synchronous Rectification

The internal synchronous rectifier eliminates the need for an external Schottky diode, thus reducing cost and board space. During the cycle off-time, the P-FET turns on and shunts the FET body diode. As a result, the synchronous rectifier significantly improves efficiency without the addition of an external component. Conversion efficiency can be as high as 92%.

### Load Disconnect

Driving EN to ground places the APW7212 in shutdown mode. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to 1μA maximum.

A special circuit is applied to disconnect the load from the input during shutdown the converter. In conventional synchronous rectifier circuits, the back-gate diode of the high-side P-FET is forward biased in shutdown and allows current flowing from the battery to the output. However, this device uses a special circuit, which takes the cathode of the back-gate diode of the high-side P-FET and disconnects it from the source when the regulator is shutdown. The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components must be added to the design to make sure that the battery is disconnected from the output of the converter.

### Current-Limit Protection

The APW7212 monitors the inductor current, flowing through the N-FET, and limits the current peak at current-limit level to prevent loads and the APW7212 from damages during overload conditions.

### Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7212. When the junction temperature exceeds 150°C, a thermal sensor turns off the both N-FET and P-FET, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature ($T_J$) during continuous thermal overload conditions, increasing the lifetime of the device.

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## Application Information

### Input Capacitor Selection

The input capacitor ($C_{IN}$) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller with larger $C_{IN}$. For reliable operation, it is recommended to select the capacitor voltage rating at least 1.2 times higher than the maximum input voltage. The capacitors should be placed close to the VIN and GND.

### Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, $\Delta I_L$, is 30% to 50% of the average inductor current. The recommended inductor value can be calculated as below:

$$L \geq \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \cdot \frac{V_{OUT}-V_{IN}}{F_{SW}\cdot I_{OUT(MAX)}} \cdot \frac{\eta}{\left(\frac{\Delta I_L}{I_{L(AVG)}}\right)}$$

where

$V_{IN}$ = input voltage

$V_{OUT}$ = output voltage

$F_{SW}$ = switching frequency in MHz

$I_{OUT}$ = maximum output current in amp.

$\eta$ = Efficiency

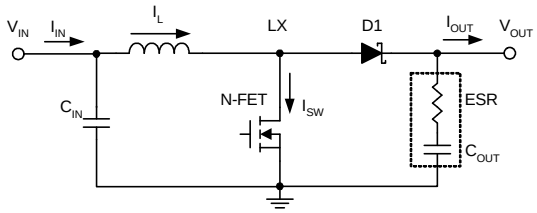
$\Delta I_L / I_{L(AVG)}$ = (0.3 to 0.5 typical)

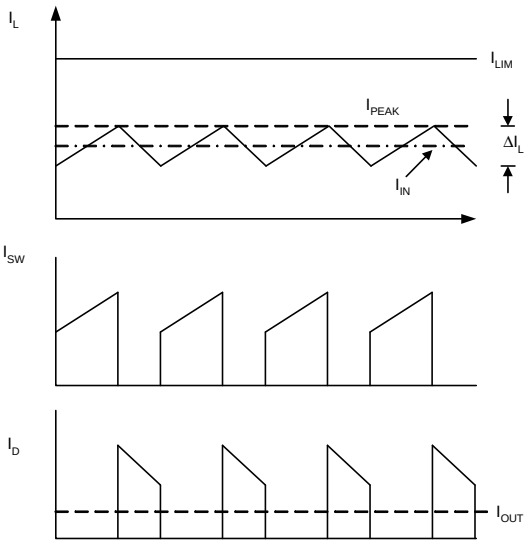
To avoid saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)}\cdot V_{OUT}}{V_{IN}\cdot \eta}$$

The peak inductor current is calculated as below:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2}\cdot\frac{V_{IN}\cdot(V_{OUT}-V_{IN})}{V_{OUT}\cdot L\cdot F_{SW}}$$




### Output Capacitor Selection

The current-mode control scheme of the APW7212 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{COUT} \cong \frac{I_{OUT}}{C_{OUT}}\cdot\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}\cdot F_{SW}}\right)$$

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$$

$$\Delta V_{ESR} \cong I_{PEAK}\cdot R_{ESR}$$

## Application Information (Cont.)

### Output Capacitor Selection (Cont.)

Where $I_{PEAK}$ is the peak inductor current. For ceramic capacitor application, the output voltage ripple is dominated by the $\Delta V_{COUT}$. When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

### Output Voltage Setting

A resistive divider sets the output voltage. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in "Typical Application Circuits". A suggestion of the maximum value of R1 is 2MΩ and R2 is 600kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

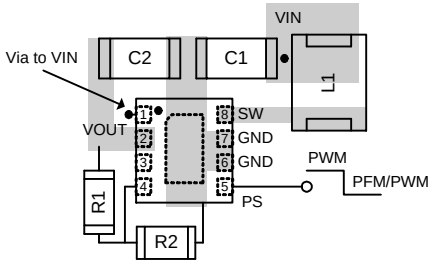
$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) = 1.23\left(1 + \frac{R1}{R2}\right)$$

### Layout Consideration

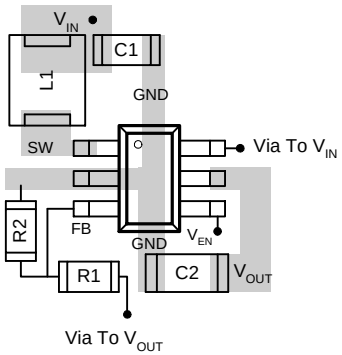
For all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not done carefully, the regulator may show noise problems and duty cycle jitter.

1. Since the VOUT supplies IC bias voltage, the output capacitor should be placed close to the VOUT and GND. Connecting the capacitor with VOUT and GND pins by short and wide tracks without using any via holes for good filtering and minimizing the voltage ripple.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
3. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
4. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

### Layout Consideration



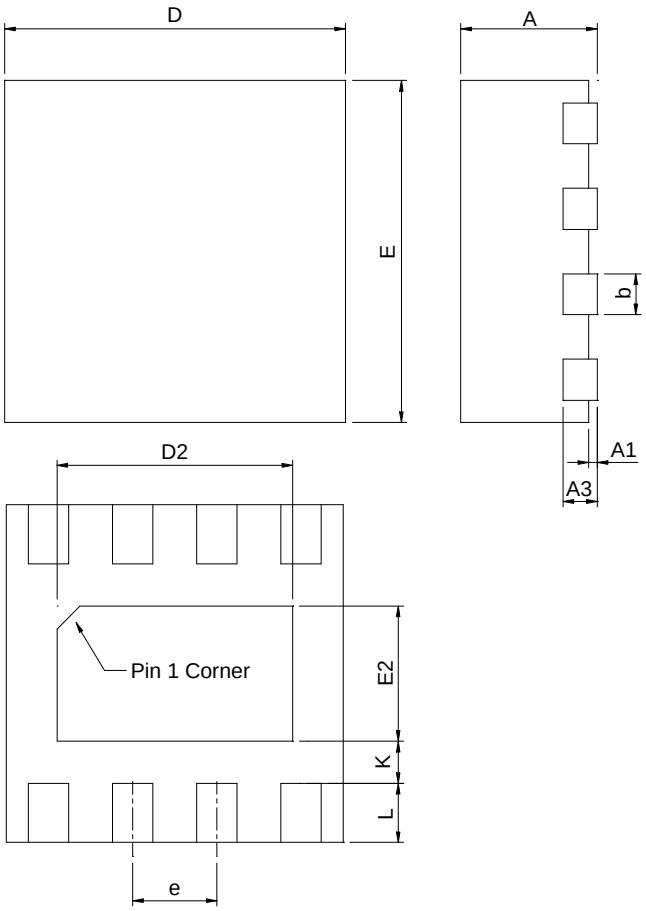

**APW7212 Layout Suggestion**




**APW7212 Layout Suggestion**

## Package Information

**TDFN2x2-8**

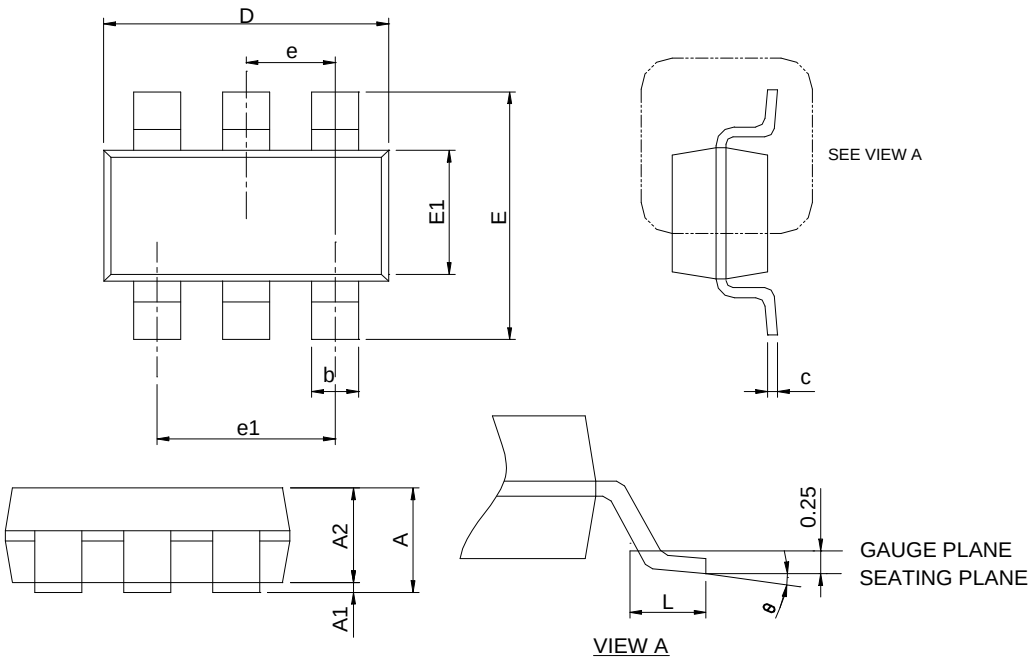



| SYMBOL | TDFN2x2-8 | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.70 | 0.80 | 0.028 | 0.031 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.20 REF | | 0.008 REF | |
| b | 0.18 | 0.30 | 0.007 | 0.012 |
| D | 1.90 | 2.10 | 0.075 | 0.083 |
| D2 | 1.00 | 1.60 | 0.039 | 0.063 |
| E | 1.90 | 2.10 | 0.075 | 0.083 |
| E2 | 0.60 | 1.00 | 0.024 | 0.039 |
| e | 0.50 BSC | | 0.020 BSC | |
| L | 0.30 | 0.45 | 0.012 | 0.018 |
| K | 0.20 | | 0.008 | |

Note : 1. Followed from JEDEC MO-229 WCCD-3.

## Package Information

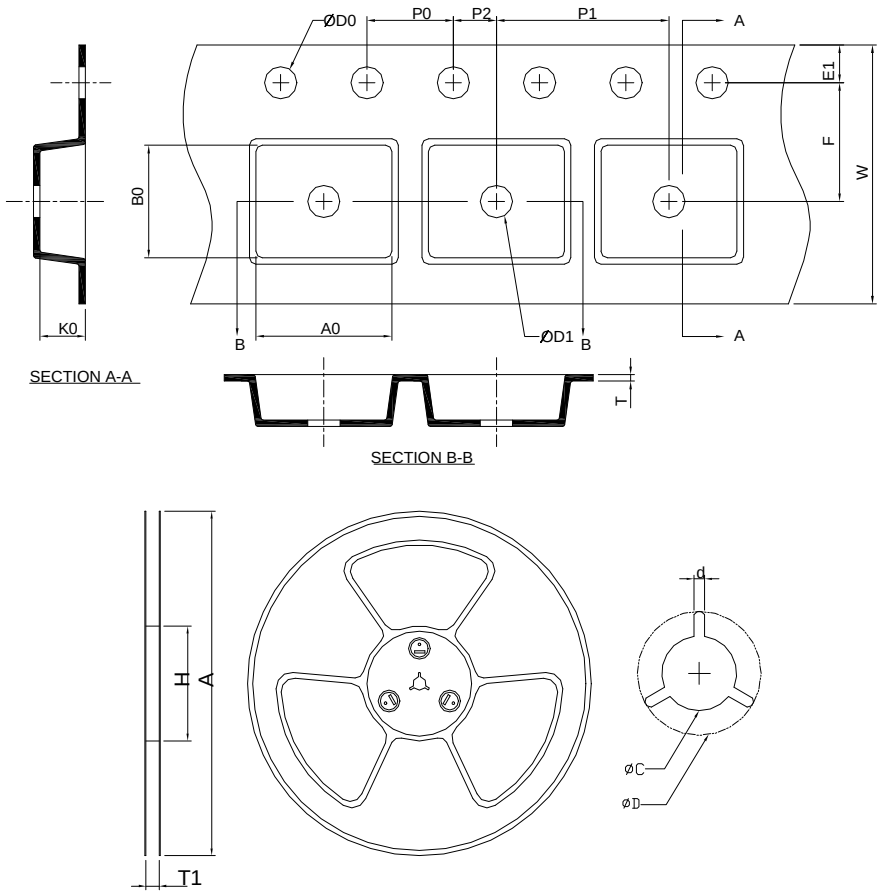
**TSOT-23-6A**




| SYMBOL | TSOT-23-6A | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.70 | 1.00 | 0.028 | 0.039 |
| A1 | 0.01 | 0.10 | 0.000 | 0.004 |
| A2 | 0.70 | 0.90 | 0.028 | 0.035 |
| b | 0.30 | 0.50 | 0.012 | 0.020 |
| c | 0.08 | 0.20 | 0.003 | 0.008 |
| D | 2.70 | 3.10 | 0.106 | 0.122 |
| E | 2.60 | 3.00 | 0.102 | 0.118 |
| E1 | 1.40 | 1.80 | 0.055 | 0.071 |
| e | 0.95 BSC | | 0.037 BSC | |
| e1 | 1.90 BSC | | 0.075 BSC | |
| L | 0.30 | 0.60 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |

Note : Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| TDFN2x2-8 | 178.0±2.00 | 50 MIN. | 8.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 8.0±0.20 | 1.75±0.10 | 3.50±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 4.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.4 | 3.35 MIN | 3.35 MIN | 1.30±0.20 |
| **Application** | **A** | **H** | **T1** | **C** | **d** | **D** | **W** | **E1** | **F** |
| TSOT-23-6A | 178.0±2.00 | 50 MIN. | 8.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 8.0±0.30 | 1.75±0.10 | 3.5±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 4.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.0 MIN. | 0.6+0.00 -0.40 | 3.20±0.20 | 3.10±0.20 | 1.50±0.20 |

(mm)

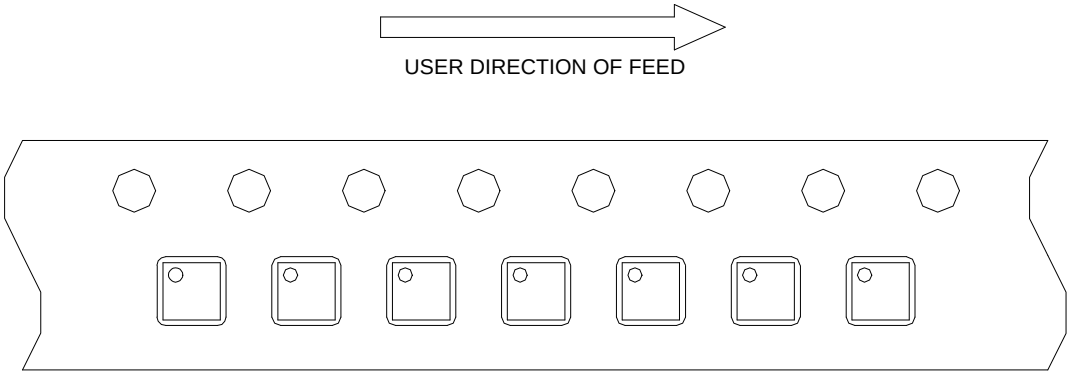
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## Devices Per Unit

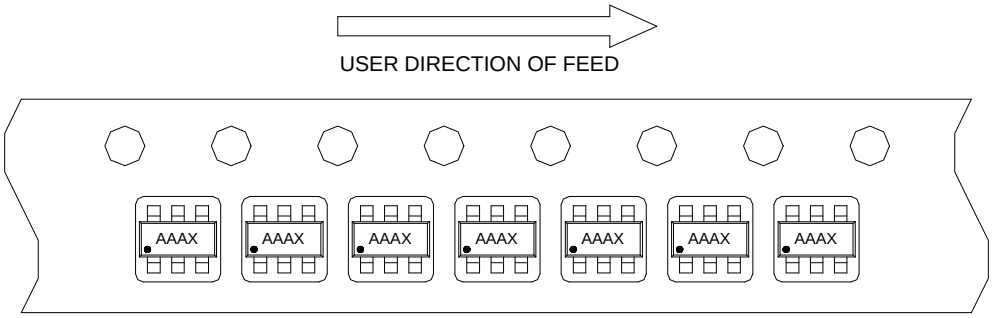
| Package Type | Unit | Quantity |
|---|---|---|
| **TDFN2x2-8** | Tape & Reel | 3000 |
| **TSOT-23-6A** | Tape & Reel | 3000 |

## Taping Direction Information

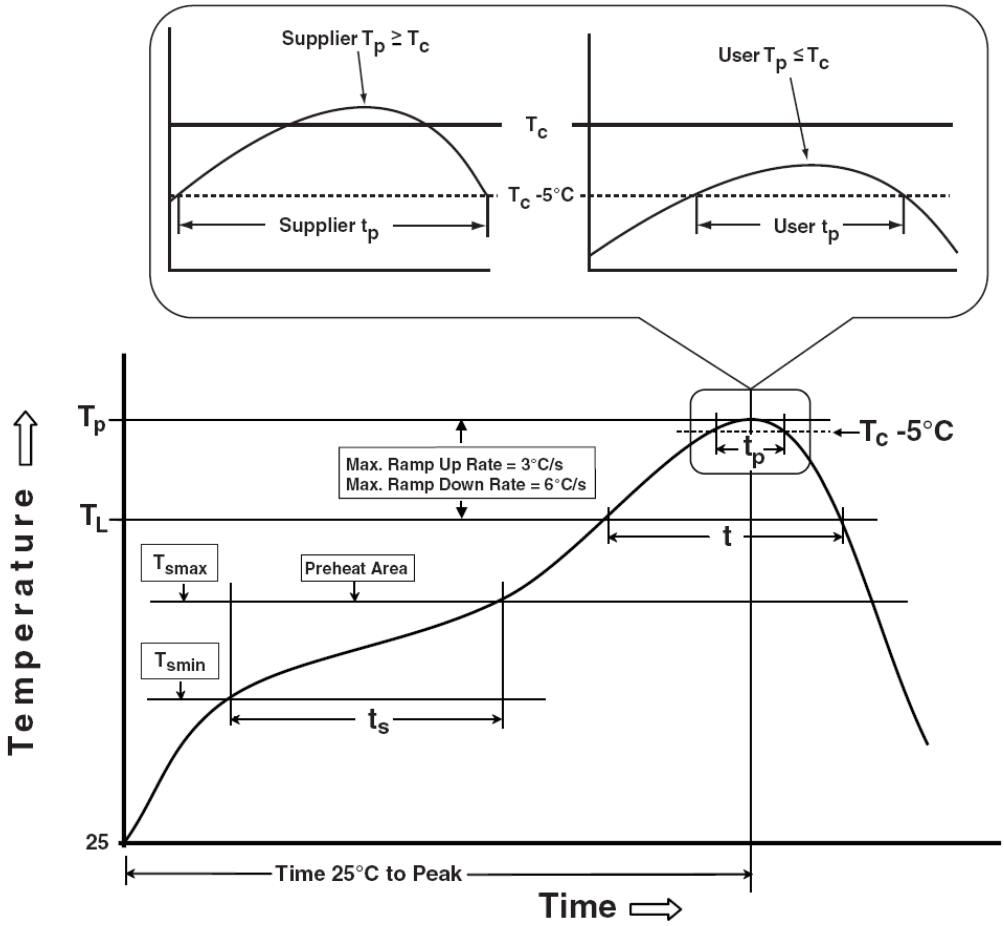
**TDFN2x2-8**




**TSOT-23-6**



## Classification Profile




## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | <br>100 °C<br>150 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3 °C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

## Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ ³350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ Tj=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

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