FAIRCHILD SEMICONDUCTOR®

March 2008

NC7SZ125
TinyLogic® UHS Buffer with 3-STATE Output

Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ Pb-Free leadless package
- Ultra High Speed; t_{PD} 2.6ns Typ. into 50pF at 5V V_{CC}
- High Output Drive; ±24mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

General Description

The NC7SZ125 is a single buffer with 3-STATE output from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V range.

The inputs and output are high impedance above ground when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage. The output tolerates voltages above V_{CC} when in the 3-STATE condition.

Ordering Information

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ125M5X	MA05B	7Z25	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZ125P5X	MAA05A	Z25	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ125L6X	MAC06A	DD	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

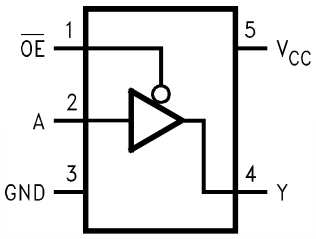
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

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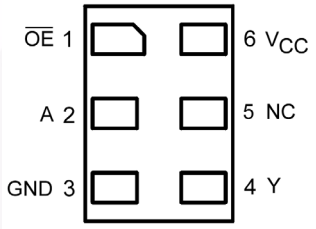
Connection Diagram

Pin Assignment for SC70 and SOT23



(Top View)

Pad Assignment for MicroPak



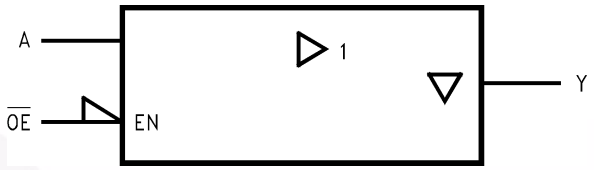
(Top Thru View)

Pin Description

Pin Names	Description
A, $\overline{OE}$	Inputs
Y	Output
NC	No Connect

Logic Symbol

IEEE/IEC



Function Table

Inputs		Output
$\overline{OE}$	In A	Out Y
L	L	L
L	H	H
H	X	Z

H = HIGH Logic Level

L = LOW Logic Level

X = HIGH or LOW Logic Level

Z = HIGH Impedance State

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +6V
V_{IN}	DC Input Voltage	–0.5V to +6V
V_{OUT}	DC Output Voltage	–0.5V to +6V
I_{IK}	DC Input Diode Current @ V_{IN} < –0.5V @ V_{IN} > 6V	 –50mA +20mA
I_{OK}	DC Output Diode Current @ V_{OUT} < –0.5V @ V_{OUT} > 6V, V_{CC} = GND	 –50mA +20mA
I_{OUT}	DC Output Current	±50mA
I_{CC}/I_{GND}	DC V_{CC}/GND Current	±50mA
T_{STG}	Storage Temperature	-65°C to +150°C
T_J	Junction Temperature under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation @ +85°C SOT23-5 SC70-5	 200mW 150mW

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage Operation	1.65V to 5.5V
V_{CC}	Supply Voltage Data Retention	1.5V to 5.5V
V_{IN}	Input Voltage	0V to 5.5V
V_{OUT}	Output Voltage Active State 3-STATE	 0V to V_{CC} 0V to 5.5V
T_A	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 1.8V, 2.5V ±0.2V V_{CC} = 3.3V ±0.3V V_{CC} = 5.0V ±0.5V	 0ns/V to 20ns/V 0ns/V to 10ns/V 0ns/V to 5ns/V
θ_{JA}	Thermal Resistance SOT23-5 SC70-5	 300°C/W 425°C/W

Notes:

1. Unused inputs must be held HIGH or LOW. They may not float.

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DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = –40°C to +85°C		Unit
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.65–1.95			0.75 x V_{CC}			0.75 x V_{CC}		V
		2.3–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	1.65–1.95					0.25 x V_{CC}		0.25 x V_{CC}	V
		2.3–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IH}	I_{OH} = –100µA	1.55	1.65		1.55		V
		1.8			1.7	1.8		1.7		
		2.3			2.2	2.3		2.2		
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		1.65		I_{OH} = –4mA	1.29	1.52		1.29		
		2.3		I_{OH} = –8mA	1.9	2.15		1.9		
		3.0		I_{OH} = –16mA	2.4	2.80		2.4		
		3.0		I_{OH} = –24mA	2.3	2.68		2.3		
		4.5		I_{OH} = –32mA	3.8	4.20		3.8		
V_{OL}	LOW Level Output Voltage	1.65	V_{IN} = V_{IL}	I_{OL} = 100µA		0.0	0.1		0.0	V
		1.8				0.0	0.1		0.1	
		2.3				0.0	0.1		0.1	
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		1.65		I_{OL} = 4mA		0.08	0.24		0.24	
		2.3		I_{OL} = 8mA		0.10	0.3		0.3	
		3.0		I_{OL} = 16mA		0.15	0.4		0.4	
		3.0		I_{OL} = 24mA		0.22	0.55		0.55	
		4.5		I_{OL} = 32mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0–5.5	0 ≤ V_{IN} ≤ 5.5V				±1		±10	µA
I_{OZ}	3-STATE Output Leakage	0–5.5	V_{IN} = V_{IH} or V_{IL}, 0 ≤ V_O ≤ 5.5V				±1		±10	µA
I_{OFF}	Power Off Leakage Current	0.0	V_{IN} or V_{OUT} = 5.5V				1		10	µA
I_{CC}	Quiescent Supply Current	1.65–5.5	V_{IN} = 5.5V, GND				2.0		20	µA

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AC Electrical Characteristics

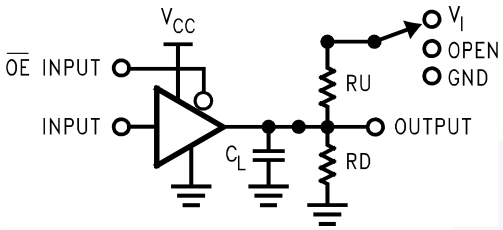
Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40°C to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PHL}	Propagation Delay	1.65	C_L = 15pF, R_D = 1MΩ, S_1 = OPEN	2.0	6.4	13.2	2.0	13.8	ns	Figure 1 Figure 3
		1.8		2.0	5.3	11.0	2.0	11.5		
		2.5 ± 0.2		0.8	3.4	7.5	0.8	8.0		
		3.3 ± 0.3		0.5	2.5	5.2	0.5	5.5		
		5.0 ± 0.5		0.5	2.1	4.5	0.5	4.8		
t_{PLH}, t_{PHL}	Propagation Delay	3.3 ± 0.3	C_L = 50pF, R_D = 500Ω, S_1 = OPEN	1.5	3.2	5.7	1.5	6.0	ns	Figure 1 Figure 3
		5.0 ± 0.5		0.8	2.6	5.0	0.8	5.3		
t_{PZL}, t_{PZH}	Output Enable Time	1.65	C_L = 50 pF, RD = 500Ω, RU = 500Ω, S_1 = GND for t_{PZH}, S_1 = V_{IN} for t_{PZL}, V_{IN} = 2 x V_{CC}	2.0	8.4	15.0	2.0	15.6	ns	Figure 1 Figure 3
		1.8		2.0	7.0	12.5	2.0	13		
		2.5 ± 0.2		1.5	4.6	8.5	1.5	9		
		3.3 ± 0.3		1.5	3.5	6.2	1.5	6.5		
		5.0 ± 0.5		0.8	2.8	5.5	0.8	5.8		
t_{PLZ}, t_{PHZ}	Output Disable Time	1.65	C_L = 50pF, RD = 500Ω, RU = 500Ω, S_1 = GND for t_{PHZ}, S_1 = V_{IN} for t_{PLZ}, V_{IN} = 2 x V_{CC}	2.0	6.5	13.2	2.0	14.5	ns	Figure 1 Figure 3
		1.8		2.0	5.4	11	2.0	12		
		2.5 ± 0.2		1.5	3.5	8	1.5	8.5		
		3.3 ± 0.3		1.0	2.8	5.7	1.0	6		
		5.0 ± 0.5		0.5	2.1	4.7	0.5	5.0		
C_{IN}	Input Capacitance	0			4				pF	
C_{OUT}	Output Capacitance	0			8				pF	
C_{PD}	Power Dissipation Capacitance	3.3	(2)		17				pF	Figure 2
		5.0			24					

Note:

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static).

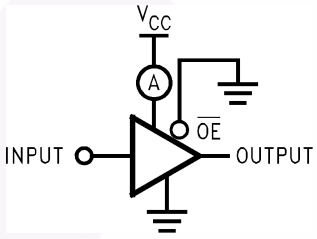
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AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0MHz; t_W = 500ns

Figure 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f$ = 1.8ns;
PRR = 10 MHz; Duty Cycle = 50%

Figure 2. I_{CCD} Test Circuit

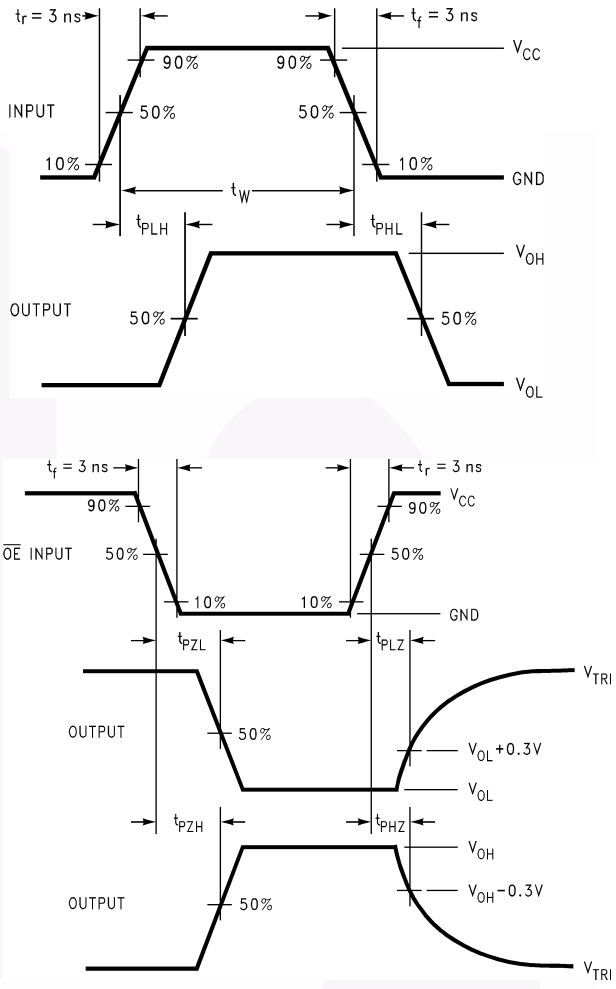


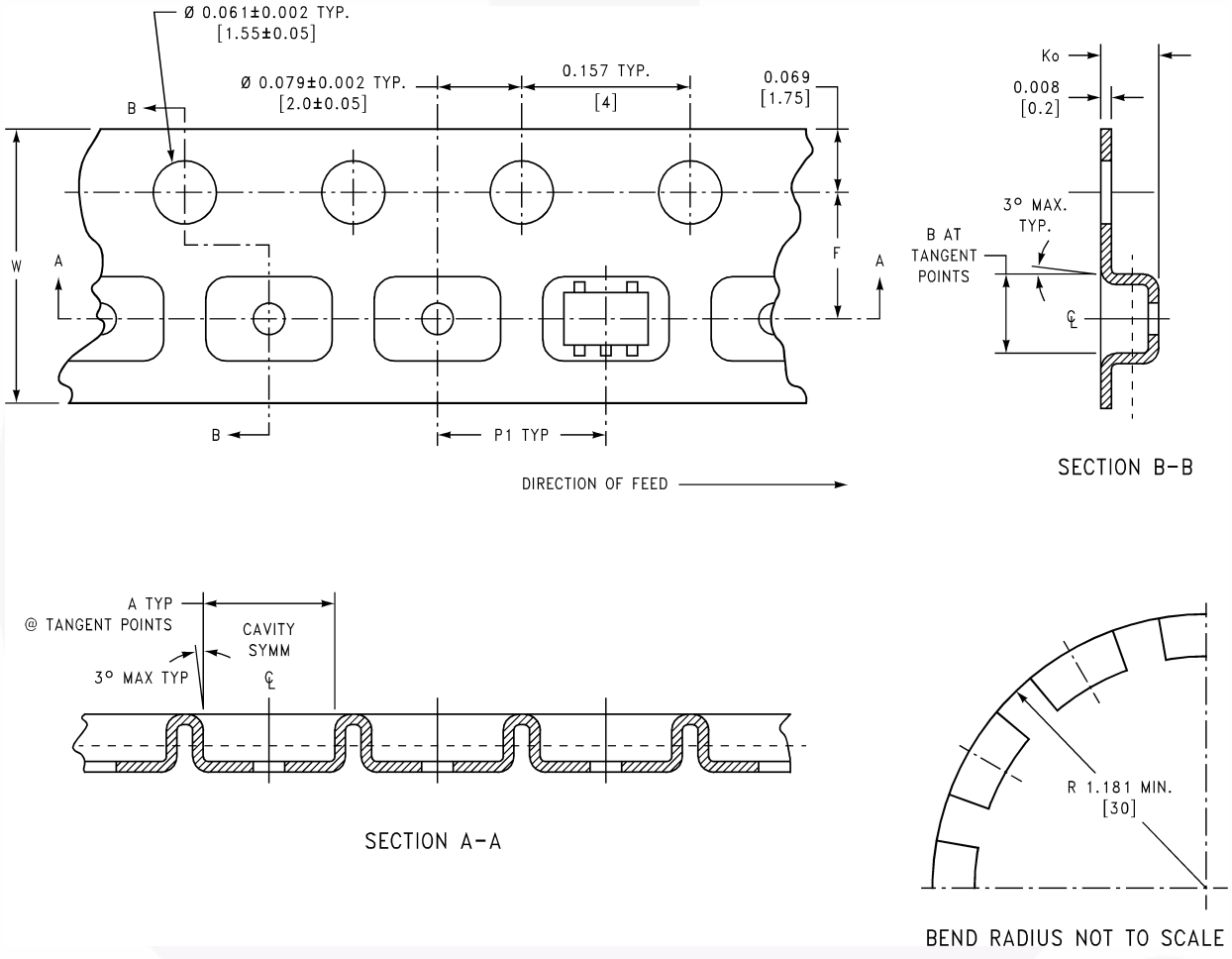
Figure 3. AC Waveforms

Tape and Reel Specifications

Tape Format for SC70 and SOT23

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions inches (millimeters)



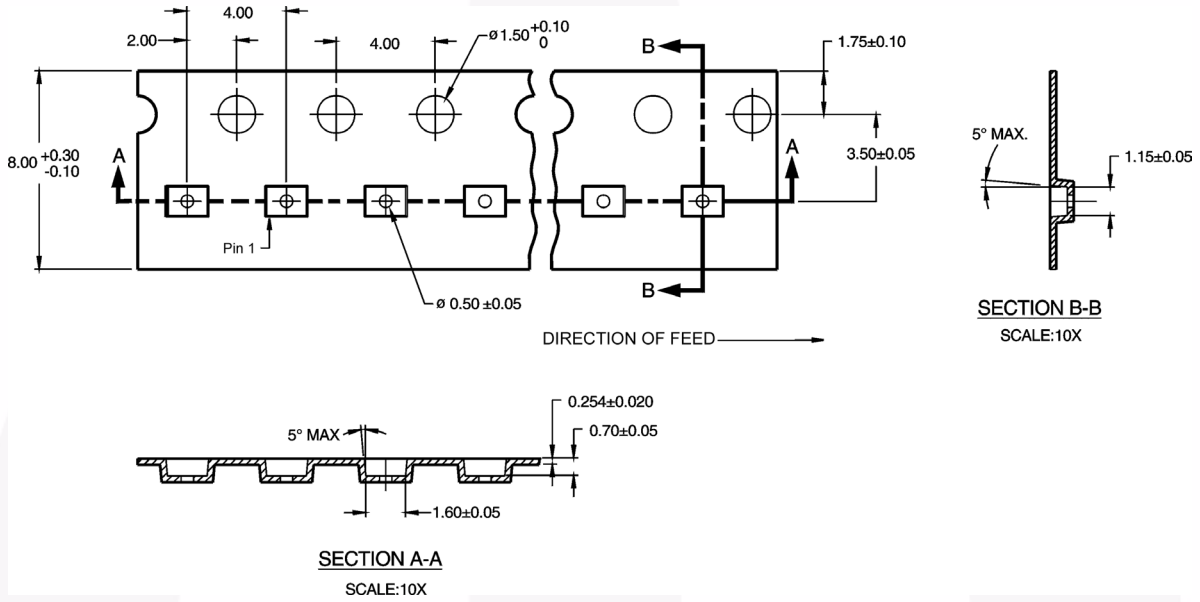
Package	Tape Size	Dim A	Dim B	Dim F	Dim K_o	Dim P1	Dim W
SC70-5	8mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

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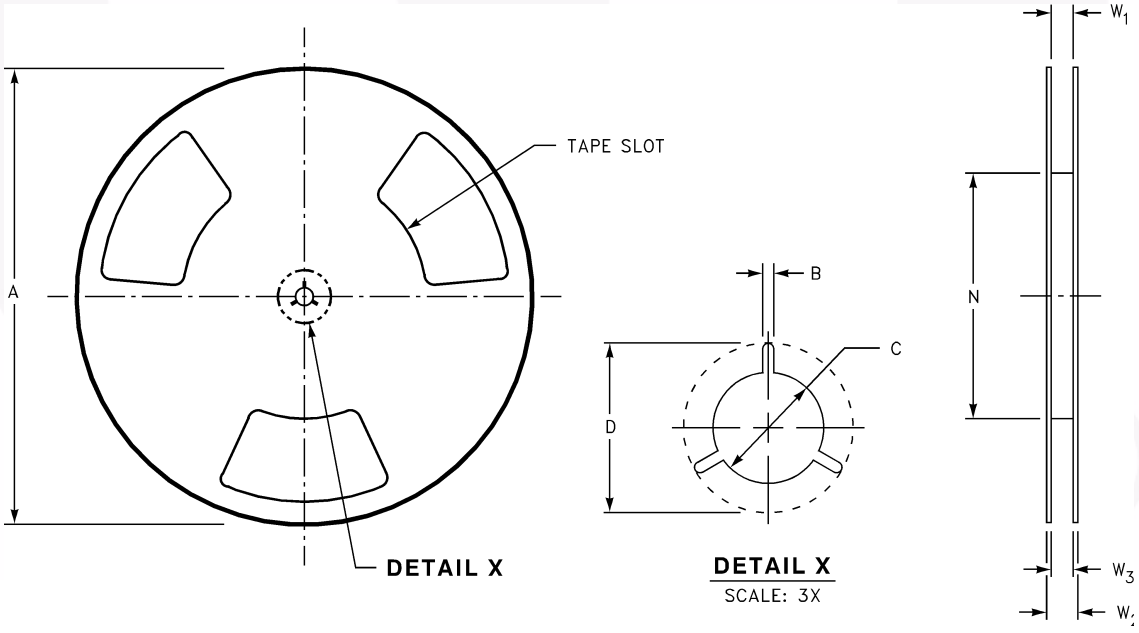
Tape and Reel Specifications (Continued)

Tape Format for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed



Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

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Physical Dimensions

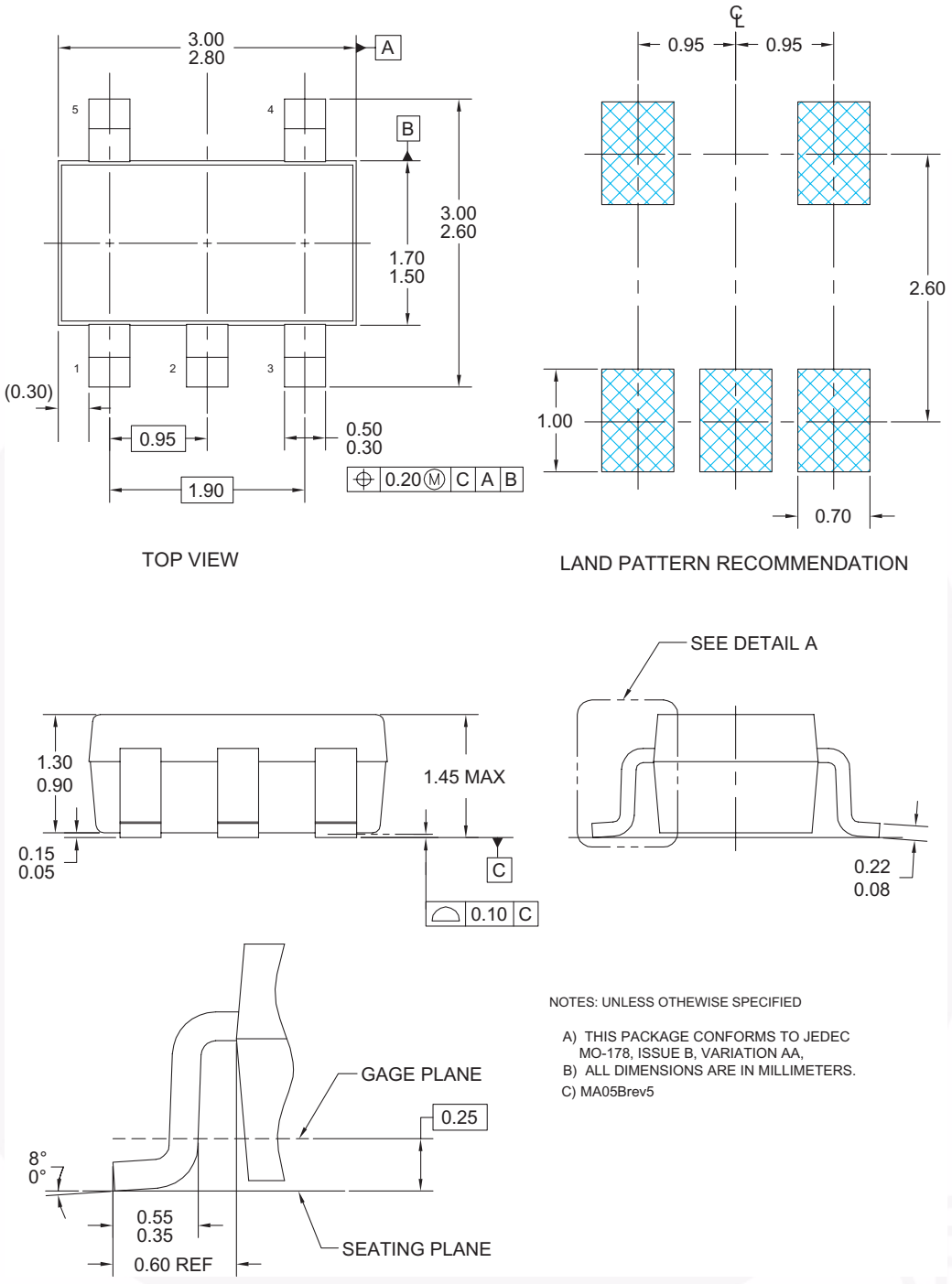


Figure 4. 5-Lead SOT23, JEDEC MO-178, 1.6mm

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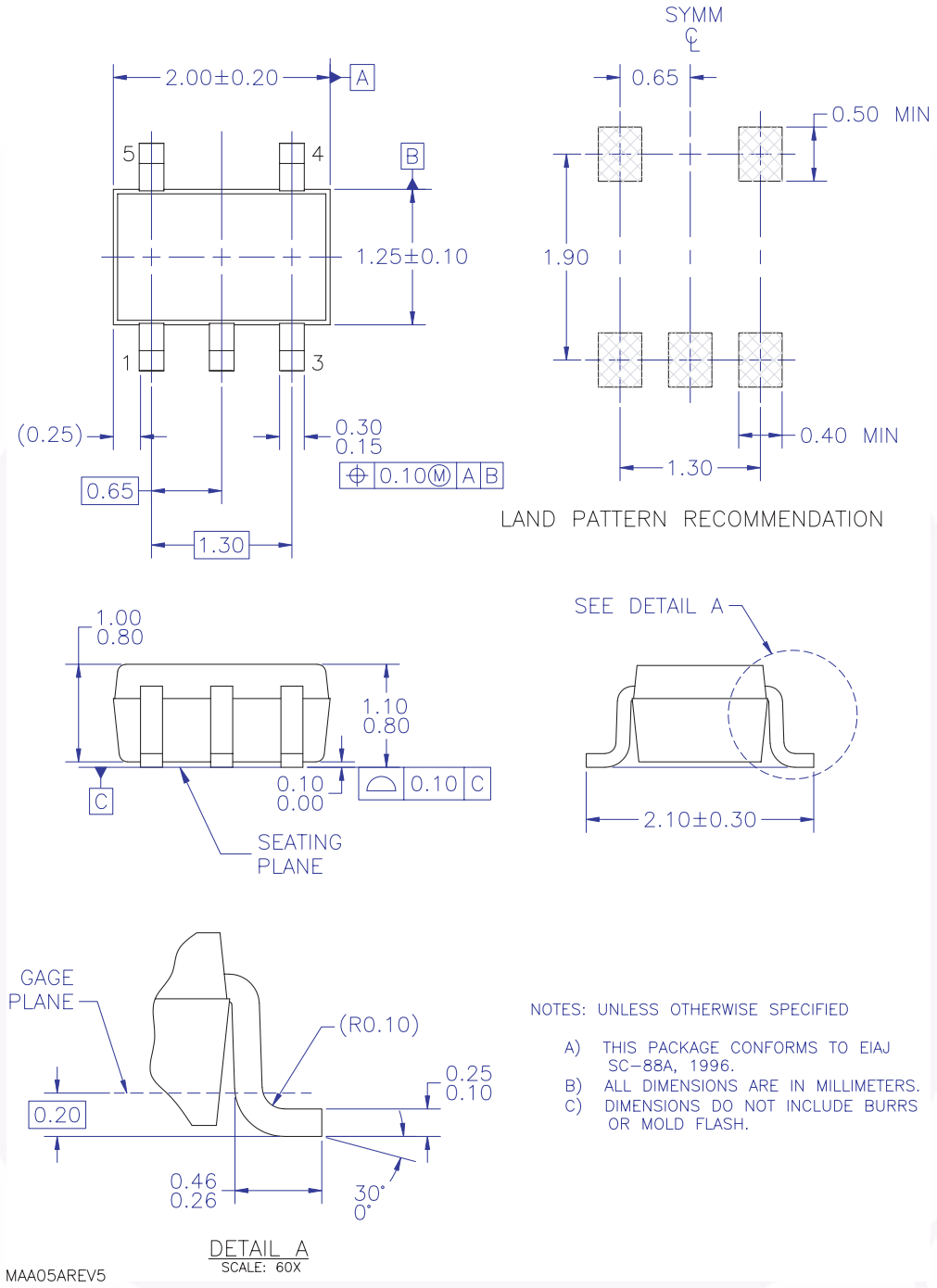
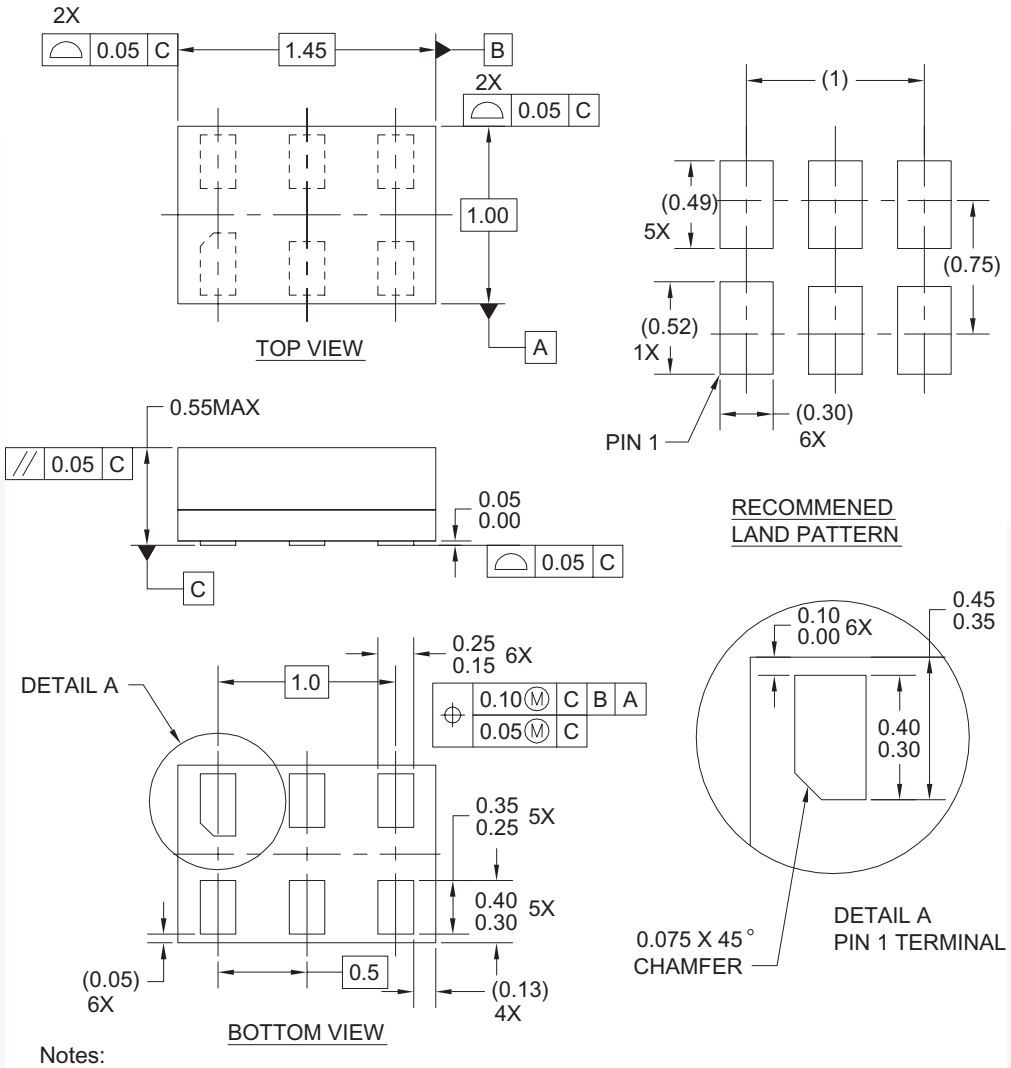


Figure 5. 5-Lead SC70, EIAJ SC-88a, 1.25mm Wide

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Physical Dimensions (Continued)



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

Figure 6. 6-Lead MicroPak, 1.0mm Wide

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